具有 4.5V 至 18V 输入电压，4A 输出电流同步降压稳压器的双路配电开关

查询样品: TPS65282

特性

集成型配电开关

- 运行输入电压的范围：**2.5V** 到 **6.5V**
- 接通阻抗为 **100mΩ** 的集成型背靠背功率金属氧化物场效应晶体管 **(MOSFET)**
- 可调电流限制：
  75mA-2.7A（典型值）
- **1.7A** 电流下 **+/-6%** 电流限制精度（典型值）
- 锁存过流保护版本
- 反向输入-输出电压保护
- 内置软启动
- 电源开关输出引脚上的 **4KV** 人体模型 **(HBM)** 和 **200V MM** 静电放电 **(ESD)** 保护

集成型降压 **DC/DC** 转换器

- 宽输入电压范围：**4.5V** 至 **18V**
- 最大持续 **4A** 输出电流
- 反馈基准电压：**0.8V±1 %**
- **300kHz** 至 **1.4MHz** 间可调开关频率
- 轻负载高效时的脉冲跳跃模式
- 具有
  内置 **1.2ms** 内部软启动时间的可调软启动和跟踪
- 逐周期电流限制
- 输出过压保护
- 电源正常指示器
- 过温保护
- **24** 导线四方扁平无引线 **(QFN)(REG) 4mm x 4mm** 封装

应用范围

- **USB** 端口和集线器
- 数字电视
- 机顶盒
- 网络语音 **(VOIP)** 电话
- 平板个人电脑

说明

TPS65282 组装有一个用于 USB 配电系统的双 N 通道 MOSFET 电源开关，此配电系统在一个单封装内需要双电源开关。 它还集成了一个降压单片转换器。 此器件用于为数字电视、机顶盒、平板电脑和网络语音 (VOIP) 电话等应用提供一个总体 USB 配电解决方案，这些应用需要精确电流限制或者在这些应用中有可能出现高电容负载或者短路。

双 100mΩ 独立配电开关通过使用一个外部电阻器将输出电流限制在典型值为 75mA 至 2.7A 的可编程电流限值阀值之间。 在更高电流限值设置时，此电流限值精度可达到 ±6%。 当输出负载超过电流限制阀值时，通过使用一个恒定电流模式，TPS65282 器件将输出电流限制在一个安全水平上。 在抗尖峰脉冲时间之后，通过在过流或者反向电压情况下锁存电源开关，TPS65282 提供电路断路器功能。 两个背靠背功率 MOSFET 防止关断时电流从输出注入输入。 当输出电压被驱动至高于输入时，一个内部反向电压比较器将电源开关禁用来保护正常运行时的开关输入端。 在过流和反向电压情况下，nFAULT1/2 输出被置为低电平有效。

为了优化电源效率并且减少外部组件数量，降压 DC/DC 转换器集成了功率 MOSFET。 到降压转换器的宽 4.5V 至 18V 输入电源范围包括大多数运行自 5V，9V，12V 或者 15V 电源总线的的中间总线电压。 峰值电流模式控制简化了补偿并提供快速瞬态响应。 配备有使能和软启动引脚，为了与系统的其它电源轨保持一致，此 DC/DC 可被精准排序并进行斜升操作。 逐周期过流保护和运行在断续模式限制了 MOSFET 在降压输出短路或者过载故障条件下的功率耗散。 借助于一个 ROSC 引脚上的外部电阻器，此转换器的开关频率可在 300kHz 至 1.4MHz 之间进行设定。 在 ROSC 引脚连接到 V7V 引脚、悬空、或者接地时，可选择一个缺省固定开关频率。 此降压转换器还特有一个脉冲跳跃模式 (PSM)，此模式可减少系统输入电源损耗以便在轻负载时实现高效率。

此器件执行一个内部热关断来在结温超过 160°C 时保护其自身不受损坏。 当结温超过热跳变阀值时，此热关断强制器件停止运行。 一旦裸片温度减少至低于 140°C，此器件重新启动加电序列。 热关断滞后值为 20°C。

TPS65282 采用一个 24 导线耐热增强型 QFN (RGE) 4mm x 4mm 薄型封装。

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	24-Pin QFN (RGE)	Reel 3000	TPS65282REGR	TPS65282
		Reel 250	TPS65282RGET	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION

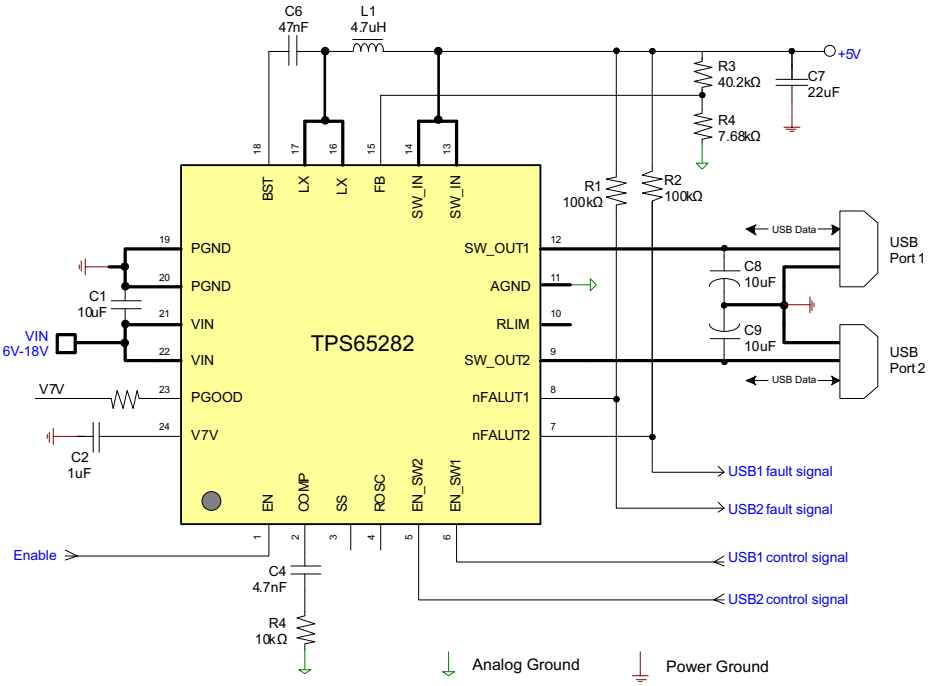


Figure 1. 12-V Power Bus

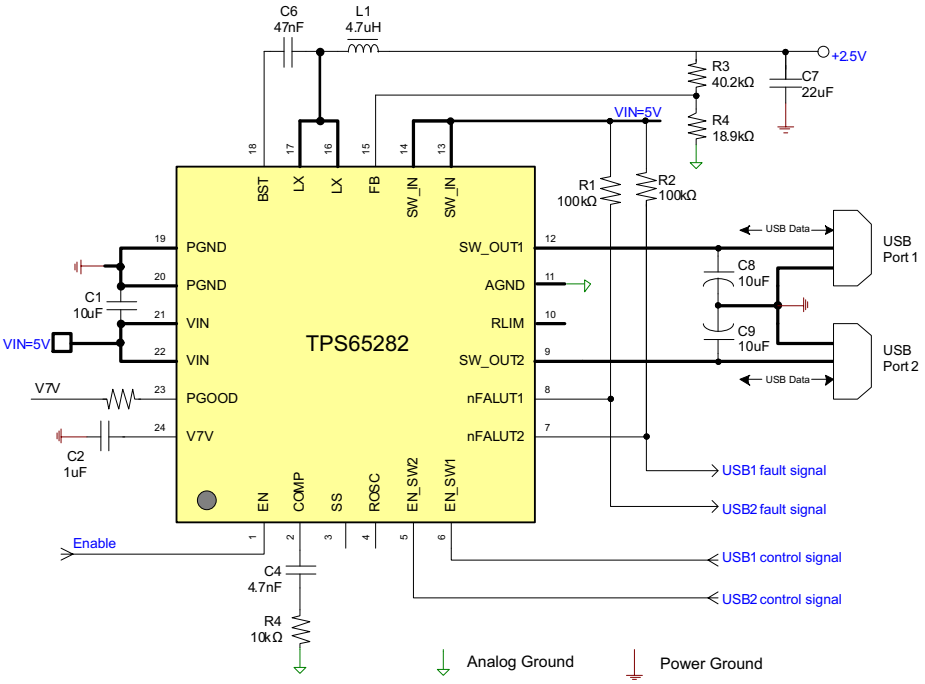
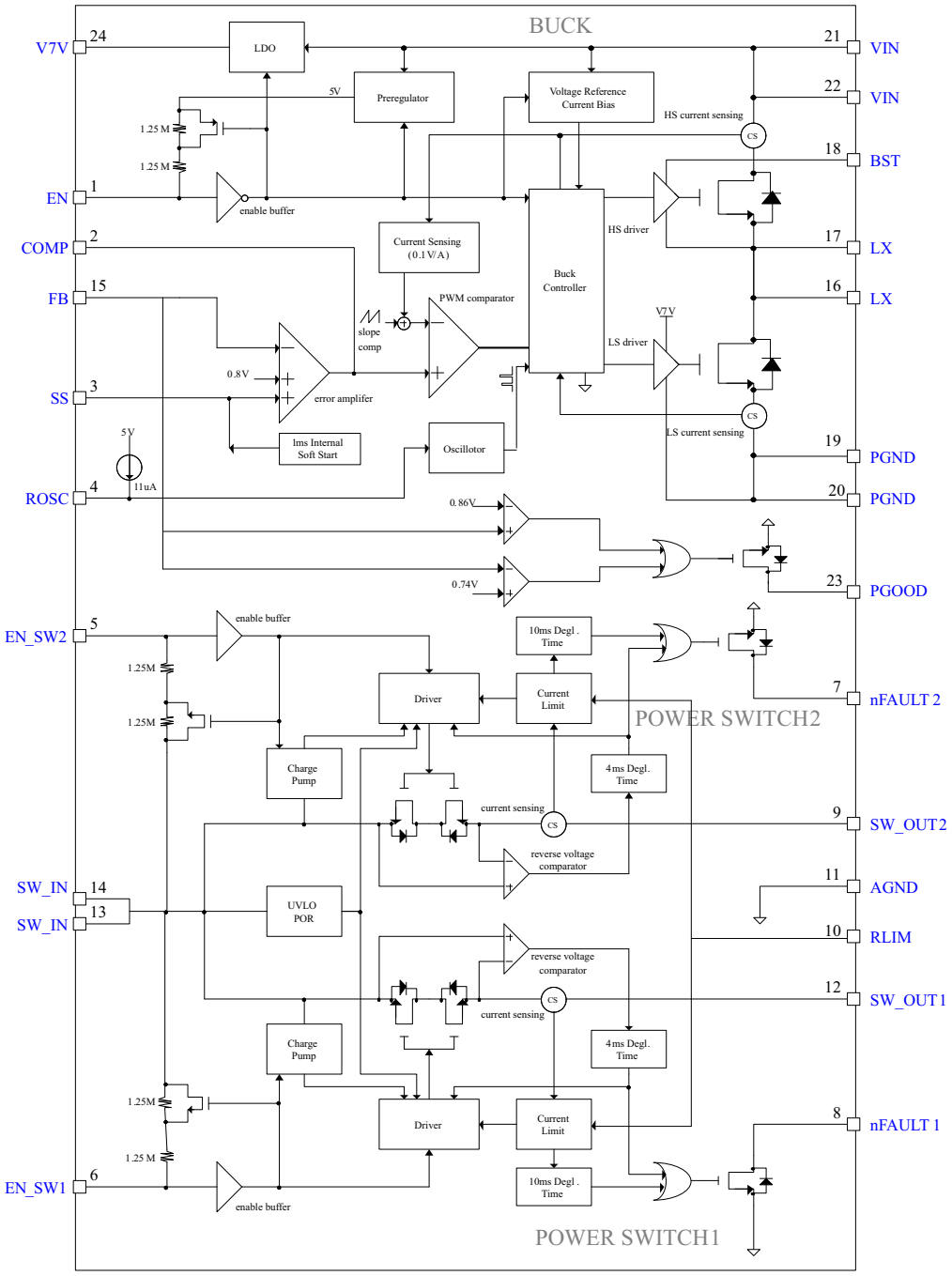
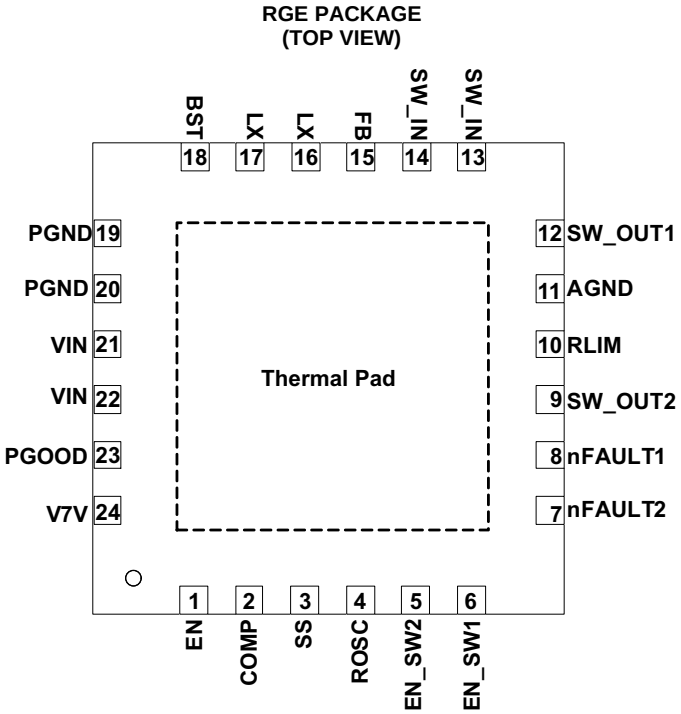


Figure 2. 5-V Power Bus

FUNCTION BLOCK DIAGRAM



PIN OUT



There is no electric signal down boned to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

TERMINAL FUNCTIONS

NAME	NO.	DESCRIPTION
EN	1	Enable for buck converter. Logic high enables buck converter and bias supply to power switches. Forcing the pin below 0.4 V shuts down the entire device, reducing the quiescent current to approximately 7 μA. There is a 1.25-MΩ pull-up resistor connecting this pin to internal 5-V power rail. Not recommend floating this pin. The device can be automatically started up with connecting EN pin to VIN though a 10-kΩ resistor or connecting a capacitor to program the delay of enabling the device.
COMP	2	Error amplifier output and Loop compensation pin for buck. Connect a series resistor and capacitor to compensate the control loop of buck converter with peak current PWM mode.
SS	3	Soft-Start and tracking input for buck converter. An internal 5-μA pull-up current source is connected to this pin. An external soft-start can be programmed by connecting a capacitor between this pin and ground. Leave the pin floating to have a default 1-ms of soft-start time. This pin allows the start-up of buck output to track an external voltage using an external resistor divider at this pin.
ROSC	4	Oscillator clock frequency control pin. Connect the pin to ground for a fixed 300-kHz switching frequency. Connect the pin to V7V or float the pin for a fixed 600-kHz switching frequency. Other switch frequencies between 300 kHz and 1.4 MHz can be programmed using a resistor connected from this pin to ground. An internal 11-μA pull-up current develops a voltage to be used in oscillator. Directly adjusting the ROSC pin voltage can linearly adjust switching frequency.
EN_SW2	5	Enable power switch 2. Logic high turns on power switch. Forcing the pin below 0.4 V shuts down power switch. Not recommend floating this pin, though there is a 1.25-MΩ pull-up resistor connecting this pin.
EN_SW1	6	Enable power switch 1. Logic high turns on power switch. Forcing the pin below 0.4 V shuts down power switch. Not recommend floating this pin, though there is a 1.25-MΩ pull-up resistor connecting this pin.
nFAULT2	7	Active low open drain output, asserted during over-current or reverse-voltage condition of power switch 2.
nFAULT1	8	Active low open drain output, asserted during over-current or reverse-voltage condition of power switch 1.
SW_OUT2	9	Power switch 2 output.
RLIM	10	Power switch current limit control pin. An external resistor used to set current limit threshold of power switch. Recommended 9.1 kΩ ≤ RLIM ≤ 232 kΩ.
AGND	11	Analog ground common to buck controller and power switch controller.
SW_OUT1	12	Power switch 1 output.
SW_IN	13,14	Power switch input voltage. Connect to buck output, or other power supply input.
FB	15	Feedback sensing pin for buck output voltage. Connect this pin to the resistor divider of buck output. The feedback reference voltage is 0.8 V ±1%.
LX	16,17	Switching node connection to the inductor and bootstrap capacitor for buck converter. This pin voltage swings from a diode voltage below the ground up to V_{IN} voltage.
BST	18	Bootstrapped supply to the high side floating gate driver in buck converter. Connect a capacitor (recommend 47 nF) from this pin to LX.
PGND	19,20	Power ground connection. Connect this pin as close as practical to the (-) terminal of input ceramic capacitor.
VIN	21,22	Input power supply for buck. Connect this pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 μF).
PGOOD	23	Power good. This pin is active high, Open drain output that indicates if the regulator output voltage is within regulation.
V7V	24	Internal low-drop linear regulator (LDO) output. The internal driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum 1-μF ceramic capacitor. The output voltage level of LDO is regulated to typical 6.3 V for optimal conduction on-resistances of internal power MOSFETs. In PCB design, the power ground and analog ground should have one-point common connection at the (-) terminal of V7V bypass capacitor.
Power PAD		Exposed pad beneath the IC. Connect to the ground. Always solder power pad to the board, and have as many thermal vias as possible on the PCB to enhance power dissipation. There is no ground or any other electric signal downbonded to the pad inside the IC package.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

	VIN	–0.3 to 20	V
	LX (Maximum withstand voltage transient < 20ns)	–1.0 to 20	V
	BST referenced to LX pin	–0.3 to 7	V
	SW_IN, SW_OUT1, SW_OUT2	–0.3 to 7	V
	EN, EN_SW1, EN_SW2, nFAULT1, nFAULT2, V7V, ROSC, PGOOD, RLIM	–0.3 to 7	V
	SS, COMP	–0.3 to 3.6	V
	AGND, PGND	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_A	Ambient temperature	–40		125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION(1)

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

(1) SW_OUT1/2 pins' human body model (HBM) ESD protection rating 4 kV, and machine model (MM) rating 200V.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65282 RGE 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	38.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	45.3	
θ_{JB}	Junction-to-board thermal resistance(4)	16.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	16.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.2	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, R_{nFAULT} = 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5		18	V
IDD_{SDN}	Shutdown supply current	EN = EN_SW1 = EN_SW2 = low		7	20	µA
IDD_{Q_NSW}	Switching quiescent current with no load at DCDC output	EN = high, EN_SWx = low With Buck switching		0.5		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}	4	4.25	4.50	V
		Falling V_{IN}	3.75	4	4.25	
		Hysteresis		0.25		
V_{7V}	Internal biasing supply	V_{7V} load current = 0 A, V_{IN} = 12 V	6.15	6.3	6.45	V
OSCILLATOR						
f_{SW_BK}	Switching frequency range	Set by external resistor ROSC	300		1400	kHz
f_{SW}	Programmable frequency	ROSC = 51 kΩ		560		kHz
		ROSC = 130 kΩ		1400		
		ROSC floating or connected to V7V	510	600	690	
		ROSC connected to ground	225	300	345	
BUCK CONVERTER						
V_{FB}	Feedback voltage	V_{COMP} = 1.2 V, T_J = 25°C	0.792	0.8	0.808	V
		V_{COMP} = 1.2 V, T_J = -40°C to 125°C	0.784	0.8	0.816	
$V_{LINEREG}$	Line regulation - DC	I_{OUT} = 2 A		0.5		%/V
$V_{LOADREG}$	Load regulation - DC	I_{OUT} = (10% - 90%)I_{OUT_max}		0.5		%/A
G_{m_EA}	Error amplifier trans-conductance	-2 µA < I_{COMP} < 2 µA		600		µs
G_{m_SRC}	COMP voltage to inductor current Gm(1)	I_{LX} = 0.5 A		36		A/V
V_{ENH}	EN high level input voltage		2	1.24		V
V_{ENL}	EN low level input voltage			0.98	0.4	V
I_{SS}	Soft-start charging current			5		µA
t_{SS_INT}	Internal soft-start time	SS pin floats		1.2		ms
I_{LIMIT}	Buck peak inductor current limit			5.2		A
R_{dson_HS}	On resistance of high side FET in buck	V_{7V} = 6.2.5 V including banding wire		100		mΩ
R_{dson_LS}	On resistance of low side FET in buck	V_{IN} = 12 V including banding wire		60		mΩ
POWER GOOD RESET GENERATOR						
VUV_{BUCK}	Threshold voltage for buck under voltage	Output falling		91.6		%
		Output rising (PG will be asserted)		94.4		
VOV_{BUCK}	Threshold voltage for buck over voltage	Output rising (high side FET will be forced off)		105.4		%
		Output falling (high side FET will be allowed to switch)		104.2		
T_{D-L}	PGOOD H-L delay time	Change FB from 0.8 V to 1 V, Measure the delay from FB = 1 V to PGOOD low		100		µs
T_{D-H}	PGOOD L-H delay time	Change FB from 1 V to 0.8 V, Measure the delay from FB = 0.8 V to PGOOD high		130		µs
V_{PGOOD}	PGOOD pin output low voltage	Force FB = 1 V to create fault condition, Sink 1-mA current to PGOOD pin, Measure the PGOOD pin voltage		100	300	mV
POWER DISTRIBUTION SWITCH						
V_{SW_IN}	Power switch input voltage range		2.5		6	V
V_{UVLO_SW}	Input under-voltage lock out	V_{SW_IN} rising	2.15	2.25	2.35	V
		V_{SW_IN} falling	2.05	2.15	2.25	V
		Hysteresis		100		mV

(1) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, R_{nFAULT} = 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON_SW}	Power switch NDMOS on-resistance	V_{SW_INx} = 5 V, I_{SW_OUT} = 0.5 A, T_J = 25°C, including bond wire resistance		100		mΩ
		V_{SW_INx} = 2.5 V, I_{SW_OUT} = 0.5 A, T_J = 25°C, includes bond wire resistance		100		
t_{D_on}	Turn-on delay time from EN_SW turns high	V_{SW_IN} = 5 V, C_L = 1 µF, R_L = 100 Ω (see Figure 3)		0.66	1.5	ms
t_{D_off}	Turn-off delay time from EN_SW turns low			1.6	2	ms
t_r	Output rise time			1.1	1.5	ms
t_f	Output fall time			1.2	1.5	ms
I_{OS}	Current limit threshold (maximum DC current delivered to load) and short circuit current, SW_OUT connect to ground	R_{LIM} = 15 kΩ	1.57	1.68	1.79	A
		R_{LIM} = 20 kΩ	1.18	1.26	1.34	
		R_{LIM} = 51 kΩ	0.47	0.5	0.53	
t_{IOS}	Response time to short circuit	V_{SW_IN} = 5 V		2		us
$t_{DEGLITCH(OCP)}$	Switch over current fault deglitch	Fault assertion or de-assertion due to over-current condition	7	10	13	ms
V_{L_nFAULT}	nFAULTx pin output low voltage	$I_{nFAULTx}$ = 1 mA		150	300	mV
V_{EN_SWH}	EN_SW high level input voltage	EN_SWx high level input voltage	2	1.29		V
V_{EN_SWL}	EN_SW high level input voltage	EN_SWx low level input voltage		0.97	0.4	V
R_{DIS}	Discharge resistance	V_{SW_IN} = 5 V, EN_SWx = 0 V		160		Ω
THERMAL SHUTDOWN						
T_{TRIP_BUCK}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST_BUCK}	Thermal protection hysteresis			20		°C

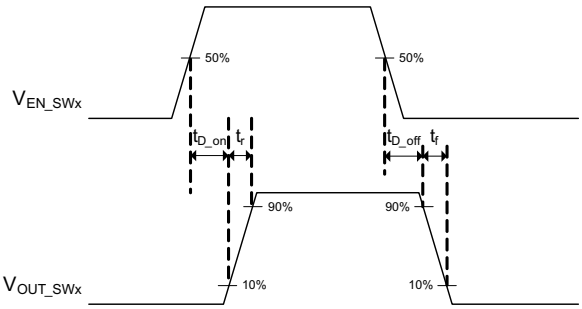


Figure 3. Power Switches Test Circuit and Voltage Waveforms

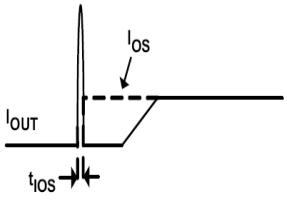


Figure 4. Response Time to Short Circuit Waveform

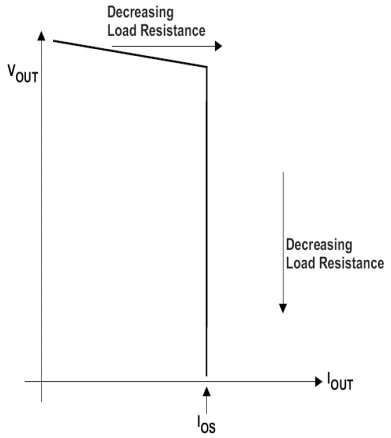


Figure 5. Output Voltage vs Current Limit Threshold

TYPICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 600 kHz, R_{nFAULT} = 100 kΩ (unless otherwise noted)

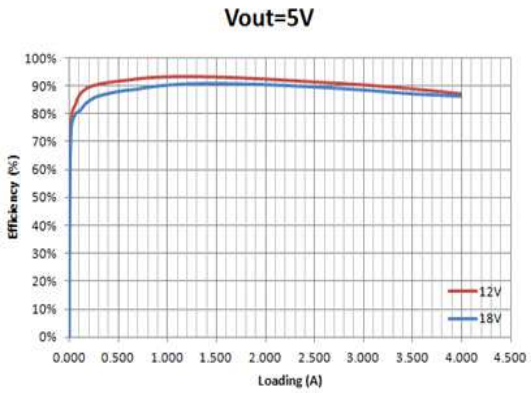


Figure 6. Buck Efficiency at V_{OUT} = 5 V

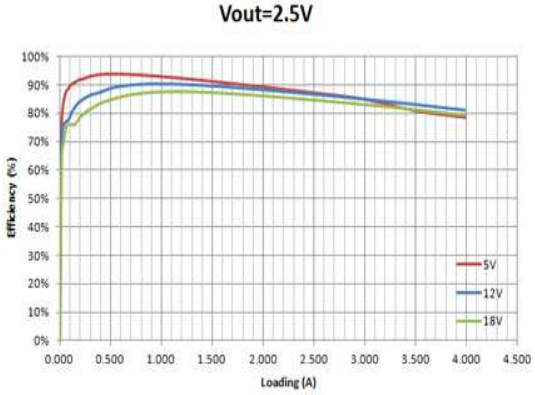


Figure 7. Buck Efficiency at V_{OUT} = 2.5 V

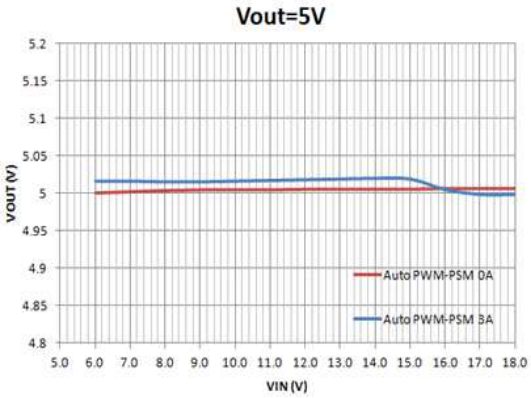


Figure 8. Buck Line Regulation at V_{OUT} = 5 V

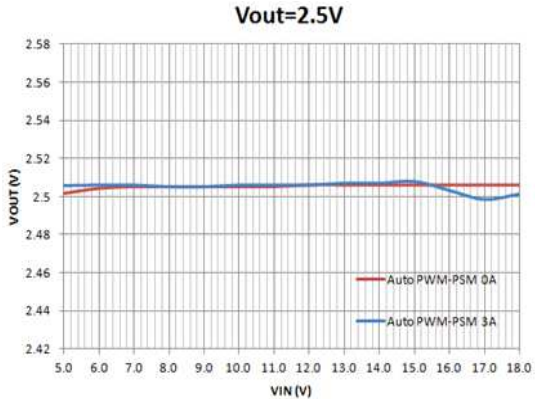


Figure 9. Buck Line Regulation at V_{OUT} = 2.5 V

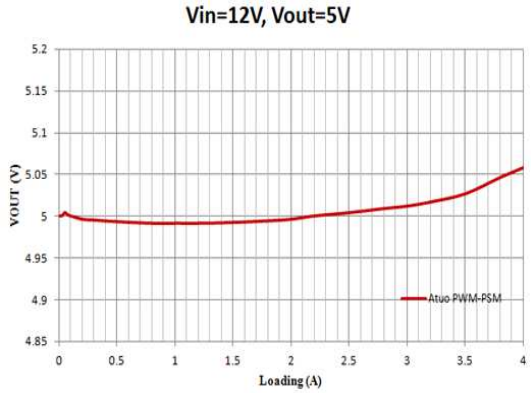


Figure 10. Buck Load Regulation at V_{OUT} = 5 V

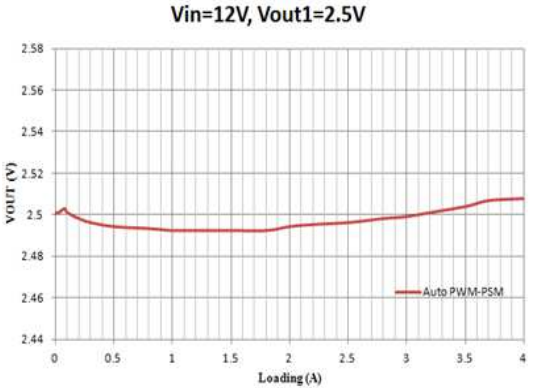


Figure 11. Buck Load Regulation at V_{OUT} = 2.5 V

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 600 kHz, R_{nFAULT} = 100 kΩ (unless otherwise noted)

Figure 12. Buck Start Up by EN Pin With External 22-nF SS Capacitor

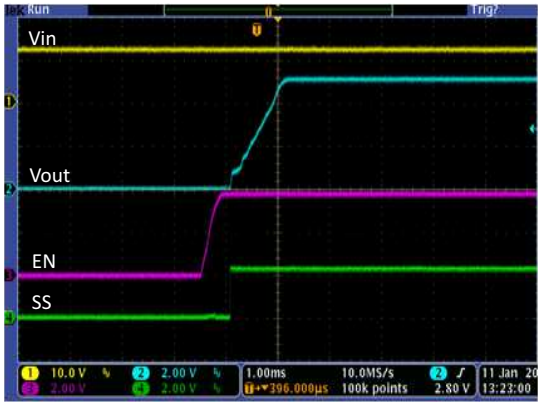


Figure 13. Buck Start Up by EN Pin With Internal SoftStart (SS Pin Open)

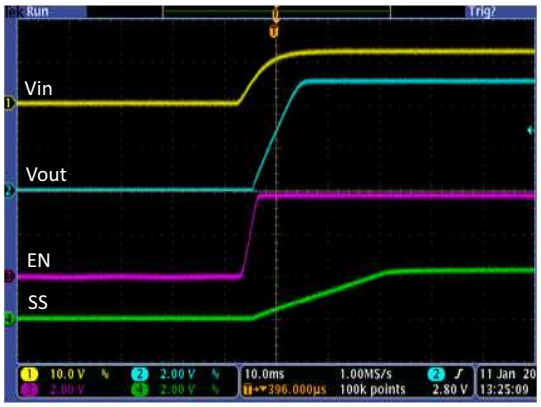


Figure 14. Ramp V_{IN} to Start Up Buck With External 22-nF SS Capacitor

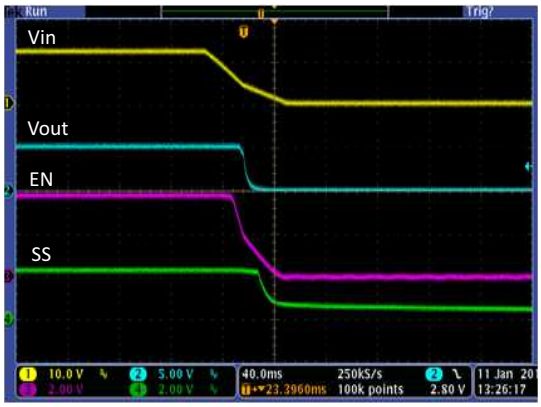


Figure 15. Ramp V_{IN} to Power Down Buck With External 22-nF SS Capacitor

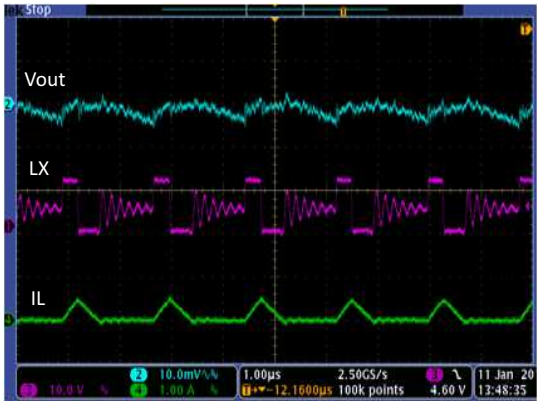


Figure 16. Buck Output Voltage Ripple I_{OUT} = 0.1 A

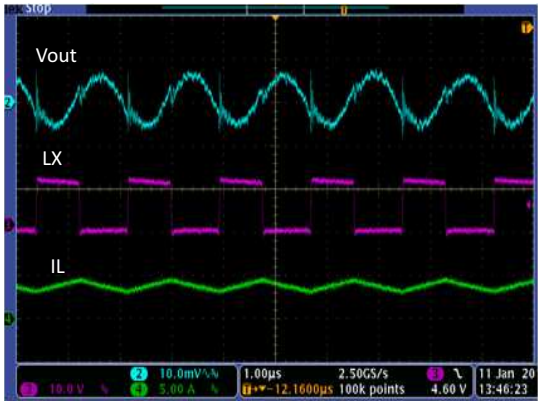


Figure 17. Buck Output Voltage Ripple I_{OUT} = 4 A

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 600 kHz, R_{nFAULT} = 100 kΩ (unless otherwise noted)

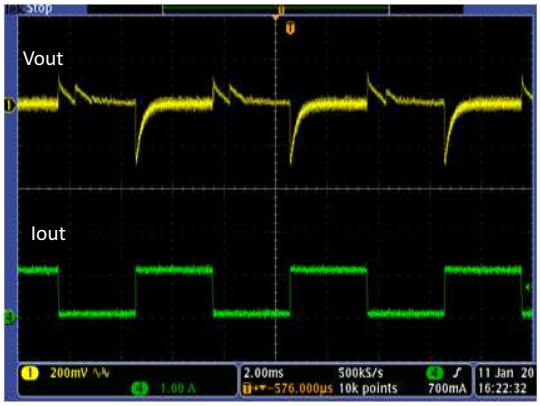


Figure 18. Buck Output Load Transient I_{OUT} = 0 A - 1 A

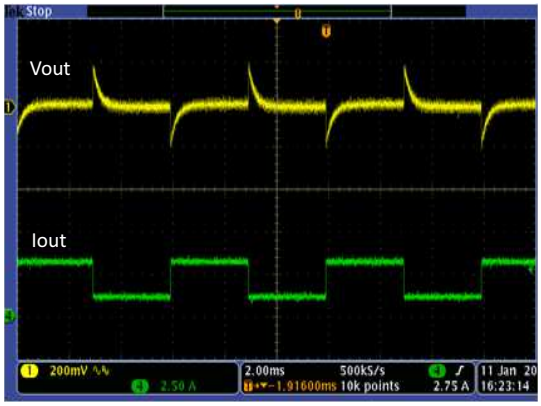


Figure 19. Buck Output Load Transient I_{OUT} = 1 A - 3 A

Figure 20. Buck Hiccup Response to Hard-Short Circuit

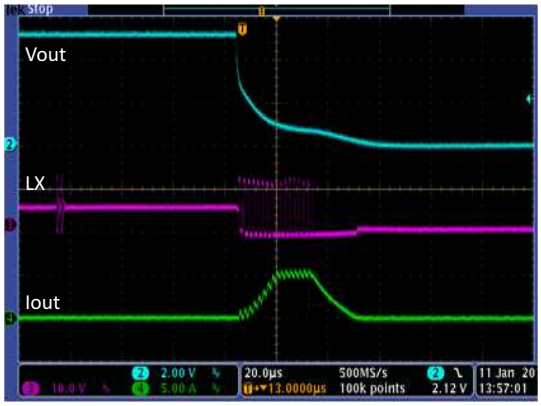


Figure 21. Zoom in Buck Output Hard-Short Response

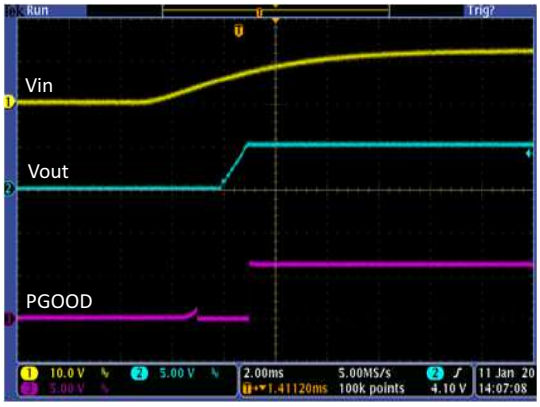


Figure 22. Power Up and PGOOD, No Load

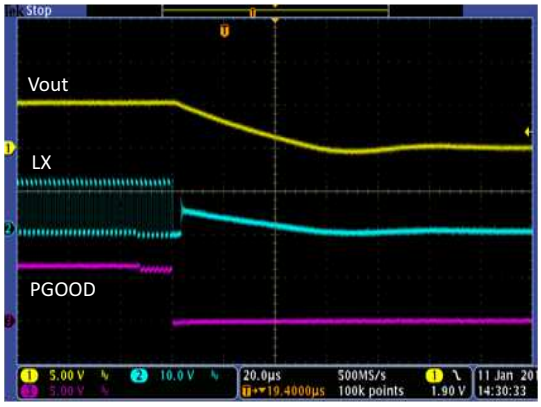


Figure 23. Over Current and PGOOD

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 600 kHz, R_{nFAULT} = 100 kΩ (unless otherwise noted)

Figure 24. Power Switch1 Turn On Delay and Rise Time

Figure 25. Power Switch2 Turn On Delay and Rise Time

Figure 26. Power Switch1 Turn Off Delay and Fall Time
R_{OUT} = 5 Ω, C_{OUT} = 22 µF

Figure 27. Power Switch2 Turn Off Delay and Fall Time
R_{OUT} = 5 Ω, C_{OUT} = 22 µF

Figure 28. Power Switch1 Enable Into Short Circuit

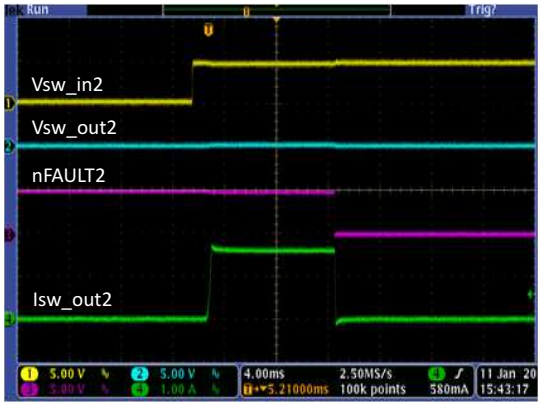


Figure 29. Power Switch2 Enable Into Short Circuit

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 600 kHz, R_{nFAULT} = 100 kΩ (unless otherwise noted)

Figure 30. Power Switch1 Current Limit Operation

Figure 31. Power Switch2 Current Limit Operation

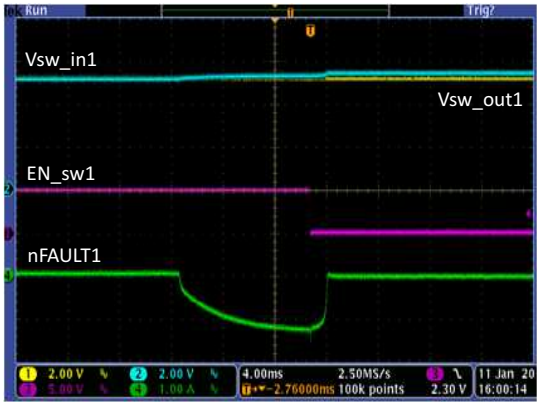


Figure 32. Power Switch1 Reverse Voltage Protection Response

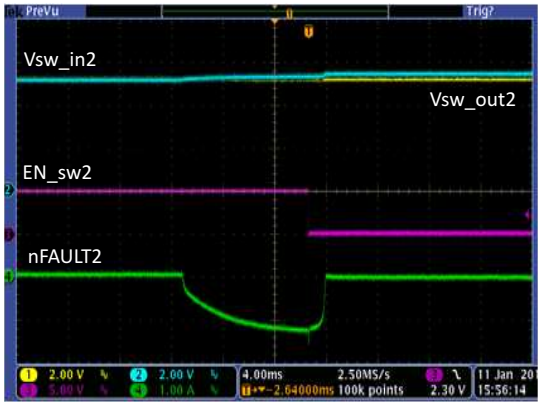


Figure 33. Power Switch2 Reverse Voltage Protection Response

OVERVIEW

TPS65282 PMIC integrates a current-limited, power distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered and provide a precision current limit protection. Additional device features include over termperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provide the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltage of power switch as low as 2.5 V and requires little supply current. The driver incorporates circuitry that controls the rise and fall times of output voltage to limit large current and voltage surges and provides built-in soft-start functionality. TPS65282 device limits output current to a safe level by using a constant current mode when the output load exceeds the current limit threshold. TPS65282 device lacthes off when the load exceeds the current limit threshold. The device asserts the nFAULT signal during over current or reverse voltage faulty condition.

TPS65282 PMIC also integrates a synchronous step-down converter with regulated 0.8-V ±1% feedback reference voltage. The synchronous buck converter incorporates 100-mΩ high side power MOSFET and 60-mΩ low side power MOSFET to achieve high efficiency power conversion. The converter supports input voltage range from 4.5 V to 18 V for a fixed 5-V output. The converter operates in continuous conduction mode with peak current mode control for simplified loop compensation. The switching clock frequency can be programmed from 300 kHz to 1.4 MHz from ROSC pin connection. The peak inductor current limit threshold is internally set at 5.2 A. The soft-start time can be adjusted with connecting an external capacitor at SS pin, or fixed at 1.2 ms with floating at SS pin.

POWER SWITCH DETAILED DESCRIPTION

Over Current Condition

The TPS65282 responds to over-current conditions on power switches by limiting the output currents to the I_{OCP_SW} level. The load current is less than the current-limit threshold and the device does not limit current. During normal operation the N-channel MOSFET is fully enhanced, and $V_{SW\_OUT} = V_{SW\_IN} - (I_{SW\_OUT} \times R_{dson\_SW})$. The voltage drop across the MOSFET is relatively small compared to V_{SW_IN}, and $V_{SW\_OUT} \approx V_{SW\_IN}$. When an over current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. During current-limit operation, the N-channel MOSFET is no longer fully enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{SW\_IN} \neq V_{SW\_OUT}$), and V_{SW_OUT} decreases. The amount that V_{SW_OUT} decreases is proportional to the magnitude of the overload condition. The expected V_{SW_OUT} can be calculated by $I_{OS} \times R_{LOAD}$, where I_{OS} is the current-limit threshold and R_{LOAD} is the magnitude of the overload condition.

Three possible overload conditions can occur as summarized in Table 1.

Table 1. Possible Overload Conditions

CONDITIONS	BEHAVIORS
Short circuit or partial short circuit present when the device is powered up or enabled	The output voltage is held near zero potential with respect to ground and the TPS65282 ramps output current to I_{OCP_SW}. The TPS65282 limits the current to I_{OS} until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled.
Gradually increasing load (<100 A/s) from normal operating current to I_{OS}	The current rises until current limit. Once the threshold has been reached, the device switches into its current limiting at I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled.
Short circuit, partial short circuit or fast transient overload occurs while the device is enabled and powered on	The device responds to the over-current condition within time t_{IOS} (see Figure 4). The current sensing amplifier is overdriven during this time, and needs time for loop response. Once T_{IOS} has passed, the current sensing amplifier recovers and limits the current to I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled.

Reverse Current and Voltage Protection

A power switch in the TPS65282 incorporates two back-to-back N-channel power MOSFETs as to prevent the reverse current flowing back the input through body diode of MOSFET when power switches are off.

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typical) for 4-ms (typical). This prevents damage to devices on the input side of the TPS65282 by preventing significant current from sinking into the input capacitance of power switch or buck output capacitance. The TPS65282 keeps the power switch turned off even if the reverse-voltage condition is removed and do not allow the N-channel MOSFET to turn on until power is cycled or the device enable is toggled. The reverse-voltage comparator also asserts the nFAULT1/2 output (active-low) after 4 ms.

nFAULT Response

The nFAULT1/nFAULT2 open-drain output is asserted (active low) during an over current, over temperature or reverse-voltage condition. The TPS65282 asserts the nFAULT signal during a fault condition and remains asserted while the part is latched-off. The nFAULT signal is de-asserted once device power is cycled or the enable is toggled and the device resumes normal operation. The TPS65282 is designed to eliminate false nFAULT reporting by using an internal delay "deglitch" circuit for over current (10 ms typical) and reverse-voltage (4 ms typical) conditions without the need for external circuitry. This ensures that nFAULT is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Deglitching circuitry delays entering and leaving fault conditions. Over temperature conditions are not deglitched and assert the FAULT signal immediately.

Under-Voltage Lockup (UVLO)

The under-voltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

Enable and Output Discharge

The logic enable EN_SW1/EN_SW2 controls the power switch, bias for the charge pump, driver, and other circuits. The supply current from power switch driver is reduced to less than 1uA when a logic low is present on EN_SW1/2. A logic high input on EN_SW1/EN_SW2 enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

When enable is de-asserted, the discharge function is active. The output capacitor of power switch is discharged through an internal NMOS that has a discharge resistance of 160 Ω. Hence, the output voltage drops down to zero. The time taken for discharge is dependent on the RC time constant of the resistance and the output capacitor.

Power Switch Input and Output Capacitance

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. The output capacitor in buck converter is recommended to place between SW_IN and AGND as close to the device as possible for local noise de-coupling. Additional capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the input of power switches in the evaluation board to the bench power-supply. Placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

Programming the Current-Limit Threshold

The over-current threshold is user programmable via an external resistor. The TPS65282 uses an internal regulation loop to provide a regulated voltage on the RLIM pin. The current-limit threshold is proportional to the current sourced out of RLIM. The recommended 1% resistor range for RLIM is 9.1 kΩ ≤ RLIM ≤232 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the over-current threshold when selecting a value for RLIM. The following equations and Figure 34 can be used to calculate the resulting over-current threshold for a given external resistor value (RLIM).

Current-Limit Threshold Equation (IOS):

$I_{OS(A)} = 25.078 \times R_{LIM}^{-0.993}$ (kΩ) (1)

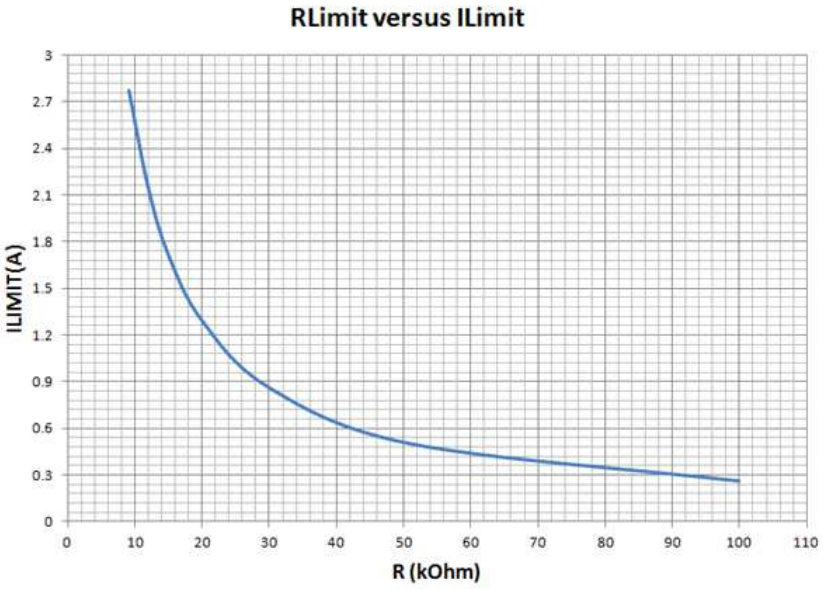


Figure 34. Current Limit Threshold (I_{OS}) vs Current Limit Resistor (R_{LIM})

UNIVERSAL SERIAL BUS (USB) POWER-DISTRIBUTION REQUIREMENTS

One application for this device is for current limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. The latest USB standard should always be referenced when considering the current-limit threshold.

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS65282 has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

Self-Powered and Bus-Powered HUBs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V and 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

USB Power Distribution Requirements

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

SPHs must:

- Current limit downstream ports
- Report over-current conditions

BPHs must:

- Enable/disable power to downstream ports
- Power up at < 100 mA
- Limit inrush current (< 44 Ω and 10 µF)

Functions must:

- Limit inrush currents
- Power up at < 100 mA

The feature set of the TPS65282 meets each of these requirements. The integrated current limiting and over-current reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

BUCK DC/DC CONVERTER DETAILED DESCRIPTION

Output Voltage

The TPS65282 regulates output voltage set by a feedback resistor divider to 0.8-V reference voltage. This pin should be directly connected to middle of resistor divider. It is recommended to use 1% tolerance or better divider resistors.Great care should be taken to route the FB line away from noise sources, such as the inductor or the LX switching node line. Start with 40.2 kΩ for the R1 resistor and use Equation 2 to calculate R2.

$$R_2 = R_1 \cdot \left(\frac{0.8V}{V_{OUT} - 0.8V}\right) \quad (2)$$

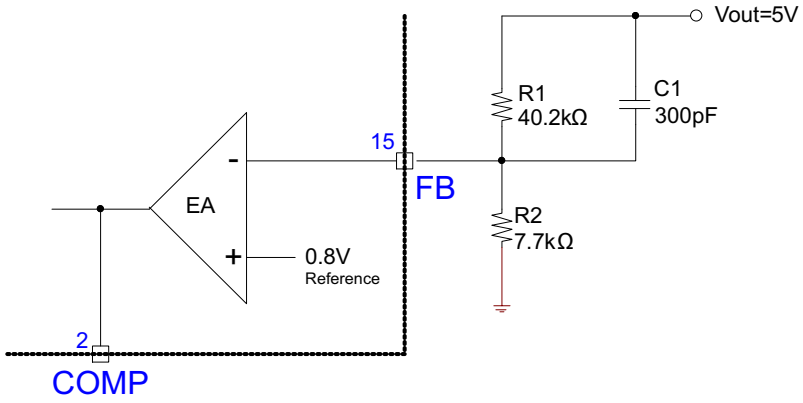


Figure 35. Buck Feedback Resistor Divider

Switching Frequency Selection

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and capacitance to maintain low output ripple voltage. The switching frequency of the TPS65282 buck controller can be selected with the connection at ROSC pin. The ROSC pin can be connected to AGND, tied to V7V, open or programmed through an external resistor. Tying ROSC pin to AGND selects 300 kHz, while tying ROSC ping to V7V or floating ROSC pin selects 600 kHz. Placing a resistor between ROSC and AGND allows the buck switching frequency to be programmed between 300 kHz to 1.4 MHz, as shown in Figure 36. The programmed clock frequency by an external resistor can be calculated with the following equation:

$$f_{SW} = 11 \times R_{OSC} \quad (3)$$

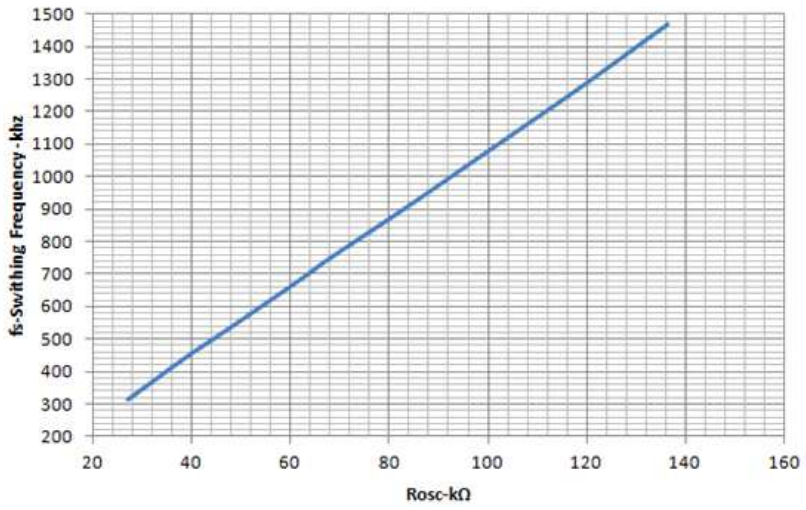


Figure 36. R_{OSC} vs Switching Frequency

Soft-Start Time

The start-up of buck output is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 0.8-V reference, the TPS65282 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.8 V. The SS pin can be used to program an external soft-start function or to allow output of the buck to track another supply during start-up. The device has an internal pull-up current source of 5 µA that charges an external soft-start capacitor to provide a linear ramping voltage at SS pin. The TPS65282 will regulate the internal feedback voltage according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from 0 V to its final regulated value. The total soft-start time will be approximately:

$$Tss = Css \cdot \left(\frac{0.8 \cdot V}{5 \cdot \mu A} \right) \quad (4)$$

Internal V7V Regulator

The TPS65282 features an internal P-channel low dropout linear regulator (LDO) that supplies power at the V7V pin from the VIN supply. V7V powers the gate drivers and much of the TPS65282's internal circuitry. The LDO regulates V7V to 6.3 V of over drive voltage on the power MOSFET for the best efficiency performance. The LDO can supply a peak current of 50 mA and must be bypassed to ground with a minimum 1-µF ceramic capacitor. The capacitor placed directly adjacent to the V7V and PGND pins is highly recommended to supply the high transient currents required by the MOSFET gate drivers.

Pulse Skipping Operation

When a buck synchronous converter operates at light load condition, the switching loss is the dominant source of power loss. Under this condition, TPS65282 operates with pulse skipping mode to reduce the switching loss by keeping the power transistors in the off-state for several switching cycles, while maintaining a regulated output voltage. The output voltage, load and inductor current are shown in Figure 37. When the V_{COMP} falls lower than V_{GS}, the COMP pin voltage is clamped to V_{GS} internally, typical 570 mV, the device enters pulse skipping mode and high side MOSFET stops switching, then the output falls and the V_{COMP} rises. When the V_{COMP} rises larger

than V_{GS}, the high side MOSFET starts switching, then the output rises and the V_{COMP} falls. When the V_{COMP} falls lower than V_{GS}, the high side MOSFET stops switching again. If the peak inductor current rise above typical 300 mA and the COMP pin voltage to rise above V_{GS}, the converter exits pulse skipping mode. Since converter detects the peak inductor current for pulse skip mode, the average load current entering pulse skipping mode varies with the applications and external output filters.

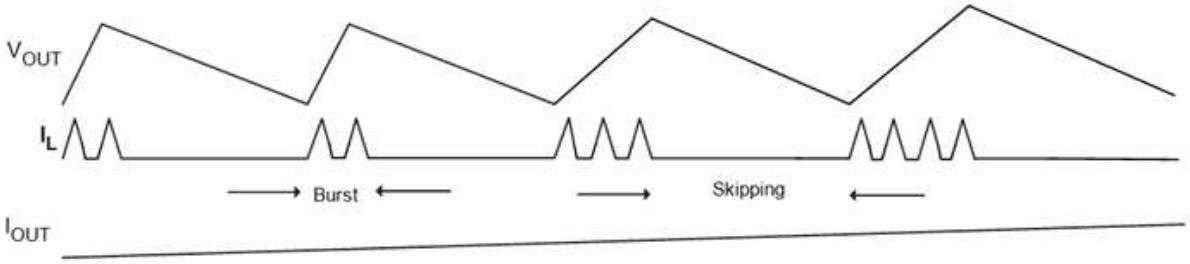


Figure 37. Low Power/Pulse Skipping

Short Circuit Protection

During the PWM on-time, the current through the internal high side switching MOSFET is sampled. The sampled current is compared to a nominal 5.2-A over-current limit. If the sampled current exceeds the over-current limit reference level, an internal over-current fault counter is set to 1 and an internal flag is set. Both internal high side and low side power MOSFETs are immediately turned off and will not be turned on again until the next switching cycle. If the over-current condition persists for eight sequential clock cycles, the over-current fault counter overflows indicating an over-current fault condition exists. The buck regulator is shut down and stays turned off for 10 ms. If the over-current condition clears prior to the counter reaching eight consecutive cycles, the internal flag and counter are reset. The protection circuitry attempts to recover from the over-current condition after 10-ms power down time. The internal over-current flag and counter are reset. A normal soft-start cycle is attempted and normal operation continues if the over-current fault condition has cleared. If the over-current fault counter overflows during soft-start, the converter shuts down and this hiccup mode operation repeats.

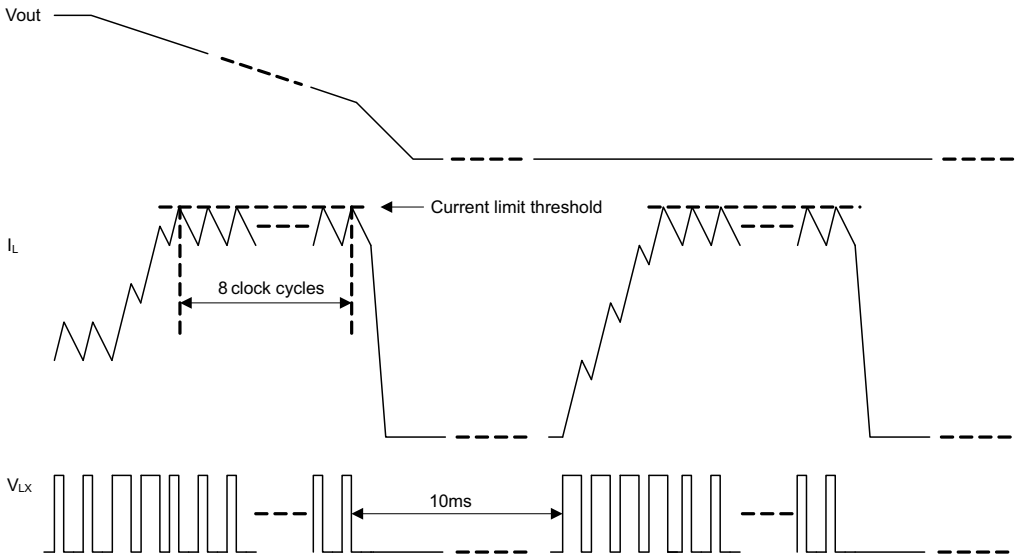


Figure 38. DC/DC Over-Current Protection

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when buck converter is pulled below 91.6% or up 105.4% of the nominal output voltage. The PGOOD is pulled up when buck converters' output is return to more than 94.4% or less than 104.2% of its nominal output voltage.

Inductor Selection

The higher operating frequency allows the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of the inductor value on ripple current and low current operation must also be considered. The ripple current depends on the inductor value. The inductor ripple current, i_L, decreases with higher inductance or higher frequency and increases with higher input voltage, V_{IN}. Accepting larger values of i_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

Use Equation 5 to calculate the value of the output inductor. LIR is a coefficient that represents inductor peak-to-peak ripple to DC load current. It is suggested to use 0.1 ~ 0.3 for most LIR applications.

Actual core loss of the inductor is independent of core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. It results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. It is important that the RMS current and saturation current ratings are not exceeding the inductor specification. The RMS and peak inductor current can be calculated from Equation 7 and Equation 8.

$$L = \frac{V_{in} - V_{out}}{I_O \cdot LIR} \cdot \frac{V_{out}}{V_{in} \cdot fsw} \tag{5}$$

$$\Delta i_L = \frac{V_{in} - V_{out}}{L} \cdot \frac{V_{out}}{V_{in} \cdot fsw} \tag{6}$$

$$i_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \cdot (V_{inmax} - V_{out})}{V_{inmax} \cdot L \cdot fsw}\right)^2}{12}} \tag{7}$$

$$I_{Lpeak} = I_O + \frac{\Delta i_L}{2} \tag{8}$$

For this design example, use LIR = 0.3, and the inductor is calculated to be 5.40 µH with V_{IN} = 12 V. Choose a 4.7 µH standard inductor, the peak to peak inductor ripple is about 34% of 3-A DC load current.

Output Capacitor Selection

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

Equation 9 gives the minimum output capacitance to meet the transient specification. For this example, L_O = 4.7 µH, ΔI_{OUT} = 3 A – 0.0 A = 3 A and ΔV_{OUT} = 500 mV (10% of regulated 5 V). Using these numbers gives a minimum capacitance of 17 µF. A standard 22 µF ceramic capacitor is used in the design.

$$Co > \frac{\Delta I_{OUT}^2 \cdot L}{V_{out} \cdot \Delta V_{out}} \tag{9}$$

The selection of C_{OUT} is driven by the effective series resistance (ESR). Equation 10 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, ΔV_{OUT} is the maximum allowable output voltage ripple, and Δi_L is the inductor ripple current. In this case, the maximum output voltage ripple is 50 mV (1% of regulated 5 V). From Equation 6, the output current ripple is 1 A. From Equation 10, the minimum output capacitance meeting the output voltage ripple requirement is 4.6 µF with 3-mΩ esr resistance.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{\Delta V_{out}}{\Delta i_L} - esr} \tag{10}$$

After considering both requirements, for this example, one 22 µF 6.3 V X7R ceramic capacitor with 3 mΩ of ESR will be used.

Input Capacitor Selection

A minimum 10 µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input pins of the converters, as they handle the RMS ripple current shown in Equation 11. For this example, I_{OUT} = 3 A, V_{OUT} = 5 V, minimum V_{in_min} = 9.6 V. Tthe input capacitors must support a ripple current of 1 A RMS.

$$I_{inrms} = I_{out} \cdot \sqrt{\frac{V_{out}}{V_{inmin}} \cdot \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \tag{11}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 12. Using the design example values, I_{out_max} = 3 A, C_{IN} = 10 µF, f_{SW} = 600 kHz, yields an input voltage ripple of 125 mV.

$$\Delta V_{in} = \frac{I_{outmax} \cdot 0.25}{C_{in} \cdot f_{sw}} \tag{12}$$

To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used.

Bootstrap Capacitor Selection

The external bootstrap capacitor connected to the BST pins supply the gate drive voltages for the topside MOSFETs. The capacitor between BST pin and LX pin is charged through an internal diode from V7V when the LX pin is low. When high side MOSFETs are to be turned on, the driver places the bootstrap voltage across the gate-source of the desired MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, LX, rises to VIN and the BST pin follows. With the internal high side MOSFET on, the bootstrap voltage is above the input supply: $V_{BST} = V_{IN} + V_{7V}$. The selection on bootstrap capacitance is related with internal high side power MOSFET gate capacitance. A 0.047-µF ceramic capacitor is recommended to be connected between the BST to LX pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

Loop Compensation

The integrated buck DC/DC converter in TPS65282 incorporates a peak current mode. The error amplifier is a trans-conductance amplifier with a gain of 600 µA/V. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow these steps:

1. Select switching frequency, f_{SW}, that is appropriate for application depending on L and C sizes, output ripple and EMI. Switching frequency between 500 kHz and 1 MHz gives the best trade off between performance and cost. To optimize efficiency, a lower switching frequency is desired.
2. Set up cross over frequency, fc, which is typically between 1/5 and 1/20 of f_{SW}.
3. RC can be determined by:

$$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}} \tag{13}$$

   where gm is the error amplifier gain (600 µA/V) and gm_{ps} is the power stage voltage to current conversion gain (36 A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole, $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$.

$$C_C = \frac{R_L \cdot Co}{R_C} \tag{14}$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{Resr \cdot Co}{R_C} \tag{15}$$

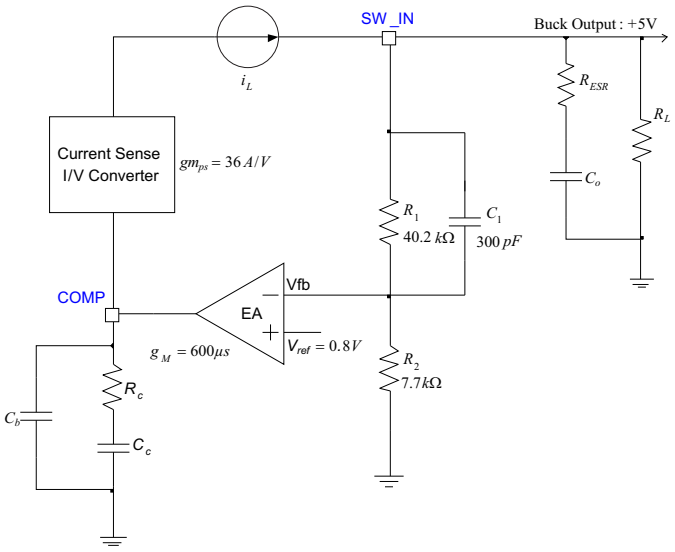


Figure 39. DC/DC Loop Compensation

APPLICATION INORMATION

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the buck converter to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

Power Dissipation and Junction Temperature

The total power dissipation inside TPS65282 should not exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package, θ_{JA}, and ambient temperature. The analysis below gives an approximation in calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

To calculate the temperature inside the device under continuous load, use the following procedure.

1. Define the total continuous current through the buck converter (including the load current through power switches). Make sure the continuous current does not exceed the maximum load current requirement.
2. From the graphs below, determine the expected losses (Y axis) in Watts for the buck converter inside the device. The loss P_{D_BUCK} depends on the input supply and the selected switching frequency. Please note, the data is measured in the provided evaluation board (EVM).
3. Determine the load current I_{OUT} through the power switch. Read $R_{DS(on)}$ of the power switch from the Electrical Characteristics table.
4. The power loss through power switches can be calculated by:
   $$P_{D\_PW} = R_{DS1(on)} \times I_{OUT1} + R_{DS2(on)} \times I_{OUT2} \quad (16)$$
5. The Dissipating Rating Table provides the thermal resistance, θ_{JA}, for specific packages and board layouts.
6. The maximum temperature inside the IC can be calculated by:
   $$T_J = P_{D\_BUCK} + P_{D\_PW} \times \theta_{JA} + T_A \quad (17)$$

   Where:

   T_A = Ambient temperature (°C)

   θ_{JA} = Thermal resistance (°C/W)

   P_{D_BUCK} = Total power dissipation in buck converter (W)

   P_{D_PW} = Total power dissipation in power switches (W)

Auto-Retry Functionality

Some applications require that an over-current condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This auto-retry functionality can be implemented with an external resistor and capacitor shown in Figure 40. During a fault condition, nFAULT pulls low disabling the part. The part is disabled when EN is pulled low, and nFAULT goes high impedance allowing CRETRY to begin charging. The part re-enables when the voltage on EN_SW reaches the turn-on threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

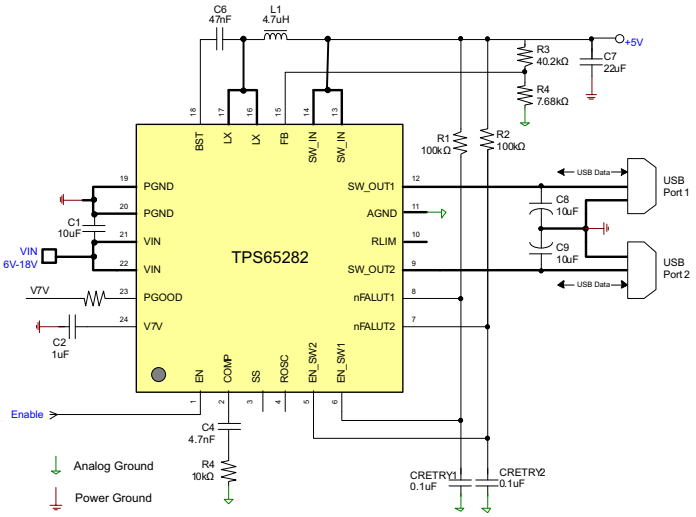


Figure 40. Auto Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. Figure 41 shows how an external logic signal can drive EN_SW through RFAULT and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

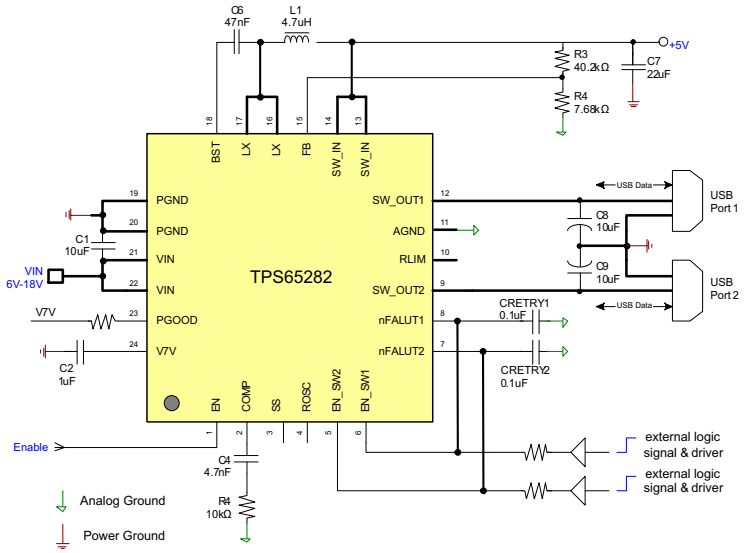


Figure 41. Auto Retry Functionality With External Enable Signal

PCB Layout Recommendation

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 42.

- There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. This capacitor provides the AC current into the internal power MOSFETs. Connect the (+) terminal of the input capacitor as close as possible to the VIN pin, and connect the (-) terminal of the input capacitor as close as possible to the PGND pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the power ground PGND connections.
- Since the LX connection is the switching node, the output inductor should be located close to the LX pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. Keep the switching node, LX, away from all sensitive small-signal nodes.
- Connect V7V decoupling capacitor (connected close to the IC), between the V7V and the power ground PGND pin. This capacitor carries the MOSFET drivers' current peaks.
- Place the output filter capacitor of the buck converter close to SW_IN pins and AGND pin. Try to minimize the ground conductor length while maintaining adequate width.
- The AGND pin should be separately routed to the (-) terminal of V7V bypass capacitor to avoid switching grounding path. A ground plane is recommended connecting to this ground path.
- The compensation should be as close as possible to the COMP pins. The COMP and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of the power components. You can connect the copper areas to PGND, AGND, VIN or any other DC rail in your system.
- There is no electric signal internal connected to thermal pad in the device. Nevertheless connect the exposed pad beneath the IC to ground. Always solder the thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation.

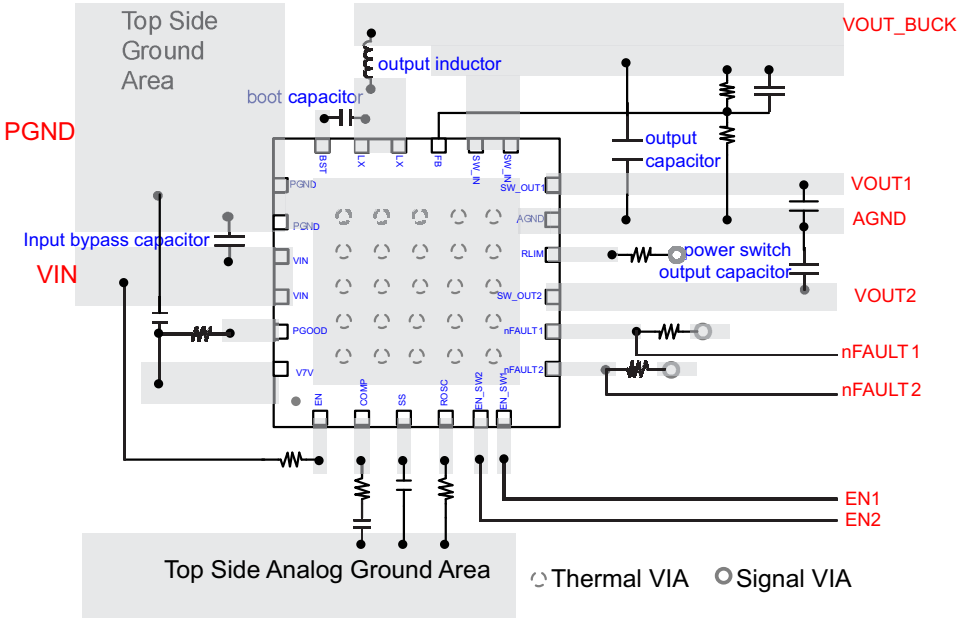


Figure 42. 2-Layers PCB Layout Recommendation Diagram

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65282RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65282
TPS65282RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65282

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

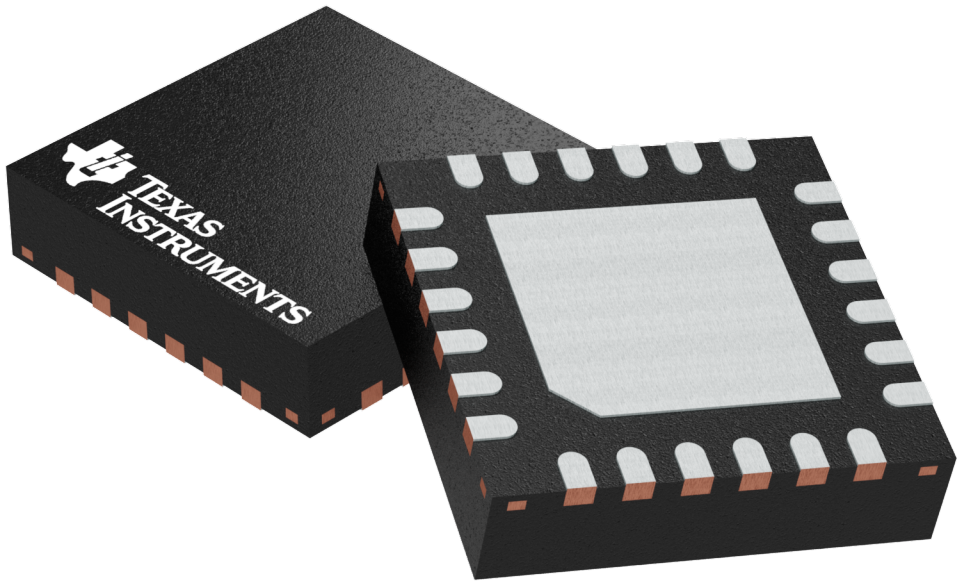
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

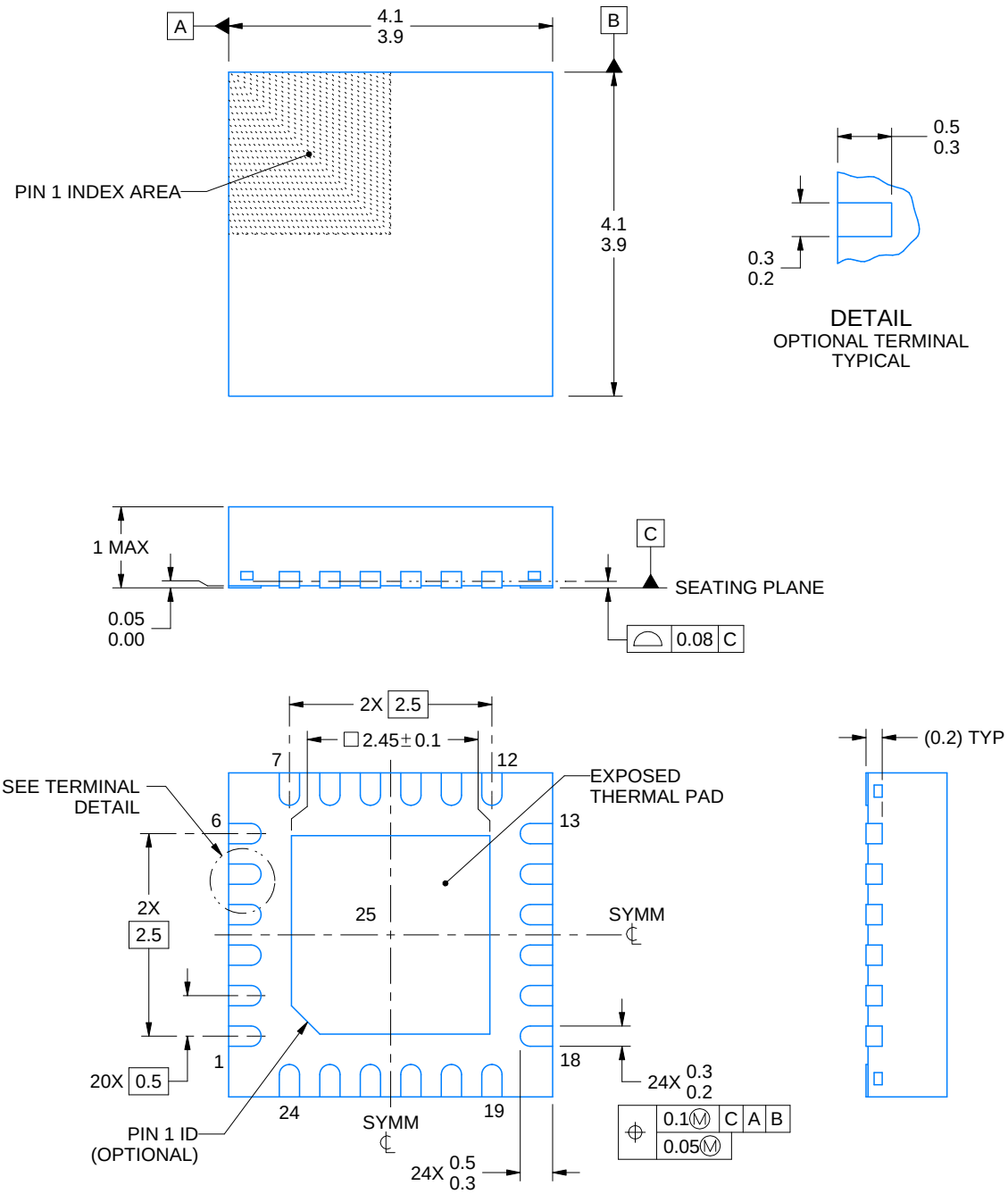
4204104/H

PACKAGE OUTLINE

RGE0024B

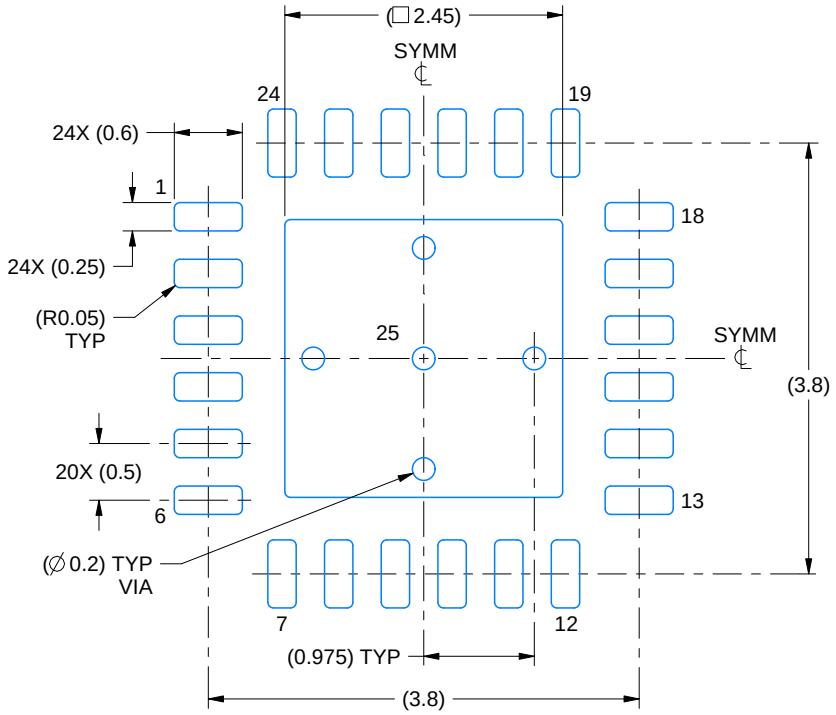
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

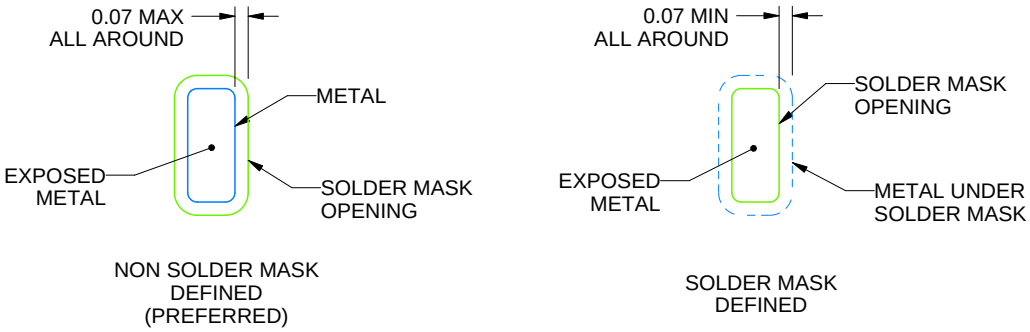


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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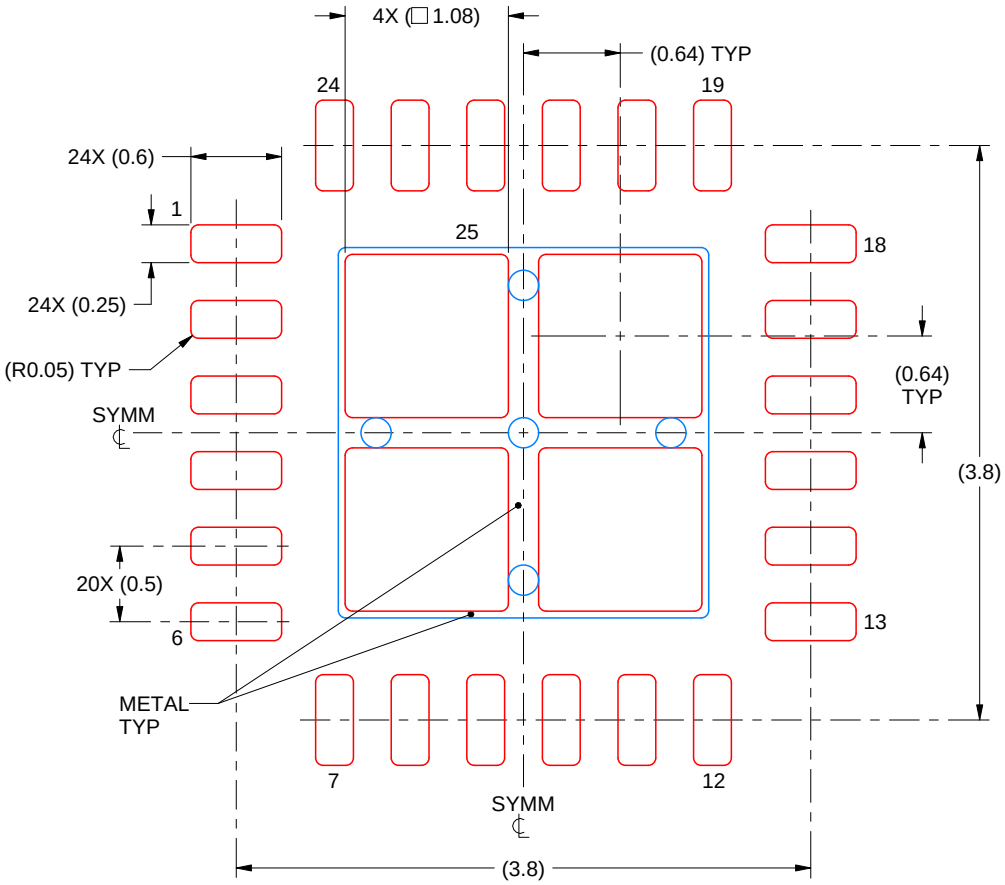
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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