1.5-A, Low-Voltage LDO Regulator with Dual Input Voltages

FEATURES

- **Small Consumption Current: 3 mA Maximum**
- **Input Voltage Range:**
  - **V_{IN}: 1.2 V to 6.0 V**
  - **V_{BIAS}: 2.9 V to 6.0 V**
- **Stable with Any Output Capacitance: ≥ 2.2 µF**
- **±1% Initial Accuracy**
- **Maximum Dropout Voltage (V_{IN} – V_{OUT}): 300 mV Over Temperature**
- **Adjustable Output Voltage: Down to 0.9 V**
- **Ultra-Fast Transient Response**
- **Excellent Line and Load Regulation**
- **Logic-Controlled Shutdown Option**
- **Thermal Shutdown and Current Limit Protection**
- **Power 8-Pin Mini Small-Outline Package (MSOP) and Jr S-PAK™ packages.**
- **Junction Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Graphics Processors**
- **PC Add-In Cards**
- **Microprocessors**
- **Low-Voltage Digital ICs**
- **High-Efficiency Linear Power Supplies**
- **Switch-Mode Power-Supply Post Regulation**

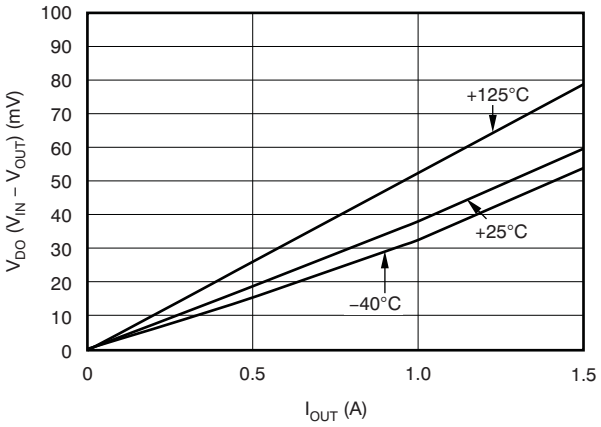
DESCRIPTION

The TPS740xx is a wide bandwidth, very low-dropout, 1.5-A voltage regulator ideal for powering microprocessors.

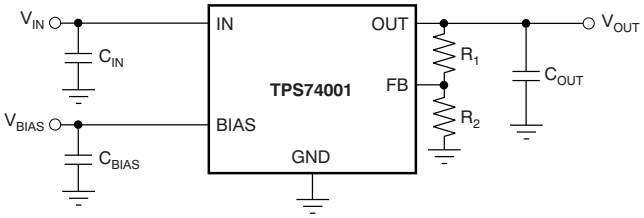
The TPS740xx uses a bias input supply to allow very low voltage of a main input supply. The main input supply operates from 1.2 V to 6.0 V and the bias input supply requires between 3.0 V to 6.0 V for proper operation. The TPS740xx offers adjustable output voltages down to 0.9 V.

The TPS740xx requires a minimum of output capacitance. A small 2.2-µF ceramic capacitor is enough for its stability.

The TPS740xx is available in an 8-pin power MSOP package and a 5-pin Jr S-PAK. Its operating temparature range is –40°C to +125°C.



Dropout Voltage



Typical Application Circuit (Adjustable)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS740**xx** ***yyy z***	**XX** is nominal output voltage (for example, 12 = 1.2 V, 15 = 1.5 V, 01 = Adjustable).(3) **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Fixed output voltages of 1.2 V is available; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 0.9-V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN, BIAS	–0.3	+6.5	V
	EN, FB, OUT	–0.3	V_{BIAS} + 0.3(2)	V
Current	OUT	Internally limited		A
Electrostatic discharge rating(3)	Human body model (HBM, JESD22-A114A)		2	kV
	Charged device model (CDM, JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{BIAS} + 0.3 V or +6.0 V, whichever is smaller.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS74001DGK	TPS74001DPT(3)	UNITS
		DGK (4 pin short)	DPT	
		8 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(4)	136.9	30.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(5)	35.3	15.3	
θ_{JB}	Junction-to-board thermal resistance(6)	68.0	14.4	
ψ_{JT}	Junction-to-top characterization parameter(7)	0.9	0.6	
ψ_{JB}	Junction-to-board characterization parameter(8)	67.8	14.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(9)	n/a	5.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DGK and DPT packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) DPT only, the exposed pad is connected to the PCB ground layer through a 8 × 8 thermal via array.
  (b) i. DPT: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  ii. DGK: The top copper layer has a dedicated pattern of 5% copper coverage and the bottom copper layer has another decicated pattern of 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = V_{OUT} + 2.0 V, V_{IN} = V_{OUT} + 1 V, C_{OUT} = 10 µF, following Recommended Resistor Values, and V_{EN} = 1.1 V, unless otherwise noted. Typical values are at T_J = +25°C. TPS74001 (adjustable output voltage) is tested at V_{OUT} = 0.9 V.

PARAMETER		TEST CONDITIONS	TPS740xx			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		1.2		6.0	V
V_{BIAS}	Bias pin voltage range		2.9		6.0	V
V_{OUT}	Accuracy(1)	T_J = 25°C	–1		1	%
		T_J = –40°C to +125°C	–2		2	%
V_{OUT}/V_{IN}	Line regulation	V_{IN} = V_{OUT} + 1 V to 6.0 V	–0.1	0.01	0.1	%/V
V_{OUT}/I_{OUT}	Load regulation	I_{LOAD} = 0 mA to 1.5 A(2)			1.5	%
V_{DO}	V_{IN} dropout voltage(3)	I_{LOAD} = 1.5 A		100	300	mV
	V_{BIAS} dropout voltage(3)	I_{LOAD} = 1.5 A, V_{IN} = V_{BIAS}		1.3	1.6	V
I_{GND}	Ground pin current(4)	I_{LOAD} = 1.5 A		2	3	mA
I_{SHDN}	Shutdown supply current (I_{GND})	Fixed output version only. V_{EN} ≤ 0.4 V, T_J = –40°C to +85°C, V_{OUT} = 0 V		1	5	µA
I_{BIAS}	Bias pin current	I_{LOAD} = 1.5 A			2	mA
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT\ (NOM)}$	1.6		6.0	A
$V_{EN,\ HI}$	Enable input high level		1.1		6.0	V
$V_{EN,\ LO}$	Enable input low level	R_{LOAD} = 1 kΩ to GND	0		0.4	V
I_{EN}	Enable pin current	V_{EN} = 1.5 V		0.1	1	µA
T_J	Operating junction temperature		–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+165		°C
		Reset, temperature decreasing		+140		
V_{REF}	Reference voltage		0.882	0.9	0.918	V

(1) Adjustable output voltage devices: resistor tolerance is not taken into account.
(2) With a fixed output device, this test condition is I_{LOAD} = 50 mA to 1.5 A.
(3) Dropout is defined as the voltage from the input voltage to V_{OUT} when V_{OUT} is 3% below nominal.
(4) I_{GND}(MAX) = 3 mA includes the maximum 2 mA of I_{BIAS}.

FUNCTIONAL BLOCK DIAGRAMS

Adjustable Output Voltage Version

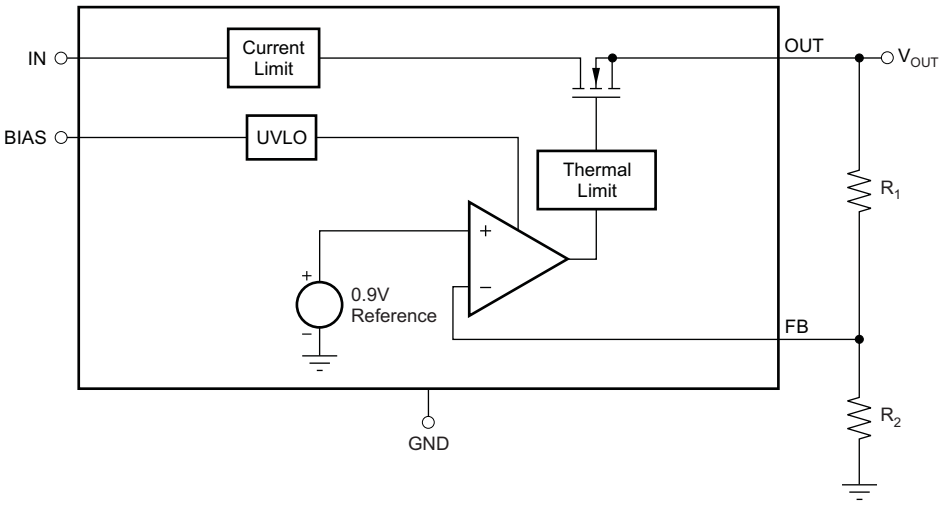


Figure 1.

Fixed Output Voltage Version

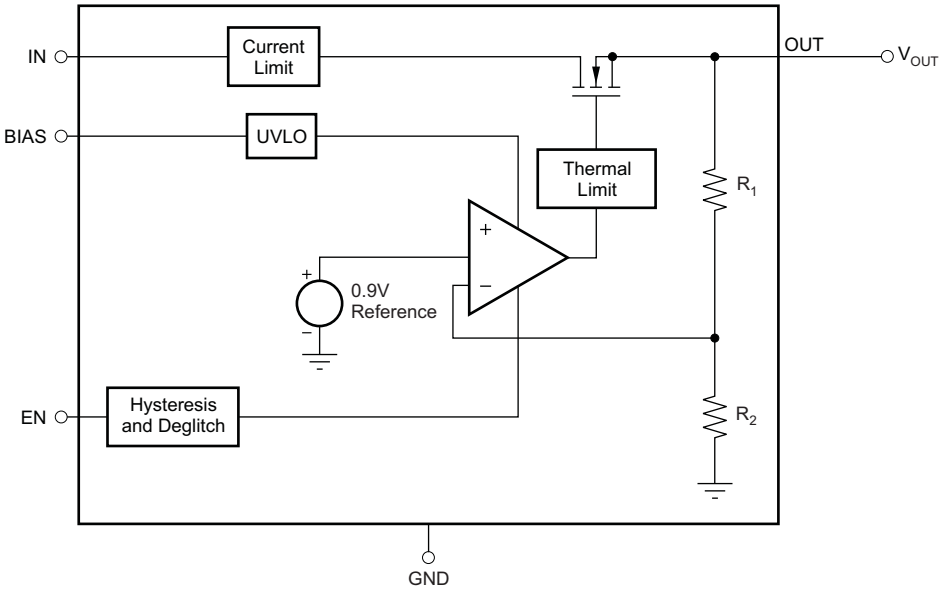
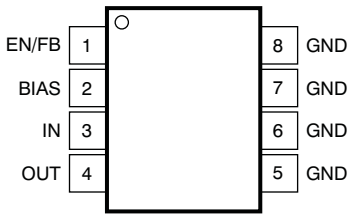


Figure 2.

PIN CONFIGURATION

DGK PACKAGE
MSOP-8
(TOP VIEW)



DPT PACKAGE
Jr S-PAK
(TOP VIEW)

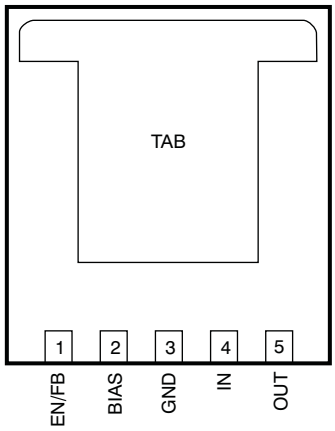


Table 1. TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	DGK (MSOP-8)	DPT (Jr S-PAK)	
EN	1	1	Enable pin; fixed output voltage version only. Driving this pin high enables the regulator; driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
FB	1	1	Feedback pin; adjustable output voltage version only. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
BIAS	2	2	Bias input voltage for error amplifier, reference, and internal control circuits.
IN	3	4	Input to the device.
OUT	4	5	Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2 µF, ceramic) is needed from this pin to ground to assure stability.
GND	5-8	3	Ground
TAB		TAB	Internally connected to ground

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = 2.5 V, V_{BIAS} = 5.0 V, $V_{OUT(target)}$ = 1.5 V, V_{EN} = V_{BIAS}, C_{IN} = 2.2 µF, C_{BIAS} = 2.2 µF, and C_{OUT} = 10 µF, unless otherwise noted.

POWER-SUPPLY RIPPLE REJECTION (INPUT SUPPLY)

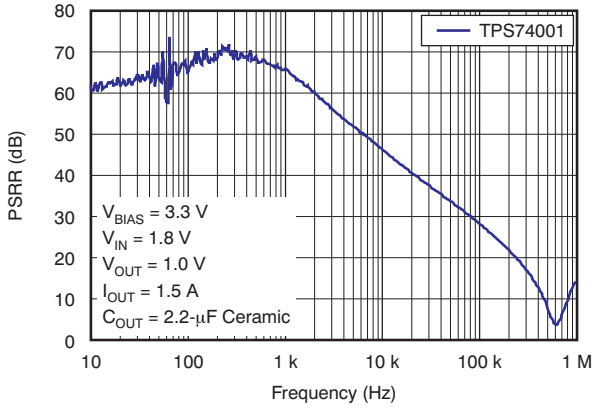


Figure 3.

POWER-SUPPLY RIPPLE REJECTION (BIAS SUPPLY)

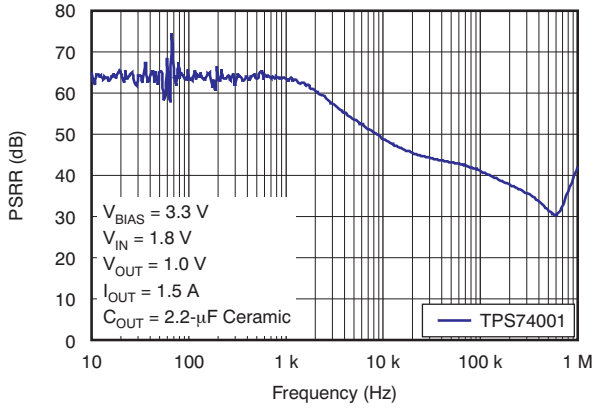


Figure 4.

DROPOUT VOLTAGE (INPUT SUPPLY)

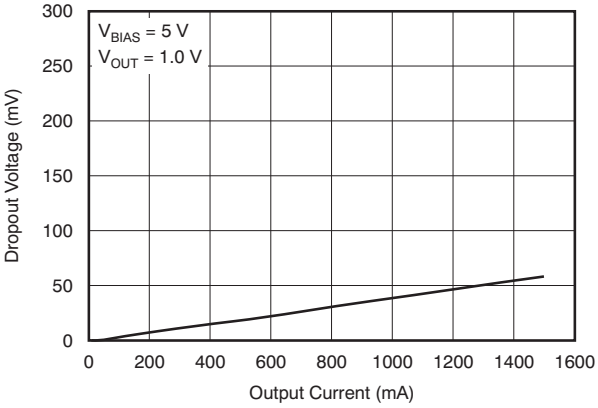


Figure 5.

DROPOUT VOLTAGE (BIAS SUPPLY)

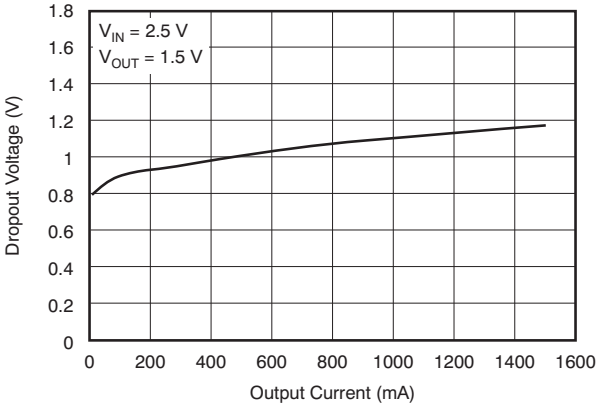


Figure 6.

DROPOUT VOLTAGE vs TEMPERATURE (INPUT SUPPLY)

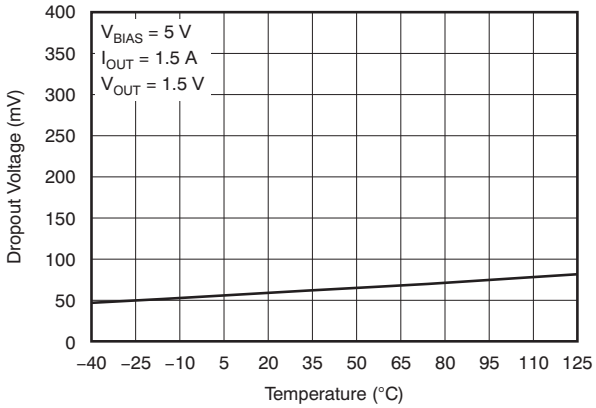


Figure 7.

DROPOUT VOLTAGE vs TEMPERATURE (BIAS SUPPLY)

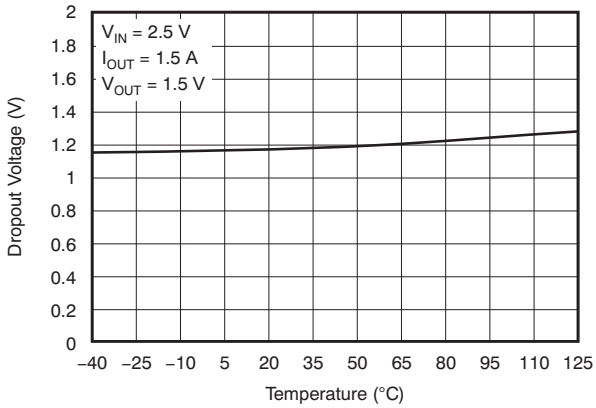


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = 2.5 V, V_{BIAS} = 5.0 V, $V_{OUT(target)}$ = 1.5 V, V_{EN} = V_{BIAS}, C_{IN} = 2.2 µF, C_{BIAS} = 2.2 µF, and C_{OUT} = 10 µF, unless otherwise noted.

DROPOUT CHARACTERISTICS (INPUT VOLTAGE)

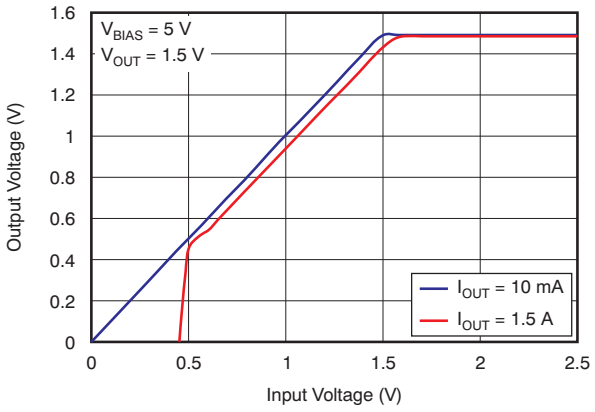


Figure 9.

DROPOUT CHARACTERISTICS (BIAS VOLTAGE)

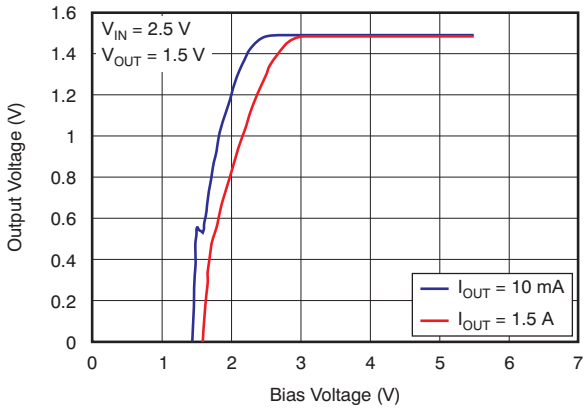


Figure 10.

LOAD REGULATION

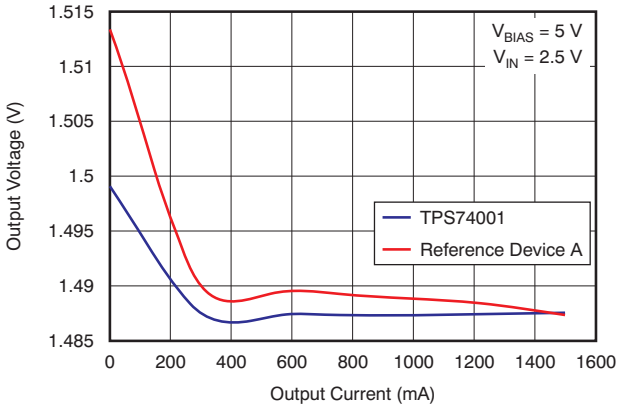


Figure 11.

MAXIMUM BIAS CURRENT vs BIAS VOLTAGE(1)

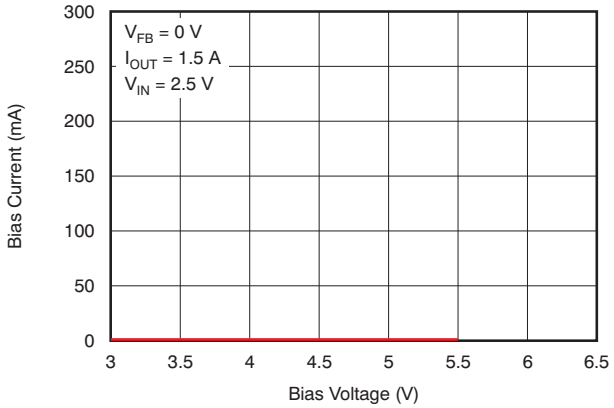


Figure 12.

MAXIMUM BIAS CURRENT vs TEMPERATURE

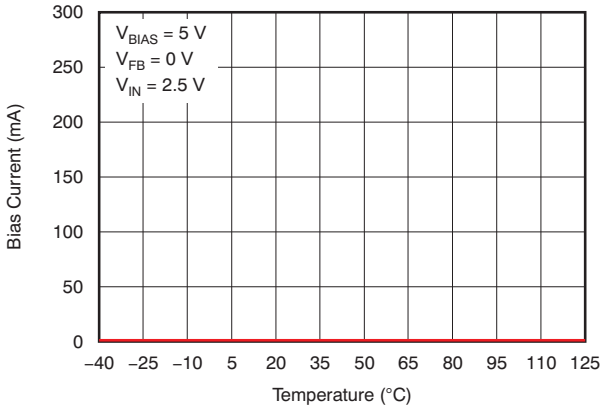


Figure 13.

BIAS CURRENT vs TEMPERATURE

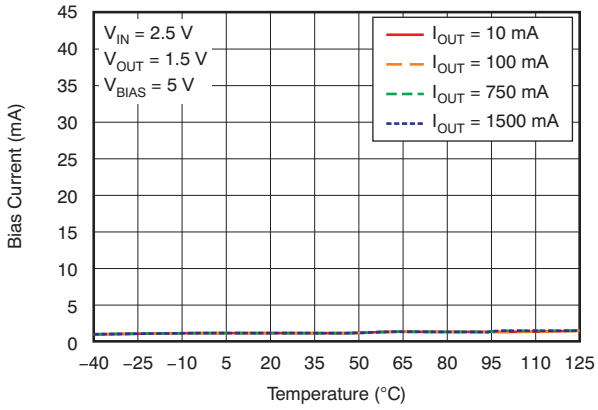


Figure 14.

(1) This device does not show large bias current at any condition.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = 2.5 V, V_{BIAS} = 5.0 V, $V_{OUT(target)}$ = 1.5 V, V_{EN} = V_{BIAS}, C_{IN} = 2.2 µF, C_{BIAS} = 2.2 µF, and C_{OUT} = 10 µF, unless otherwise noted.

BIAS CURRENT vs OUTPUT CURRENT

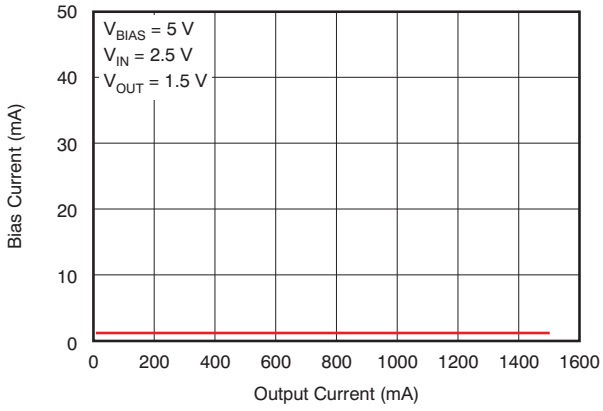


Figure 15.

GROUND CURRENT vs BIAS VOLTAGE

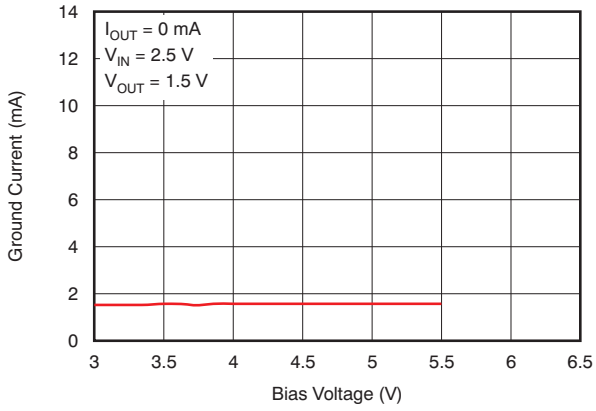


Figure 16.

BIAS CURRENT vs BIAS VOLTAGE

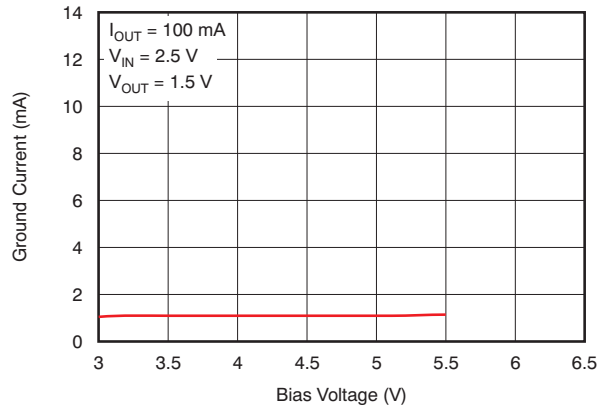


Figure 17.

BIAS CURRENT vs BIAS VOLTAGE

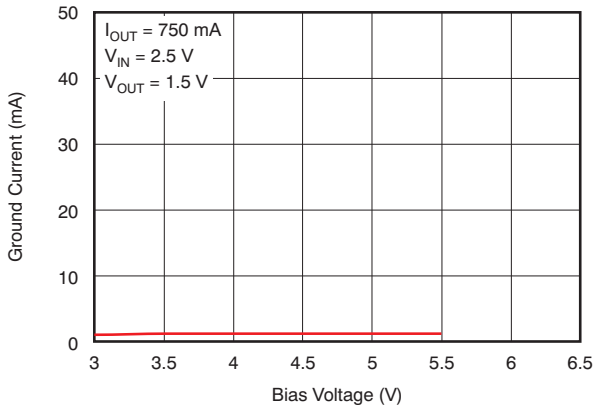


Figure 18.

BIAS CURRENT vs BIAS VOLTAGE

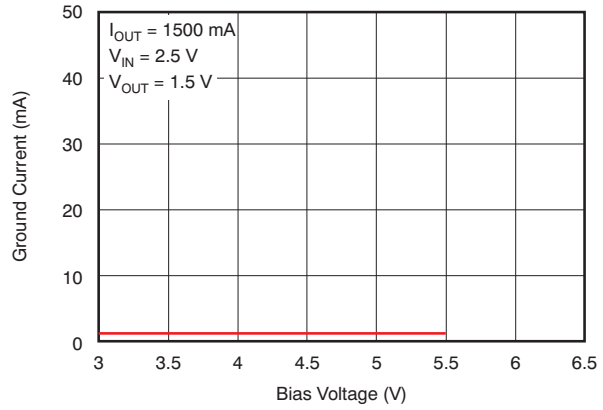


Figure 19.

BIAS CURRENT vs INPUT VOLTAGE

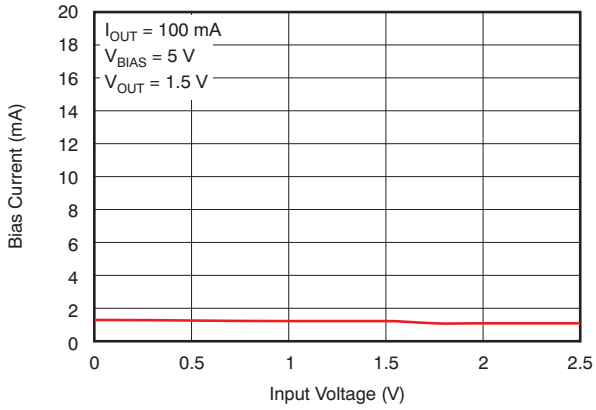


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = 2.5 V, V_{BIAS} = 5.0 V, $V_{OUT(target)}$ = 1.5 V, V_{EN} = V_{BIAS}, C_{IN} = 2.2 µF, C_{BIAS} = 2.2 µF, and C_{OUT} = 10 µF, unless otherwise noted.

BIAS CURRENT vs INPUT VOLTAGE

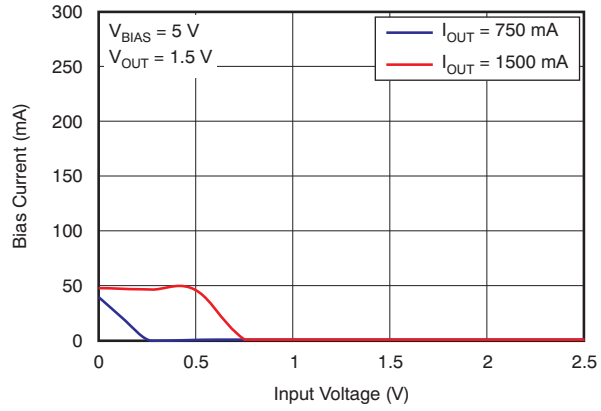


Figure 21.

REFERENCE VOLTAGE vs INPUT VOLTAGE

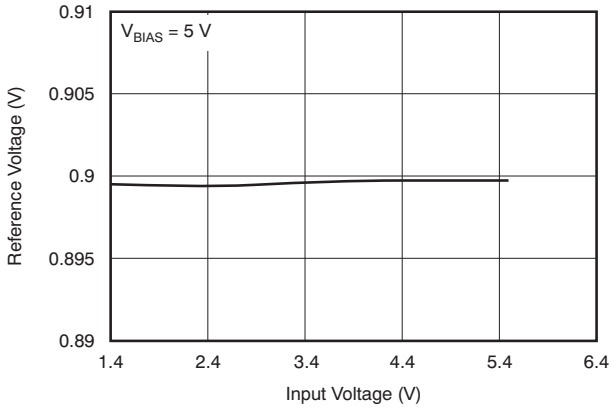


Figure 22.

REFERENCE VOLTAGE vs BIAS VOLTAGE

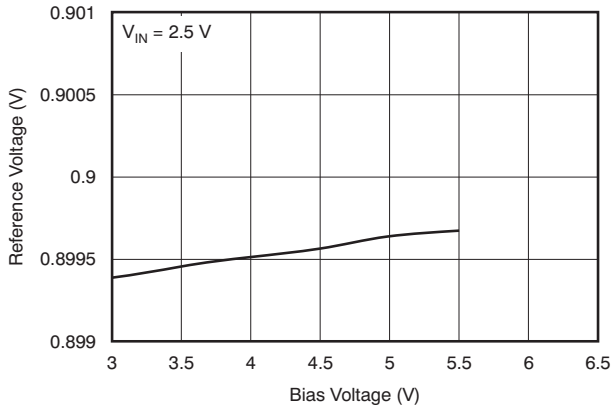


Figure 23.

OUTPUT VOLTAGE vs TEMPERATURE

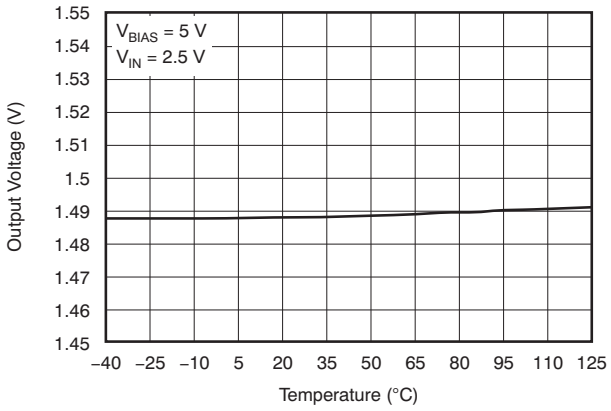


Figure 24.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

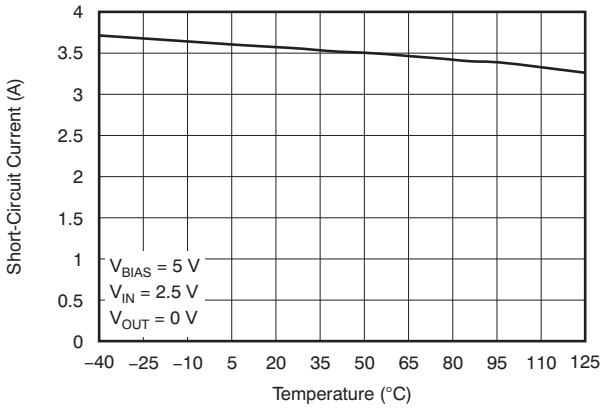


Figure 25.

ENABLE THRESHOLD vs BIAS VOLTAGE

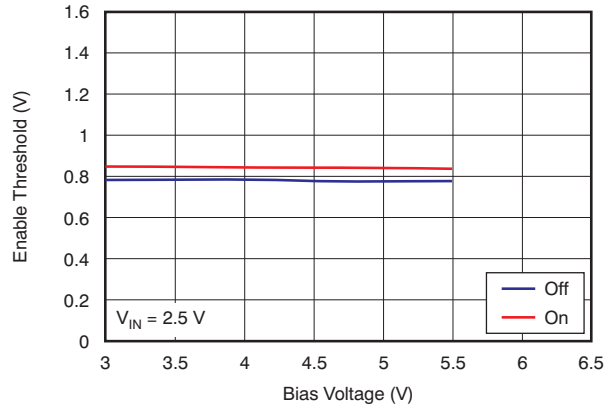


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = 2.5 V, V_{BIAS} = 5.0 V, $V_{OUT(target)}$ = 1.5 V, V_{EN} = V_{BIAS}, C_{IN} = 2.2 µF, C_{BIAS} = 2.2 µF, and C_{OUT} = 10 µF, unless otherwise noted.

ENABLE THRESHOLD vs TEMPERATURE

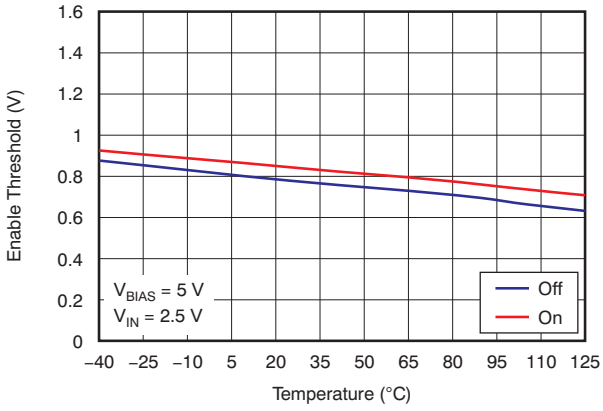


Figure 27.

LOAD TRANSIENT RESPONSE

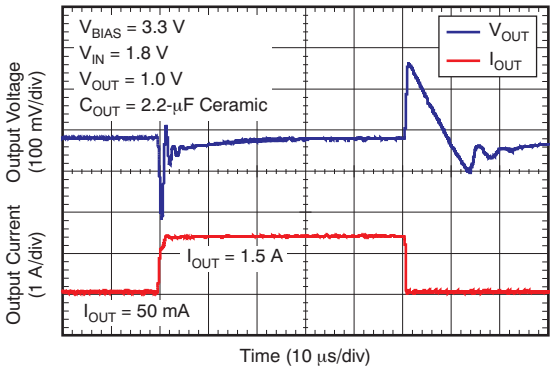


Figure 28.

BIAS VOLTAGE LINE TRANSIENT RESPONSE

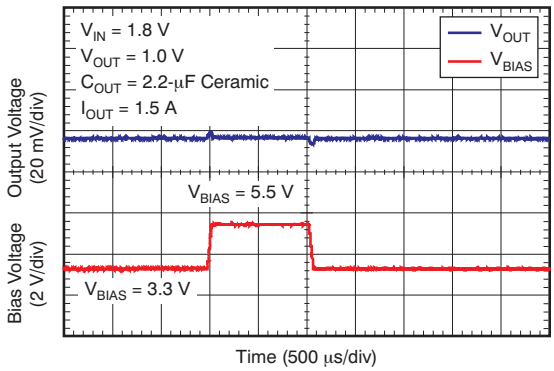


Figure 29.

INPUT VOLTAGE LINE TRANSIENT RESPONSE

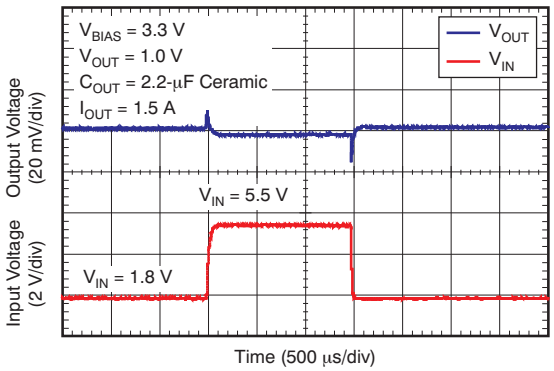


Figure 30.

APPLICATION INFORMATION

The TPS740xx belongs to a family of low dropout (LDO) regulators. These regulators use a low-current bias input to power all internal control circuitry, allowing the NMOS-pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS740xx to be stable with any capacitor type of 2.2 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

With the fixed output voltage version, an enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability is ideal for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

Figure 31 illustrates the typical application circuit for the TPS74001 adjustable output device.

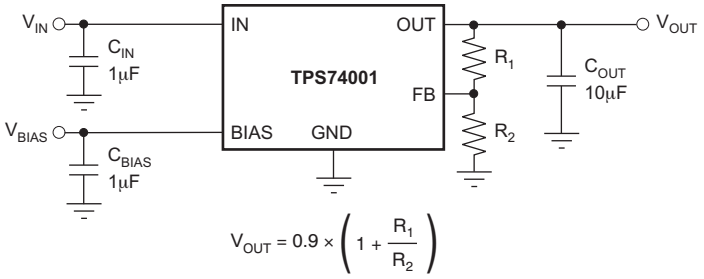


Figure 31. Typical Application Circuit for the TPS74001 (Adjustable)

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 31. Table 2 lists sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 is recommended to be lower than 4.99 kΩ.

Figure 32 illustrates the typical application circuit for the TPS740xx fixed output device.

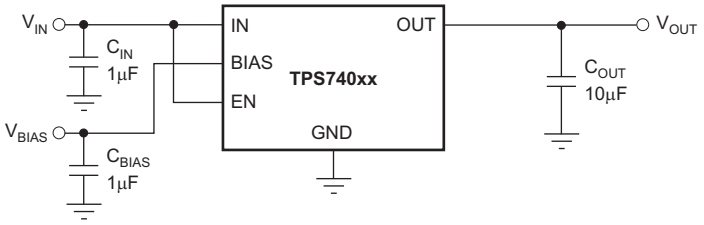


Figure 32. Typical Application Circuit for the TPS740xx (Fixed Voltage Versions)

Table 2. Standard 1% Resistor Values for Programming the Output Voltage

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.9
0.562	5.11	1.0
0.75	4.53	1.05
1.07	4.99	1.1
1.58	4.75	1.2
1.91	2.87	1.5
2.43	2.43	1.8
3.01	1.69	2.5
4.22	1.58	3.3
5.23	1.74	3.6

INPUT, OUTPUT, AND BIAS CAPACITOR REQUIREMENTS

The device is designed to be stable for all available types and values of output capacitors greater than or equal to 2.2 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good-quality, low-ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close to the pins as possible for optimum performance.

TRANSIENT RESPONSE

The TPS740xx is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In these cases, adding additional input capacitance improves the transient response much more than simply adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; refer to the Typical Characteristics section. Because the TPS740xx is stable with output capacitors as low as 2.2 µF, many applications may then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

DROPOUT VOLTAGE

The TPS740xx offers very low dropout performance, making it well-suited for high-current, low V_{IN}/low V_{OUT} applications. The low dropout of the TPS740xx allows the device to be used in place of a dc/dc converter and still achieve good efficiency. This performance provides designers with the power architecture for the application to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS740xx. The first specification (shown in Figure 33) is referred to as *V_{IN} Dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 2.0 V above V_{OUT}. If V_{BIAS} is higher than V_{OUT} + 2.0 V, V_{IN} dropout is less than specified.

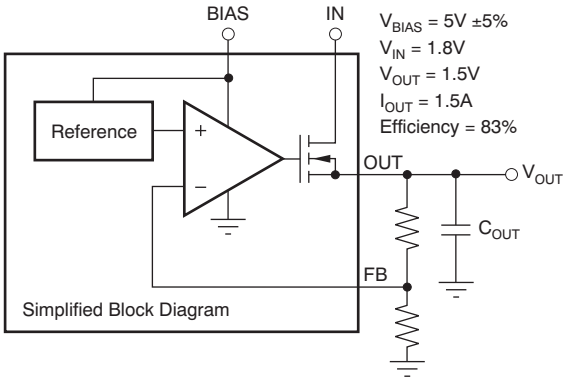


Figure 33. Typical Application of the TPS74001 Using an Auxiliary Bias Rail

The second specification (shown in Figure 34) is referred to as *V_{BIAS} Dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET; therefore, V_{BIAS} must be 2.0 V above V_{OUT}. Because of this usage, when IN and BIAS are tied together they easily consume large amounts of power. Do not to exceed the power rating of the IC package.

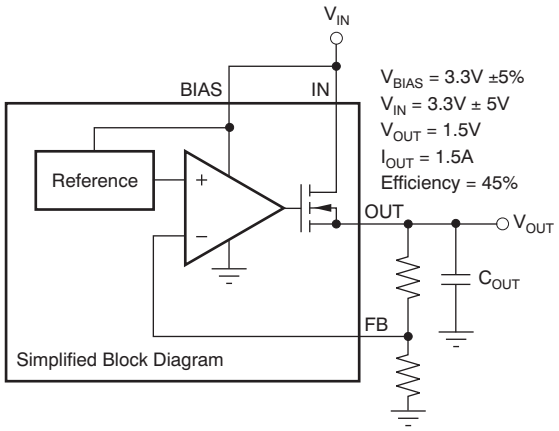


Figure 34. Typical Application of the TPS74001 Without an Auxiliary Bias Rail

SEQUENCING REQUIREMENTS

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device.

NOTE: When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

ENABLE/SHUTDOWN (Fixed Voltage Version Only)

The enable (EN) pin is active high and is compatible with standard digital signaling levels. When V_{EN} is below 0.4 V, it turns the regulator off; when V_{EN} is above 1.1 V, it turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slow ramping analog signals. This configuration allows the TPS740xx to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on/off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4 V and 1.1 V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS740xx.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

INTERNAL CURRENT LIMIT

The TPS740xx features a current limit that is flat over temperature and supply voltage. The current limit responds in approximately 10µs to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS740xx is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS740xx above the rated current degrades device reliability.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS740xx is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS740xx into thermal shutdown degrades device reliability.

LAYOUT RECOMMENDATIONS AND POWER DISSIPATION

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 31 should be connected as close as possible to the load. If BIAS is connected to IN, it is recommended to connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 1:

$$PD = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the DGK (MSOP-8) package, the primary conduction path for heat is through four GND pins (right side of the IC) to the printed circuit board (PCB). On the DPT (Jr S-PAK) package, the primary conduction path for heat is through the tab to the PCB. This tab should be connected to ground. On both packages, ground pattern on PCB should have an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 2:

$$R_{\theta JA} = \frac{(+125°C – T_A)}{P_D} \quad (2)$$

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2011) to Revision C **Page**

- Changed upper voltage in both sub-bullets of second Features bullet 1
- Changed input supply description in the *Description* section 1
- Changed V_{OUT} parameter test conditions in Electrical Characteristics table 4
- Added footnote 2 to Electrical Characteristics table 4
- Changed $V_{EN,\ HI}$ parameter maximum specification in Electrical Characteristics table 4

Changes from Revision A (June 2011) to Revision B **Page**

- Changed *Voltage IN, BIAS* parameter maximum specification in Absolute Maximum Ratings table 2
- Changed V_{IN} and V_{BIAS} parameter maximum specifications in Electrical Characteristics table 4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS74001DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXE
TPS74001DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXE
TPS74001DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXE
TPS74001DGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXE
TPS74012DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXF
TPS74012DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXF
TPS74012DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXF
TPS74012DGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QXF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

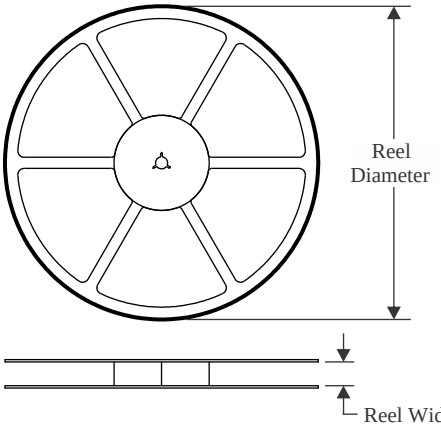
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

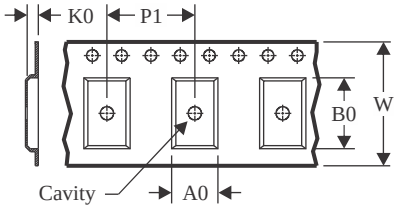
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

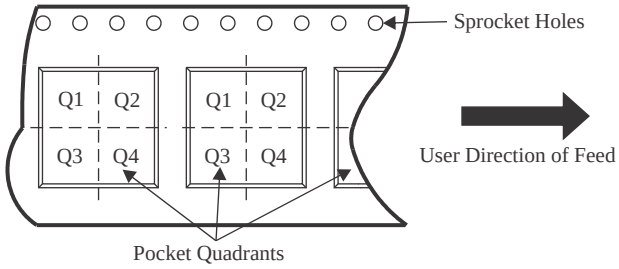


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

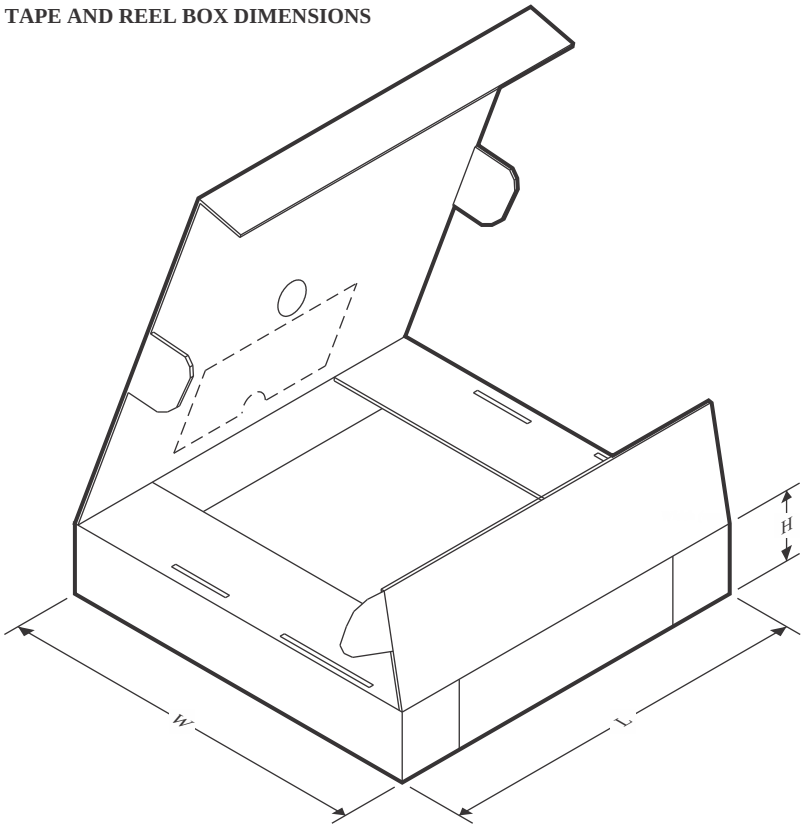
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74001DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS74001DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS74012DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS74012DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

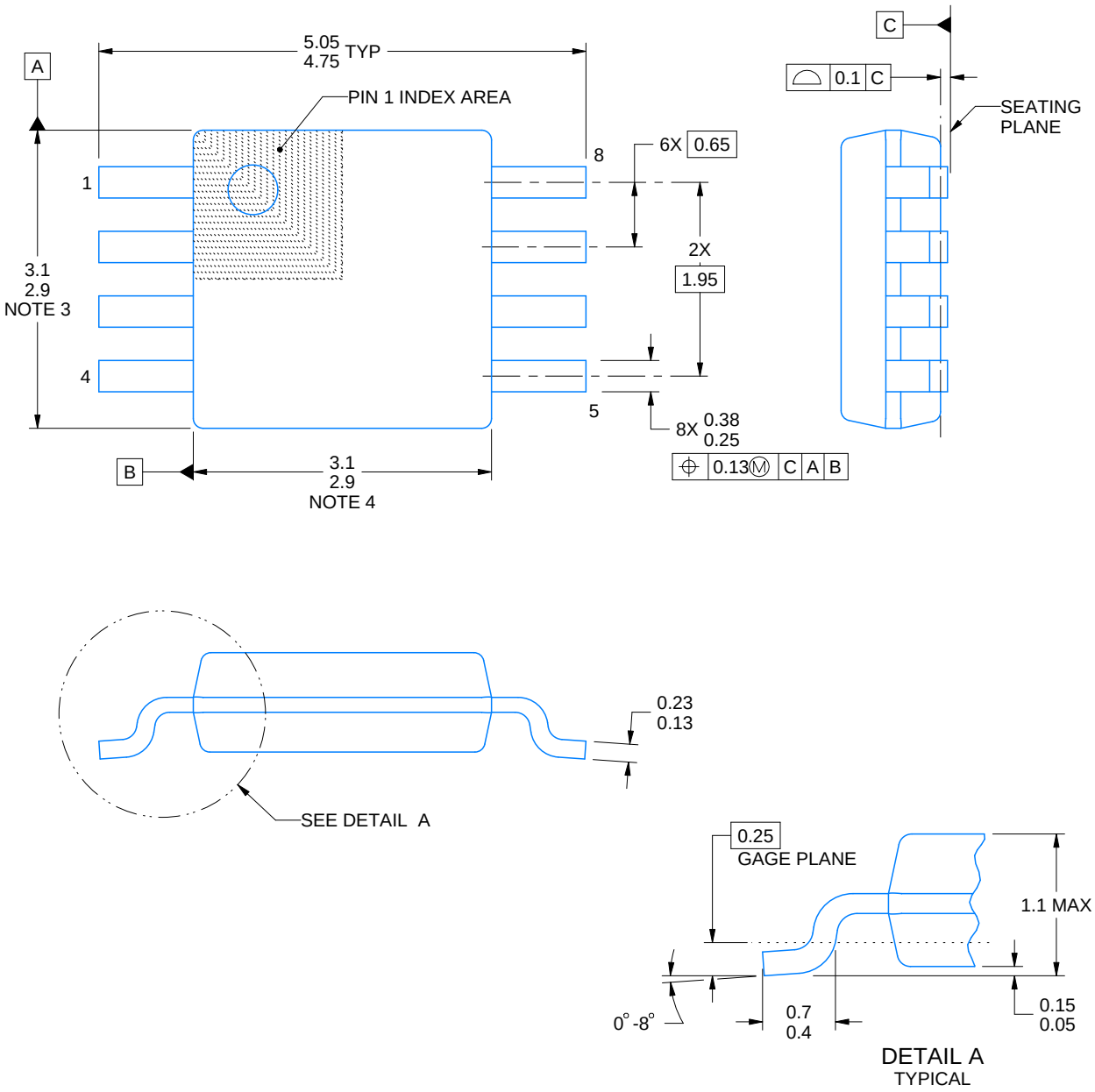
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74001DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TPS74001DGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
TPS74012DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TPS74012DGKT	VSSOP	DGK	8	250	213.0	191.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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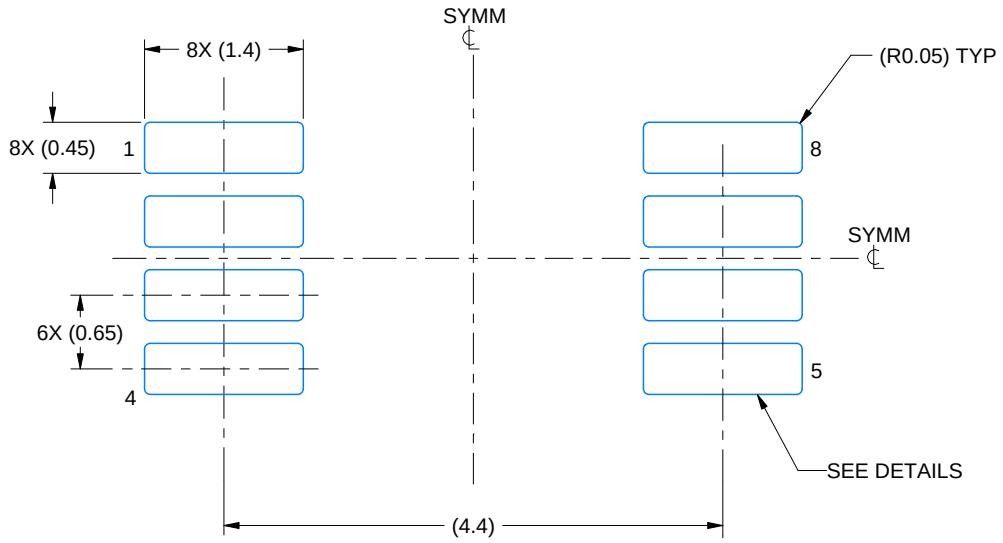
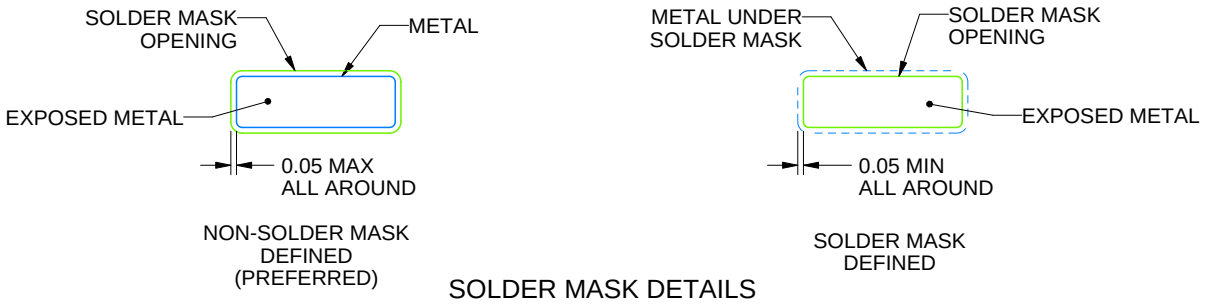
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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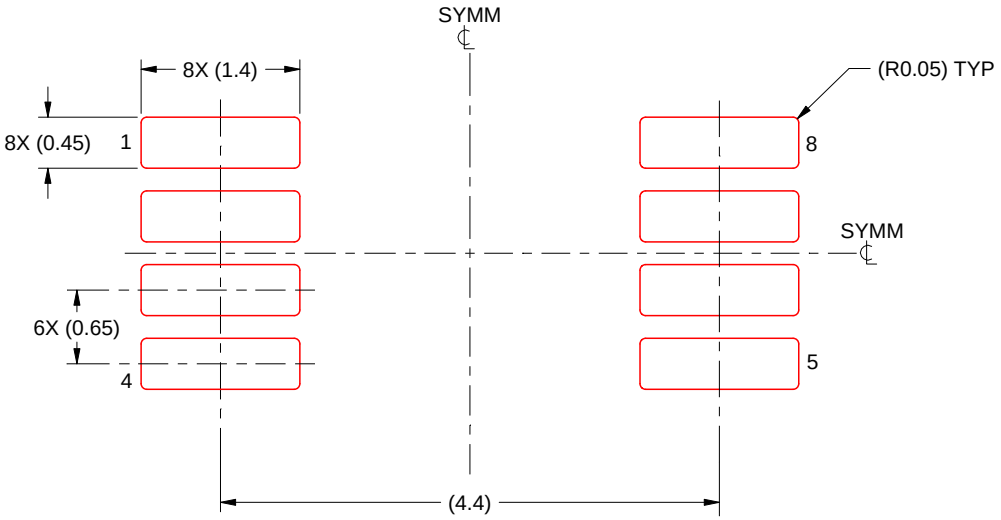
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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