TPS7A6x-Q1 高电压、超低 $I_{(q)}$、低压降稳压器

1 特性

- 符合汽车应用 应用
- 具有符合 AEC-Q100 测试指导的以下结果：
  - 将整个文档中的器件温度等级 1
  - 器件温度等级 0 级（仅限 TPS7A6650EDGNRQ1）
  - 器件人体放电模型 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件带电器件模型 (CDM) ESD 分类等级 C4
- 器件结温范围：–40°C 至 +150°C
- 4V 至 40V 宽输入电压范围，瞬态电压高达 45V
- 输出电流：150mA
- 低静态电流，$I_{(q)}$：
  - EN = 低电平（关断模式）时为 2μA
  - 轻负载时典型值为 12μA
- 低等效串联电阻 (ESR) 陶瓷输出稳定电容器 (2.2μF-100μF)
- 150mA 时的压降电压为 300mV（$V_{(Vin)}$= 4V 时的典型值）
- 固定（3.3V 和 5V）和可调（1.5V 至 5V）输出电压（可调输出电压仅适用于 TPS7A66-Q1）
- 低输入电压跟踪
- 集成型加电复位：
  - 可编程复位脉冲延迟
  - 漏极开路复位输出
- 集成故障保护：
  - 热关断
  - 短路保护功能
- 输入电压检测比较器（仅限 TPS7A69-Q1）
- 封装：
  - 8 引脚 SOIC-D (TPS7A69-Q1)
  - 8 引脚 HVSSOP-DGN (TPS7A6601-Q1)

2 应用

- 具有睡眠模式的信息娱乐系统
- 车身控制模块
- 常开电池 标准：
  - 网关 应用
  - 遥控免钥匙进入系统
  - 发动机防盗系统

3 说明

TPS7A66-Q1 和 TPS7A69-Q1 是针对输入电压高达 40V 的运行电路而设计的低压降线性稳压器。这些器件在无负载时的静态电流仅为 12μA，非常适合待机微处理器控制单元系统，尤其是汽车 应用低功耗是一个关键问题。

此器件特有集成的短路和过流保护。此器件在加电时执行复位延迟以表示输出电压稳定且在稳压中。用户可使用一个外部电容器来设定此延迟。低压跟踪特性允许使用更小的输入电容器并且有可能在冷启动条件下无需使用升压转换器。

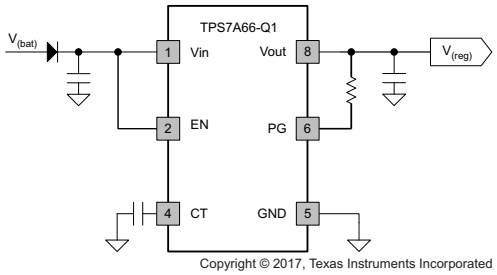
此器件运行在 -40°C 至 125°C 的温度范围内。TPS7A6650EDGNRQ1 器件符合 AEC-Q100 0 级标准，工作温度范围为 –40°C 至 150°C。这些 特性 非常适用于各类汽车应用中的 电源中对于高效率、高电源密度和稳健性的需求。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A66-Q1	HVSSOP (8)	3.00mm × 3.00mm
TPS7A69-Q1	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

硬件启用选项



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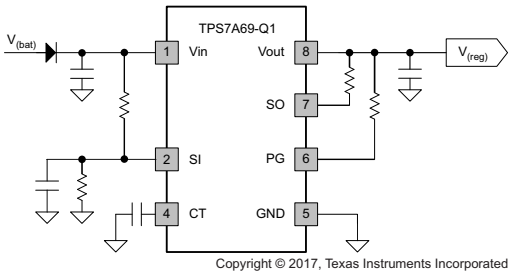
输入电压感测选项



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目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 4
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 7
6.7 Typical Characteristics ... 8
7 **Detailed Description** ... 11
7.1 Overview ... 11
7.2 Functional Block Diagrams ... 11
7.3 Feature Description ... 13
7.4 Device Functional Modes ... 17
8 **Application and Implementation** ... 18
8.1 Application Information ... 18
8.2 Typical Applications ... 18
9 **Power Supply Recommendations** ... 21
10 **Layout** ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Examples ... 21
10.3 Power Dissipation and Thermal Considerations ... 22
11 器件和文档支持 ... 23
11.1 相关链接 ... 23
11.2 接收文档更新通知 ... 23
11.3 社区资源 ... 23
11.4 商标 ... 23
11.5 静电放电警告 ... 23
11.6 Glossary ... 23
12 机械、封装和可订购信息 ... 23

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (November 2014) to Revision F **Page**

- 已更改 *AEC-Q100 测试指南* 特性 列表项并从前两个 AEC-Q100 子列表项中删除了温度范围 ... 1
- 已更改 $V_{(Vin)}$ 更改为 V_{IN}、将 Vin 更改为 VIN、将 V（输出电压）更改为 V_{OUT}，将 Vout 更改为 VOUT，以及将 $V_{(CT)}$ 更改为 V_{CT} ... 1
- 已添加 *器件结温范围* 特性 要点 ... 1
- 已更改 将整个文档中的相关器件更改成了 TPS7A66-Q1 和 TPS7A69-Q1 ... 1
- 已更改 将整个文档中的 MSOP 更改为 HVSSOP ... 1
- Changed CT, EN, FB/DNC, PG, SO, and VOUT descriptions in *Pin Functions* table ... 4
- Changed pin names FB/NU to FB/DNC, Vin to VIN, and Vout to VOUT in *Pin Configuration and Functions* section ... 4
- Changed SI parameter name description and added maximum specification to SI and FB, SO, PG rows in *Absolute Maximum Ratings* table ... 4
- Added parameter names to CT and FB, SO, PG rows in *Absolute Maximum Ratings* table ... 4
- Added *lockout* to *Undervoltage lockout detection* parameter name ... 6
- Added *up to* to I_{lkg} test conditions ... 6
- Added V_{OUT} to unit of $V_{(TH-POR)}$ and $V_{(Thres)}$ ... 6
- Added CT to $V_{(th)}$ parameter name ... 6
- Added header for first section of *Switching Characteristics* table ... 7
- Added *UVLO Thresholds vs Temperature* and *Enable Thresholds vs Temperature* figures ... 8
- Added *CT Charging Current (V_{CT} = 0)* and *CT Charging Threshold* figures ... 9
- Changed *Device Functional Modes* section ... 17

Changes from Revision D (October 2014) to Revision E **Page**

- Corrected voltage unit in Handling Ratings table from V to kV ... 5

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Changes from Revision C (December 2013) to Revision D **Page**

- 已更改 CDM ESC 分类等级 1
- Changed FB/NC pin to FB/NU in Pin Functions table Added NC and NU notes to pinout drawings 4
- Removed ESD and T_{stg} specifications from the *Absolute Maximum Ratings* table 4
- Added *ESD Ratings* table 5
- Numerous changes throughout the *Electrical Characteristics* table 6
- Added *Switching Characteristics* table 7
- Moved an oscilloscope trace to the Applications Information section 10
- Changed de-glitch time in *Power-On Reset (PG) section* 13
- Changed reset delay timer default delay to 290 µs from 150 µs 13
- Changed voltage at which Power-on reset initializes to 91.6% of $V_{(Vout)}$ 13
- Changed selectable output voltage range and calculation for FB resistor divideer 15

Changes from Revision B (August 2013) to Revision C **Page**

- 通过添加 -Q1 更正了 说明 部分中的部件号 1
- Changed Operating ambient temperature to Operating junction temperature 4
- Added PSRR graph to Typical Characteristics 10
- Deleted a paragraph from the Thermal Protection section 16

Changes from Revision A (March 2013) to Revision B **Page**

- Added two conditions to $V_{dropout}$ in the Electrical Characteristics table 6

Changes from Original (December 2012) to Revision A **Page**

- Deleted the ORDERING INFORMATION table 4
- Changed From: T_A Operating ambient temperature range –40 to 125°C To: T_J Operating ambient temperature range –40 to 150°C 4

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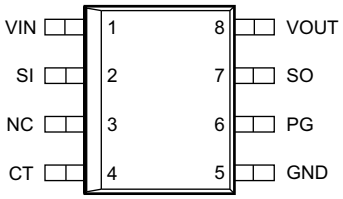
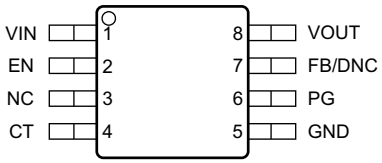
5 Pin Configuration and Functions

D Package (TPS7A69-Q1)
8-Pin SOIC
Top View



NC - No internal connection

DGN Package (TPS7A66-Q1)
8-Pin HVSSOP
Top View



NC - No internal connection
NU - Make no external connection

Pin Functions

PIN NAME	PIN NO.		TYPE	DESCRIPTION
	SOIC-D	HVSSOP-DGN		
CT	4	4	O	Reset-pulse delay adjustment. Connecting a capacitor from this pin to GND changes the PG reset delay; see the *Reset Delay Timer (CT)* section for more details.
EN	—	2	I	Enable pin. The device enters the standby state when the enable pin becomes lower than the enable threshold.
FB/DNC	—	7	I	Feedback pin when using external resistor divider or DNC pin when using the device with a fixed output voltage.
GND	5	5	G	Ground reference
NC	3	3	—	Not-connected pin
PG	6	6	O	Power good. This open-drain pin must connect to VOUT via an external resistor. V_{PG} is logic level high when V_{OUT} is above the power-on-reset threshold.
SI	2		I	Sense input pin to supervise input voltage. Connect via an external voltage divider to VIN and GND.
SO	7		O	Sense output. This open-drain pin must connect to VOUT via an external resistor. V_{SO} is logic level low when V_{SI} falls below the sense-low threshold.
VIN	1	1	P	Input power-supply voltage
VOUT	8	8	O	Regulated output voltage
Thermal pad	Pad	—	—	Thermal pad for HVSSOP-DGN package

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VIN, EN	Unregulated input (2) (3)	–0.3	45	V
VOUT	Regulated output	–0.3	7	V
SI	Sense input (2)	–0.3	V_{IN}	V
CT	Reset delay input	–0.3	25	V
FB, SO, PG	Feedback, sense output, power good	–0.3	V_{OUT}	V
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND
(3) Absolute maximum voltage, withstand 45 V for 200 ms

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6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	0	4	kV
		Charged device model (CDM), per AEC Q100-011 — Corner pins (1, 4, 5, and 8)	0	1	
		Charged device model (CDM), per AEC Q100-011 — Other pins	0	1	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Unregulated input	4		40	V
V_{EN}, V_{SI}	High voltage (I/O)	0		40	V
V_{CT}	CT pin voltage	0		20	V
V_{OUT}	Regulated output	1.5		5.5	V
V_{PG}, V_{SO}, V_{FB}	Low voltage (I/O)	0		5.5	V
C_{IN}	Input capacitor[1]		10		µF
C_{OUT}	Output capacitor[1]	2.2		100	µF
T_J	Operating junction temperature	–40		150	°C

(1) Values on this row refer to the nominal value of the capacitor.

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A66-Q1 HVSSOP (8 PINS)	TPS7A69-Q1 SOIC (8 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	113.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.0	59.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	59.57	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	52.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.5	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V_{IN} = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (VIN)						
V_{IN}	Input voltage	Fixed 5-V output, I_O = 1 mA	5.5		40	V
		Fixed 3.3-V output, I_O = 1 mA	4		40	
$I_{(q)}$	Quiescent current	V_{IN} = 5.5 V to 40 V, EN = ON, I_O = 0.2 mA		12	20	µA
$I_{(Sleep)}$	Input sleep current	No load current and EN = OFF			4	µA
$I_{(EN)}$	EN pin current	$V_{(EN)}$ = 40 V			1	µA
$V_{(bg)}$	Band gap	Reference voltage for FB	1.199	1.223	1.247	V
$V_{(VinUVLO)}$	Undervoltage lockout detection	Ramp V_{IN} down until output turns OFF			2.6	V
$V_{(UVLOhys)}$	Undervoltage hysteresis			1		V
ENABLE INPUT (EN)						
V_{IL}	Logic input low level		0		0.4	V
V_{IH}	Logic input high level		1.7			V
REGULATED OUTPUT (VOUT)						
V_{OUT}	Regulated output	I_O = 1 mA, T_J = 25°C	–1%		1%	
		V_{IN} = 6 V to 40 V, I_O = 1 mA to 150 mA, fixed 5-V version	–2%		2%	
		V_{IN} = 4 V to 40 V, I_O = 1 mA to 150 mA, fixed 3.3-V version	–2%		2%	
		V_{IN} = V_{OUT} + 0.45 V and Vin ≥ 4 V, I_O = 1 mA to 150 mA, adjustable version(1)	–2%		2%	
$V_{(line-reg)}$	Line regulation	V_{IN} = 5.5 V to 40 V, I_O = 50 mA			5	mV
$V_{(load-reg)}$	Load regulation	I_O = 1 mA to 150 mA			20	mV
$V_{(dropout)}$	Dropout voltage	$V_{(dropout)}$ = V_{IN} – V_{OUT}, I_{OUT} = 80 mA		180	240	mV
		V_{IN} – V_{OUT}, I_{OUT} = 150 mA		300	450	
		V_{IN} = 3 V, $V_{(dropout)}$ = V_{IN} – V_{OUT}, I_O = 5 mA	12	27.5	58	
		V_{IN} = 3 V, $V_{(dropout)}$ =V_{IN} –V_{OUT}, I_O = 30 mA	44	80	145	
I_O	Output current	V_{OUT} in regulation	0		150	mA
$I_{(lreg-CL)}$	Output current limit	V_{OUT} short to ground		500	800	mA
PSRR	Power supply ripple rejection(2)	V_{IN} = 12 V, I_L = 10 mA, output capacitance = 2.2 µF				dB
		Frequency = 100 Hz		60		
		Frequency = 100 kHz		40		
VOLTAGE SENSING PRE-WARNING						
$V_{I(S-th)}$	Sense low threshold	$V_{(SI)}$ decreasing	1.089	1.123	1.157	V
$V_{I(S-th,hys)}$	Sense threshold hysteresis		50	100	150	mV
$V_{OL(S)}$	Sense output low voltage	($V_{(SI)}$ ≤ 1.06 V, V_{IN} ≥ 4 V, $R_{(SO)}$ = 10 kΩ to V_{OUT}			0.4	V
$I_{OH(S)}$	Sense output leakage	($V_{(SO)}$ = 5 V, $V_{(SI)}$ ≥ 1.5 V)			1	µA
$I_{I(S)}$	Sense input current		–1	0.1	1	µA
RESET (PG)						
V_{OL}	Reset output, low voltage	I_{OL} = 0.5 mA			0.4	V
I_{lkg}	Leakage current	Reset pulled up to VOUT through a 10-kΩ resistor			1	µA
$V_{(TH-POR)}$	Power-on-reset threshold	V_{OUT} increasing	89.6	91.6	93.6	% of V_{OUT}
$V_{(Thres)}$	Hysteresis			2		% of V_{OUT}
RESET DELAY (CT)						
$I_{(Chg)}$	Delay-capacitor charging current	V_{CT} = 0 V		1.4		µA
$V_{(th)}$	CT threshold to release PG high			1		V
OPERATING TEMPERATURE RANGE						
T_J	Junction temperature		–40		150	°C
$T_{(shutdown)}$	Junction shutdown temperature			175		°C
$T_{(hyst)}$	Hysteresis of thermal shutdown			20		°C

(1) Adjustable version with precision external feedback resistor with tolerance of less than ±1%.
(2) Design information – not tested.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING FOR SENSE INPUT AND OUTPUT (SI, SO)						
$t_{(SDeglitch,rise)}$	SI or SO rising deglitch time		50		260	µs
$t_{(SDeglitch,drop)}$	SI or SO falling deglitch time		30		240	µs
TIMING FOR RESET (PG)						
$t_{(POR)}$	Power-on-reset delay	Where C = delay capacitor value; capacitance C = 100 nF(1)	50	100	180	ms
$t_{(POR-fixed)}$		No capacitor on pin	100	290	650	µs
$t_{(Deglitch)}$	Reset deglitch time		20	250		µs

(1) This information only is not tested in production and equation basis is $(C \times 1) / 1 \times 10^{-6} = t_d$ (delay time).
Where C = Delay capacitor value. Capacitance C range = 100 pF to 100 nF.

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6.7 Typical Characteristics

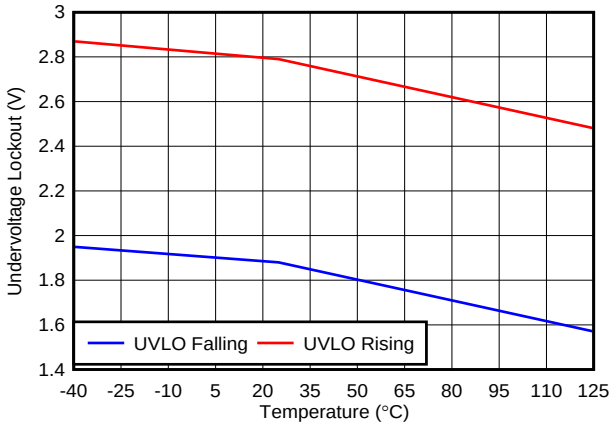

Figure 1. UVLO Thresholds vs Temperature

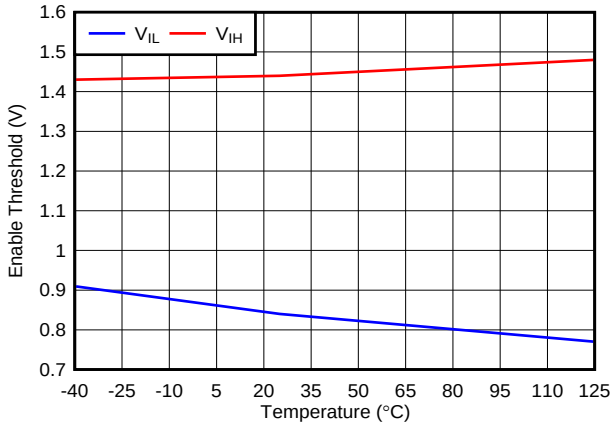

Figure 2. Enable Thresholds vs Temperature

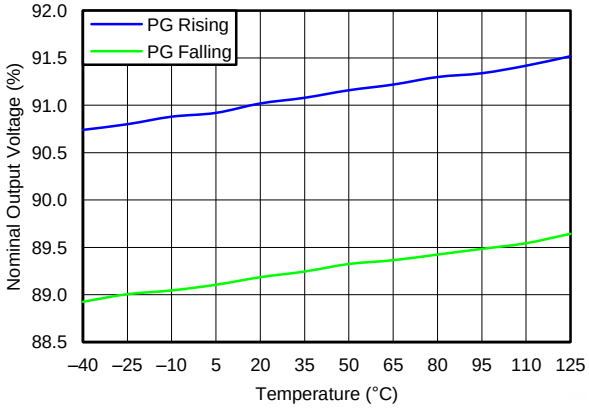

Figure 3. Power-Good Threshold Voltage vs Temperature (V_{IN} = 14 V, No Load)

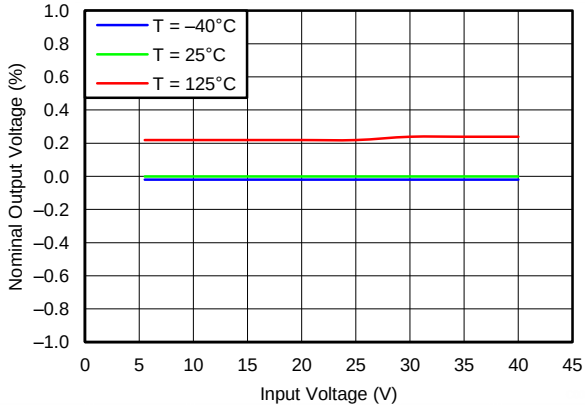

Figure 4. Line Regulation (V_{IN} = 14 V, I_L = 1 mA)

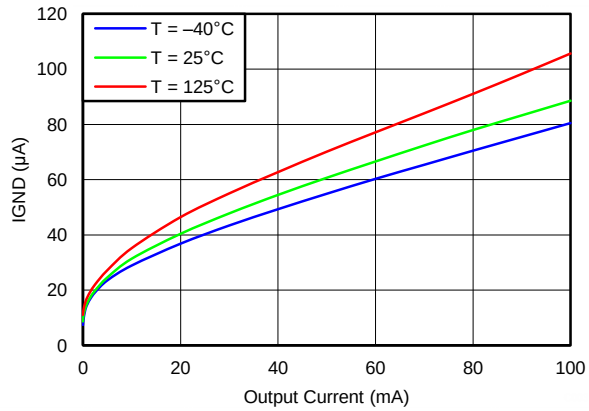

Figure 5. Ground Current vs Output Current (V_{IN} = 14 V)

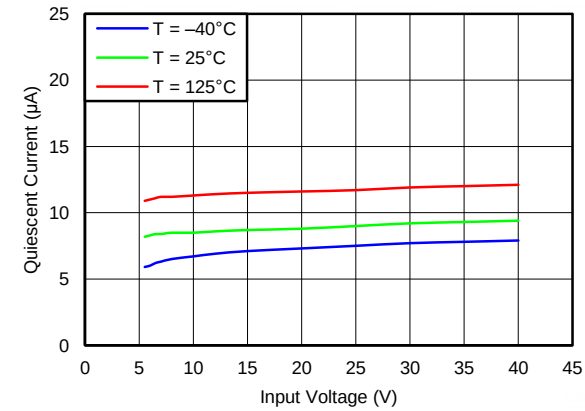

Figure 6. Quiescent Current vs Input Voltage (I_L = 0)

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Typical Characteristics (continued)

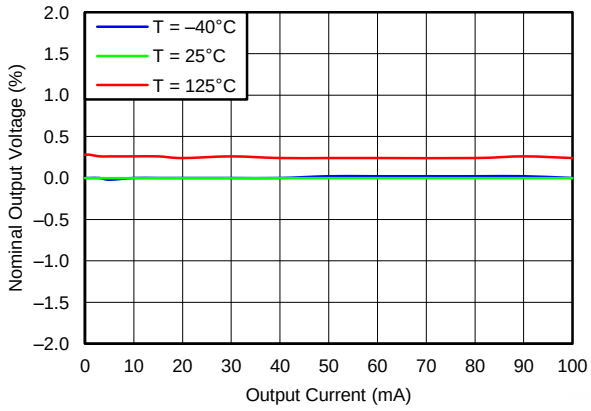

Figure 7. Load Regulation (V_{IN} = 14 V)

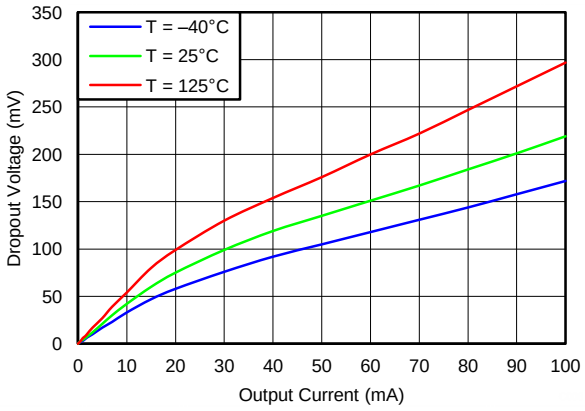

Figure 8. Dropout Voltage vs Output Current (V_{IN} = 4 V)

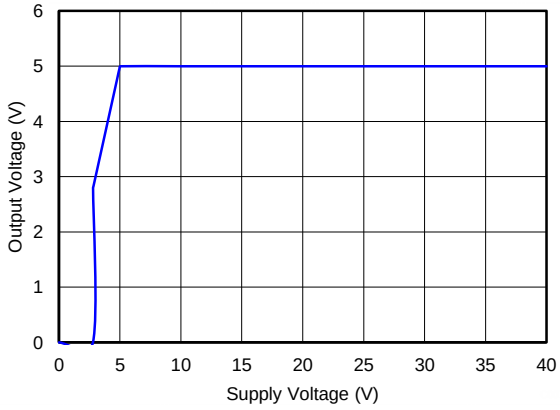

Figure 9. Output Voltage vs Supply Voltage (Fixed 5-V Version, I_L = 0)

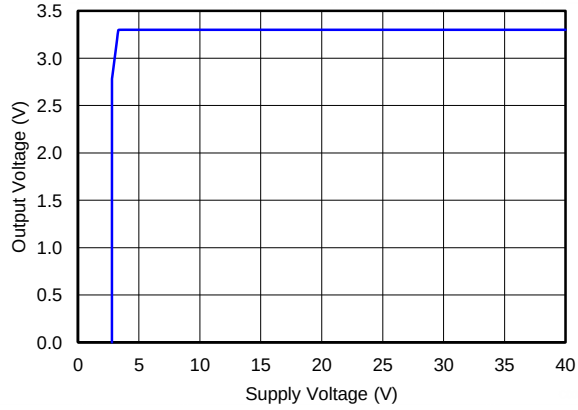

Figure 10. Output Voltage vs Supply Voltage (Fixed 3.3-V Version, I_L = 0)

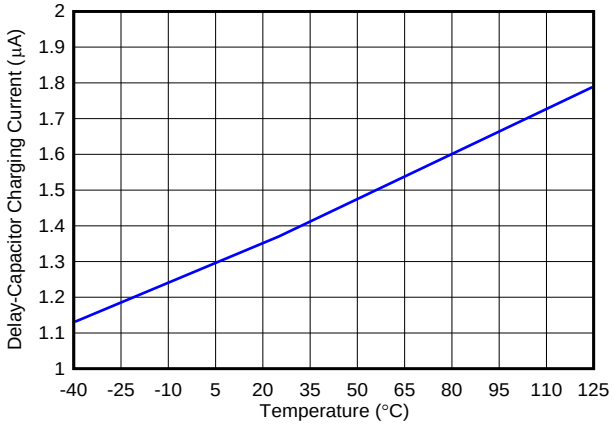

Figure 11. CT Charging Current (V_{CT} = 0)

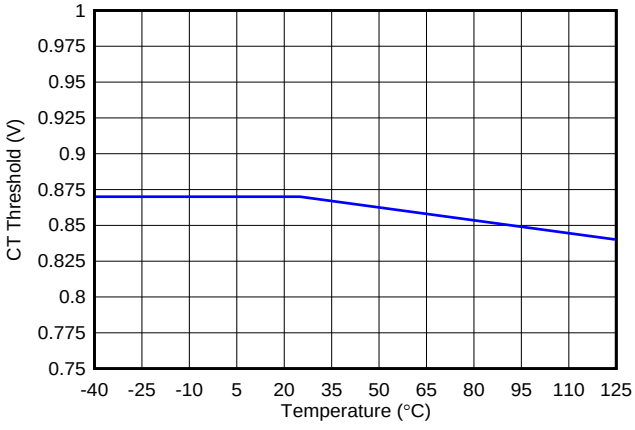

Figure 12. CT Charging Threshold

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Typical Characteristics (continued)

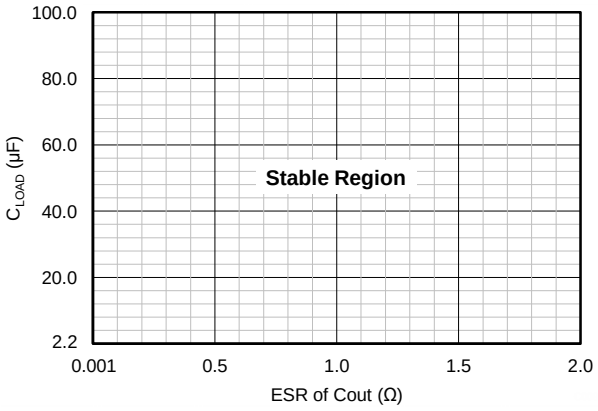


Figure 13. Load Capacitance vs ESR Stability

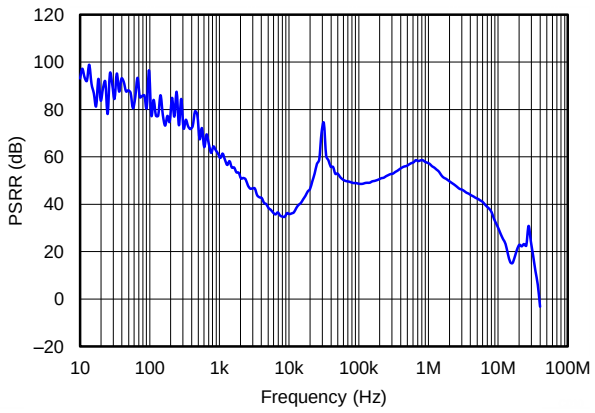
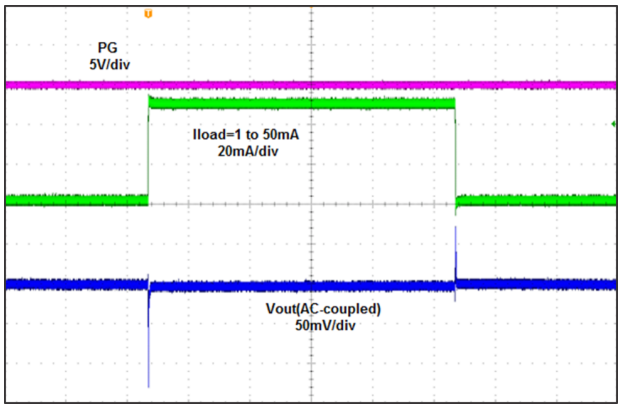
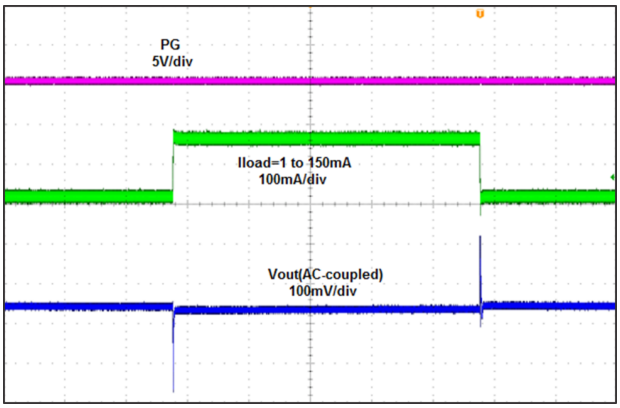


Figure 14. Power-Supply Rejection Ratio vs Frequency



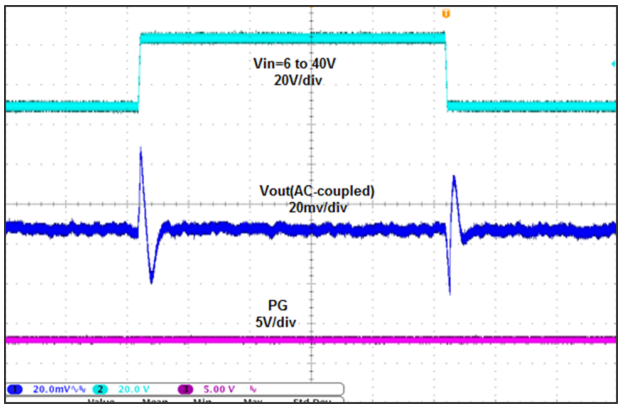
All oscilloscope waveforms were taken at room temperature.

Figure 15. Load Transient Response, 10 ms/div



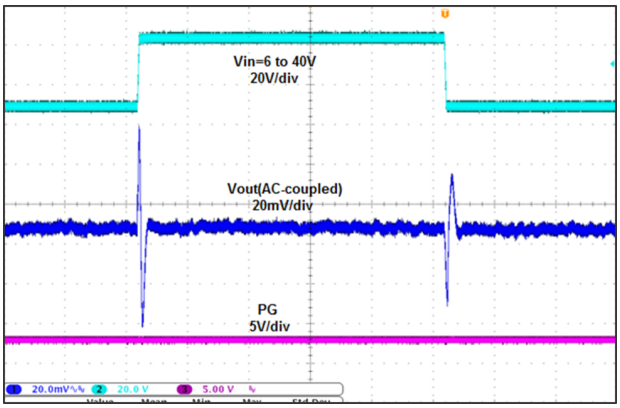
All oscilloscope waveforms were taken at room temperature.

Figure 16. Load Transient Response, 10 ms/div



All oscilloscope waveforms were taken at room temperature.

Figure 17. Line Transient Response, I_L = 1 mA, 1 V/µs



All oscilloscope waveforms were taken at room temperature.

Figure 18. Line Transient Response, I_L = 10 mA, 1 V/µs

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7 Detailed Description

7.1 Overview

This device is a combination of a low-dropout linear regulator with reset function. The power-on reset initializes once the V_{OUT} output exceeds 91.6% of the target value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before releasing the PG pin high.

7.2 Functional Block Diagrams

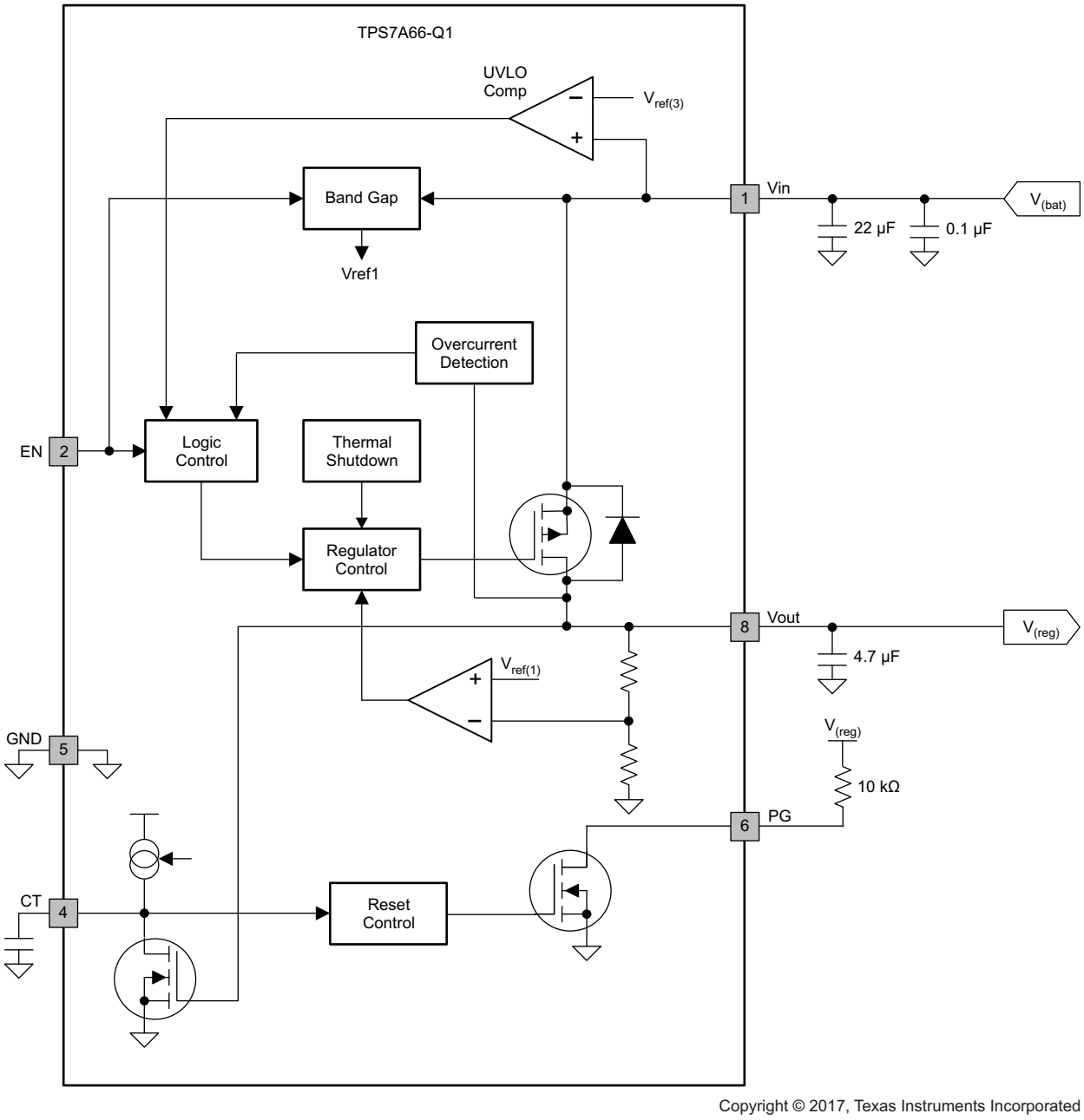

Figure 19. TPS7A66-Q1 Functional Block Diagram

Functional Block Diagrams (continued)

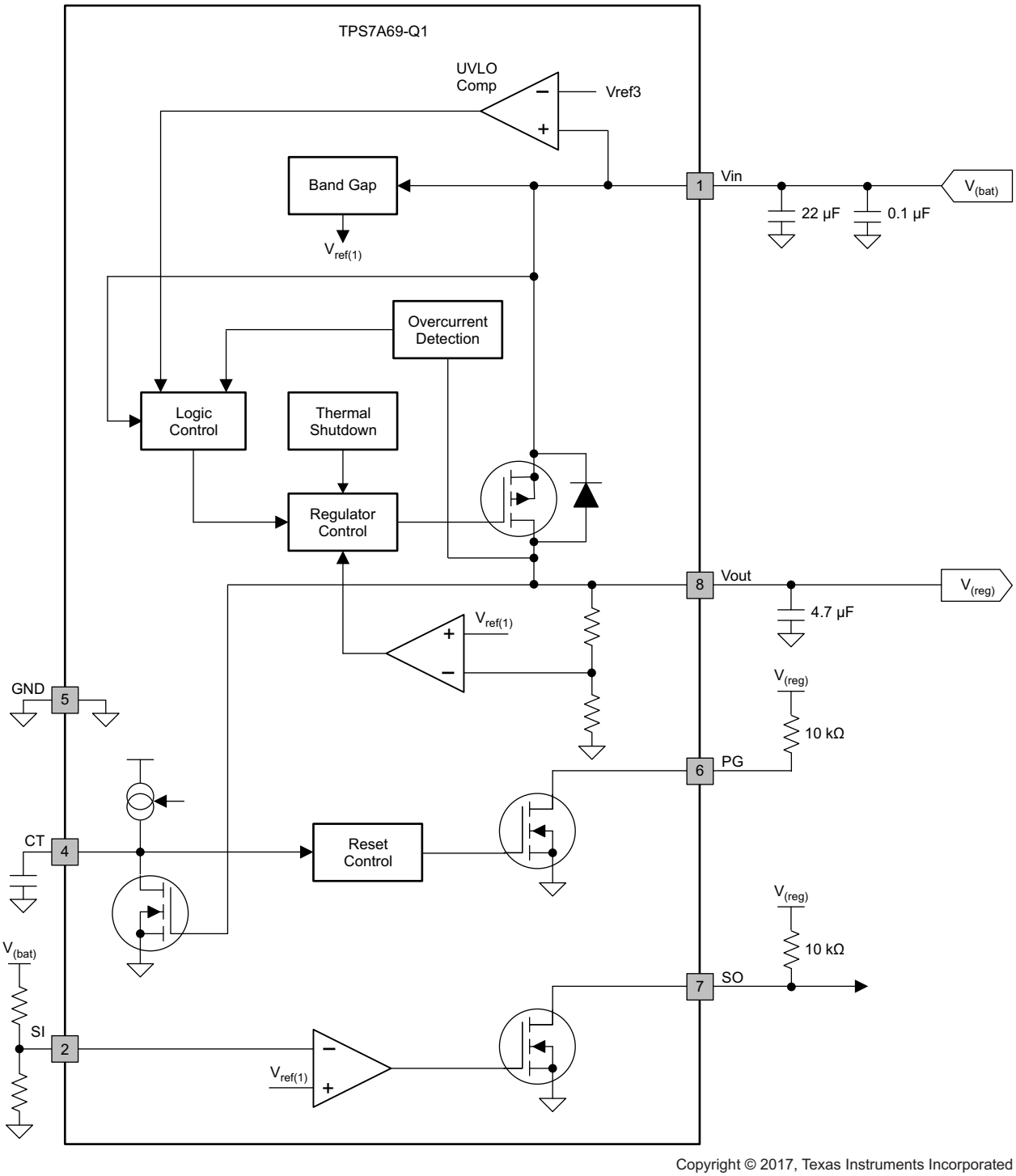

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Figure 20. TPS7A69-Q1 Functional Block Diagram

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7.3 Feature Description

7.3.1 Enable (EN)

This is a high-voltage-tolerant pin; high input activates the device and turns the regulator ON. One can connect this input to the VIN pin for self-bias applications.

7.3.2 Regulated Output (V_{OUT})

This is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

In the event the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 Power-On Reset (PG)

This is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated V_{OUT} has exceeded approximately 90% of the set value and the power-on-reset delay has expired. The on-chip oscillator presets the delay. The regulated output falling below the 90% level asserts this output low after a short de-glitch time of approximately 250 µs (typical).

7.3.4 Reset Delay Timer (CT)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 290 µs (typ). After releasing the PG pin high, the capacitor on this pin discharges, thus allowing the capacitor to charge from approximately 0.2 V for the next power-on-reset delay-timer function.

An external capacitor, CT, defines the reset-pulse delay time, $t_{(POR)}$, with the charge time of:

$$t_{(POR)} = \frac{C_{(CT)} \times 1\,V}{1\,\mu A} \quad (1)$$

The power-on reset initializes once the output V_{OUT} exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before the releasing of the PG pin high.

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Feature Description (continued)

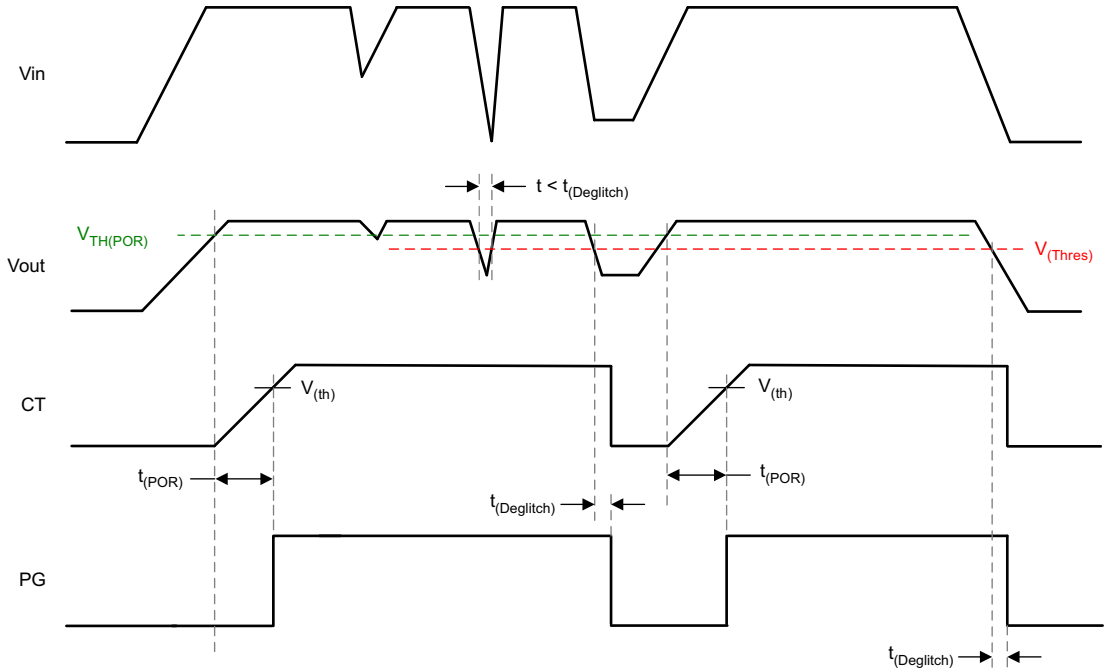

Figure 21. Conditions for Activation of Reset

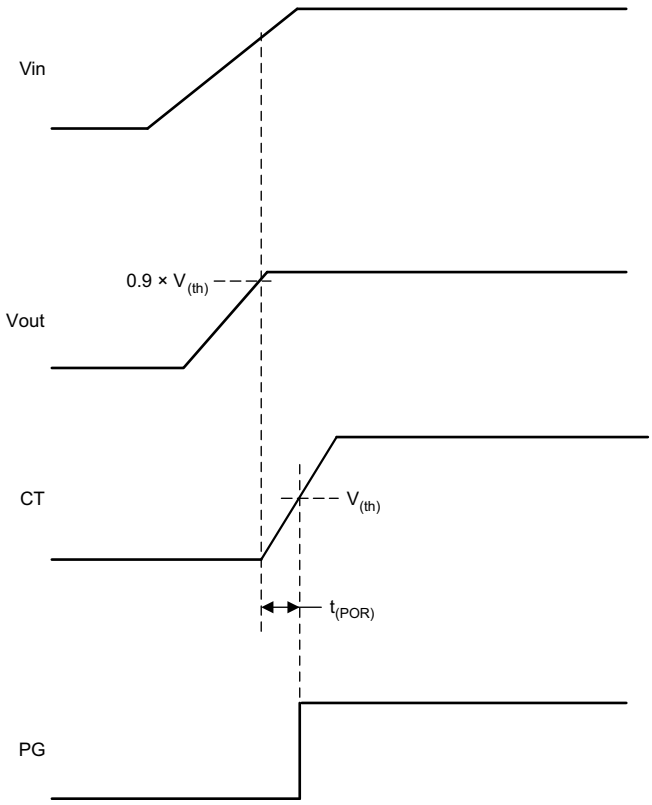

Figure 22. External Programmable Reset Delay

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Feature Description (continued)

7.3.5 Sense Comparator (SI and SO for TPS7A69-Q1)

The sense comparator compares the input signal with an internal voltage reference of 1.223 V for rising and 1.123 V for falling threshold. The use of an external voltage divider makes this comparator very flexible in the application.

The device can supervise the input voltage either before or after the protection diode and give additional information to the microprocessor, like low-voltage warnings.

The regulator operates in low-power mode when the output load is below 2 mA (typical, 1-mA to 10-mA range). In this mode, the regulator output tolerance is approximately V_{OUT} ± 1%.

7.3.6 Adjustable Output Voltage (FB for TPS7A6601-Q1)

One can select an output voltage between 1.5 V and 5 V by using an external resistor divider. Calculate the output voltage using the following equation, where $V_{(FB)}$ = 1.223 V. The recommendation for R1 and R2 is that both be less than 100 kΩ.

$$V_{(Vout)} = V_{(FB)} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

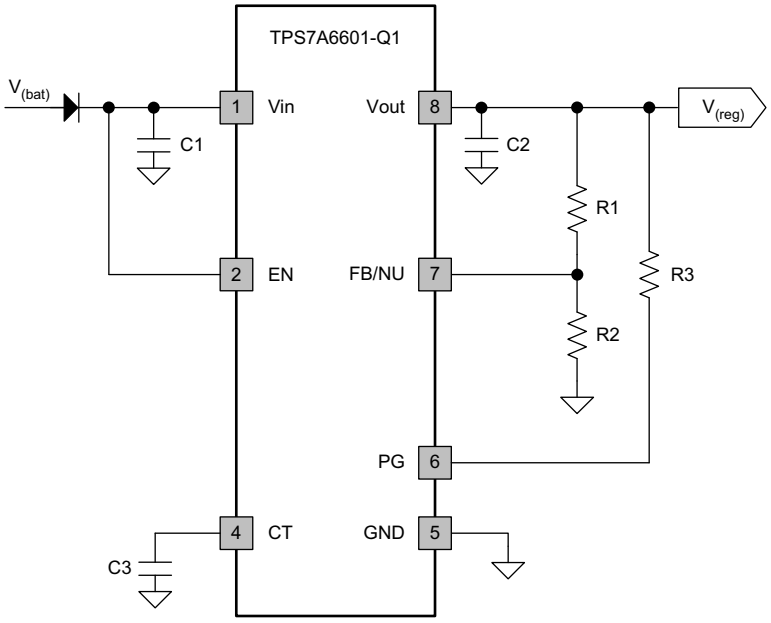

Figure 23. External Feedback Resistor Divider

7.3.7 Undervoltage Shutdown

There is an internally fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on VIN drops below $V_{(VinUVLO)}$. This ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required levels.

7.3.8 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_O) and switch resistance ($R_{(SW)}$). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

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Feature Description (continued)

7.3.9 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. Cooling of the junction temperature to approximately 150°C enables the output circuitry. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7A66-Q1, TPS7A69-Q1 is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7A66-Q1 or TPS7A69-Q1 into thermal shutdown degrades device reliability.

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7.4 Device Functional Modes

Table 1 provides a quick comparison between the regulation, disabled, and current limit modes of operation.

Table 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN(1)	I_O	T_J
Regulation(2)	$V_{IN} > V_{OUT(nom)} + V_{(dropout)}$	$V_{EN} > V_{IH}$	$I_O < I_{(Ireg-CL)}$	$T_J \le T_{J(maximum)}$
Disabled(3)	$V_{IN} < V_{(VinUVLO)}$	$V_{EN} < V_{IL}$	—	$T_J > T_{sd}$
Current limit operation	—	—	$I_O \ge I_{(Ireg-CL)}$	—

(1) EN is only required for the TPS7A66-Q1 devices.
(2) All table conditions must be met.
(3) The device is disabled when any condition is met.

7.4.1 Regulation

The device regulates the output to the nominal output voltage when all the conditions in Table 1 are met.

7.4.2 Disabled

When disabled, the pass device is turned off and the internal circuits are shut down.

7.4.3 Operation With $V_{(VinUVLO)} < V_{IN} < V_{IN(min)}$

When the input voltage is ramping up the device typically turns on when the input voltage is greater than $V_{(VinUVLO)}$ plus $V_{(UVLOhys)}$. When the input voltage is ramping down the device is specified to turn off when the input voltage becomes less than or equal to $V_{(VinUVLO)}$.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A66-Q1 and TPS7A69-Q1 devices are 150-mA low-dropout linear regulators designed for up to 40-V V_{IN} operation with only 12 µA quiescent current at no load. One can use the Pspice transient model, which is downloadable from the product folder (see *相关链接*), for evaluating the base function of the devices. in addition, there are specific EVMs designed for these devices. Both the EVM and its user guide are available on the product folder as well.

8.2 Typical Applications

Figure 24 and Figure 26 depict typical application circuits for the TPS7A66-Q1 and TPS7A69-Q1, respectively. One may use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R.

8.2.1 TPS7A66-Q1 Typical Application

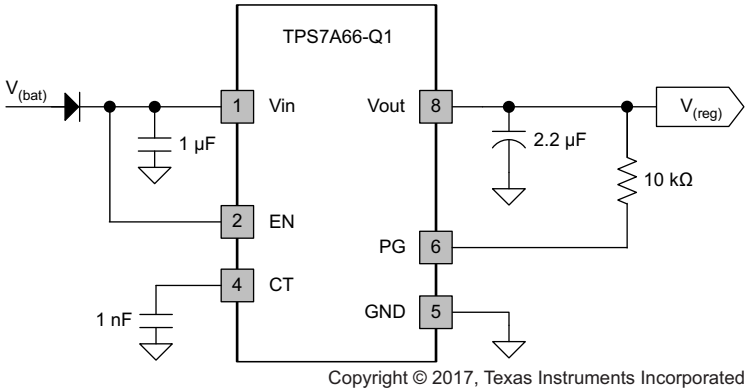

Figure 24. Typical Application Schematic for TPS7A66-Q1

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the design parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF

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8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 µF. The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

The device requires an output capacitor to stablize the output voltage. The capacitor value should be between 2.2 µF and 100 µF. The ESR range should be between 1 mΩ and 2 Ω. TI recommends to selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.1.3 Application Curve

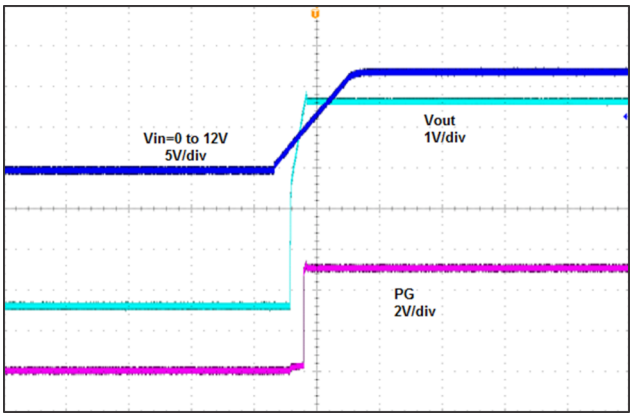

Figure 25. Power Up (5 V), 20 ms/div, I_L = 20 mA

8.2.2 TPS7A69-Q1 Typical Application

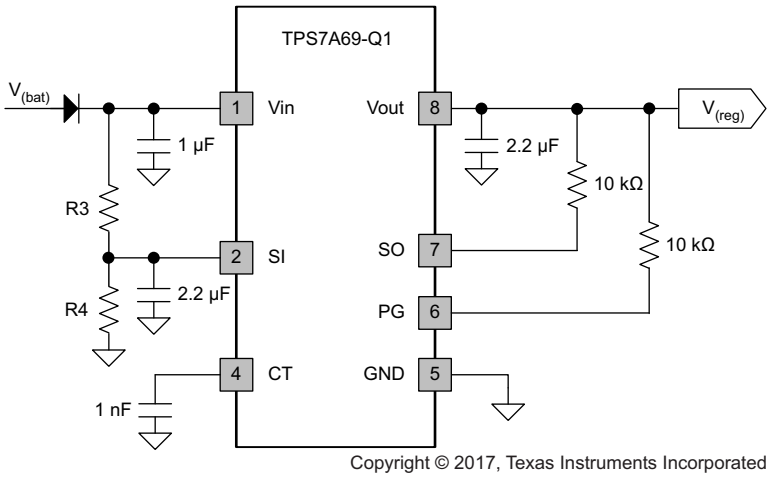

Figure 26. Typical Application Schematic for TPS7A69-Q1

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF
Low-voltage tracking threshold	6 V to 9 V

8.2.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time
- Low-voltage tracking threshold

8.2.2.2.1 Low-Voltage Tracking Threshold

After determining the low-voltage tracking threshold, calculate the ratio of the resistor divider connected to VIN, SI, and GND by the following equation:

$$\frac{R3}{R4} = \frac{V_{(LT)}}{1.223} - 1 \quad (3)$$

TI recommends that the values of both R3 and R4 be less than 100 kΩ.

8.2.2.3 Application Curve

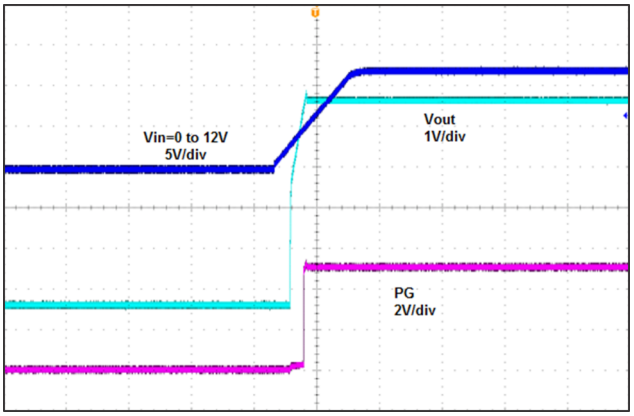

Figure 27. Power Up (5 V), 20 ms/div, I_L = 20 mA

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9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 4 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A66-Q1 or TPS7A69-Q1 device, TI recommends adding an electrolytic capacitor with a value of 22 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitive-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends the use of a fixed-voltage version of the TPS7A66-Q1, or isolation of the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7A66-Q1 and TPS7A69-Q1 are available at the end of this product data sheet and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

For the layout of TPS7A66-Q1 and TPS7A69-Q1, place the input and output capacitors close to the devices as shown in Figure 28 and Figure 29, respectively. In order to enhance the thermal performance, TI recommends surrounding the device with some vias.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7A66-Q1 and TPS7A69-Q1 evaluation board, available at www.ti.com.

10.2 Layout Examples

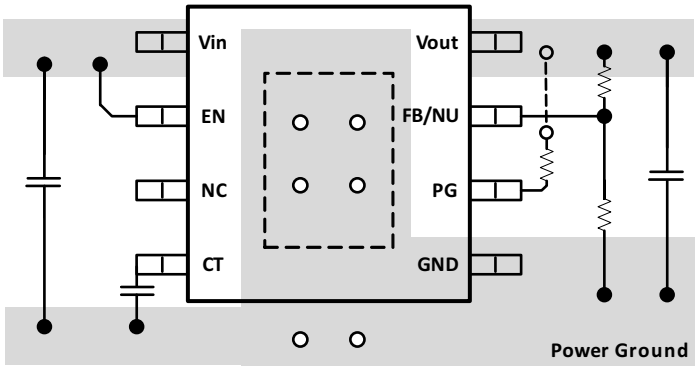

Figure 28. TPS7A66-Q1 Board Layout Diagram

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Layout Examples (continued)

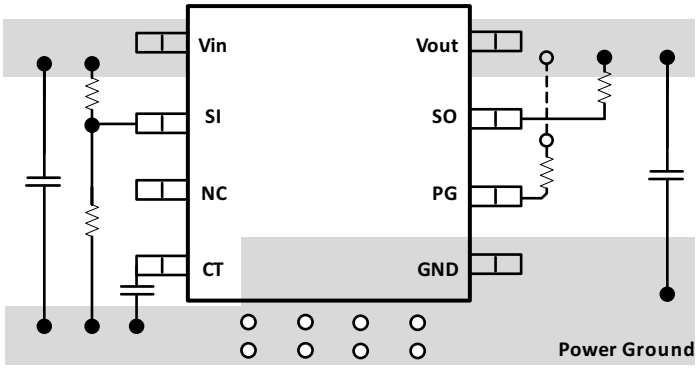

Figure 29. TPS7A69-Q1 Board Layout Diagram

10.3 Power Dissipation and Thermal Considerations

Calculate power dissipated in the device using Equation 4.

$$P_D = I_O \times (V_{(Vin)} - V_{(Vout)}) + I_{(q)} \times V_{(Vin)} \quad (4)$$

where:

P_D = continuous power dissipation
I_O = output current
V_{IN} = input voltage
V_{OUT} = output voltage

As $I_{(q)}$ << I_O, therefore ignore the term $I_{(q)} \times V_{IN}$ in Equation 4.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 5.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

where:

$R_{\theta JA}$ = junction-to-ambient air thermal impedance

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (6)$$

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11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 4. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TPS7A66-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7A69-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订，恕不另行通知。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A6601QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA4Q
TPS7A6601QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA4Q
TPS7A6633QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA2Q
TPS7A6633QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA2Q
TPS7A6650QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA1Q
TPS7A6650QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA1Q
TPS7A6933QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6933
TPS7A6933QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6933
TPS7A6950QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6950
TPS7A6950QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6950

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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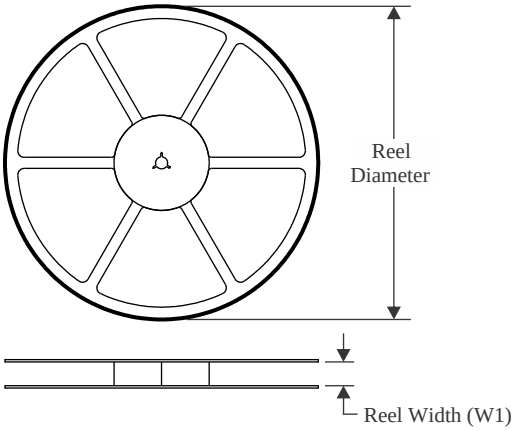
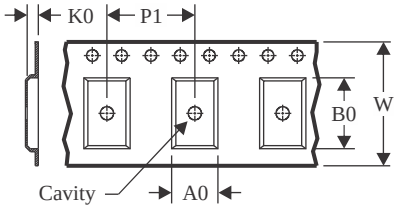
TAPE AND REEL INFORMATION

REEL DIMENSIONS

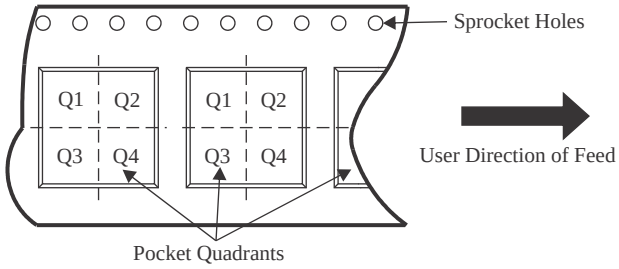


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

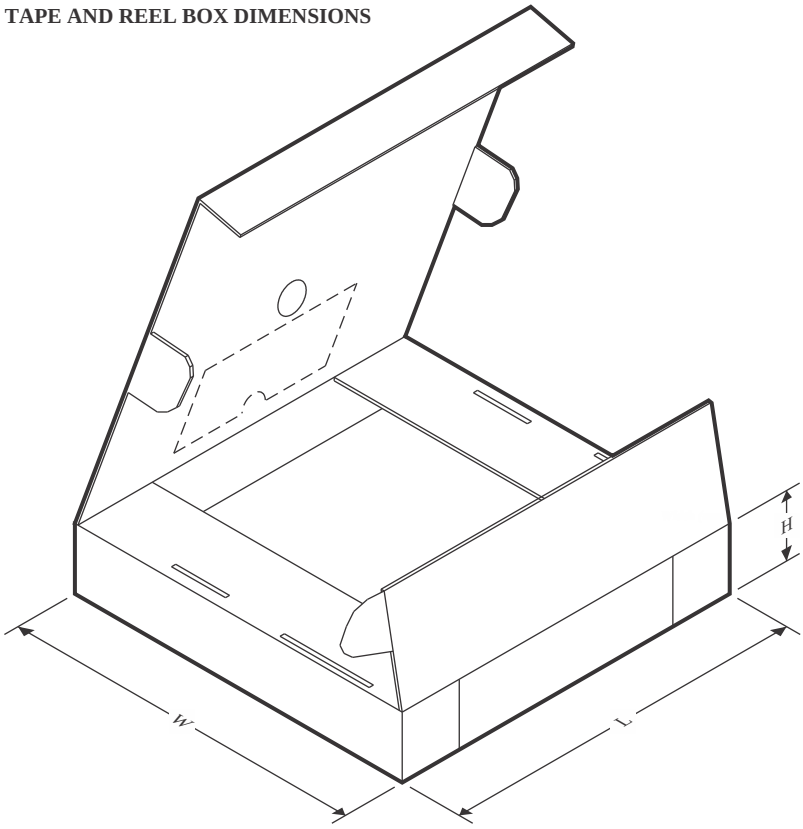
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6601QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6633QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6650QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6933QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7A6950QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6601QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6633QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6650QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6933QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TPS7A6950QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

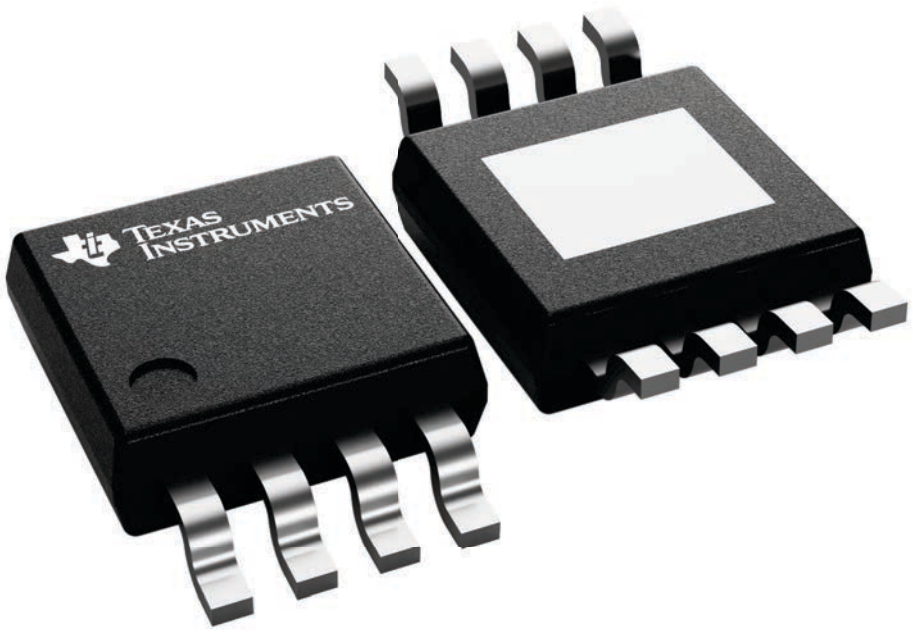
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

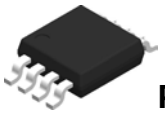
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



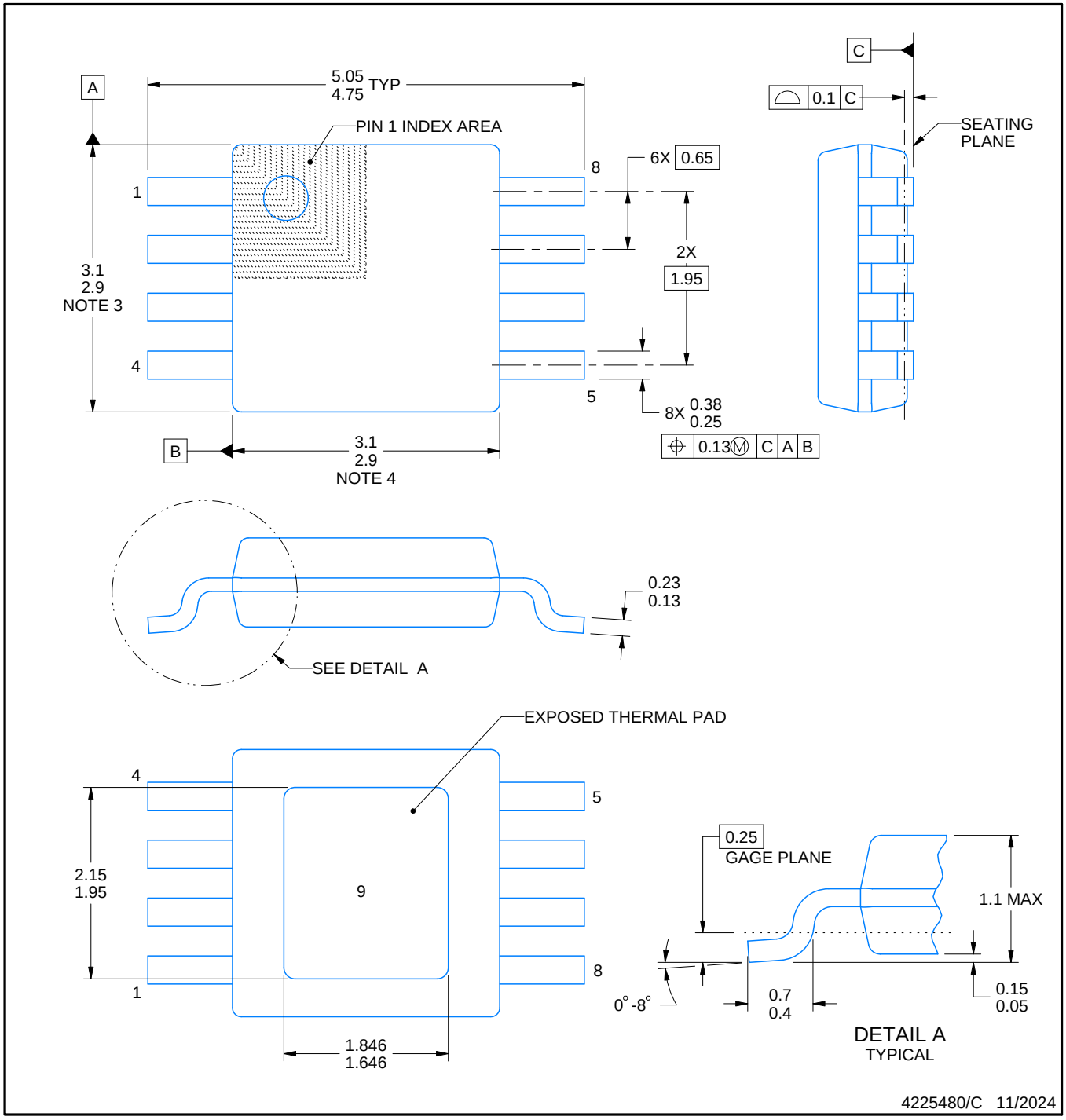
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

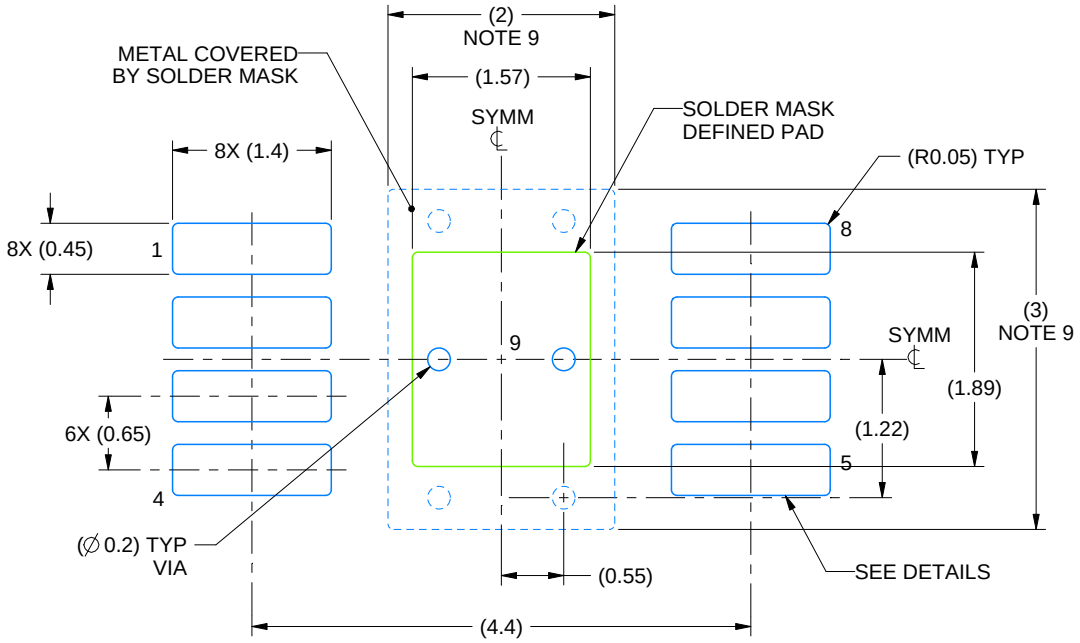
SMALL OUTLINE PACKAGE



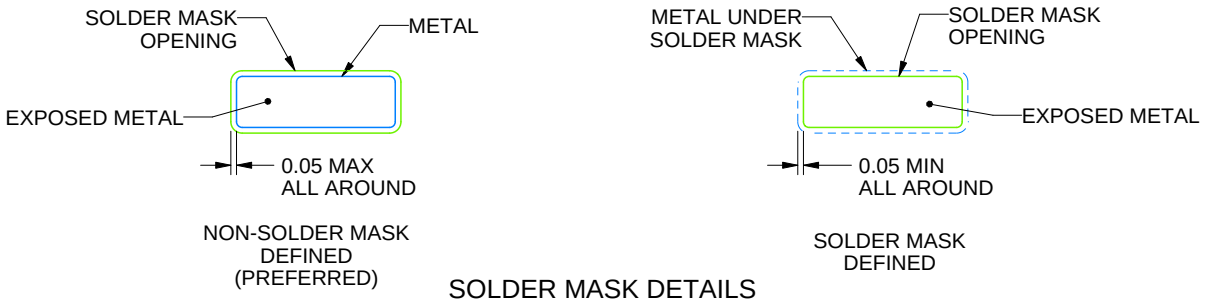
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

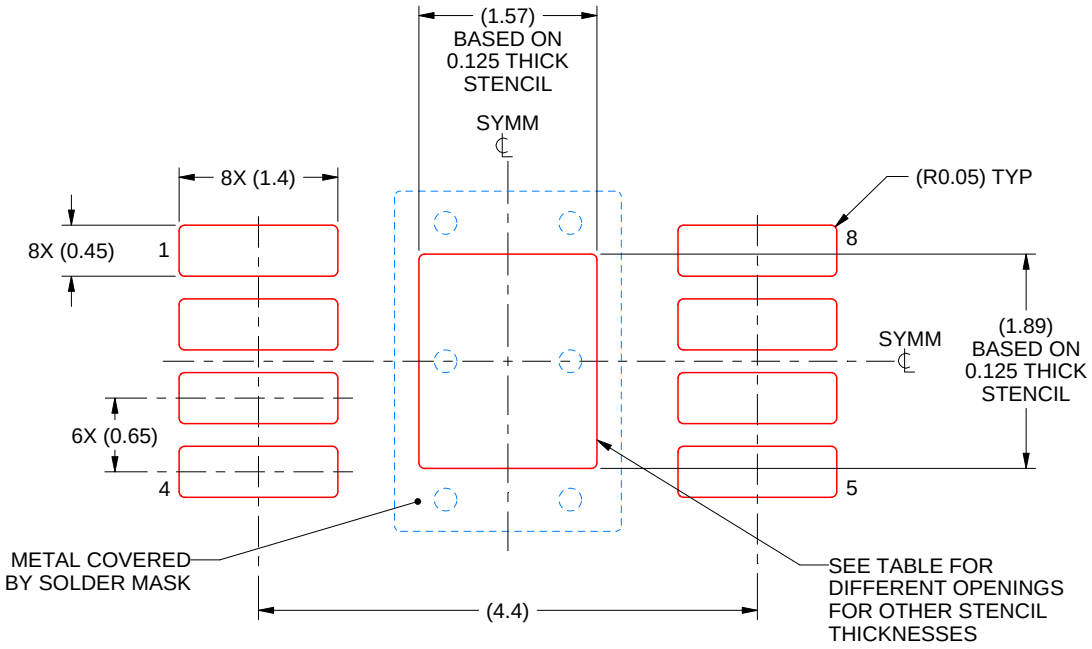


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



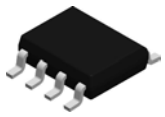
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

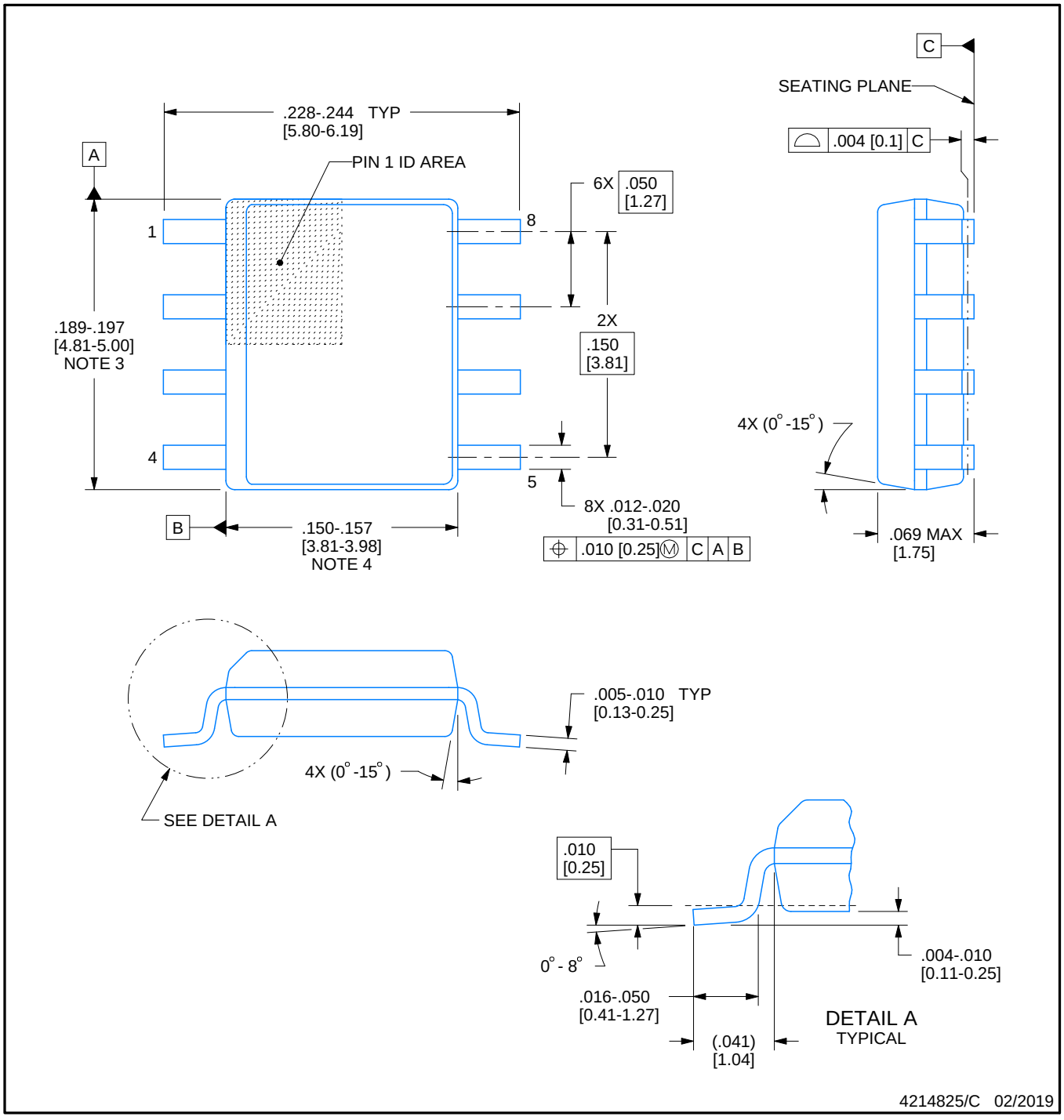


PACKAGE OUTLINE

D0008A

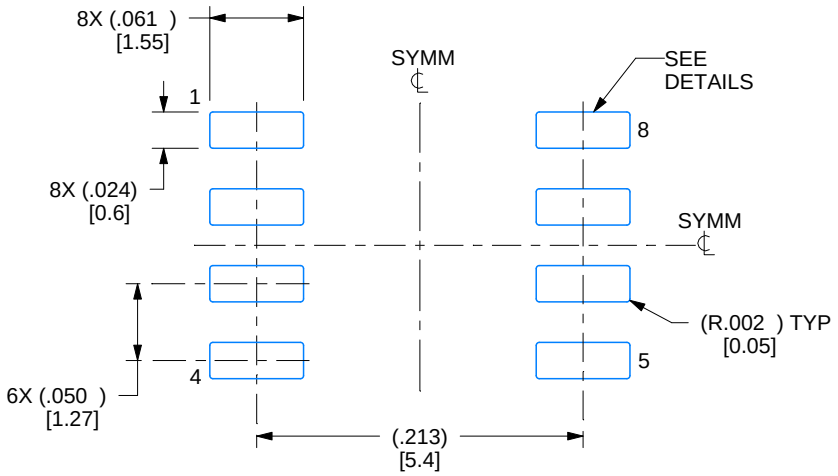
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

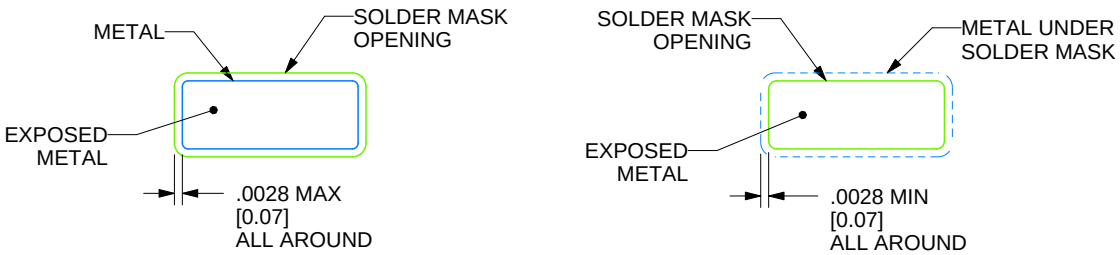


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

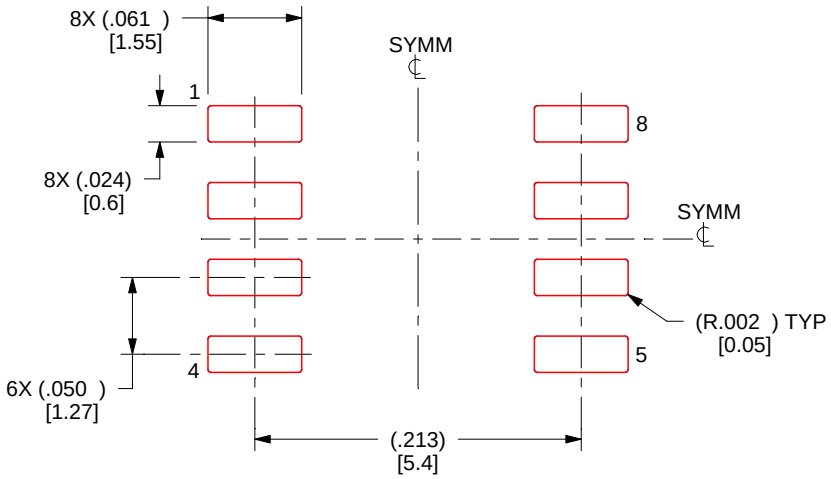
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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