TPS7B69xx 150mA、40V 超低静态电流 LDO

1 特性

- 4V 至 40V 的宽 V_I 输入电压范围，瞬态电压高达 45V
- 最大输出电流：150mA
- 低静态电流 (I_Q)：
  - 轻负载时典型值为 15µA
  - 整体温度范围下最大电流为 25µA
- 负载电流为 100mA 时，低压降电压典型值为 450mV
- 线路稳定度最高达 10mV
- 负载稳定度最高达 10mV
- 与低等效串联电阻 (ESR) 陶瓷输出电容（2.2µF 至 100µF）一起工作时保持稳定
- 固定输出电压选项为 3.3V 和 5V
- 集成故障保护：
  - 热关断
  - 短路保护功能
- 封装：
  - 5 引脚小外形尺寸晶体管 (SOT)-23 封装
  - 4 引脚小外形尺寸晶体管 (SOT)-223 封装

2 应用

- 电表、水表和燃气表
- 电器和大型家电
- 火灾警报器和烟雾探测器
- 医疗、保健和健身器材 应用

3 说明

TPS7B69xx 器件是一款低压降线性稳压器，适用于 V_I 高达 40V 的操作。该器件在轻负载模式下的静态电流仅为
15µA（典型值），适用于待机微控制器系统，尤其是常开 应用 ，比如电表、火灾警报器和烟雾探测器。

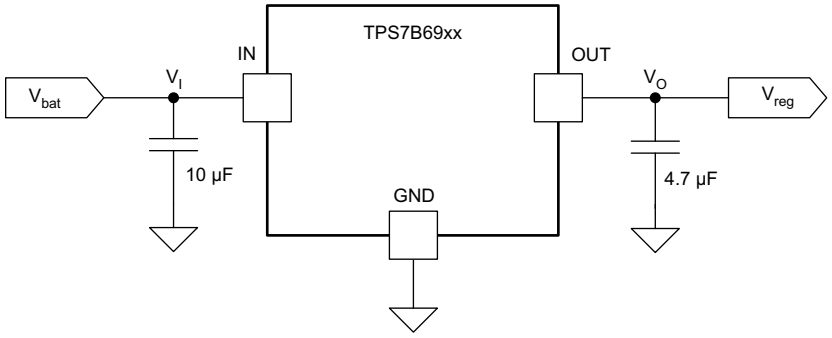
该器件集成有短路保护和过流保护功能。TPS7B69xx 器件的工作温度范围为 –40°C 至 105°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7B6933 TPS7B6950	SOT-223 (4)	6.50mm x 3.50mm
	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



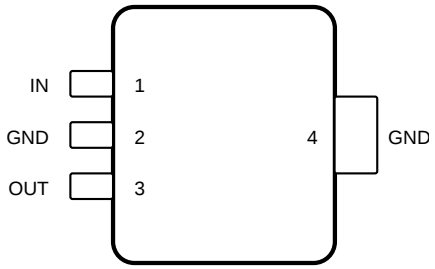
目录

4 修订历史记录

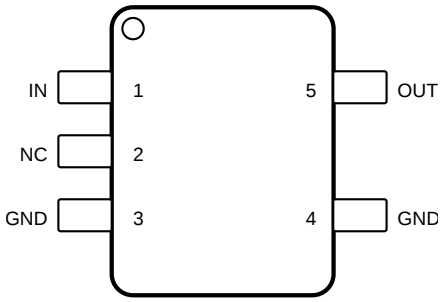
日期	修订版本	注
2016 年 4 月	*	最初发布版本

5 Pin Configuration and Functions

DCY Package
4-Pin SOT-223
Top View



DBV Package
5-Pin SOT-23
Top View



NC - No internal connection

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	SOT-223	SOT-23		
GND	2, 4	3, 4	G	Ground reference
IN	1	1	P	Input power-supply voltage
NC	—	2	—	Not connected pin
OUT	3	5	P	Output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Unregulated input voltage	IN(2)(3)	–0.3	45	V
Regulated output voltage	OUT(2)	–0.3	7	V
Operating junction temperature range, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal.
(3) Absolute maximum voltage, withstands 45 V for 200 ms.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Unregulated input voltage	4	40	V
V_O	Output voltage	0	5.5	V
C_O	Output capacitor requirements(1)	2.2	100	µF
ESR_{CO}	Output ESR requirements(2)	0.001	2	Ω
T_A	Operating ambient temperature range	–40	105	°C

(1) The output capacitance range specified in this table is the effective value.
(2) Relevant ESR value at f = 10 kHz

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS7B69xx		UNIT
		DCY (SOT-223)	DBV (SOT-23)	
		4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.2	210.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.8	126.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.3	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.3	16	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.2	37.5	°C/W

(1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, 2s2p four layer board with 2-oz copper. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 125 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_I	Input voltage	Fixed 3.3-V output, I_O = 1 mA	4		40	V
		Fixed 5-V output, I_O = 1 mA	5.5		40	
I_Q	Quiescent current	Fixed 3.3-V version, V_I = 4 to 40 V, , I_O = 0.2 mA Fixed 5-V version, V_I = 5.5 to 40 V, I_O = 0.2 mA		15	25	µA
$V_{IN(UVLO)}$	IN undervoltage detection	Ramp V_I up until the output turns on	3.65			V
		Ramp V_I down until the output turns OFF			3	
REGULATED OUTPUT (OUT)						
V_O	Regulated output	Fixed 3.3-V version, V_I = 5 to 40 V, I_O = 1 to 150 mA	–3%		3%	
		Fixed 5-V version, V_I = 6.5 to 40 V, I_O = 1 to 150 mA	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	V_I = 6 to 40 V, ΔV_O, I_O = 10 mA			10	mV
$\Delta V_{O(\Delta IL)}$	Load regulation	I_O = 1 to 150 mA, ΔV_O			20	mV
V_{DROP}	Dropout voltage	Fixed 3.3-V version, V_I – V_O, I_O = 50 mA			799	mV
		Fixed 3.3-V version, V_I – V_O, I_O = 100 mA			800	
		Fixed 5-V version, V_I – V_O, I_O = 50 mA		220	400	
		Fixed 5-V version, V_I – V_O, I_O = 100 mA		450	800	
I_O	Output current	V_O in regulation	0		150	mA
I_{OCL}	Output current-limit	OUT short to ground	150		500	mA
PSRR	Power supply ripple rejection(1)	V_{rip} = 0.5 V_{pp}, Load = 10 mA, f = 100 Hz, C_O = 2.2 µF		60		dB
OPERATING TEMPERATURE RANGE						
T_{sd}	Junction shutdown temperature			175		°C
T_{hys}	Hysteresis of thermal shutdown			25		°C

(1) Design Information—Not tested, ensured by characterization.

6.6 Typical Characteristics

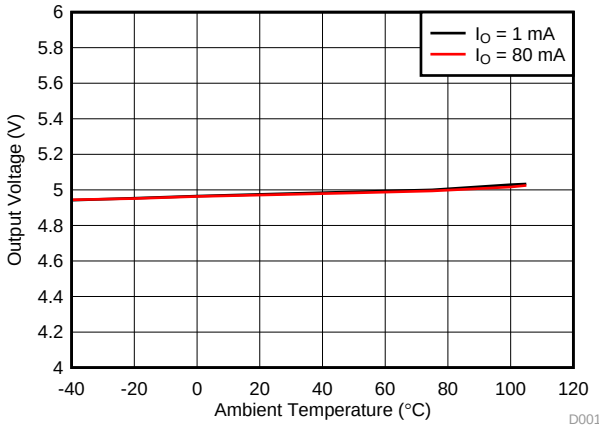


Figure 1. 5-V Output Voltage vs Ambient Temperature

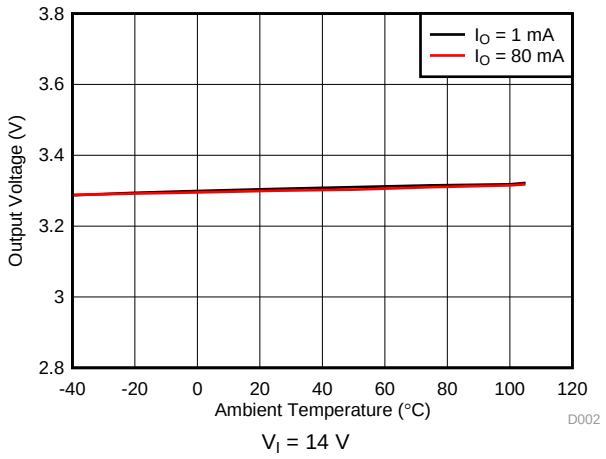


Figure 2. 3.3-V Output Voltage vs t Temperature

Typical Characteristics (continued)

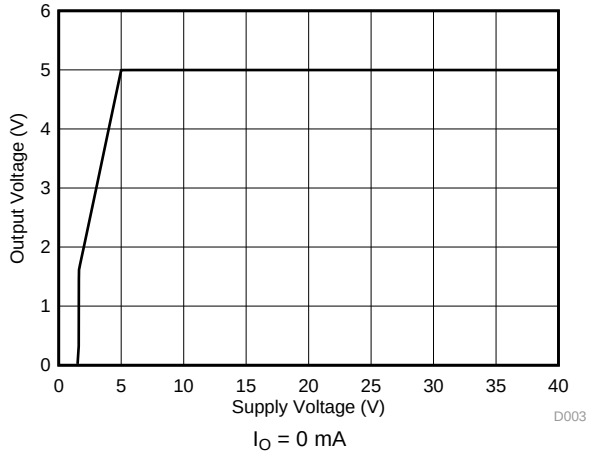


Figure 3. 5-V Output Voltage vs Supply Voltage

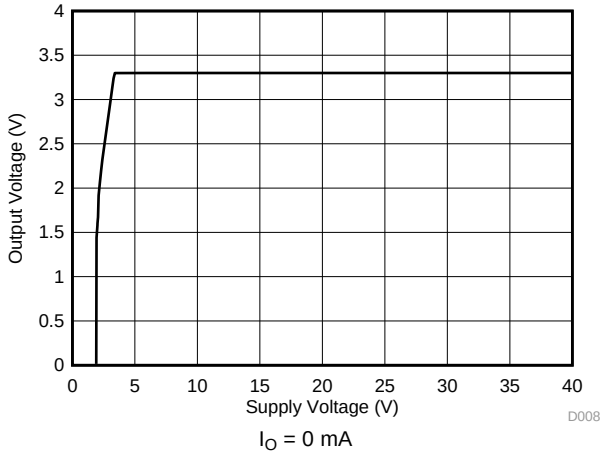


Figure 4. 3.3-V Output Voltage vs Supply Voltage

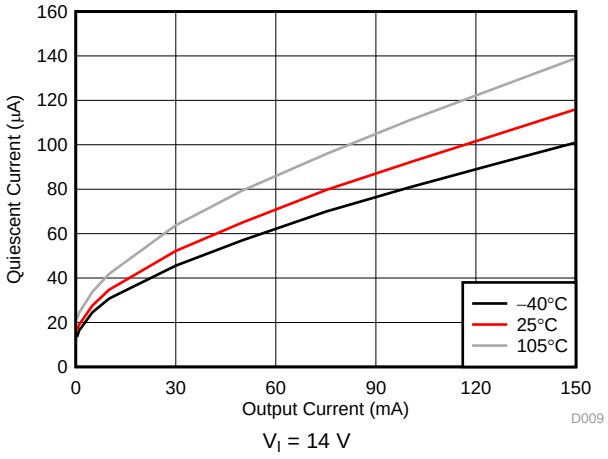


Figure 5. Quiescent Current vs Output Current

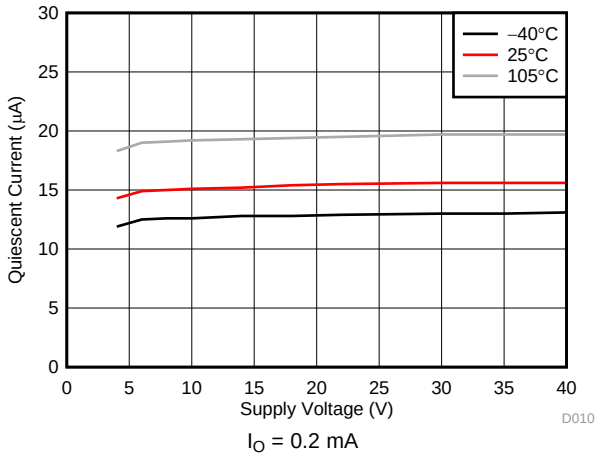


Figure 6. Quiescent Current vs Supply Voltage

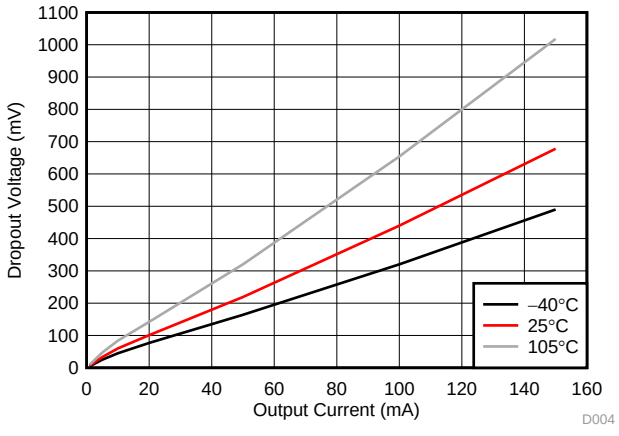


Figure 7. Dropout Voltage vs Output Current

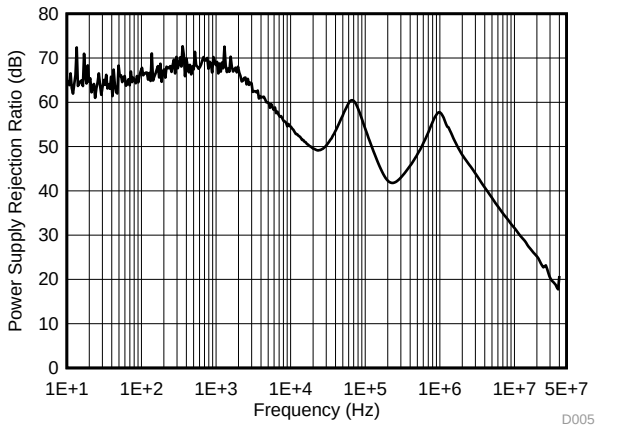
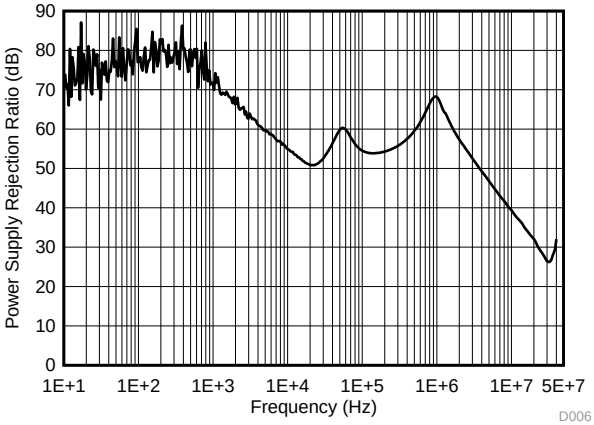


Figure 8. Power Supply Rejection Ratio

Typical Characteristics (continued)



I_O = 10 mA V_I = 14 V T_A = 25°C
C_O = 2.2 µF

Figure 9. Power Supply Rejection Ratio

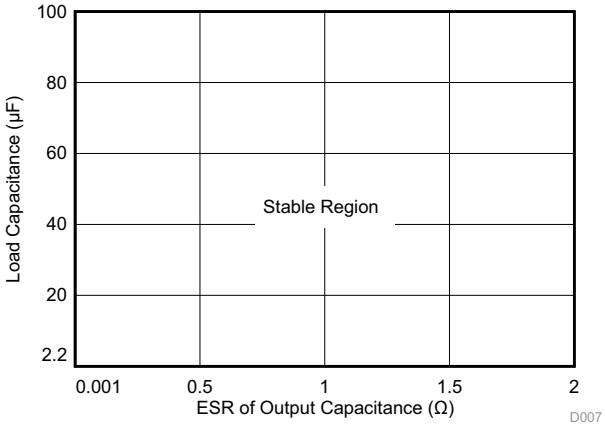
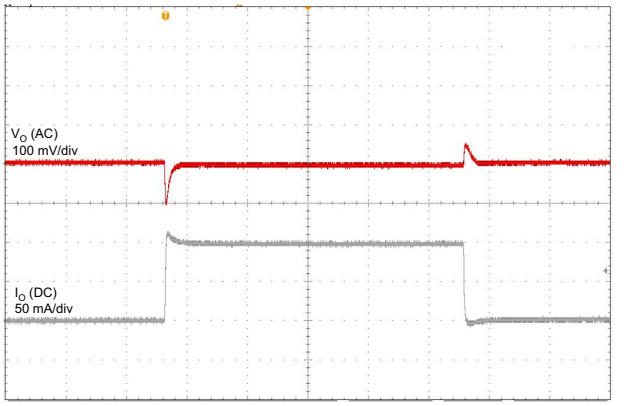
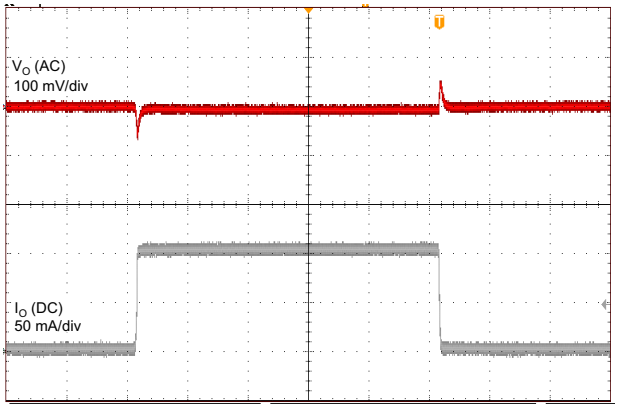


Figure 10. ESR Stability vs Output Capacitance



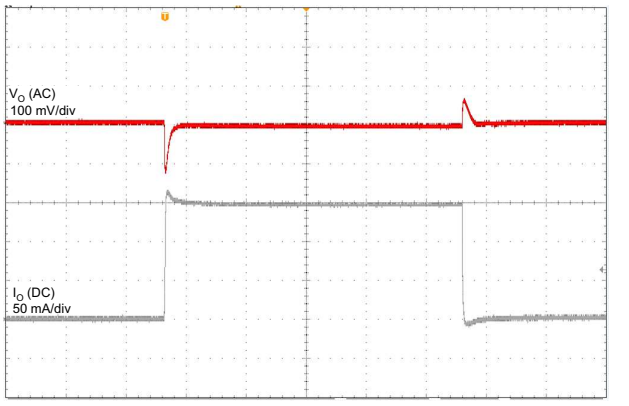
V_I = 14 V C_O = 2.2 µF 1 ms/div
V_O = 5 V

Figure 11. Load Transient (1 to 100 mA, 5 V)



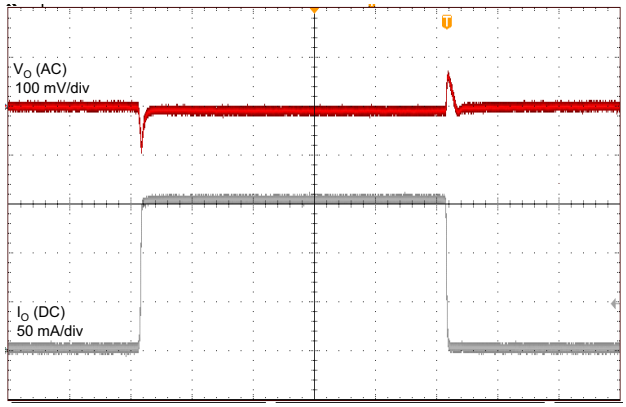
V_I = 14 V C_O = 2.2 µF 1 ms/div
V_O = 3.3 V

Figure 12. Load Transient (1 to 100 mA, 3.3 V)



V_I = 14 V C_O = 2.2 µF 1 ms/div
V_O = 5 V

Figure 13. Load Transient (1 to 150 mA, 5 V)



V_I = 14 V C_O = 2.2 µF 1 ms/div
V_O = 3.3 V

Figure 14. Load Transient (1 to 150 mA, 3.3 V)

Typical Characteristics (continued)

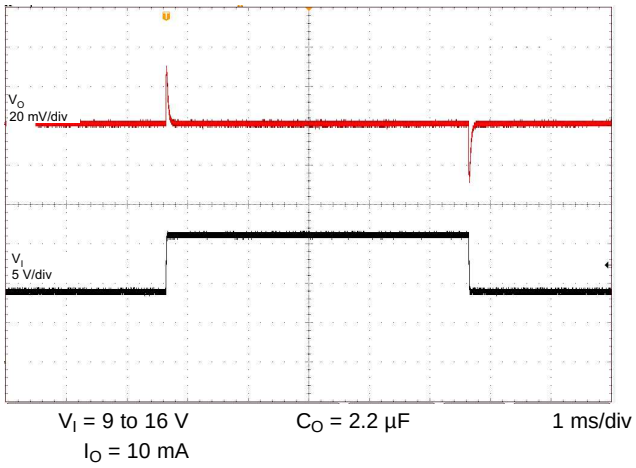


Figure 15. Line Transient (V_O = 5 V)

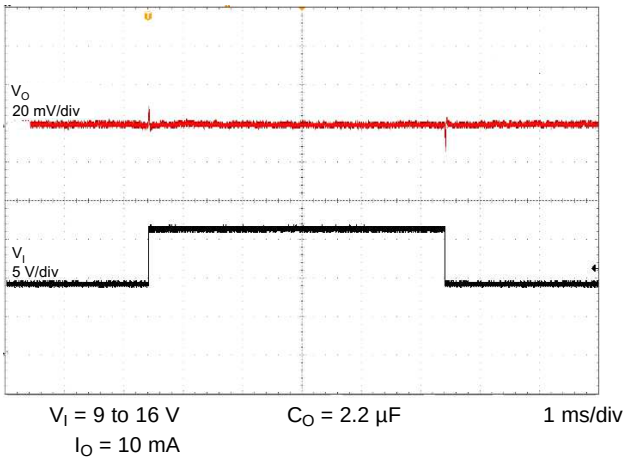


Figure 16. Line Transient (V_O = 3.3 V)

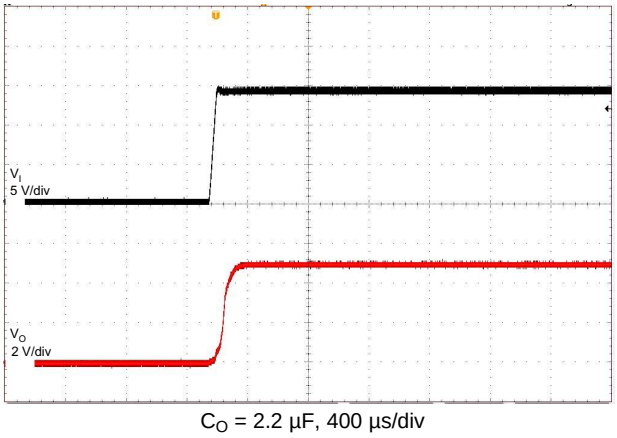


Figure 17. 5-V Power Up

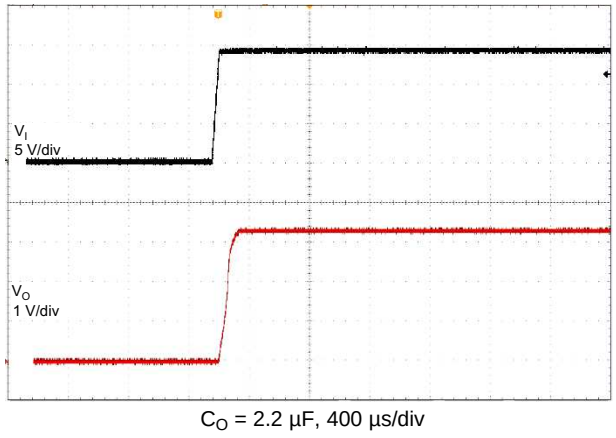


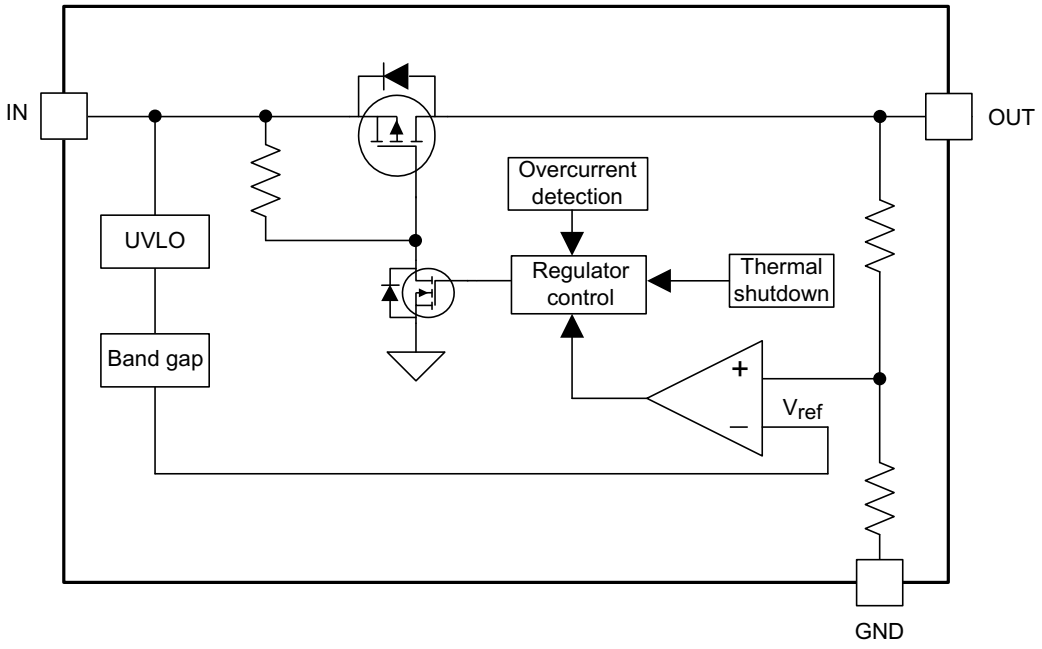
Figure 18. 3.3-V Power Up

7 Detailed Description

7.1 Overview

The TPS7B69xx high-voltage linear regulator operates across a 4-V to 40-V input-voltage range. The device has an output current capacity of 150 mA and fixed output voltages of 3.3 V (TPS7B6933) or 5 V (TPS7B6950). The device features thermal shutdown and short-circuit protection to prevent damage during overtemperature and overcurrent conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input (IN)

The IN pin is a high-voltage-tolerant pin. TI recommends that a capacitor with a value higher than 0.1 µF be connected near this pin to improve the transient performance.

7.3.2 Output (OUT)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During the initial power up, the regulator has a soft start incorporated to control the initial current through the pass element and the output capacitor.

In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 Output Capacitor Selection

For stable operation over the full temperature range and with load currents up to 150 mA, use a capacitor with an effective value between 2.2 µF and 100 µF and ESR smaller than 2 Ω. To improve the load-transient performance, an output capacitor, such as a ceramic capacitor with low ESR, is recommended.

Feature Description (continued)

7.3.4 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_L) and switch resistor. This tracking allows for a smaller input capacitor and can possibly eliminate the need for a boost converter during cold-crank conditions.

7.3.5 Thermal Shutdown

The TPS7B69xx family of devices incorporates a thermal-shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the hysteresis of TSD, the output turns on again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7B69xx family of devices is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7B69xx family of devices into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Operation With V_I Less Than 4 V

The TPS7B69xx family of devices operates with input voltages above 4 V. The maximum UVLO voltage is 3 V and the device operates at an input voltage above 4 V. The device can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO, the device shuts down.

7.4.2 Operation With V_I Greater Than 4 V

When V_I is greater than 4 V, if the input voltage is higher than V_O plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to V_I minus the dropout voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B69xx family of devices is a 150-mA low-dropout linear regulator designed for up to 40-V V_I operation with only 15-µA quiescent current at light loads. Use the PSpice transient model to evaluate the base function of the device. To download the PSpice transient model, go to the device product folder on www.TI.com. In addition to this model, specific evaluation modules (EVM) are available for these devices. For the EVM and the EVM user guide, go to the device product folder.

8.2 Typical Application

Figure 19 shows the typical application circuit for the TPS7B69xx family of devices. Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to achieve better load transient response. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

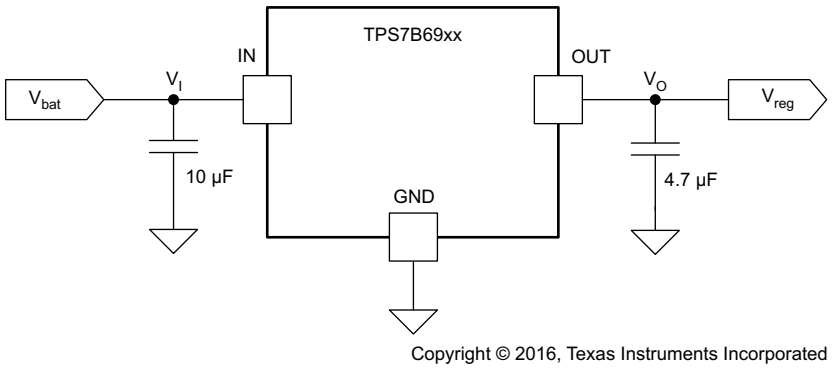


Figure 19. Typical Application Schematic for TPS7B69xx

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	4 V to 40 V
Output voltage	3.3 V, 5 V
Output current rating	150 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating

8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommend value for the decoupling capacitor is higher than 0.1 µF. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The output capacitor value should be between 2.2 µF and 100 µF. The ESR value range should be between 1 mΩ and 2 Ω. TI recommends a ceramic capacitor with low ESR to improve the load-transient response.

8.2.2.3 Power Dissipation and Thermal Considerations

Use Equation 1 to calculate the power dissipated in the device.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I \quad (1)$$

where

- P_D = continuous power dissipation
- I_O = output current
- V_I = input voltage
- V_O = output voltage

Because I_Q « I_O, the term $I_Q \times V_I$ in Equation 1 can be ignored.

For a device under operation at a given ambient air temperature (T_A), use Equation 2 to calculate the junction temperature (T_J).

$$T_J = T_A + (Z_{\theta JA} \times P_D) \quad (2)$$

where

$Z_{\theta JA}$ = junction-to-ambient air thermal impedance

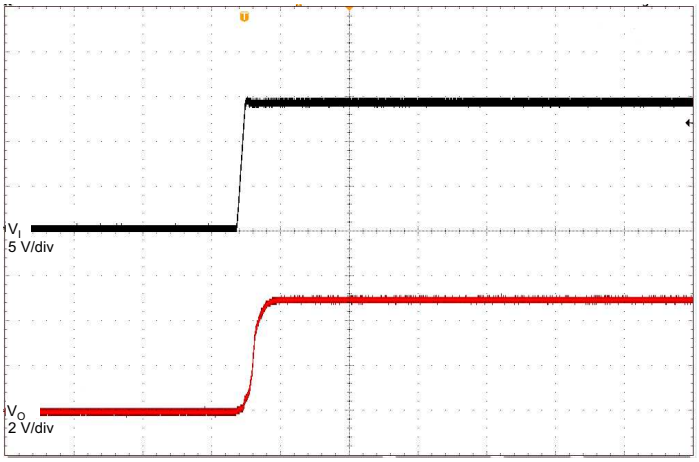
Use Equation 3 to calculate the rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (Z_{\theta JA} \times P_D) \quad (3)$$

For a given maximum junction temperature (T_{Jmax}), use Equation 4 to calculate the maximum ambient air temperature (T_{Amax}) at which the device can operate.

$$T_{Amax} = T_{Jmax} - (Z_{\theta JA} \times P_D) \quad (4)$$

8.2.3 Application Curve



C_O = 2.2 µF, 400 µs/div

Figure 20. Power Up (5 V)

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B69xx device, TI recommends adding an electrolytic capacitor with a value of 10 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the layout of TPS7B69xx family of devices, place the input and output capacitors near the devices as shown in Figure 21 and Figure 22. To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of long traces because they can impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7B69xx evaluation board.

10.2 Layout Example

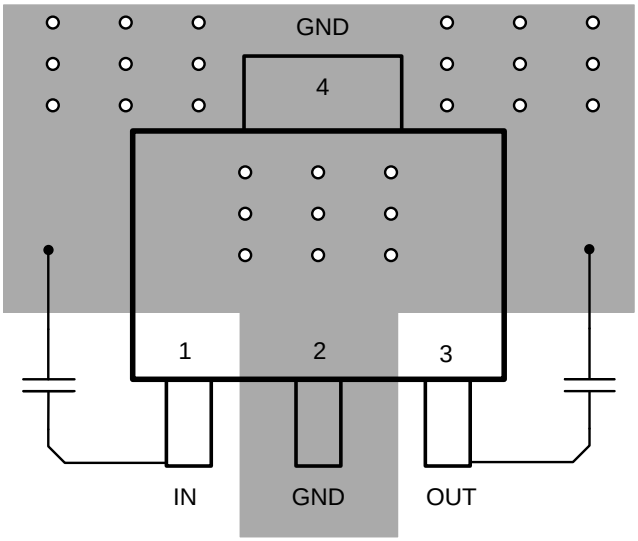


Figure 21. Layout Example for SOT-223 Package

Layout Example (接下页)

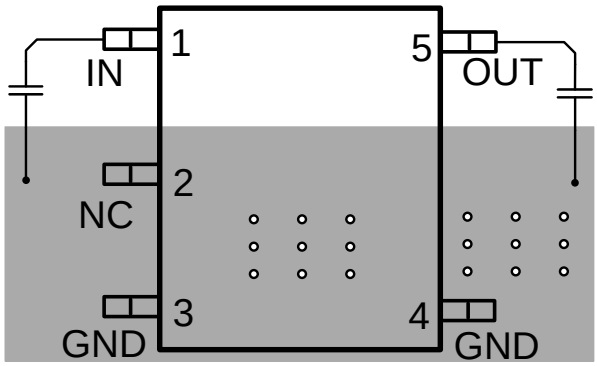


Figure 22. Layout Example for SOT-23 Package

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参见以下部分：

《TPS7B6950EVM 用户指南》，SLVUAC0。

11.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS7B6933	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7B6950	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订，恕不另行通知。要获得这份数据表的浏览器版本，请查阅左侧的导航窗格。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B6933DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 105	ZBFY
TPS7B6933DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	ZBFY
TPS7B6950DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 105	ZAZT
TPS7B6950DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	ZAZT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS7B69 :

- Automotive : TPS7B69-Q1

NOTE: Qualified Version Definitions:

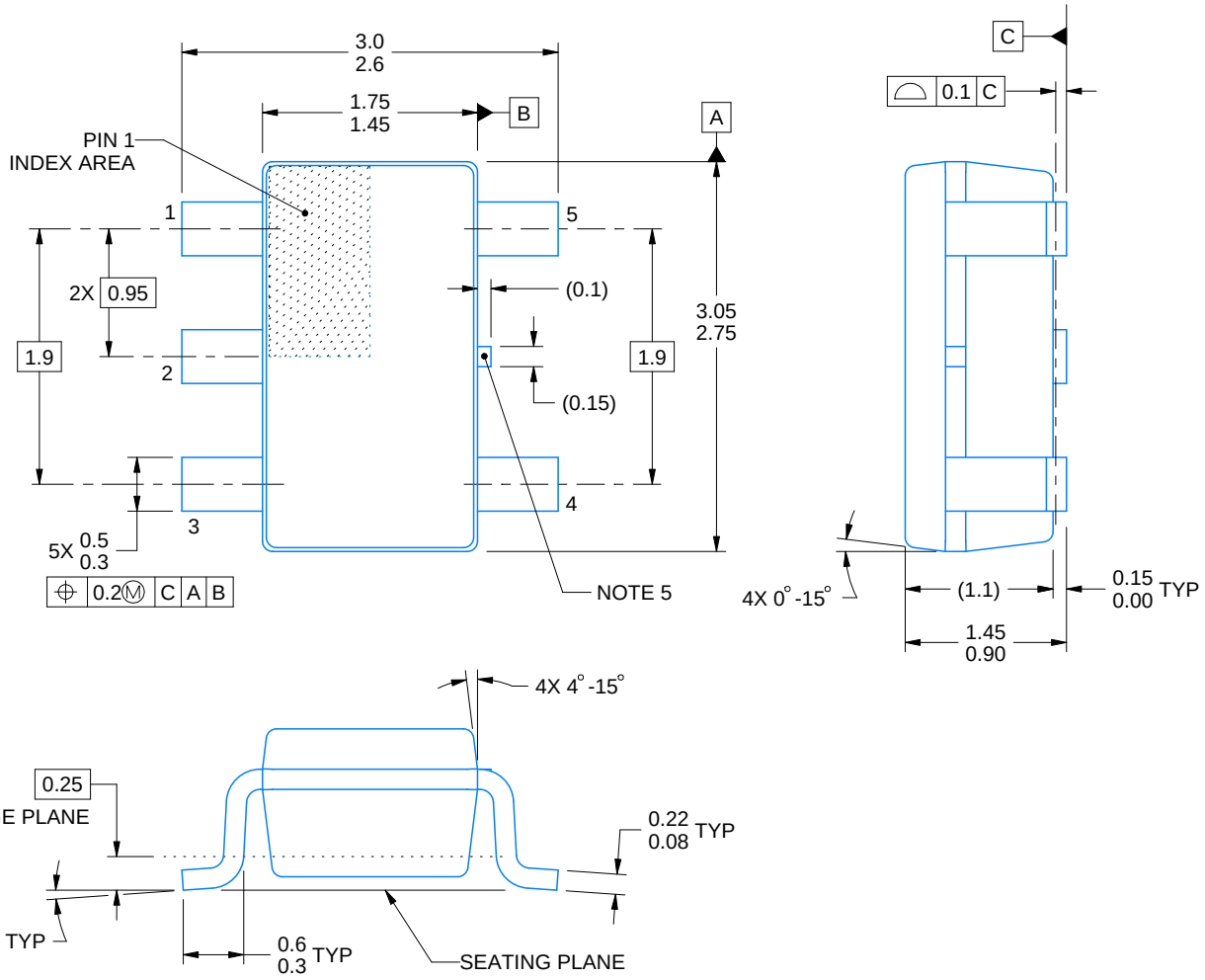
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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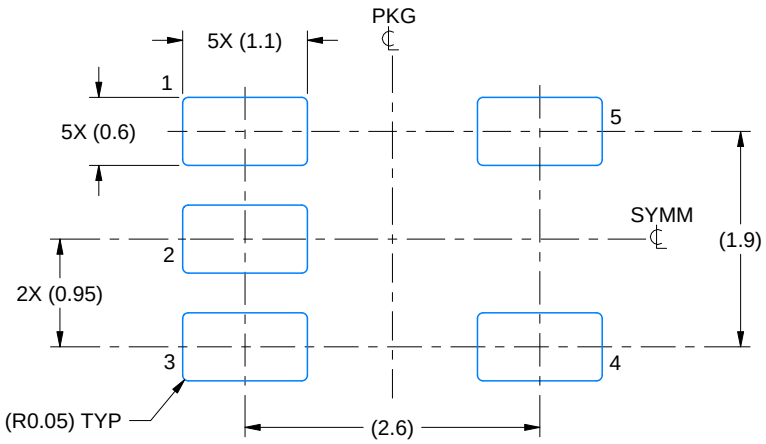
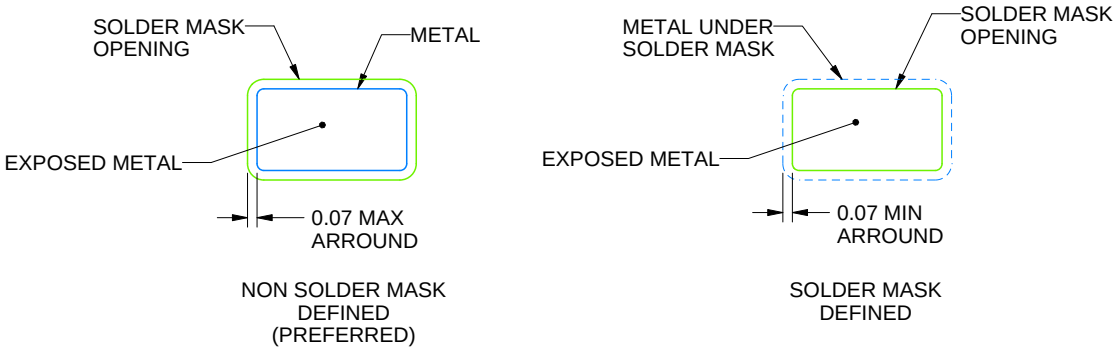
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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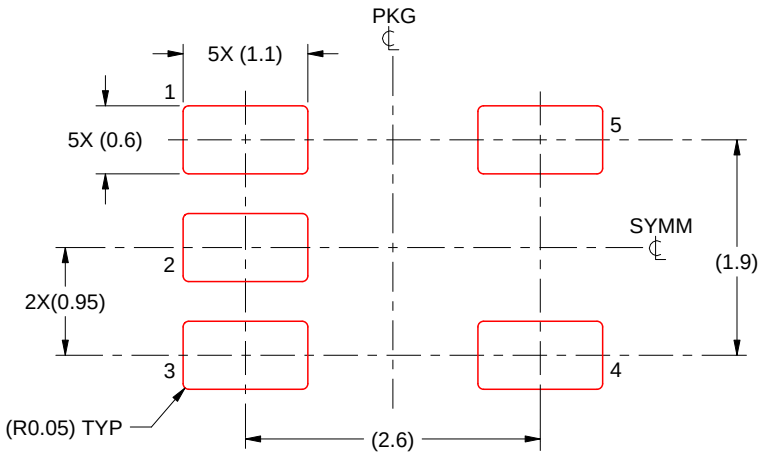
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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