

TPS84259 4.5V 至 40V 输入、15W 负输出集成式电源解决方案

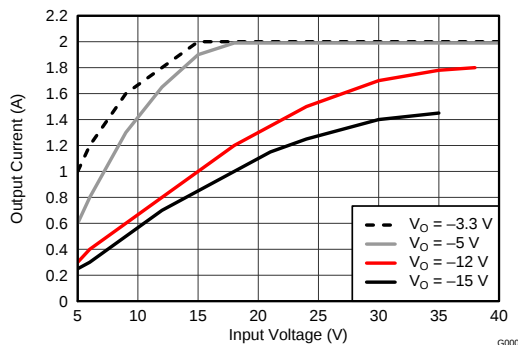
1 特性

- 完整的集成式电源解决方案可实现小尺寸和扁平设计
- 4.5V 至 40V 的宽输入电压范围
- 可调节输出电压范围为 -3V 至 -17V
- 输出电流高达 2A
- 45V 浪涌能力
- 与外部时钟同步
- 可调慢速启动
- 可编程欠压锁定 (UVLO)
- 输出过流保护
- 过热保护
- 运行温度范围: -40°C 至 +85°C
- 增强的热性能: 14°C/W
- 符合 EN55022 B 类辐射标准
- 设计帮助请访问<http://www.ti.com/TPS84259>

2 应用范围

- 工业和电机控制
- 自动测试设备
- 音频/视频中的双极放大器
- 高密度电源系统

安全工作电流

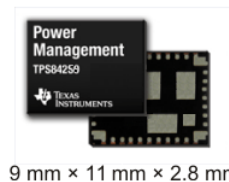
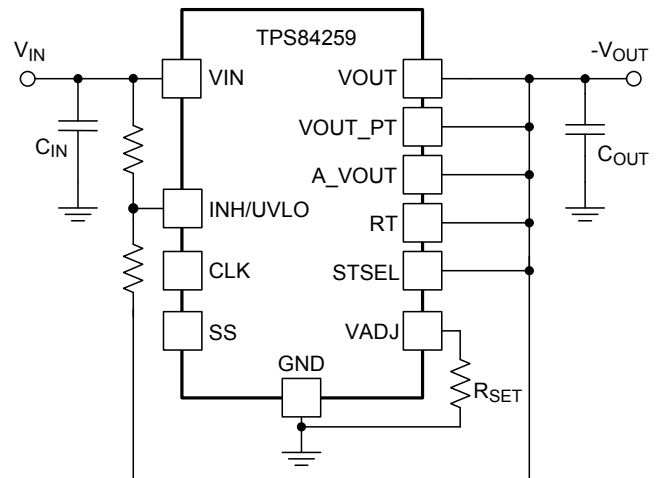


3 说明

TPS84259 是一款易于使用的负输出电压电源模块，它在一个扁平的 QFN 封装内整合了一个 15W 直流/直流转换器、一个电感器和多个无源器件。此整体电源解决方案仅需五个外部组件，并省去了环路补偿和磁性元件选择过程。

9 × 11 × 2.8mm QFN 封装可以轻松焊接到印刷电路板上。该器件设计紧凑，使用较少的组件且具有出色的功率耗散能力。TPS84259 具有离散设计的灵活性和特性集并且非常适合为多种 IC 和要求负输出电压的模拟电路供电。先进的封装技术可提供一个与标准 QFN 贴装和测试技术兼容的稳健耐用且可靠的电源解决方案。

简化应用



9 mm × 11 mm × 2.8 mm



Table 1. ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

4 Specifications

4.1 ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over Operating Temperature Range (Unless Otherwise Noted)		MIN	MAX	UNIT
Input Voltage	V _{IN}	−0.3	45	V
	INH/UVLO	−0.3	5 ⁽²⁾	V
	V _{ADJ}	−0.3	3 ⁽²⁾	V
	SS	−0.3	3 ⁽²⁾	V
	STSEL	−0.3	3 ⁽²⁾	V
	RT	−0.3	3.6 ⁽²⁾	V
	CLK	−0.3	3.6 ⁽²⁾	V
Output Voltage	PH	−0.6	45	V
	PH 10ns Transient	−2	45	V
	V _{OUT}	−0.6	V _{IN} ⁽²⁾	V
V _{DIFF} (V _{OUT} to exposed thermal pad)			±200	mV
Source Current	INH/UVLO		100	μA
Sink Current	SS		200	μA
Operating Junction Temperature		−40	105 ⁽³⁾	°C
Storage Temperature		−65	150	°C
Peak Reflow Case Temperature ⁽⁴⁾⁽⁵⁾			250	°C
Maximum Number of Reflows Allowed ⁽⁴⁾⁽⁵⁾			3	
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This voltage rating is referenced to A_− V_{OUT}, not GND.
- (3) See the temperature derating curves in the Typical Characteristics section for thermal information.
- (4) For soldering specifications, refer to the [Soldering Requirements for BQFN Packages](#) application note.
- (5) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

4.2 RECOMMENDED OPERATING CONDITIONS

Over Operating Free-Air Temperature Range (Unless Otherwise Noted)		MIN	MAX	UNIT
V _{IN}	Input Voltage	4.5	40	V
V _{OUT}	Output Voltage	−3.0	−17	V

4.3 PACKAGE SPECIFICATIONS

TPS84259		UNIT
Weight		0.9 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T _A = 40°C, ground benign	31.7 Mhrs

4.4 ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $V_{\text{IN}} = 12\text{ V}$, $V_{\text{OUT}} = -5.0\text{ V}$, $I_{\text{OUT}} = 2.0\text{ A}$

$C_{\text{IN}} = 2 \times 2.2\text{ }\mu\text{F}$ ceramic, $C_{\text{OUT}} = 2 \times 47\text{ }\mu\text{F}$ ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{OUT}	Output current	Over input voltage and output voltage range		0 ⁽¹⁾		2.0 ⁽²⁾	A
V _{IN}	Input voltage range	Over output current range		4.5		40 ⁽³⁾	V
UVLO	V _{IN} Undervoltage lockout	Rising only, R _{UVLO1} = 174 kΩ, R _{UVLO2} = 63.4 kΩ			4.5		V
V _{OUT(adj)}	Output voltage adjust range	Over output current range		−3.0		−17 ⁽³⁾	V
V _{OUT}	Set-point voltage tolerance	T _A = 25°C, I _{OUT} = 100 mA				2.0% ⁽⁴⁾	
	Temperature variation	−40°C ≤ T _A ≤ +85°C			±0.5%	±1.0%	
	Line regulation	Over input voltage range			±0.1%		
	Load regulation	From 100 mA to I _{OUT(max)}			±0.4%		
	Total output voltage variation	Includes set-point, line, load, and temperature variation				3.0% ⁽⁴⁾	
η	Efficiency	V _{IN} = 24 V	V _{OUT} = −12 V, I _{OUT} = 1.0 A		85 %		
			V _{OUT} = −5.0 V, I _{OUT} = 1.0 A		81 %		
			V _{OUT} = −3.3 V, I _{OUT} = 1.0 A		77 %		
		V _{IN} = 12 V	V _{OUT} = −12 V, I _{OUT} = 0.6 A		86 %		
			V _{OUT} = −5.0 V, I _{OUT} = 1.0 A		81 %		
			V _{OUT} = −3.3 V, I _{OUT} = 1.0 A		78 %		
Output voltage ripple		20 MHz bandwidth, 100 mA ≤ I _{OUT} ≤ I _{OUT(max)}			1%		V _{OUT}
I _{LIM}	Current limit threshold				3.0 ⁽⁵⁾		A
Transient response		1.0 A/μs load step from 25 to 75% I _{OUT(max)}	Recovery time		500		μs
			V _{OUT} over/undershoot		80		mV
V _{INH}	Inhibit threshold voltage	INH with respect to A_VOUT		1.15	1.25	1.36 ⁽⁶⁾	V
I _{INH}	INH Input current	V _{INH} < 1.15 V			−0.9		μA
		V _{INH} > 1.36 V			−3.8		μA
I _{I(stby)}	Input standby current	INH pin to A_VOUT			1.3	4	μA
f _{SW}	Switching frequency	RT pin to A_VOUT		700	800	900	kHz
f _{CLK}	Synchronization frequency		R _{RT} = 0 Ω	700 ⁽⁷⁾		900 ⁽⁷⁾	kHz
			R _{RT} = 93.1 kΩ	400 ⁽⁷⁾		600 ⁽⁷⁾	kHz
V _{CLK-H}	CLK High-Level Threshold	With respect to A_VOUT			1.9	2.2	V
V _{CLK-L}	CLK Low-Level Threshold	With respect to A_VOUT		0.5	0.7		V
D _{CLK}	CLK Duty cycle			25%	50%	75%	
Thermal Shutdown		Thermal shutdown			180		°C
		Thermal shutdown hysteresis			15		°C
C _{IN}	External input capacitance	Ceramic		4.7 ⁽⁸⁾	10		μF
		Non-ceramic			22		
C _{OUT}	External output capacitance			100 ⁽⁹⁾		430 ⁽⁹⁾	μF

- (1) This device can regulate V_{OUT} down to 0 A, however the ripple may increase due to pulse-skipping at light loads. See [Light-Load Behavior](#) for more information. See [No-Load Operation](#) when operating at 0 A.
- (2) The maximum current is dependant on V_{IN} and V_{OUT} , see [Figure 33](#).
- (3) The sum of $V_{\text{IN}} + |V_{\text{OUT}}|$ must not exceed 50 V.
- (4) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
- (5) This product is not designed to endure a sustained ($> 5\text{ sec}$) over-current condition.
- (6) If this pin is left open circuit, the device operates when input power is applied. An external level-shifter is required to interface with this pin. See [Output On/Off Inhibit \(INH\)](#) for further guidance.
- (7) The synchronization frequency is dependant on V_{IN} and V_{OUT} as shown in [Switching Frequency](#). R_{RT} must be either $0\text{ }\Omega$ or $93.1\text{ k}\Omega$.
- (8) A minimum of $4.7\text{ }\mu\text{F}$ of ceramic external capacitance is required across the input (V_{IN} and PGND connected) for proper operation. Locate the capacitor close to the device. See [Table 3](#) for more details.
- (9) The amount of required capacitance must include at least $2 \times 47\text{ }\mu\text{F}$ ceramic capacitor (or $4 \times 22\text{ }\mu\text{F}$). Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See [Table 3](#) for more details. See [Inrush Current](#) section when adding additional output capacitance.

4.5 THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS84259	UNIT
		RKG	
		41 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	14	°C/W
ψ_{JT}	Junction-to-top characterization parameter ⁽³⁾	3.3	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁴⁾	6.8	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, literature number [SPRA953](#).
- (2) The junction-to-ambient thermal resistance, θ_{JA} , applies to devices soldered directly to a 100 mm x 100 mm double-sided PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA} .
- (3) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
- (4) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

5 DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM

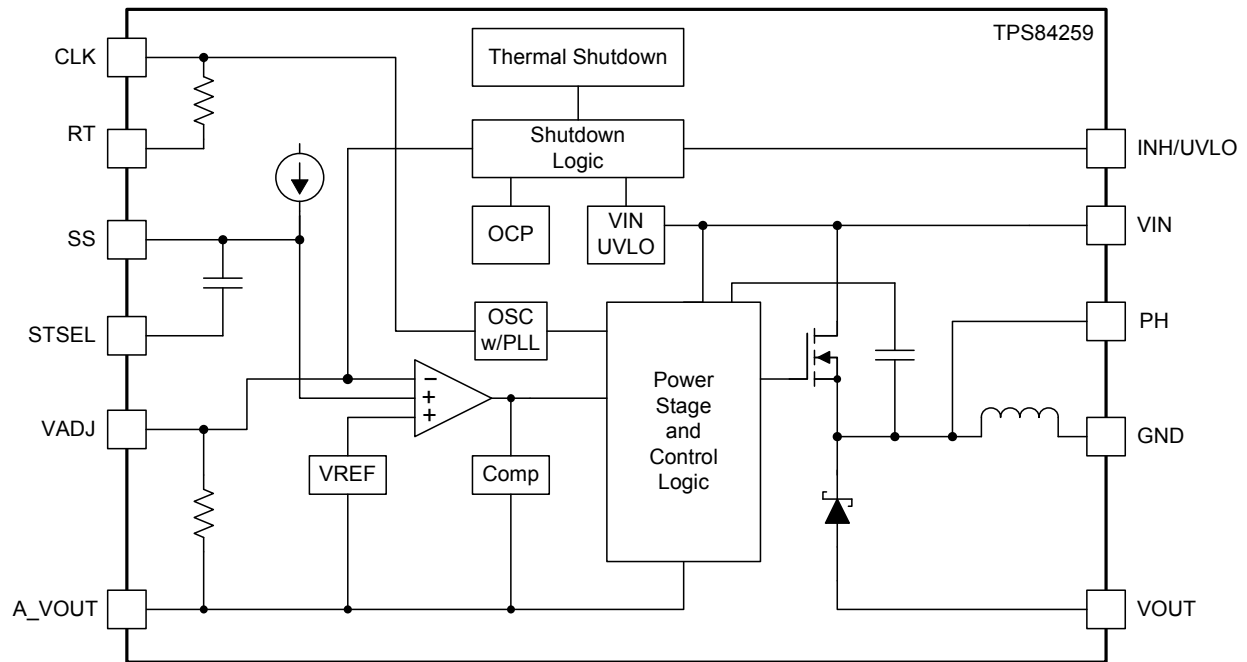
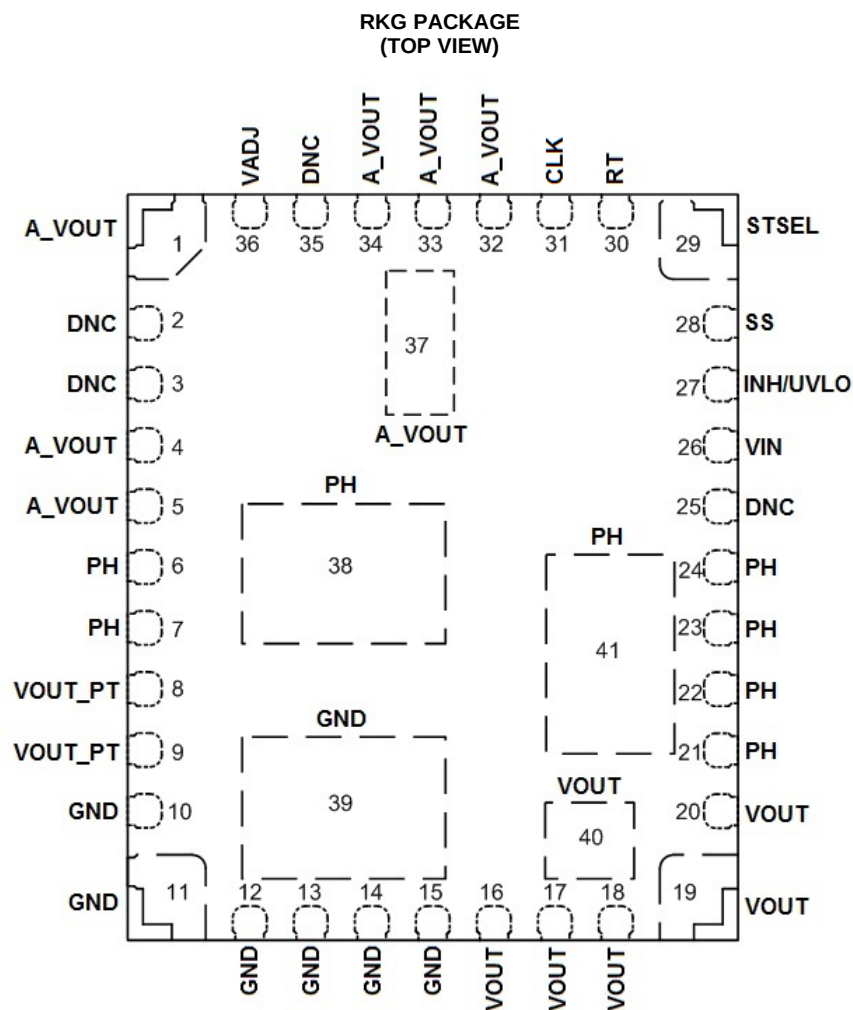


Table 2. PIN DESCRIPTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
VIN	26	Input voltage. This pin supplies all power to the converter. Connect this pin to the input supply and connect bypass capacitors between this pin and GND.
VOUT	16	Negative output voltage with respect to GND. Connect these pins to the output load and connect external bypass capacitors between these pins and GND. Pad 40 should be connected to PCB VOUT planes using multiple vias for good thermal performance.
	17	
	18	
	19	
	20	
	40	
GND	10	This is the return current path for the power stage of the device. These pins are connected to the internal output inductor. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT.
	11	
	12	
	13	
	14	
	15	
PH	39	Phase switch node. Do not place any external component on these pins or tie them to a pin of another function.
	6	
	7	
	21	
	22	
	23	
	24	
VOUT_PT	38	VOUT and A_VOUT Connection Point. Connect VOUT to A_VOUT at these pins as shown in the Layout Considerations section. These pins are not connected to internal circuitry, and are not connected to one another.
	41	
DNC	8	Do Not Connect. Do not connect these pins to GND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
	9	
	2	
	3	
A_VOUT	25	These pins are connected to the internal analog reference (A_VOUT) of the device. This node should be treated as the negative voltage reference for the analog control circuitry. Pad 37 should be connected to the PCB A_VOUT plane using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the module. Connect A_VOUT to VOUT at a single point (VOUT_PT; pins 8 & 9). See Layout Recommendations .
	35	
	1	
	4	
	5	
	32	
RT	33	Switching frequency adjust pin. To operate at the recommended free-running frequency, connect this pin to A_VOUT. Connecting a resistor between this pin and A_VOUT will reduce the switching frequency. See Switching Frequency section.
	34	
CLK	37	Use this pin to synchronize to an external clock. If unused, isolate this pin from any other signal.
INH/UVLO	30	Inhibit and UVLO adjust pin. Use an external level-shifter device to ground this pin to control the INH function. A resistor divider between this pin, A_VOUT, and VIN sets the UVLO voltage.
SS	27	Slow-start pin. Connecting an external capacitor between this pin and A_VOUT adjusts the output voltage rise time.
STSEL	28	Slow-start select. Connect this pin to A_VOUT to enable the internal SS capacitor.
VADJ	29	Connecting a resistor between this pin and GND sets the output voltage. A dedicated GND sense line connected at the load will improve regulation at the load. See Figure 48 in the Layout Considerations section.



6 TYPICAL CHARACTERISTICS (VIN = 5 V) ⁽¹⁾ ⁽²⁾

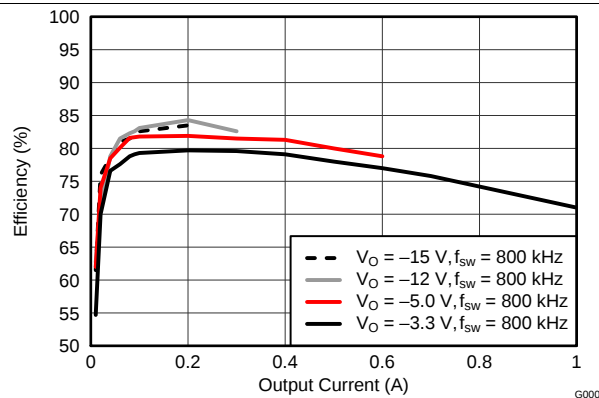


Figure 1. Efficiency vs. Output Current

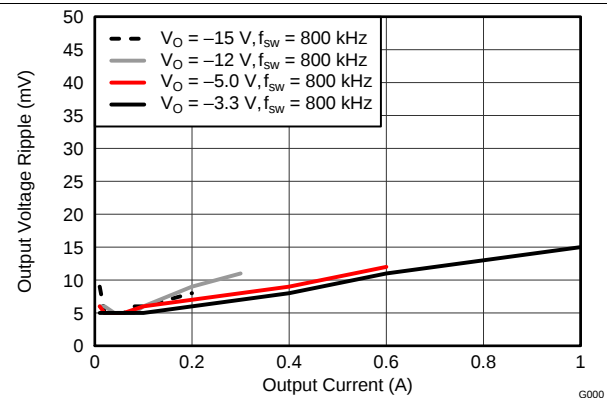


Figure 2. Voltage Ripple vs. Output Current

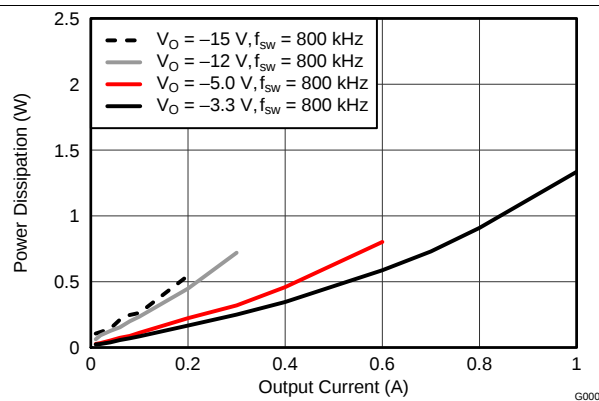


Figure 3. Power Dissipation vs. Output Current

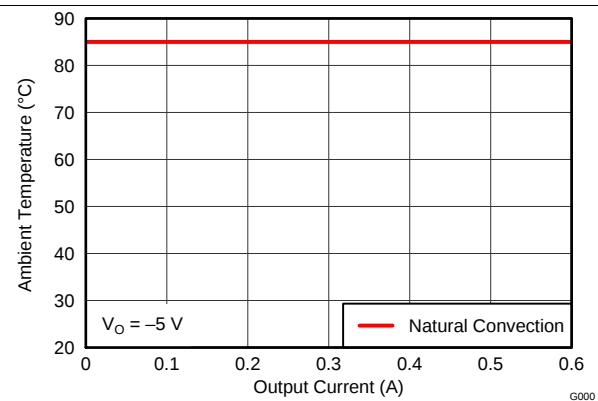


Figure 4. Safe Operating Area

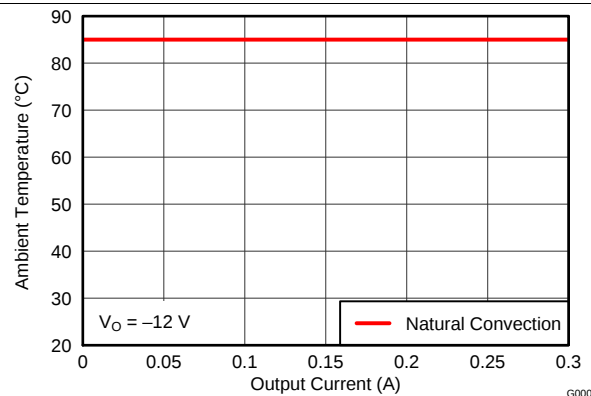


Figure 5. Safe Operating Area

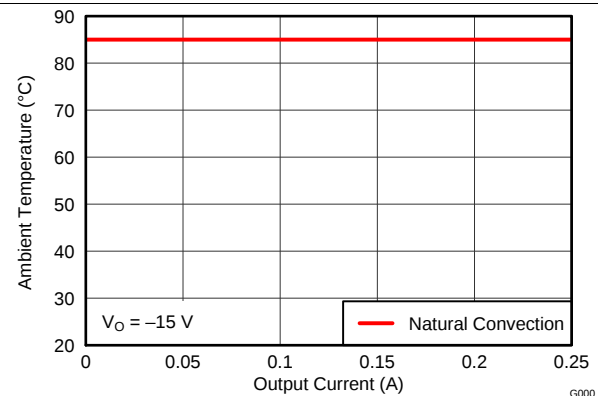


Figure 6. Safe Operating Area

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 1](#), [Figure 2](#), and [Figure 3](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to [Figure 4](#), [Figure 5](#), and [Figure 6](#).

7 TYPICAL CHARACTERISTICS (VIN = 12 V) ⁽¹⁾ ⁽²⁾

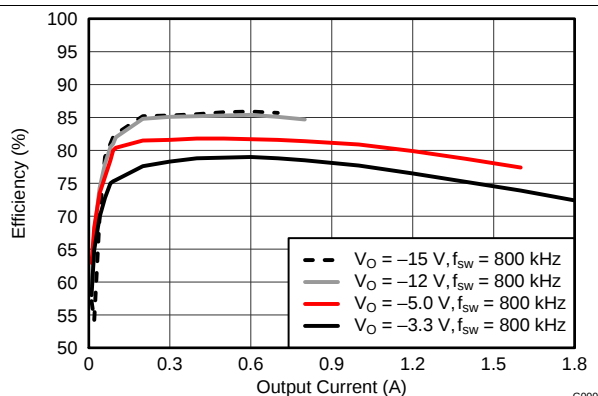


Figure 7. Efficiency vs. Output Current

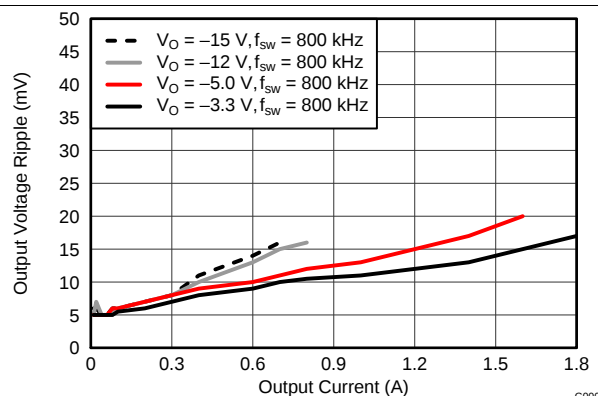


Figure 8. Voltage Ripple vs. Output Current

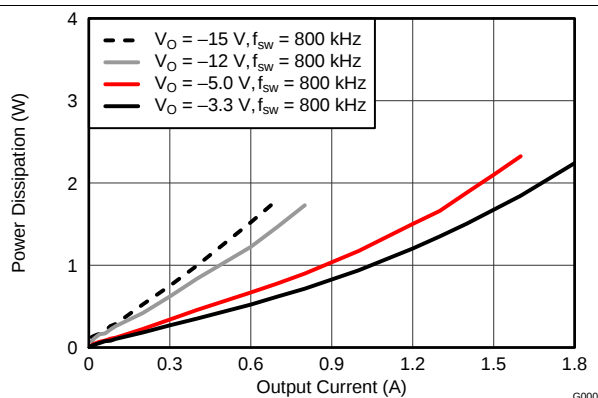


Figure 9. Power Dissipation vs. Output Current

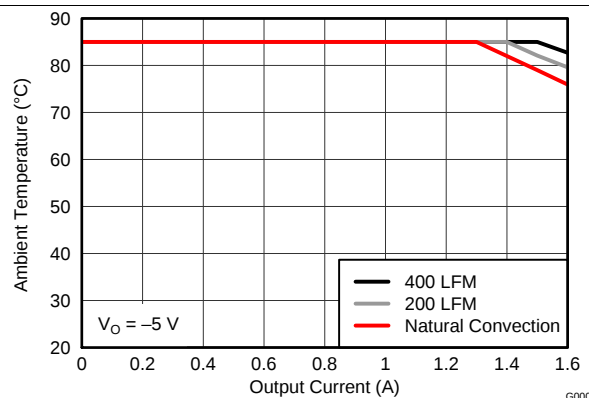


Figure 10. Safe Operating Area

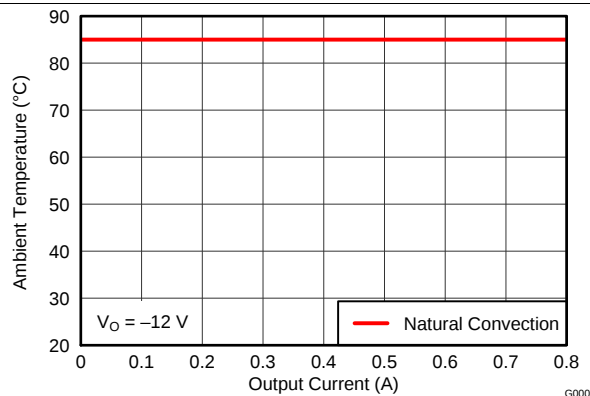


Figure 11. Safe Operating Area

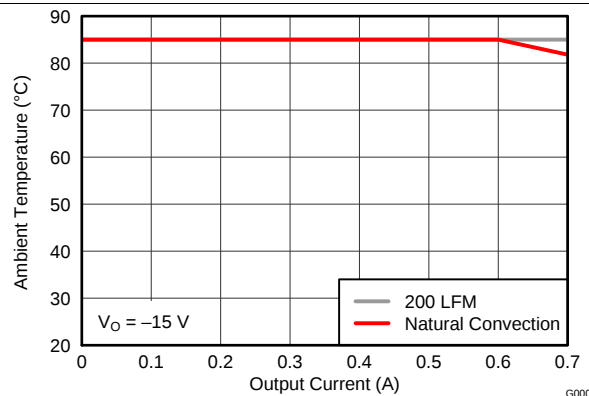


Figure 12. Safe Operating Area

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 7](#), [Figure 8](#), and [Figure 9](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to [Figure 10](#), [Figure 11](#), and [Figure 12](#).

8 TYPICAL CHARACTERISTICS (VIN = 24 V) (1) (2) (3)

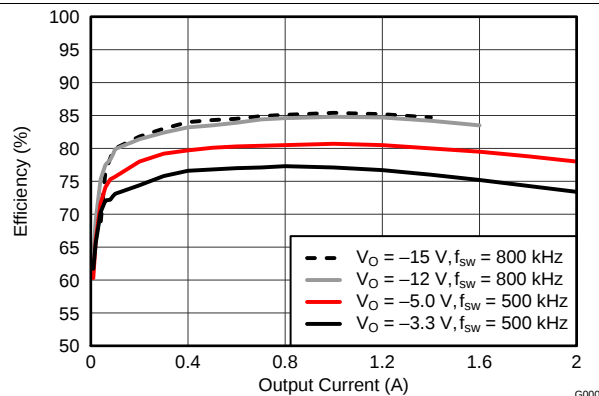


Figure 13. Efficiency vs. Output Current

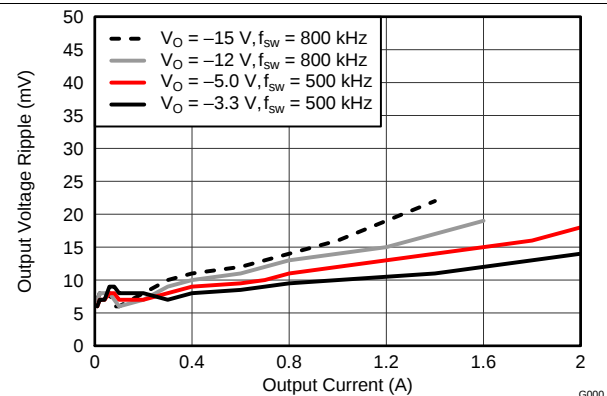


Figure 14. Voltage Ripple vs. Output Current

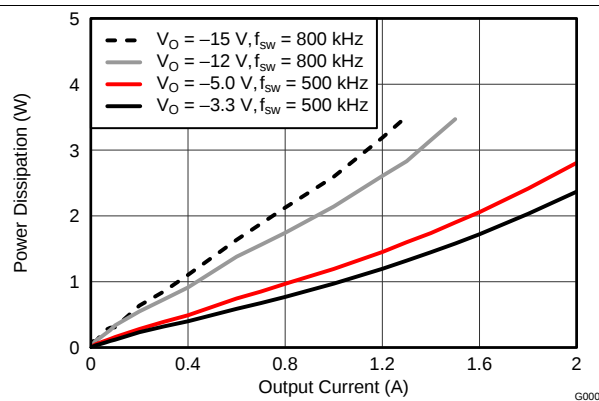


Figure 15. Power Dissipation vs. Output Current

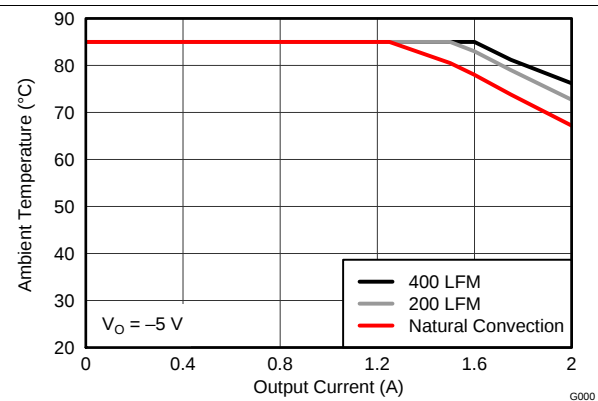


Figure 16. Safe Operating Area

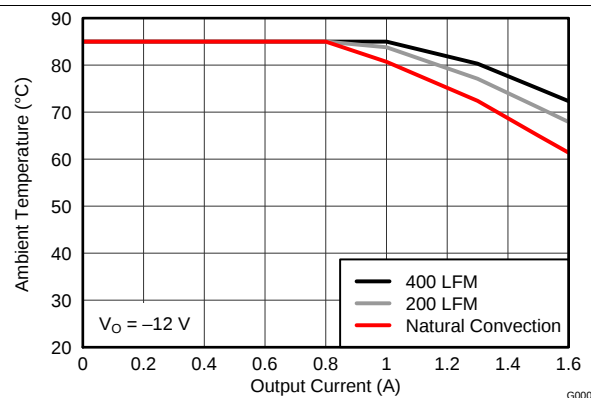


Figure 17. Safe Operating Area

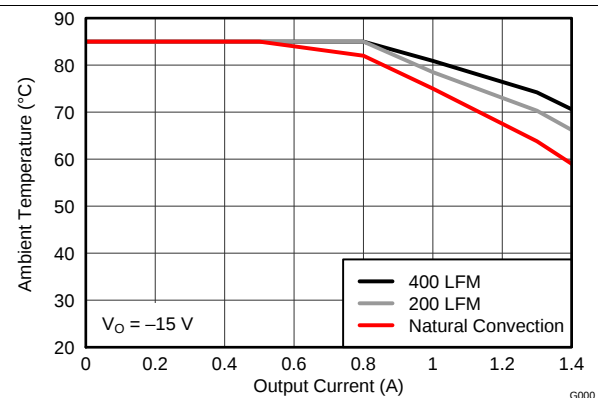


Figure 18. Safe Operating Area

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 13](#), [Figure 14](#), and [Figure 15](#).
- (2) At light load the output voltage ripple may increase due to pulse skipping. See [Light-Load Behavior](#) for more information. Applies to [Figure 14](#).
- (3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to [Figure 16](#), [Figure 17](#), and [Figure 18](#).

9 TYPICAL CHARACTERISTICS (VIN = 36 V) (1) (2) (3)

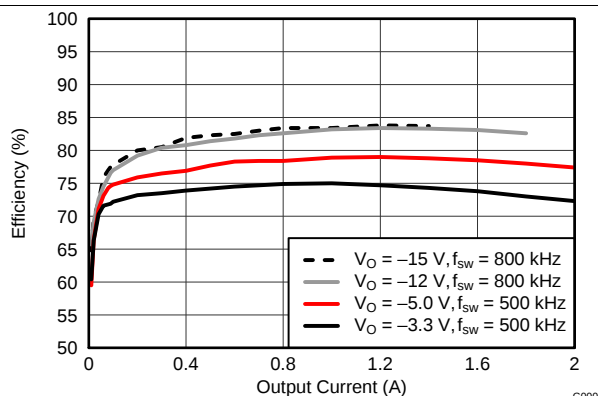


Figure 19. Efficiency vs. Output Current

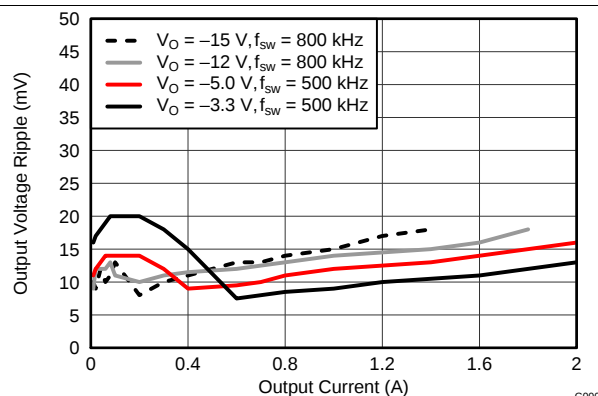


Figure 20. Voltage Ripple vs. Output Current

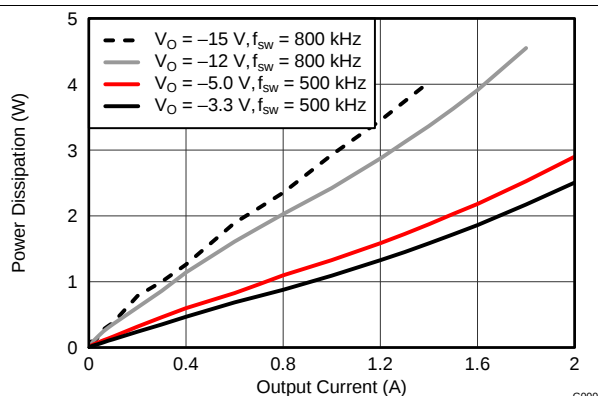


Figure 21. Power Dissipation vs. Output Current

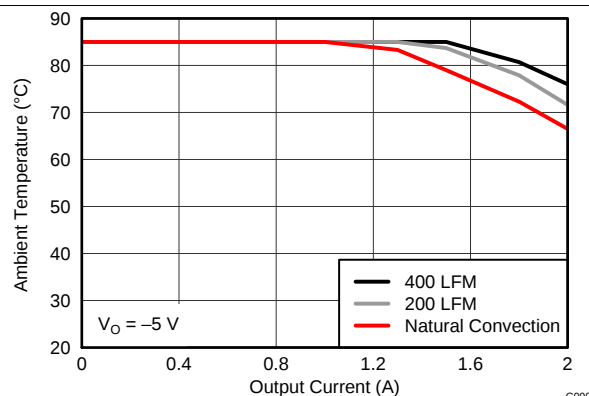


Figure 22. Safe Operating Area

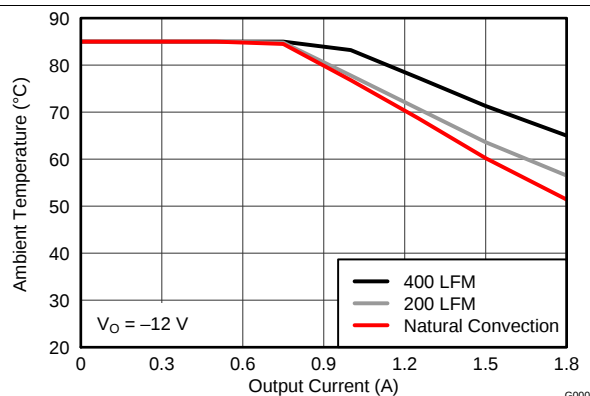


Figure 23. Safe Operating Area

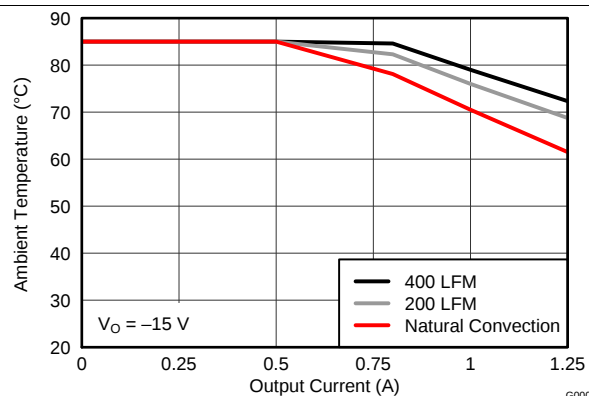
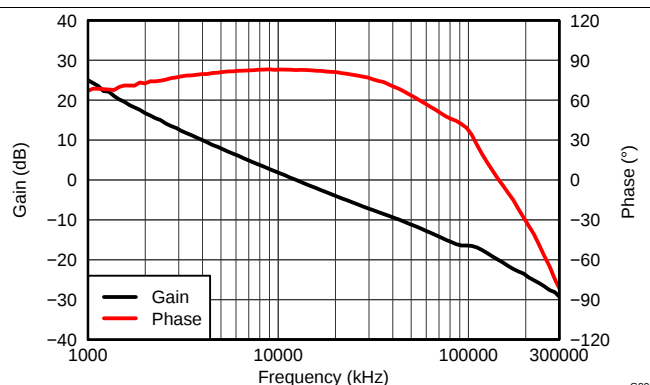
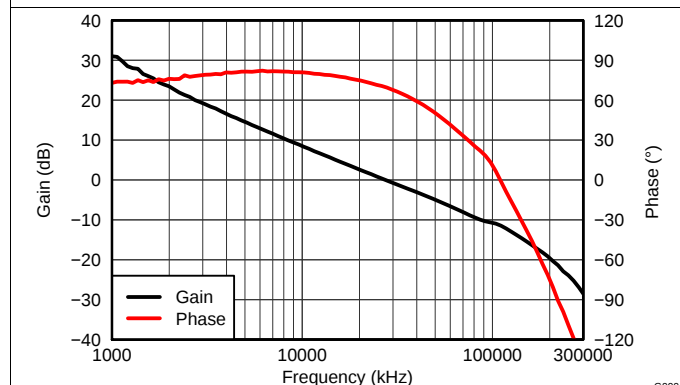
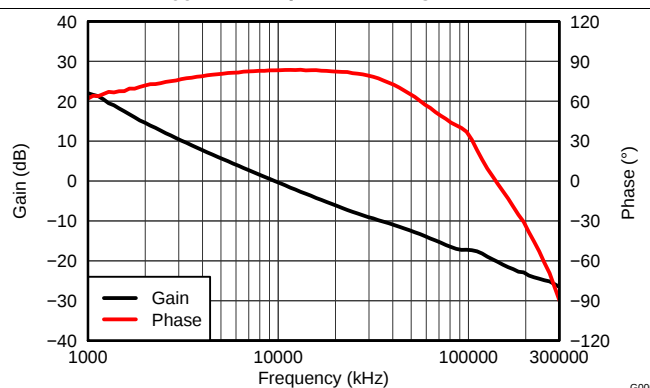
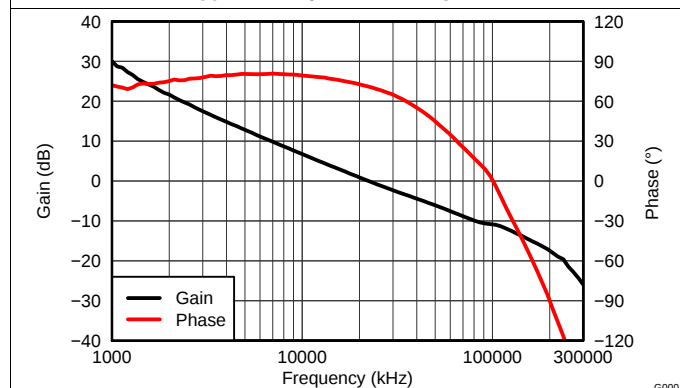
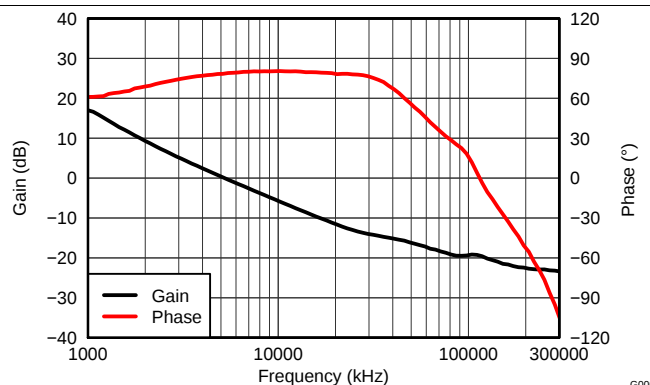
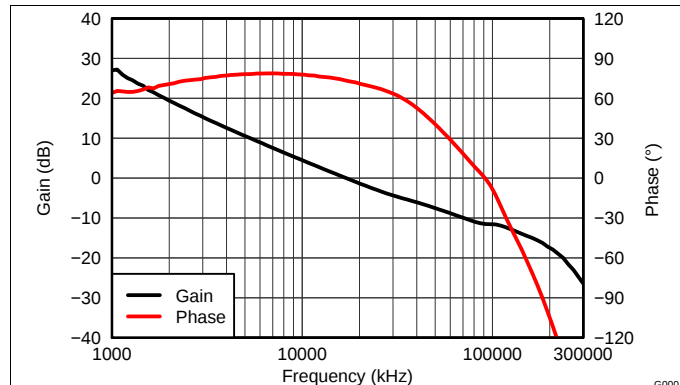


Figure 24. Safe Operating Area

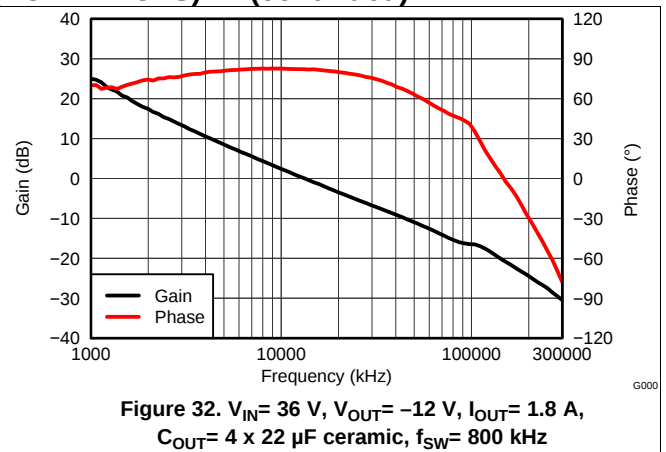
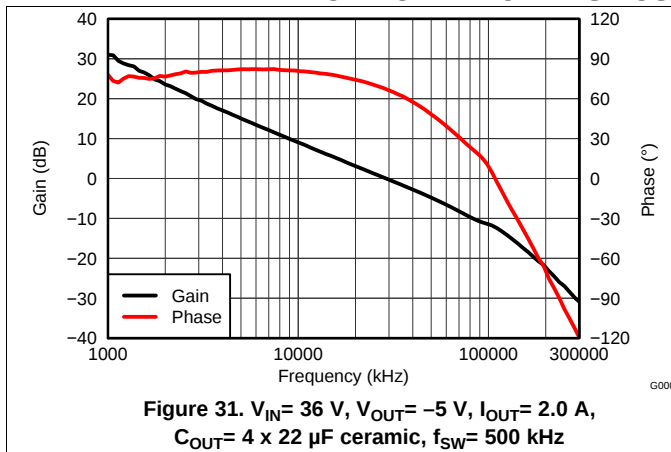
- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 19](#), [Figure 20](#), and [Figure 21](#).
- (2) At light load the output voltage ripple may increase due to pulse skipping. See [Light-Load Behavior](#) for more information. Applies to [Figure 20](#).
- (3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to [Figure 22](#), [Figure 23](#), and [Figure 24](#).

10 TYPICAL CHARACTERISTICS (BODE PLOTS) ⁽¹⁾



(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter.

TYPICAL CHARACTERISTICS (BODE PLOTS) ⁽¹⁾ (continued)



11 CAPACITOR RECOMMENDATIONS FOR THE TPS84259 POWER SUPPLY

11.1 Capacitor Technologies

11.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

11.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

11.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

11.2 Input Capacitor

The TPS84259 requires a minimum input capacitance of 4.7 µF of ceramic type. The voltage rating of input capacitors must be greater than the maximum input voltage. The ripple current rating of the capacitor must be at least 450 mArms. [Table 3](#) includes a preferred list of capacitors by vendor.

11.3 Output Capacitor

The required output capacitance of the TPS84259 can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 2 × 47 µF of ceramic type (or 4 × 22 µF). The voltage rating of output capacitors must be greater than the output voltage. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in [Table 3](#) are required. Additional capacitance above the required minimum is determined by actual transient deviation requirements. [Table 3](#) includes a preferred list of capacitors by vendor.

Table 3. Recommended Input/Output Capacitors⁽¹⁾

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR ⁽²⁾ (mΩ)
Murata	X5R	GRM31CR61H225KA88L	50	2.2	2
TDK	X5R	C3216X5R1H475K	50	4.7	2
Murata	X5R	GRM32ER61E226K	16	22	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Sanyo	POSCAP	16TQC68M	16	68	50
Sanyo	POSCAP	6TPE100MI	6.3	100	25
Kemet	T530	T530D227M006ATE006	6.3	220	6

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**

Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.

(2) Maximum ESR @ 100 kHz, 25°C.

12 APPLICATION INFORMATION

12.1 Adjusting the Output Voltage

The TPS84259 is designed to provide output voltages from –3 V to –17 V. The output voltage is determined by the value of R_{SET} , which must be connected between the VADJ pin (Pin 36) and GND. Table 4 gives the standard external R_{SET} resistor for a number of common bus voltages.

Table 4. Standard R_{SET} Resistor Values for Common Output Voltages

OUTPUT VOLTAGE V_{OUT} (V)	–3.3	–5.0	–8.0	–12.0	–15.0
R_{SET} (k Ω)	31.6	52.3	90.9	140	178

For other output voltages the value of R_{SET} can be calculated using the following formula, or simply selected from the range of values given in Table 5.

$$R_{SET} = 10 \times \left(\frac{|V_{OUT}|}{0.798} - 1 \right) \text{ (k}\Omega\text{)} \quad (1)$$

Table 5. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (k Ω)	V_{OUT} (V)	R_{SET} (k Ω)	V_{OUT} (V)	R_{SET} (k Ω)
–3.0	27.4	–7.5	84.5	–12.5	147
–3.3	31.6	–8.0	90.9	–13.0	154
–3.5	34.0	–8.5	97.6	–13.5	158
–4.0	40.2	–9.0	102	–14.0	165
–4.5	46.4	–9.5	110	–14.5	174
–5.0	52.3	–10.0	115	–15.0	178
–5.5	59.0	–10.5	121	–15.5	187
–6.0	64.9	–11.0	127	–16.0	191
–6.5	71.5	–11.5	133	–16.5	196
–7.0	78.7	–12.0	140	–17.0	205

12.2 Safe Operating Current

The amount of output current that can safely be delivered by the TPS84259 depends on the input voltage and the output voltage. Figure 33 shows the maximum output current for four standard output voltages over input voltage.

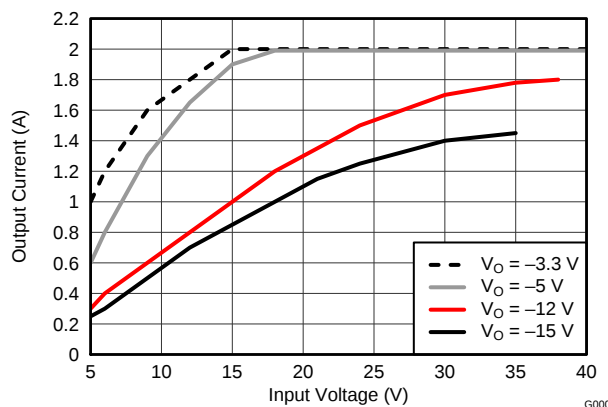


Figure 33. Safe Operating Current

12.3 Application Schematics

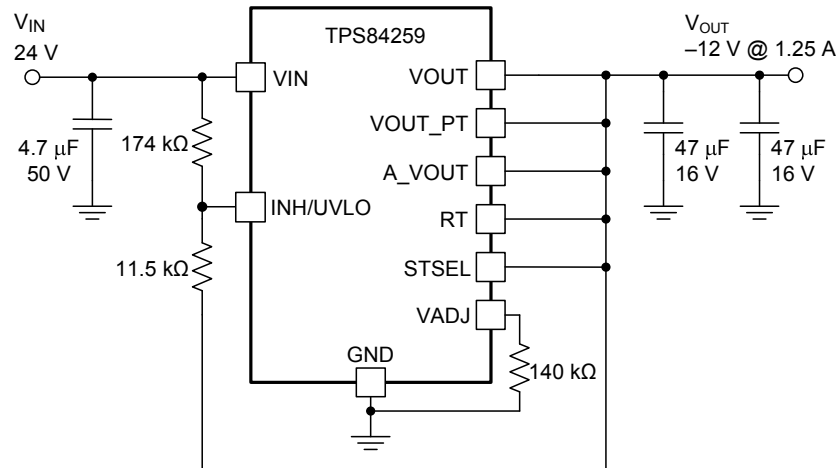


Figure 34. Typical Schematic
 $V_{IN} = 24\text{ V}$, $V_{OUT} = -12\text{ V}$

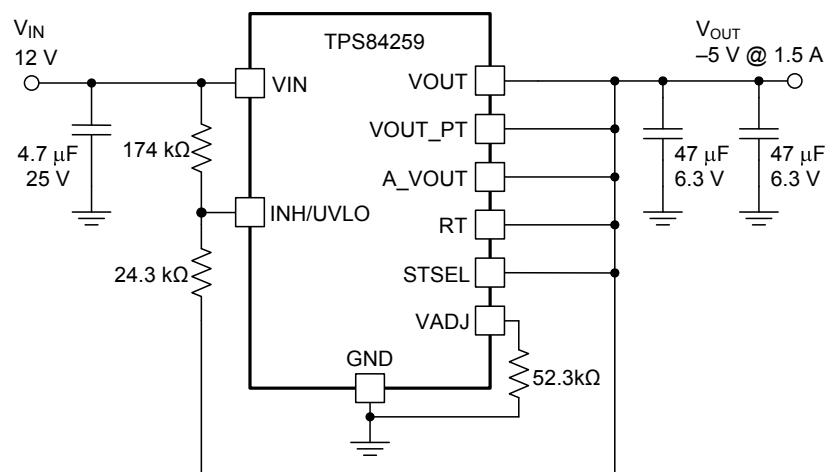


Figure 35. Typical Schematic
 $V_{IN} = 12\text{ V}$, $V_{OUT} = -5\text{ V}$

12.4 Input Voltage

The TPS84259 operates over the input voltage range of 4.5 V to 40 V. The maximum input voltage is 40 V, however, the sum of $V_{IN} + |V_{OUT}|$ must not exceed 50 V.

See the [Undervoltage Lockout \(UVLO\) Threshold](#) section of this datasheet for more information.

12.5 Undervoltage Lockout (UVLO) Threshold

At turn-on, the V_{ON} UVLO threshold determines the input voltage level where the device begins power conversion. R_{UVLO1} and R_{UVLO2} set the turn-on threshold as shown in [Figure 36](#). The UVLO threshold is not present during the power-down sequence. Applications requiring a turn-off threshold must monitor the input voltage with external circuitry and shut-down using the INH control (see [Output On/Off Inhibit \(INH\)](#)).

The V_{ON} UVLO threshold must be set to at least 4.5 V to insure proper start-up and reduce current surges on the host input supply as the voltage rises. If possible, it is recommended to set the UVLO threshold to approximately 80 to 85% of the minimum expected input voltage.

Use [Equation 2](#) and [Equation 3](#) to calculate the values of R_{UVLO1} and R_{UVLO2} . V_{ON} is the voltage threshold during power-up when the input voltage is rising. [Table 6](#) lists standard resistor values for R_{UVLO1} and R_{UVLO2} for adjusting the V_{ON} UVLO threshold for several input voltages.

$$R_{UVLO1} = \frac{0.5}{2.9 \times 10^{-3}} (k\Omega) \quad (2)$$

$$R_{UVLO2} = \frac{1.25}{\left(\frac{(V_{ON} - 1.25)}{R_{UVLO1}} \right) + 0.9 \times 10^{-3}} (k\Omega) \quad (3)$$

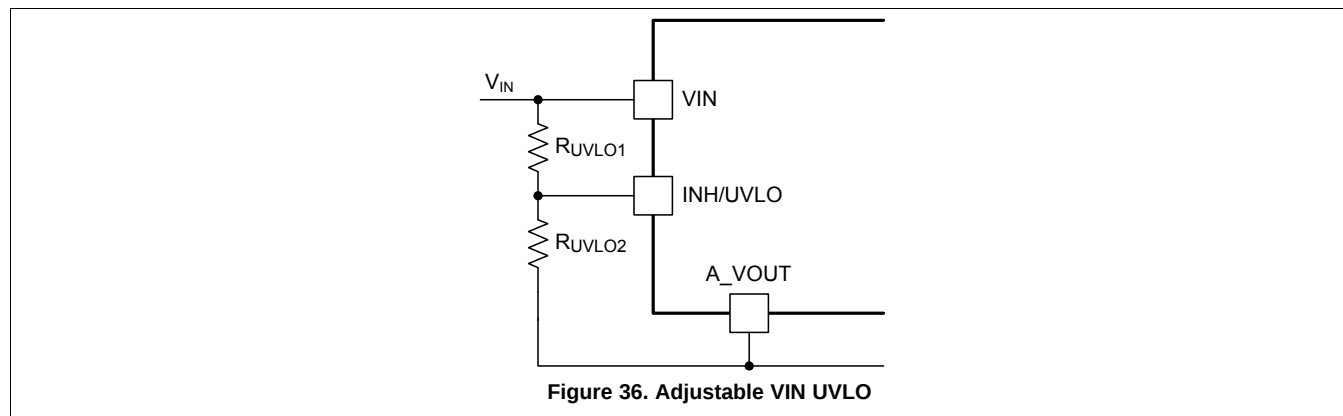


Table 6. Standard Resistor Values to set V_{ON} UVLO Threshold

V_{ON} THRESHOLD (V)	4.5	5.0	6.5	8.0	9.0	10.0	15.0	20.0	30.0
R_{UVLO1} (k Ω)	174	174	174	174	174	174	174	174	174
R_{UVLO2} (k Ω)	63.4	56.2	40.2	31.6	27.4	24.3	15.8	11.5	7.50

12.6 Power-Up Characteristics

When configured as shown in the application schematics, the TPS84259 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. [Figure 37](#) shows the start-up waveforms for a TPS84259, operating from a 12 V input and the output voltage adjusted to –5 V. The waveform were measured with a 1.5-A constant current load.

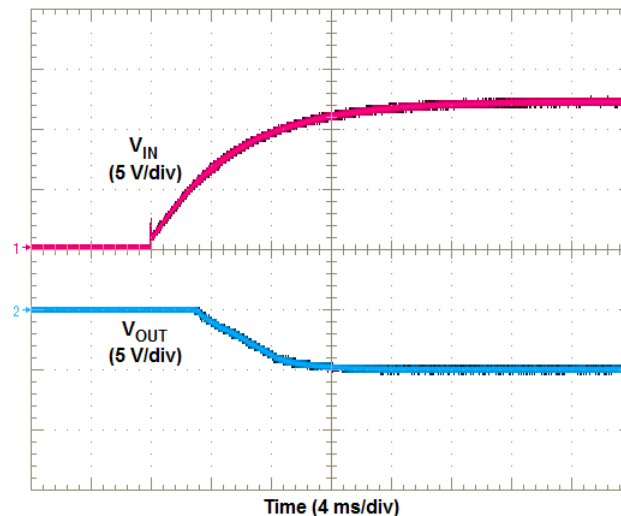


Figure 37. Start-Up Sequence

12.7 Light-Load Behavior

The TPS84259 is a non-synchronous converter. One of the characteristics of non-synchronous operation is that as the output load current decreases, a point is reached where the energy delivered by a single switching pulse is more than the load can absorb. This energy causes the output voltage to rise slightly. This rise in output voltage is sensed by the feedback loop and the device responds by skipping one or more switching cycles until the output voltage falls back to the set point. At very light loads or no load, many switching cycles are skipped. The observed effect during this pulse skipping mode of operation is an increase in the peak to peak ripple voltage, and a decrease in the ripple frequency. The amount of load current when pulse skipping begins is a function of the input voltage, the output voltage, and the switching frequency.

12.8 No-Load Operation

When operating at no load or very light load and the input voltage is removed, the output voltage discharges very slowly. If the input voltage is re-applied before the output voltage discharges, the slow-start circuit does not activate and the amount of inrush current is extremely large and may cause an over-current condition. To avoid this condition the output voltage must be allowed to discharge before re-applying the input voltage. Applying a 50-mA to 100-mA minimum load helps discharge the output voltage. Additionally, monitoring the input voltage with a supervisor and shutting-down using the INH control (see [Output On/Off Inhibit \(INH\)](#)) activates the internal slow-start circuit.

12.9 Switching Frequency

The recommended switching frequency of the TPS84259 is 800 kHz. To operate at the recommended switching frequency, connect the RT pin (Pin 30) to A_VOUT (at pin 32).

It is recommended to adjust the switching frequency in applications with both, higher input voltage (> 18V) and lower output voltage (< -8V). For these applications, improved operating performance can be obtained by decreasing the operating frequency to 500 kHz by adding a resistor, R_{RT} of 93.1 k Ω between the RT pin and A_VOUT as shown in Figure 38. Figure 39 shows the recommended switching frequency over input voltage and output voltage.

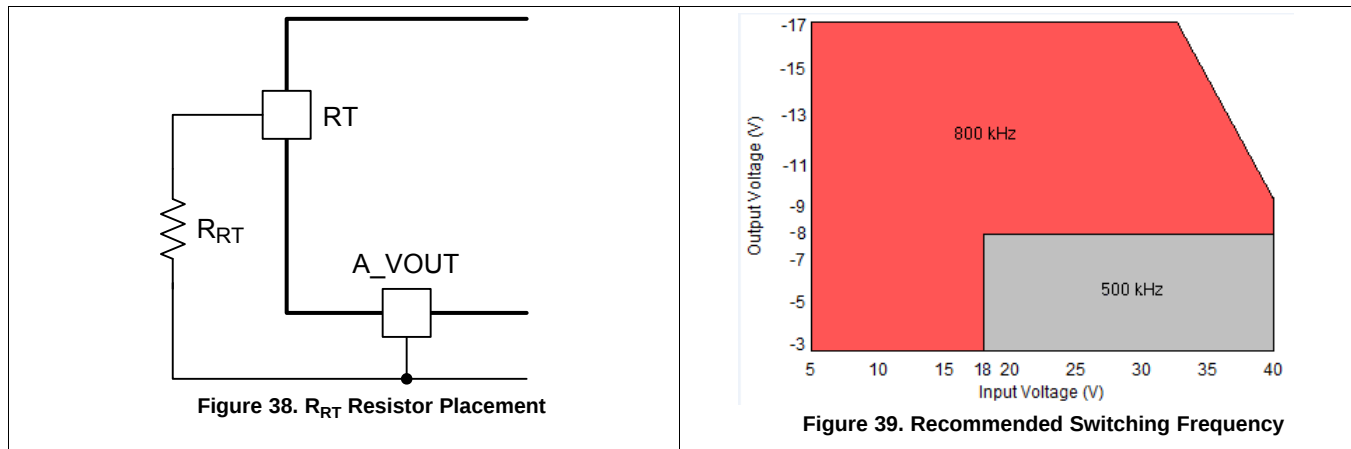


Table 7. Standard Resistor Values For Setting Switching Frequency

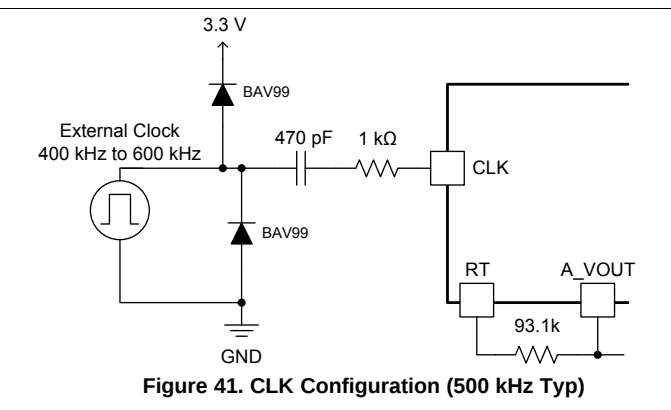
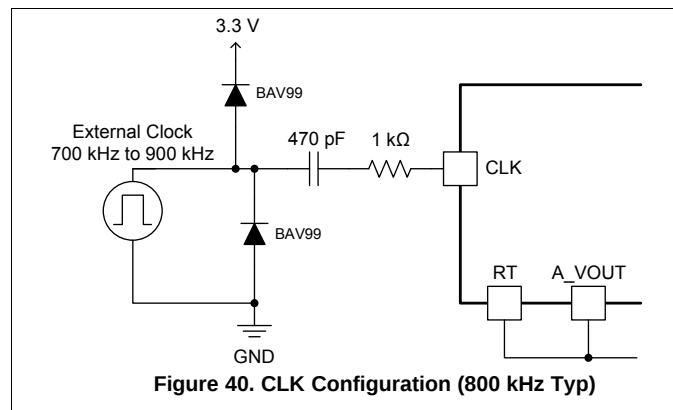
f_{sw} (kHz)	500	800
R_{RT} (k Ω)	93.1	0 (short)

12.10 Synchronization (CLK)

An internal phase locked loop (PLL) allows synchronization from 700 kHz to 900 kHz for 800 kHz applications, or 400 kHz to 600 kHz for 500 kHz applications. See Figure 39 to determine switching frequency based on input voltage and output voltage. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 25% to 75%. The clock signal amplitude must transition lower than 0.5 V and higher than 2.2 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications requiring CLK mode, configure the device as shown in Figure 40 (800 kHz) and Figure 41 (500kHz).

Before the external clock is present, the device works in RT mode where the switching frequency is set by the R_{RT} resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.2 V), the device switches from RT mode to CLK mode and the CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the RT resistor.

Synchronization (CLK) (continued)



12.11 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, an external level-shifter is required to interface with the pin because in a positive-to-negative buck-boost supply, the INH pin is referenced to VOUT, not GND. Adding a level-shifter (U1) as shown in Figure 42, allows the INH control to be referenced to GND. A recommended level-shifter part # is DCX144EH-7 from Diodes Inc.

Pulling the input of U1 to GND applies a low voltage to the inhibit control pin and disables the output of the supply, shown in . Releasing the input of U1 enables the device, which executes a soft-start power-up sequence, as shown in Figure 44. The device produces a regulated output vFigure 43oltage within 10 ms. The waveforms were measured with a 1.5-A constant current load.

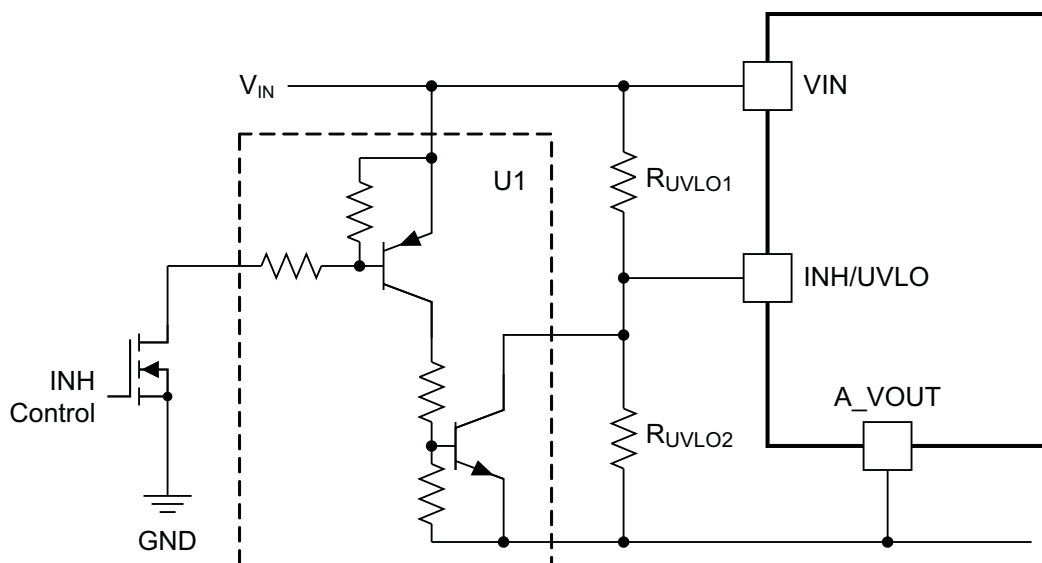


Figure 42. Typical Inhibit Control

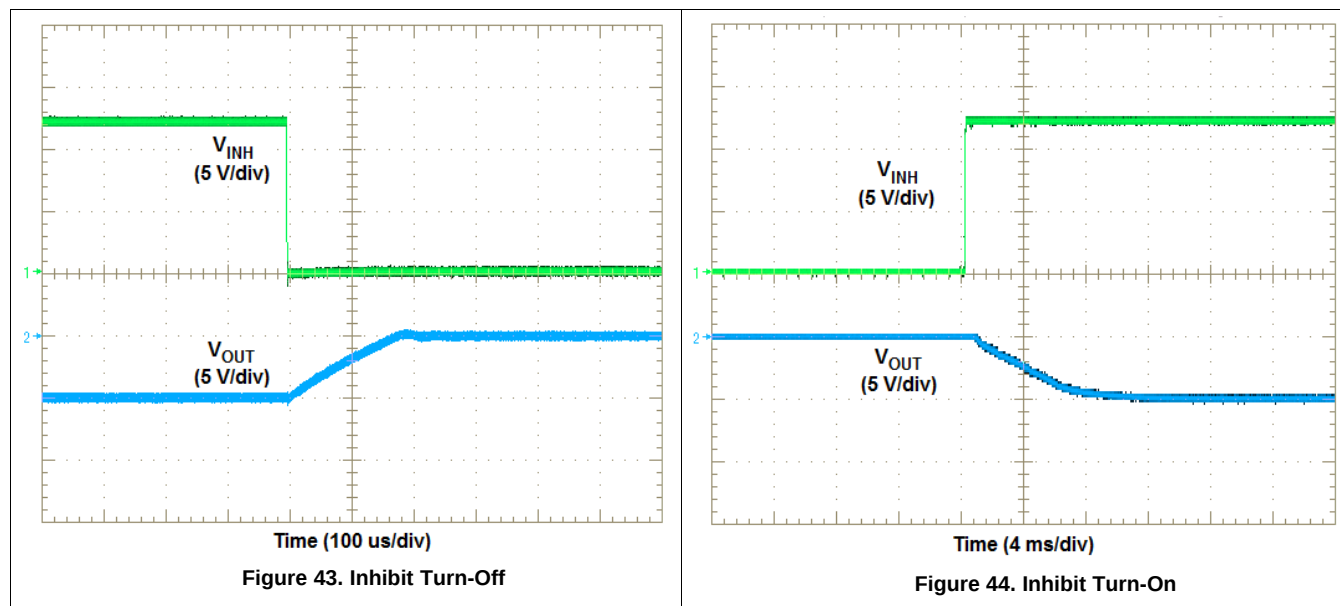


Figure 43. Inhibit Turn-Off

Figure 44. Inhibit Turn-On

12.12 Slow-Start Circuit (SS)

Connecting the STSEL pin (Pin 29) to A_VOUT while leaving SS pin (Pin 28) open, enables the internal SS capacitor with a slow-start interval of approximately 10 ms. Adding additional capacitance between the SS pin and A_VOUT increases the slow-start time. [Figure 45](#) shows an additional SS capacitor connected to the SS pin and the STSEL pin connected to A_VOUT. See [Table 8](#) below for SS capacitor values and timing interval.

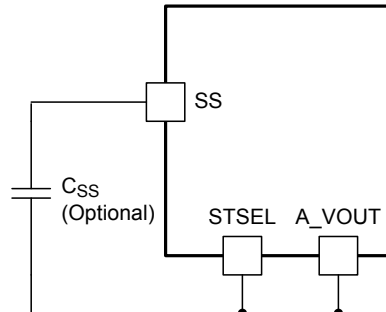


Figure 45. Slow-Start Capacitor (C_{SS}) and STSEL Connection

Table 8. Slow-Start Capacitor Values and Slow-Start Time

C_{SS} (nF)	Open	10	15	22
SS Time (ms)	10	15	17	20

12.13 Inrush Current

During turn-on, as the TPS84259 performs a slow-start sequence, an inrush current is induced as the output capacitors charge up. The inrush current is in addition to the DC input current. The amount of inrush current depends on the input voltage, output voltage and amount of output capacitance. [Table 9](#) shows the typical inrush current for the input voltage, output voltage and the amount of output capacitance. Increasing the slow-start capacitor reduces the inrush current by slowing down the ramp of the output voltage. See [Slow-Start Circuit \(SS\)](#).

Table 9. Typical Inrush Current

Output Capacitance →		100 μ F Ceramic	200 μ F ⁽¹⁾	320 μ F ⁽¹⁾	430 μ F ⁽¹⁾
VIN (V)	VOUT (V)	Inrush Current (A)			
5	–3.3	0.1	0.1	0.1	0.1
	–5	0.1	0.2	0.2	0.3
	–12	0.3	0.8	1.2	1.8
	–15	0.4	1.3	2.5	3.6
12	–3.3	0.1	0.1	0.1	0.1
	–5	0.1	0.1	0.1	0.2
	–12	0.2	0.4	0.6	0.8
	–15	0.3	0.5	0.9	1.3
24	–3.3	0.1	0.1	0.1	0.1
	–5	0.1	0.1	0.2	0.2
	–12	0.2	0.2	0.3	0.5
	–15	0.3	0.3	0.5	0.7
36	–3.3	0.2	0.2	0.2	0.2
	–5	0.2	0.2	0.2	0.2
	–12	0.2	0.3	0.4	0.4

(1) This amount of capacitance includes the required 100 μ F of ceramic capacitance with additional bulk capacitance.

12.14 Input to Output Coupling Capacitor

Adding an input to output coupling capacitor (C_{IO}) across V_{IN} to V_{OUT} as shown in Figure 46 can help reduce output voltage ripple and improve transient response. A typical value for C_{IO} is 2.2 μF ceramic with a voltage rating greater than the sum of $V_{IN} + |V_{OUT}|$.

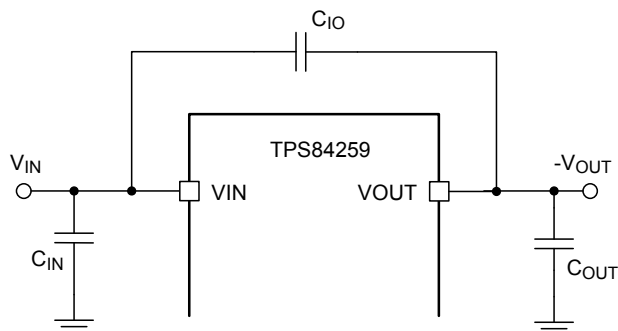


Figure 46. Input to Output Coupling Capacitor

12.15 Overcurrent Protection

For protection against load faults, the TPS84259 incorporates cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced. If the output voltage drops more than 25%, the switching frequency is lowered to reduce power dissipation within the device. When the overcurrent condition is removed, the output voltage returns to the established voltage.

The TPS84259 is not designed to endure a sustained short circuit condition. The use of an output fuse, voltage supervisor circuit, or other overcurrent protection circuit is recommended.

12.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 180°C typically. The device reinitiates the power up sequence when the junction temperature drops below 165°C typically.

12.17 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 47 through Figure 50 show a typical four layer PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated A_VOUT copper area beneath the TPS84259.
- Isolate the PH copper area from the GND copper area using the VOUT copper area.
- Connect the VOUT and A_VOUT copper areas at one point; at pins 8 & 9.
- Place R_{SET} , R_{RT} , and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.
- Use a dedicated sense line to connect R_{SET} to GND near the load for best regulation.

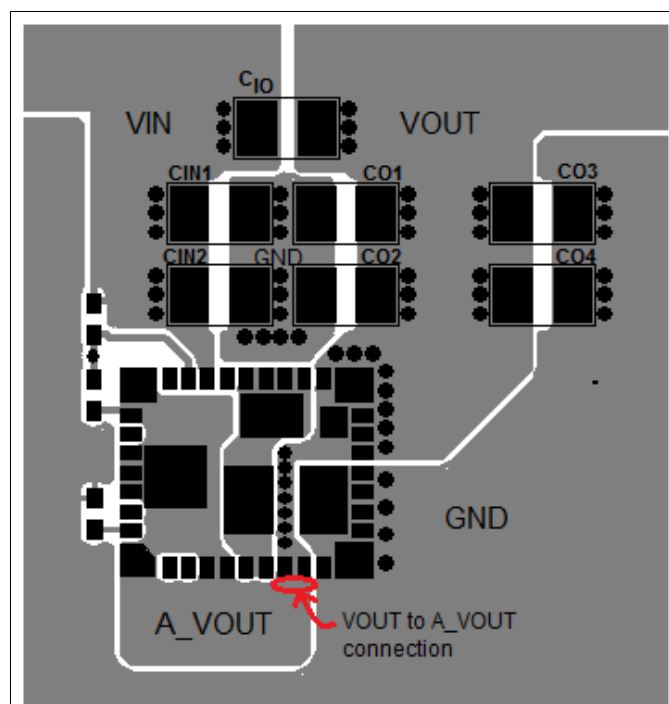


Figure 47. Typical Top-Layer Recommended Layout

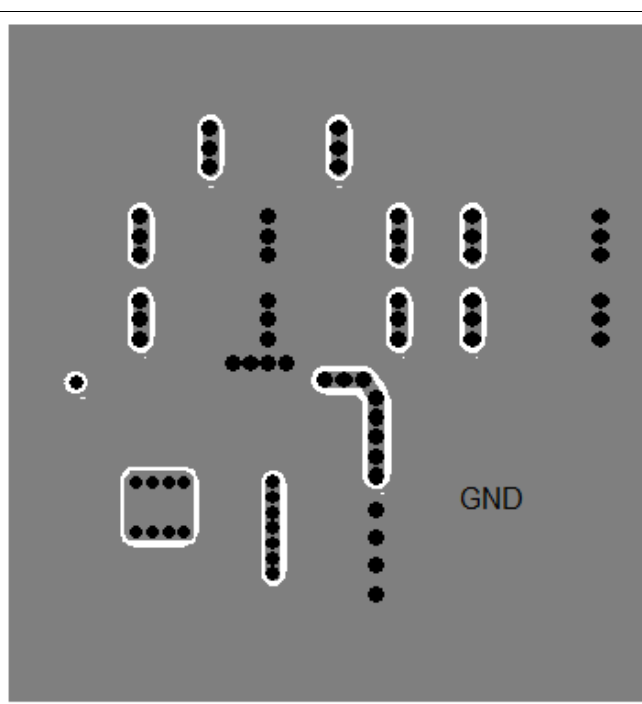


Figure 48. Typical GND-Layer Recommended Layout

Layout Considerations (continued)

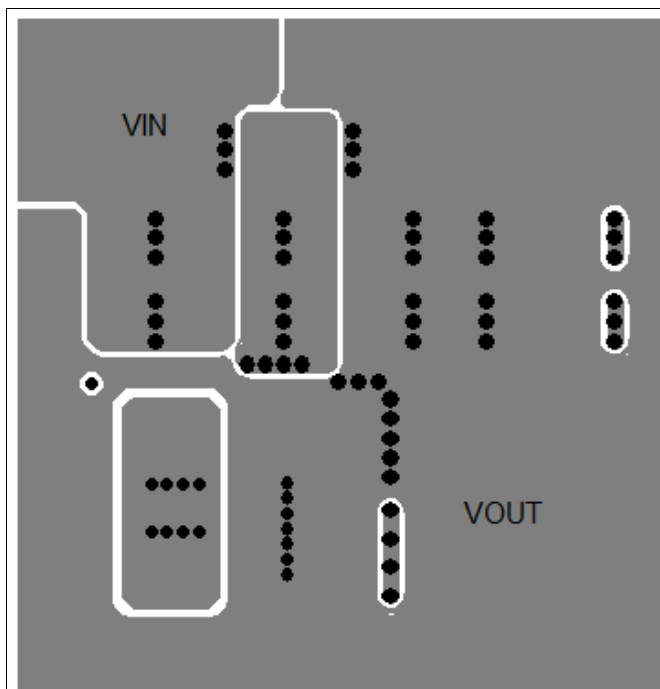


Figure 49. Typical VOUT-Layer Recommended Layout

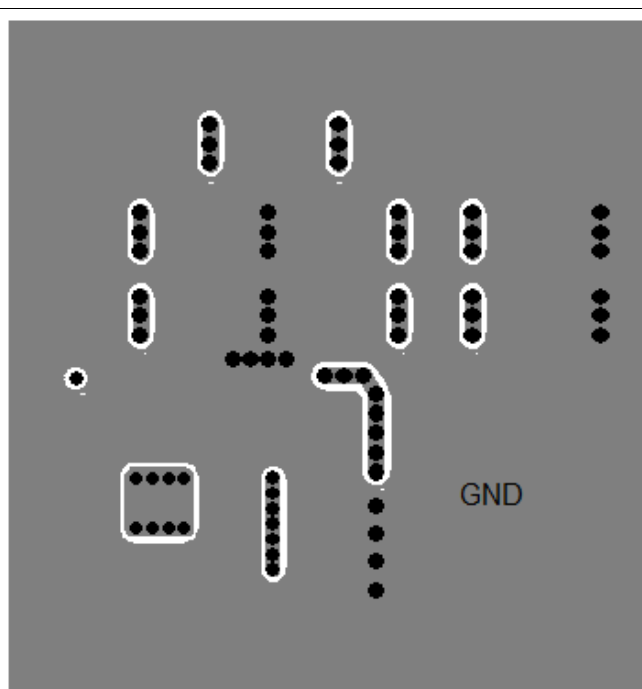


Figure 50. Typical Bottom-Layer Recommended Layout

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2017) to Revision D	Page
- 已添加 TI 参考设计顶部导航图标 1 - Increased the peak reflow temperature and maximum number of reflows to JEDEC specification for improved manufacturability. 2	
Changes from Revision B (September 2013) to Revision C	Page
Added peak reflow and maximum number of reflows information 2	
Changes from Revision A (June 2013) to Revision B	Page
Changed incorrect R_{SET} value for $-5.5 V_{OUT}$ in Table 5. 15	
Changes from Original (August 2012) to Revision A	Page
- Changed describing pins 8 & 9 not connected together internally. 6 - Added multiple layout layers to the recommended layout. 24	

14 器件和文档支持

14.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

14.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

14.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

14.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

14.5 术语表

[SLYZ022](#) — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS84259RKGR	Active	Production	B1QFN (RKG) 41	500 LARGE T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84259)
TPS84259RKGR.A	Active	Production	B1QFN (RKG) 41	500 LARGE T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84259)
TPS84259RKGRG4	Active	Production	B1QFN (RKG) 41	500 LARGE T&R	No	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84259
TPS84259RKGRG4.A	Active	Production	B1QFN (RKG) 41	500 LARGE T&R	No	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84259
TPS84259RKGRG4.B	Active	Production	B1QFN (RKG) 41	500 LARGE T&R	No	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84259
TPS84259RKGT	Active	Production	B1QFN (RKG) 41	250 SMALL T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84259)
TPS84259RKGT.A	Active	Production	B1QFN (RKG) 41	250 SMALL T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84259)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84259RKGR	B1QFN	RKG	41	500	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
TPS84259RKGRG4	B1QFN	RKG	41	500	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
TPS84259RKGT	B1QFN	RKG	41	250	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



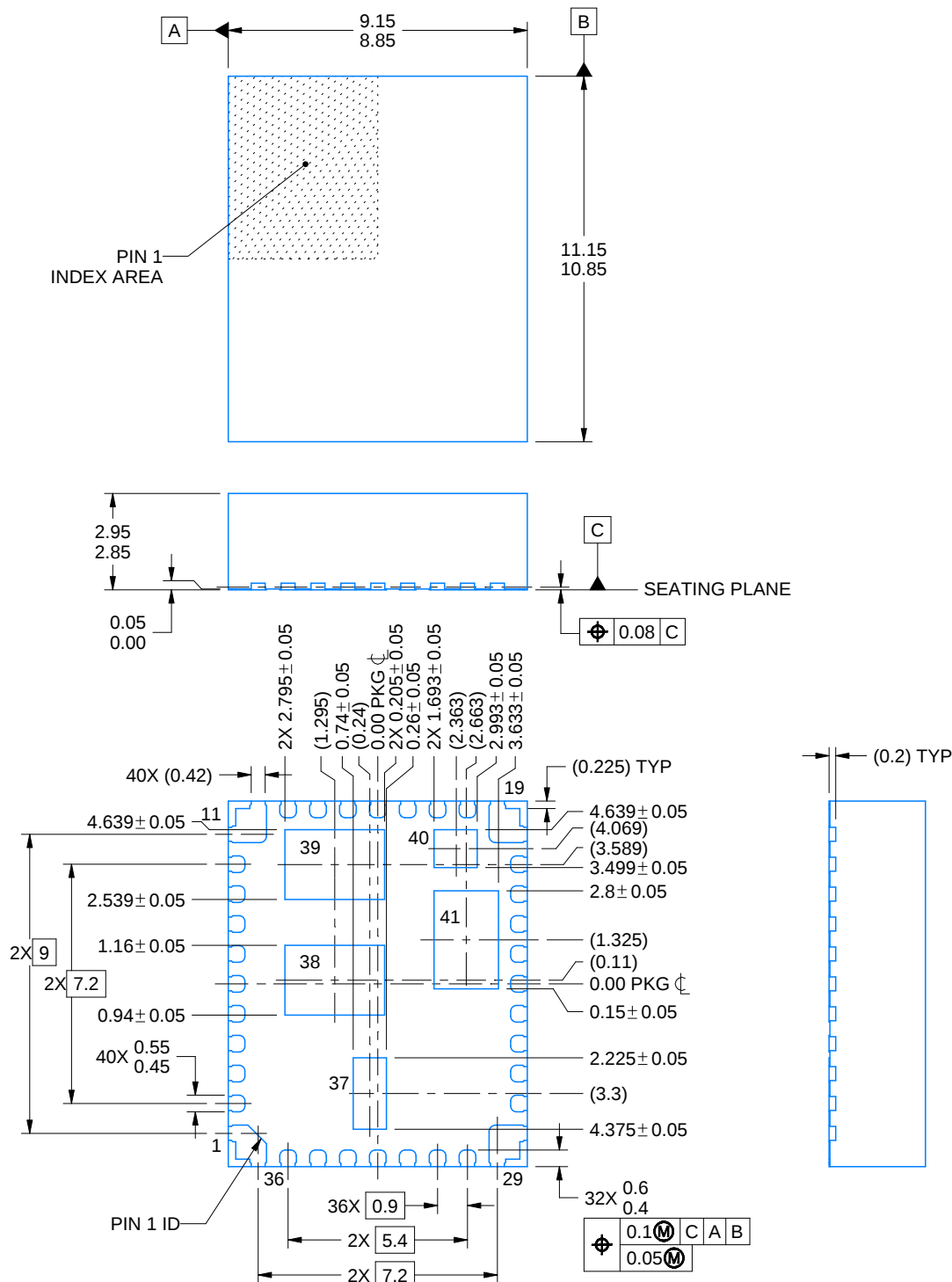
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84259RKGR	B1QFN	RKG	41	500	383.0	353.0	58.0
TPS84259RKGRG4	B1QFN	RKG	41	500	383.0	353.0	58.0
TPS84259RKGT	B1QFN	RKG	41	250	383.0	353.0	58.0



B1QFN - 2.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES:

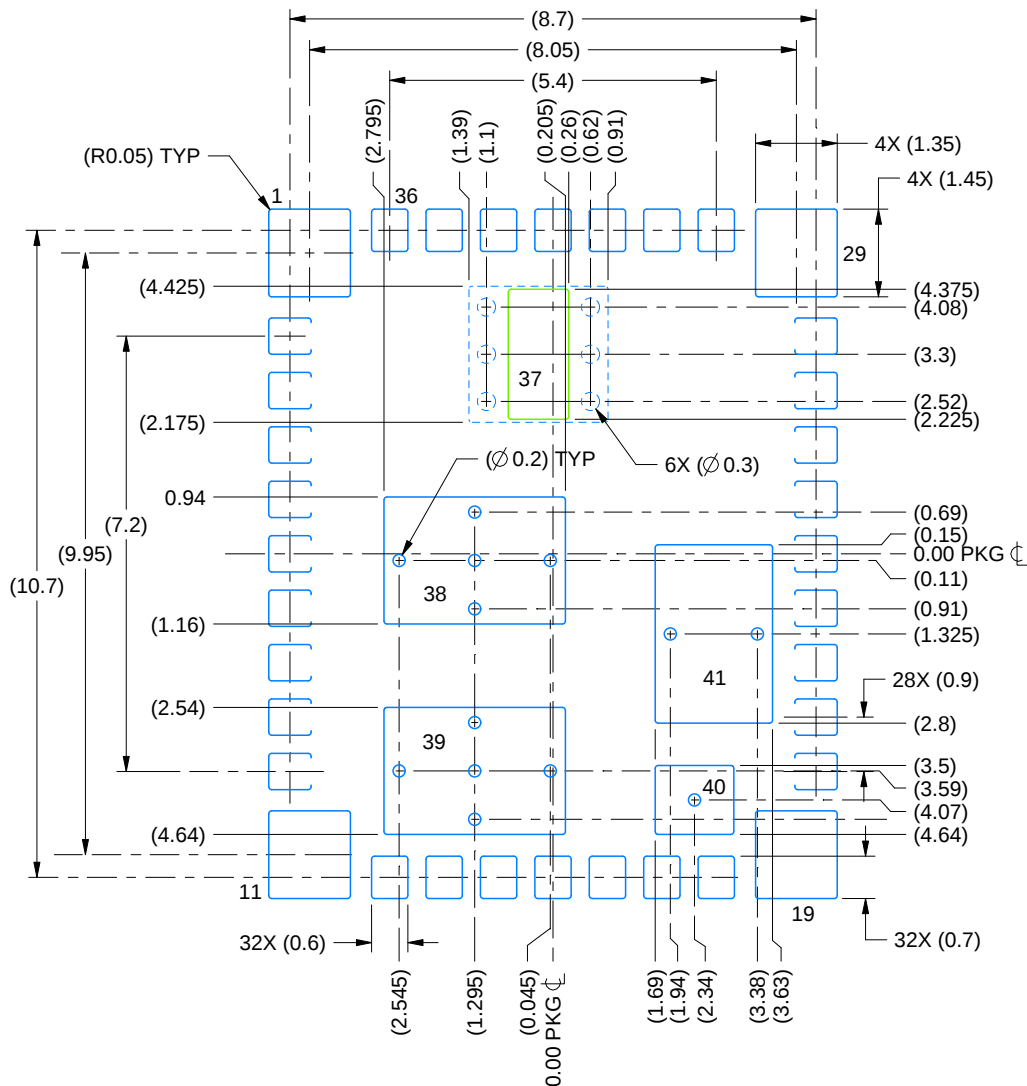
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

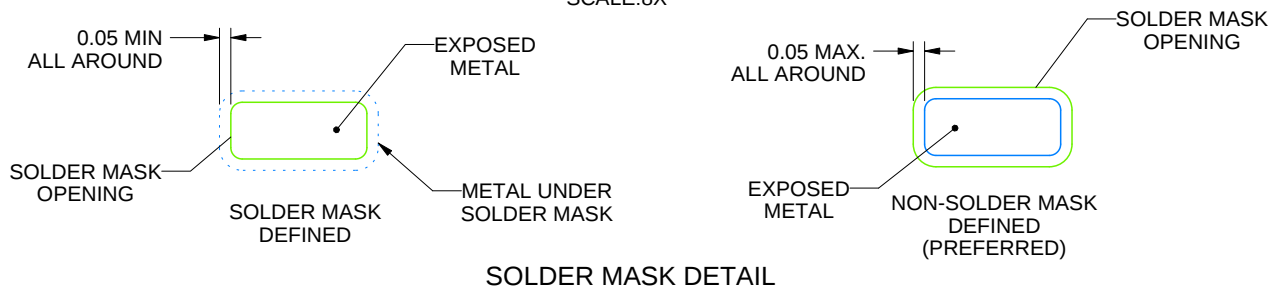
RKG0041A

B1QFN - 2.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



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NOTES: (continued)

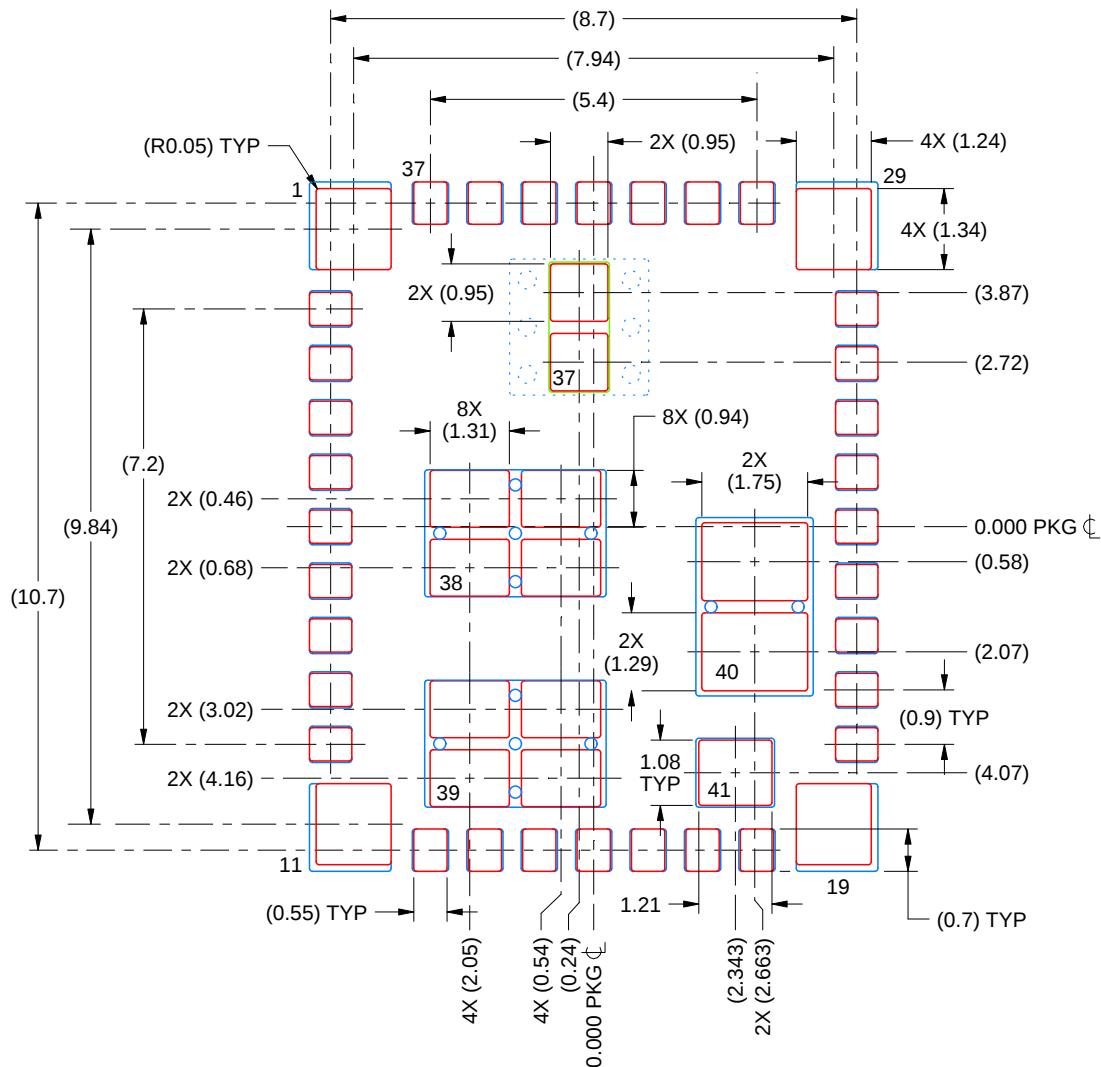
4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RKG0041A

B1QFN - 2.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm STENCIL THICKNESS

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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