具有 I²C 一次性可编程 (OTP) ROM 电流调整的两灯串发光二级管 (LED)

查询样品: TPS92660

特性

- 输入电压：高达 **80V**
- 两输出 **LED** 电流控制器
- 通过带有 **I²C** 接口的一次性可编程 **(OTP) ROM** 来调整 **LED** 电流
- 针对每个 **LED** 灯串脉宽调制 **(PWM)** 调光的可调 **SADJ** 和 **LADJ** 引脚
- 输入欠压闭锁和输出过压保护
- 使能接通/关闭
- 精确的 **3.0V** 基准电压
- 效率大于 **95%**
- 热关断保护
- **20** 引脚薄型小尺寸 **(TSSOP)** 外露垫封装

应用范围

- 专业照明
- 工业用和商用照明
- 通用照明

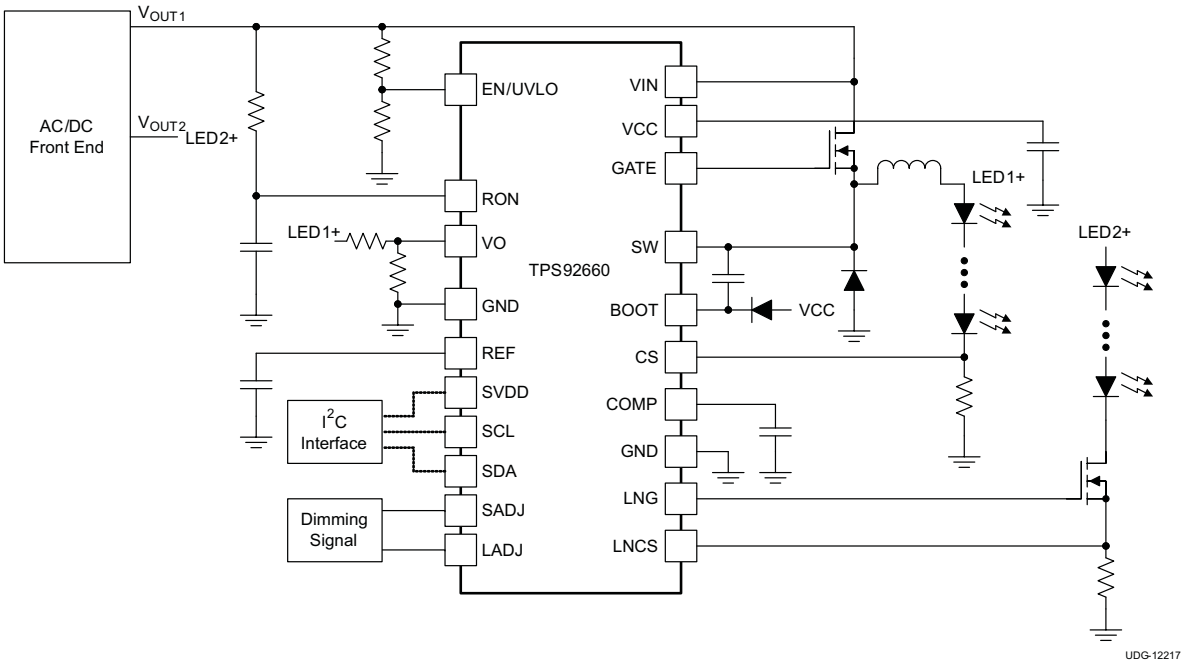
说明

TPS92660 是一款双输出 LED 驱动器，此驱动器具有用于 LED 电流调整的一次性可编程 (OTP) ROM 和 I²C 接口。 此电流调整为 LED 灯具制造商提供了一个生产 LED 照明灯具的方法，这个方法可在不对 LED 灯进行颜色分级的情况下保持恒定的流明输出。

此器件的一个输出是非同步降压控制器，此控制器被用来调节较高功率白光 LED 的电流。 此器件的另外一个输出是线性稳压器控制器，此控制器被用来调节较低功率红光 LED 的电流。 通过将白光 LED 与红光 LED 混用，TPS92660 被用于受控 CCT（相关色温）LED 灯应用。

此器件采用 20 引脚，TSSOP 外露垫封装。

典型应用



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1) (2)

T_J	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY
–40°C to 125°C	TSSOP exposed pad	TPS92660PWP	20	Tube	73
		TPS92660PWPR		Tape and Reel	2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	VCC	–0.3	14	V
Input voltage range(2)	VIN, UVLO/EN	–0.3	80	
	BOOT to SW	–0.3	14	
	SADJ, LADJ, RON, VO, COMP, CS, LNCS	–0.3	6	
	SW	–2.0	80	
	BOOT	–0.3	90	
	SVDD, SCL, SDA	–0.3	5.5	
Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2000	V
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		750	
Junction temperature range, T_J (3)			165	°C
Storage temperature range, T_{stg}		–55	150	
Lead temperature range, soldering, 10 s			260	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Maximum junction temperature is internally limited

THERMAL INFORMATION

THERMAL METRIC(1)		TPS92660 TSSOP exposed pad (PWP) 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	36.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	22.7	
θ_{JB}	Junction-to-board thermal resistance(4)	18.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	18.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.9	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VIN}	Input Voltage	8.6	80	V
V_{SVDD}	I^2C VDD	2.7	5.5	V
V_{VO}	Output voltage sense for control and protection	0	2.5	V
$V_{UVLO/EN}$	Enable/Under Voltage lock-out	0	5.5	V
V_{SADJ}	Switching regulator analog or PWM LED current adjust	0	5.5	V
V_{LADJ}	Linear regulator analog or PWM LED current adjust	0	5.5	V
V_{RON}	Resistor and capacitor sets switching frequency of device	0	5.5	V
T_J	Operating junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified V_{IN} = 48 V, –40°C <T_A = T_J< 125°C .

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} REGULATOR (VCC)						
V_{CC}	V_{CC} Voltage		7.75	8.2	8.55	V
I_{VCC}	V_{CC} current limit	V_{CC} = 0	14	20	27	mA
V_{CCUVLO}	Rising threshold			6.4		V
	Falling threshold			6.1		
I_Q	Quiescent current	V_{IN} = 80 V		2.2		mA
UVLO/DEVICE ENABLE (EN/UV)						
V_{EN}	Device enable voltage threshold	V_{EN} increasing	1.14	1.2	1.26	V
V_{EN_HYS}	Enable input hysteresis			20		mV
I_{EN}	Enable source current	V_{EN} = 0		10		µA
ON/OFF TIMER/OVER VOLTAGE PROTECTION (RON, VO)						
R_{PD_RON}	RON pull-down resistance			60	83	Ω
V_{OV}	VO pin overvoltage threshold		2.4	2.5	2.6	V
V_{OV_HYS}	VO pin overvoltage hysteresis			0.1		V
t_{ON_DLY}	RON pin to GATE delay			58		ns
$t_{OFF(min)}$	Minimum off-time	V_{CS} = 0 V	200	255	340	ns
$t_{ON(min)}$	Minimum on-time		80	120	180	ns
I^2C LOGIC INTERFACE (SCL, SDA) (2.7V ≤ V_{SVDD} ≤ 5.5V)						
V_{IL}	Low-level input voltage				0.2 × V_{SVDD}	V
V_{IH}	High-level input voltage		0.8 × V_{SVDD}			V
I_L	Logic input current		–1	0	1	µA
f_{SCL}	SCL input frequency			100	200	kHz
V_{OL}	Low-level output voltage	I_{SDA} = 3 mA		0.2	0.38	V
I_L	Output leakage current	V_{SDA} = 5 V			1	µA
SWITCHER LED CURRENT SENSE (CS, COMP)						
V_{SW_REF}	Switcher LED current reference voltage	Non-programmed	196	202	209	mV
Δ V_{SW_REF}	Switcher LED current reference voltage adjust range			±40 –40		mV
I_{CS}	CS bias current				1	µA
g_M	CS amplifier transconductance			600		µA/V
V_{CS_COMP}	CS to COMP offset voltage			1.8		V
I_{COMP}	COMP source current			75		µA
	COMP sink current			75		µA
HIGH SIDE SWITCH CURRENT LIMIT (VIN, SW)						
V_{SW_LIM}	High side switch current limit (referenced from VIN)		232	275	329	mV
t_{LIM_OFF}	Current limit OFF time			280		µS
t_{LEB}	Switch current sense leading edge blank time			200		nS

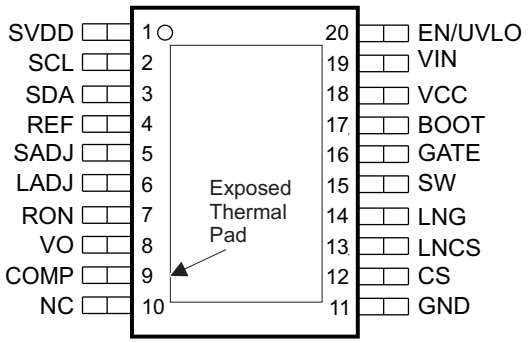
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified V_{IN} = 48 V, –40°C <T_A = T_J< 125°C .

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR LED CURRENT SENSE (LNCS)						
V_{LN_REF}	Linear LED current reference voltage	Non-programmed	190	200	209	mV
ΔV_{LN_REF}	LinearLED current reference voltage adjust range			+44 –50		mV
I_{LNCS}	LNCS Input bias current				1	µA
SWITCHING GATE DRIVER (GATE, BOOT, SW)						
R_{SRC_GATE}	Gate sourcing resistance	GATE = High		2		Ω
R_{SNK_GATE}	Gate sinking resistance	GATE = Low		2		Ω
V_{BOOT}	BOOT UVLO threshold	BOOT-SW rising	4.2	5.6	7.0	V
V_{BOOT_HYS}	BOOT UVLO threshold			750		mV
I_{SW_PD}	SW node pull down current			60		mA
LINEAR GATE DRIVER (LNG)						
V_{LNG_MAX}	LNG Maximum output voltage			6.3		V
V_{LNG_MIN}	LNG Minimum output voltage			1.4		V
I_{LNG_MAX}	LNG Maximum output current				5.5	mA
ANALOG/PWM DIMMING (SADJ, LADJ)						
f_{DIM}	Internal PWM dimming frequency			500		Hz
V_{tri}	SADJ triangle voltage for analog input	High		2.5		V
		Low		0.1		
	LADJ triangle voltage for analog input	High		2.5		V
		Low		0.1		
t_{TIMER}	SADJ Pulse detect timer			10		ms
	LADJ Pulse detect timer			10		
V_{ADJ}	SADJ PWM input threshold			2.7		V
	LADJ PWM input threshold			2.7		
V_{ADJ_HYS}	SADJ PWM input hysteresis			500		mV
	LADJ PWM input hysteresis			500		
I_{ADJ_PU}	SADJ Pull up current			5		µA
	LADJ Pull up current			5		
t_{SADJ}	SADJ to GATE delay	Rising		1.2		µs
		Falling		1.2		
t_{LADJ}	LADJ to LNG delay	Rising		1.2		µs
		Falling		1.2		
REFERENCE VOLTAGE (REF)						
V_{REF}	Voltage reference		2.92	3	3.08	V
I_{REF}	VREF maximum source current		1.6			mA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			25		°C

DEVICE INFORMATION

TSSOP PACKAGE
20-PINS
(TOP VIEW)



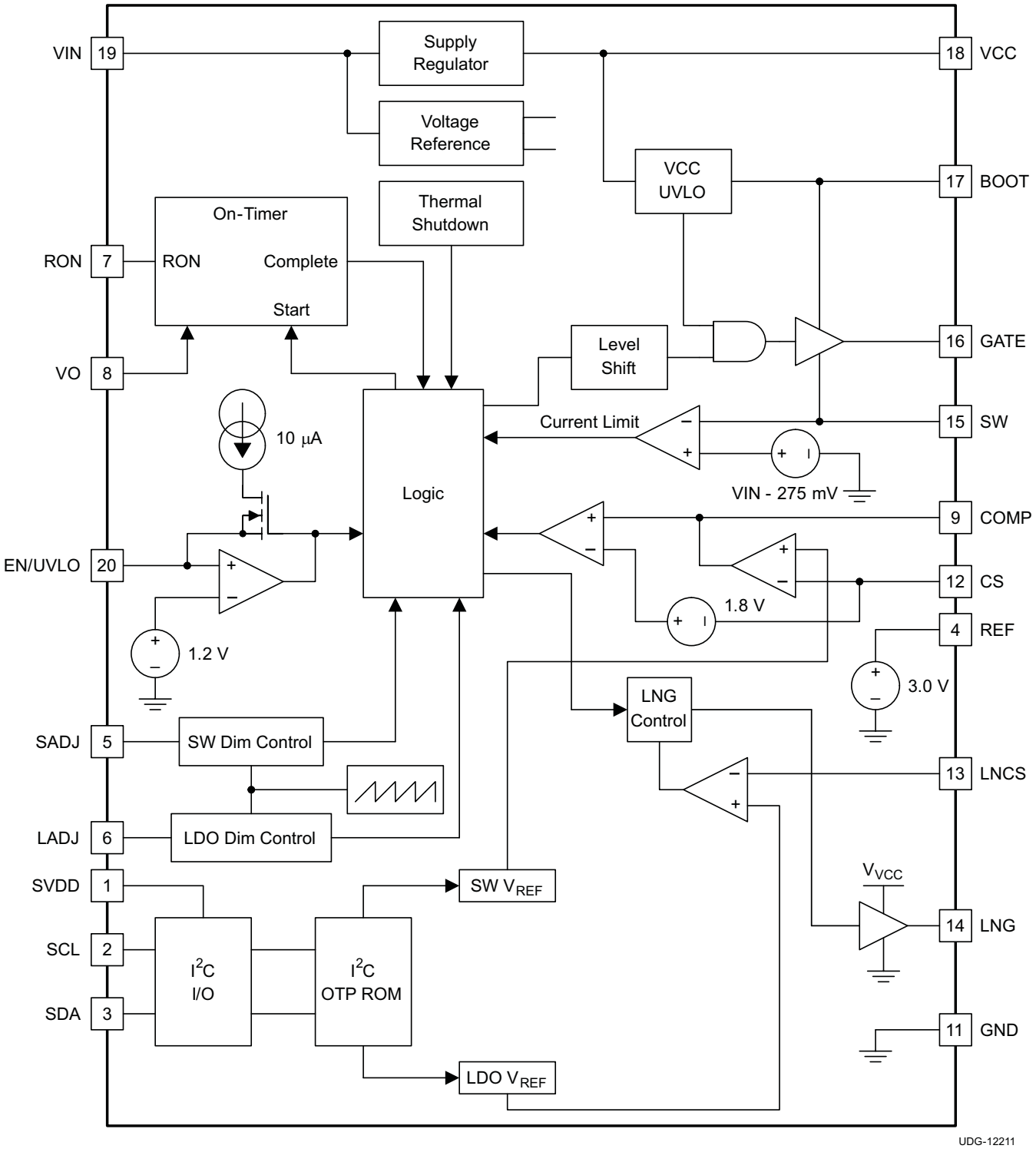
NC – No internal connection

PIN FUNCTIONS(1)

NAME	NO.	I/O	DESCRIPTION
SVDD	1	P	I^2C VDD input.
SCL	2	I	I^2C clock input.
SDA	3	I/O	I^2C data input/output.
REF	4	O	3.0V output reference.
SADJ	5	I	Switching regulator dimming input.
LADJ	6	I	Linear regulator dimming input.
RON	7	I	Connect to resistor and capacitor which sets the switching frequency of the switching regulator.
VO	8	I	Output voltage sense for control and protection.
COMP	9	O	Switching regulator error amplifier (EA) compensation connection.
NC	10	-	No internal connection.
GND	11	G	System ground connection.
CS	12	I	Switching regulator LED Current sense input.
LNCS	13	I	Linear regulator current sense input.
LNG	14	O	Linear FET gate driver output.
SW	15	I	Connect to the switch node of the switching regulator.
GATE	16	O	Switching controller high-side N-channel FET driver output.
BOOT	17	I	MOSFET drive bootstrap pin.
VCC	18	O	Output of internal regulator. Bypass it with 1µFminimum ceramic capacitor to GND.
VIN	19	P	Input voltage supply for device. Maximum of 80V operating voltage.
EN/UVLO	20	I	This pin is a multi function input. Enable of device, Under-voltage lock-out (UVLO).
DAP	-	-	Exposed thermal pad. Connected to the system ground. Place vias on DAP.

(1) I=Input, O=Output, P=Power, G=Ground

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤+125°C, V_{IN} = 48 V, R_T= 51.1 kΩ, C_T = 1000 pF, C_{VCC} = 1 µF, C_{COMP} = 1 µF

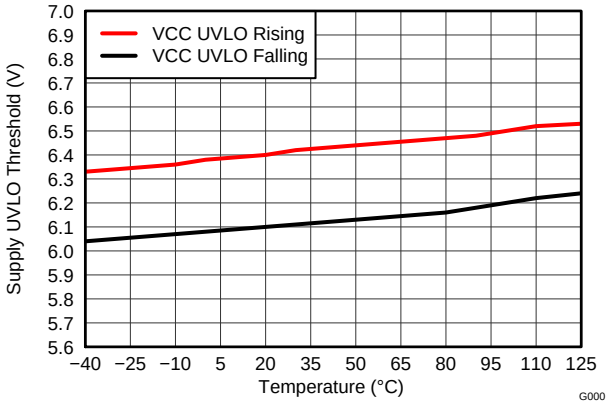


Figure 1. Supply Voltage (VCC) UVLO Threshold vs Junction Temperature

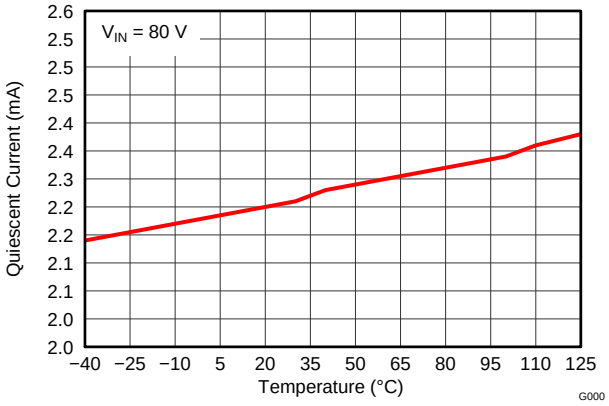


Figure 2. Quiescent Current vs Junction Temperature

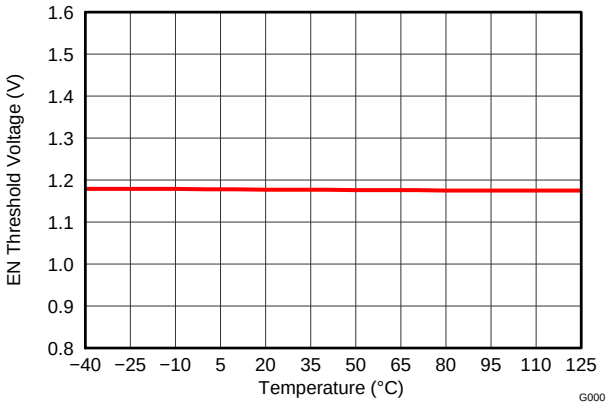


Figure 3. Enable Threshold Voltage vs Junction Temperature

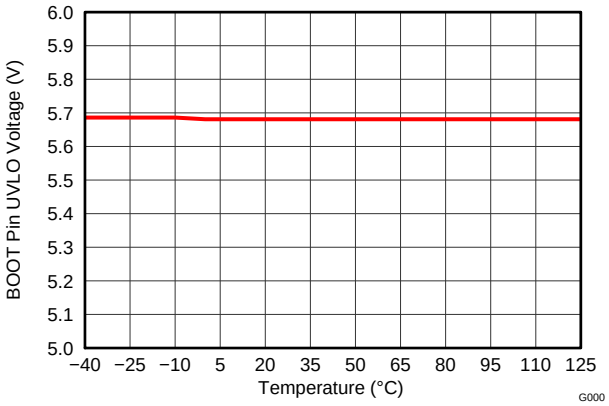


Figure 4. Boot UVLO Threshold vs Junction Temperature

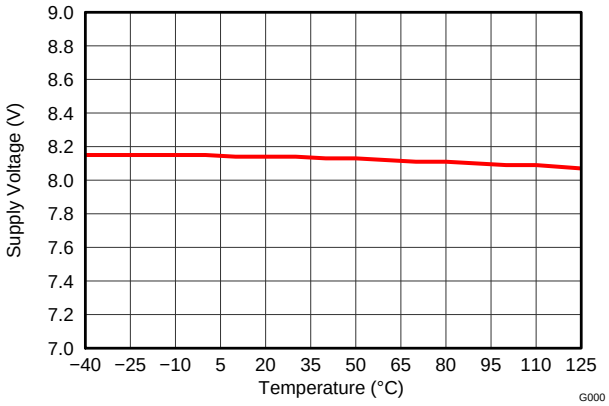


Figure 5. Supply Voltage (VCC) vs Junction Temperature

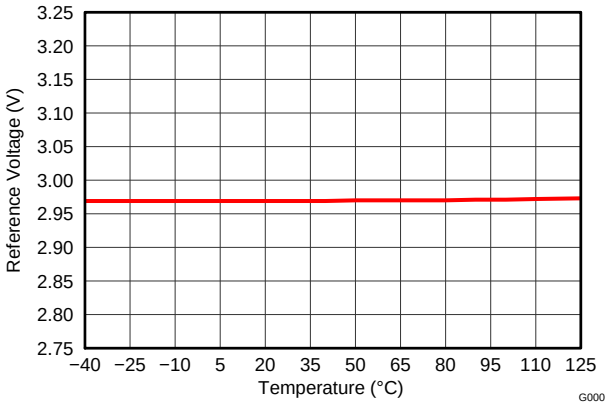


Figure 6. Voltage Reference vs Junction Temperature

TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤+125°C, V_{IN} = 48 V, R_T= 51.1 kΩ, C_T = 1000 pF, C_{VCC} = 1 µF, C_{COMP} = 1 µF

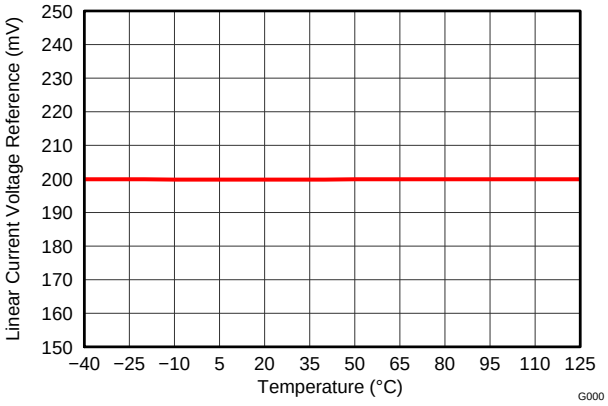


Figure 7. Linear Current Voltage Regulation vs Junction Temperature

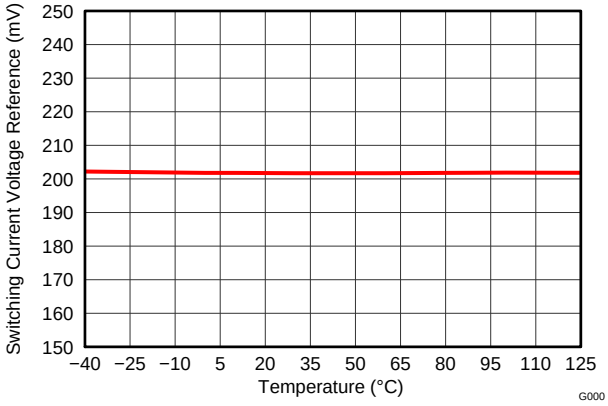


Figure 8. Switching Current Voltage Regulation vs Junction Temperature

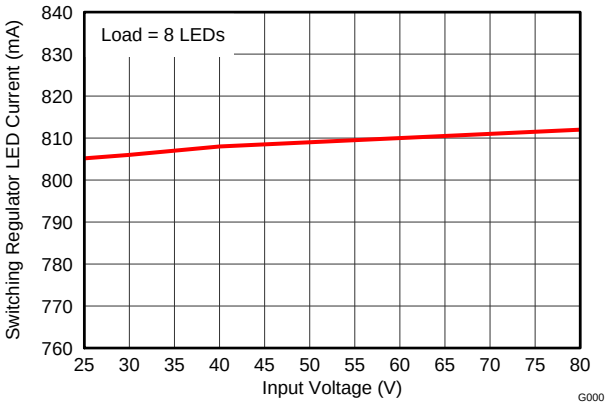


Figure 9. Switching Regulator LED Current vs Input Voltage

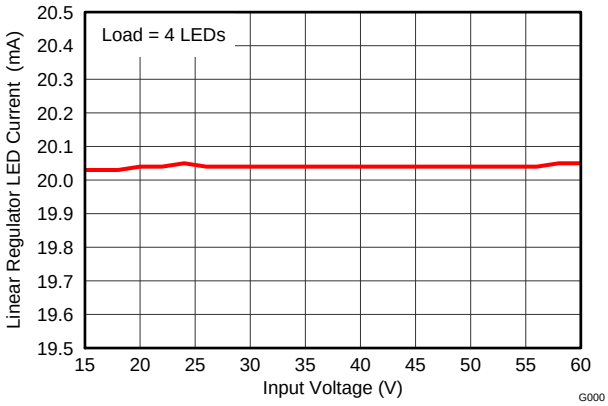


Figure 10. Linear Regulator LED Current vs Input Voltage

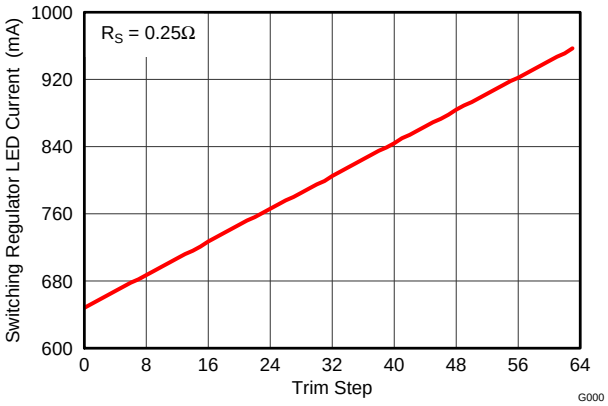


Figure 11. Switching Regulator LED Current vs I²C Trim Step

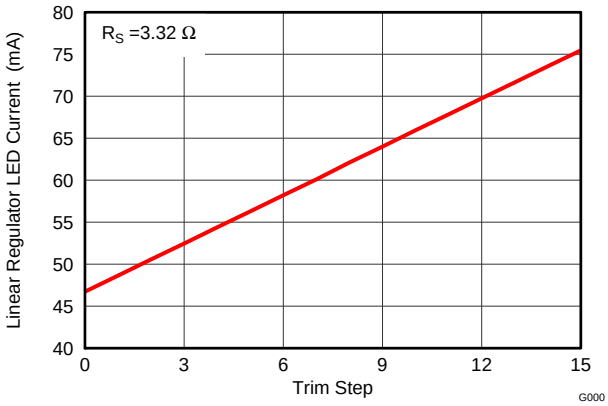


Figure 12. Linear Regulator LED Current vs I²C Trim Step

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, –40°C ≤ T_A = T_J ≤+125°C, V_{IN} = 48 V, R_T= 51.1 kΩ, C_T = 1000 pF, C_{VCC} = 1 µF, C_{COMP} = 1 µF

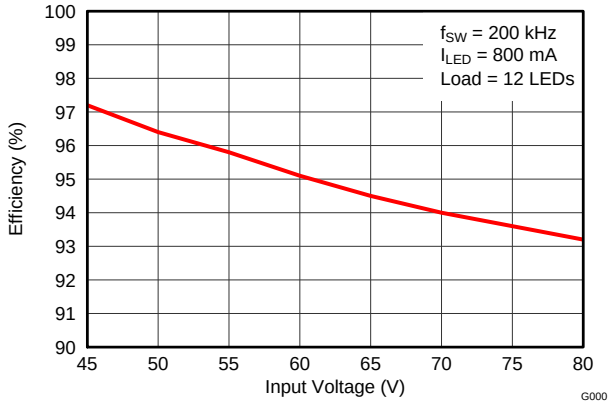


Figure 13. Switching Regulator Efficiency vs Input Voltage

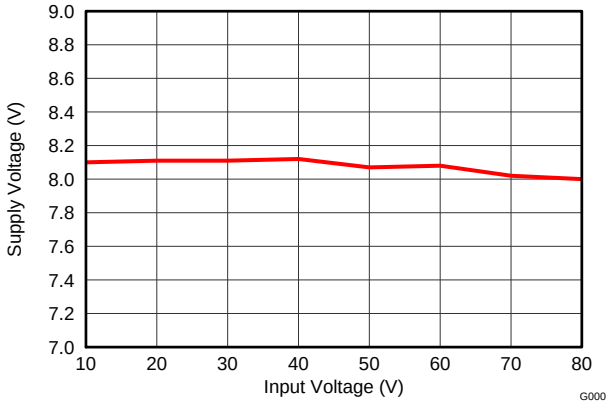


Figure 14. VCC vs Input Voltage

APPLICATION INFORMATION

Theory of Operation

The TPS92660 is a dual-channel LED current controller. It has a high-voltage, non-synchronous buck controller capable of driving an N-channel high-side MOSFET and a linear controller capable of driving an N-channel low-side MOSFET. The buck controller uses a controlled on-time (COT) control scheme to regulate the LED current. The controlled on-time varies with input and output voltage to produce pseudo-fixed frequency operation.

The TPS92660 buck controller also employs a transconductance error amplifier that regulates average the LED current. When the buck converter operates in continuous conduction mode (CCM) the controlled on-time maintains a relatively constant switching frequency over the change of input and output voltages. The linear controller regulates the LED current by controlling the gate voltage of the N-channel low side MOSFET. This MOSFET is connected in series with the LED string and operates in the linear region when LED current is in regulation. The linear controller senses the LED current and compares it with the internal reference voltage (default 200 mV without OTP trim) to generate the MOSFET gate-drive voltage.

Figure 15 shows a simplified version of the feedback system used to control the current through the LED string connected to the buck converter. The LED current flows through the current sense resistor R_{SNS} and generates the current sense voltage. This voltage is fed to the CS pin. Inside the IC, the current sense voltage is internally integrated and compared to a reference voltage. The error amplifier is a transconductance (g_M) amplifier which sorces/sinks current to/from the comp pin and effectively maintains the voltage at the CS pin to be equal to the voltage V_{SW_REF} (default 202 mV without OTP trim). The comparator turns on the high-side MOSFET of the buck converter when the CS voltage falls below the COMP pin voltage minus 1.8V level shift.

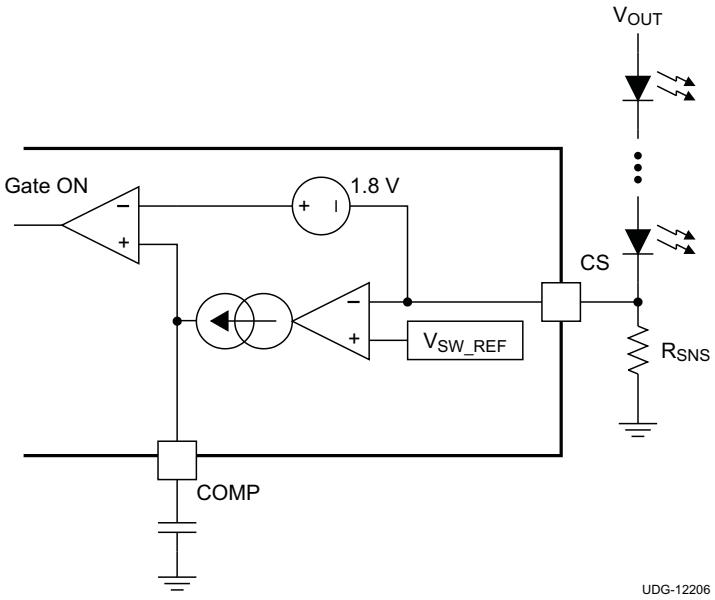


Figure 15. Current Control Circuitry

Figure 16 shows how the MOSFET conducts for a controlled on-time (t_{ON}), set by the external resistor R_T, the external capacitor C_T, the input voltage and the output voltage. At the conclusion of the controlled on-time period, the MOSFET turns off and must remain off for a minimum of 255 ns. Once the minimum off-time period is complete, the comparator compares the CS voltage with the COMP pin voltage again to start the next cycle.

A capacitor with a value of 0.1 µF or higher is recommended between the COMP pin and GND. This compensation capacitor provides a dominant pole in the feedback loop and makes the control loop stable.

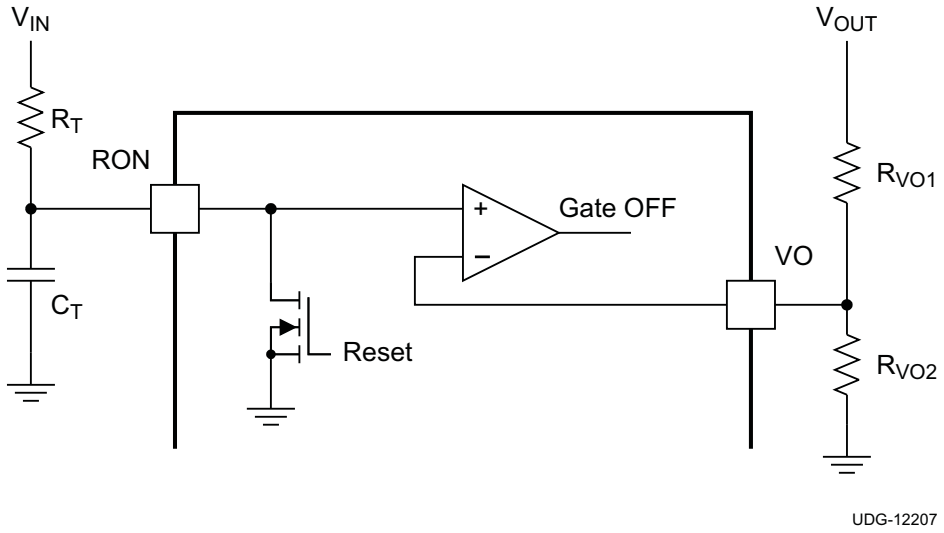


Figure 16. On-Time Circuitry

Switching Frequency

The TPS92660 does not contain a clock, however the on-time is modulated in proportion to both the input voltage and the output voltage in order to maintain a relatively constant switching frequency.

The on-time circuitry is shown in Figure 16. Estimate the switching frequency based on timing resistor R_T, timing capacitor C_T and the resistor divider of R_{VO1} and R_{VO2}. Equation 1 and Equation 2 show how to derive the switching frequency estimation.

$$f_{SW} = \frac{D}{t_{ON}} \quad (1)$$

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

The on-time period ends when the voltage at the capacitor C_T is charged to the voltage on the VO pin. The charging current ratio is shown in Equation 3.

$$I_{CHRG} = \frac{V_{IN}}{R_T}$$

where

- $V_{IN} >> V_{VO}$ (3)

$$t_{ON} = \frac{R_T \times C_T}{V_{IN}} \times \frac{R_{VO2}}{(R_{VO1} + R_{VO2})} \times V_{OUT} \quad (4)$$

Use Equation 3 and Equation 4 to derive Equation 5.

$$f_{SW} = \frac{(R_{VO1} + R_{VO2})}{R_{VO2} \times R_T \times C_T} \quad (5)$$

LED Current Setting

The current sense resistor (R_{SNS}), which is connected between the CS pin and GND, sets the LED current of the switching regulator. The current sense resistor (R_{SNSLN}), which is connected between the LNCS pin and GND, sets the LED current of the linear regulator. The average LED current is calculated using Equation 6 and Equation 7.

Equation 6 shows the calculation for the switching regulator current.

$$I_{LED\_SW} = \frac{V_{SW\_REF}}{R_{SNS}}$$

where

- V_{SW_REF} is the switching regulator reference voltage which is default 202 mV without OTP trim (6)

Equation 7 shows the linear regulator current calculation.

$$I_{LED\_LN} = \frac{V_{LN\_REF}}{R_{SNS\_LN}}$$

where

- V_{LN_REF} is the linear regulator reference voltage which is default 200mV without OTP trim (7)

High Voltage Bias Regulator (VCC)

The TPS92660 contains an internal low dropout linear regulator (LDO), with an 8.2V output, connected between the VIN and the VCC pins. Bypass the VCC pin to the GND pin with a 1µF ceramic capacitor connected close to the pins of the device. VCC tracks VIN until VIN reaches 8.2 V and then regulates at 8.2V as VIN increases. The TPS92660 comes out of UVLO and begins operating when VCC rises above 6.4V. The TPS92660 shuts down when VCC falls below 6.1V. The VCC regulator current limit is 20mA.

Peak Switching Current Limit

The TPS92660 contains a current limit comparator to limit the peak current of the high-side switching MOSFET. When the high-side switching MOSFET turns on, there is a 200ns leading edge blank time. After that if the voltage difference between the VIN pin and the SW pin exceeds 275 mV, the switching MOSFET is turned off for a cool down period of approximately 280µs. In the meanwhile, the COMP pin is pulled low. If the current limit condition persists, this cycle of cool down period and restarting continues, creating a low-power hiccup mode, and minimizes the thermal stress on the switching MOSFET. Equation 8 shows the peak current limit calculation.

$$I_{PEAK} = \frac{275\,mV}{R_{DS(on)}}$$

where

- $R_{DS(on)}$ is the on resistance of the switching MOSFET (8)

Output Open Circuit Protection

The most common failure mode for power LEDs is a broken bond wire, and the result is an open circuit. When this happens the feedback path is disconnected, and the output voltage of the switching regulator begins to rise. The VO pin voltage (which senses the output voltage of the switching regulator through a resistor divider) rises with it. When the VO pin voltage reaches 2.5 V, it triggers the output OV protection and the high-side gate driver turns off. During this time, the COMP pin is also pulled low. There is 0.1 V hysteresis on the OVP. The converter does not resume switching until the voltage on the OV pin falls below 2.4 V.

BOOT Under Voltage Lockout (UVLO)

The TPS92660 has a BOOT UVLO circuit. The switching regulator starts switching once the BOOT-SW voltage rises to 5.6 V. There is 750 mV of hysteresis on the BOOT UVLO. It stops switching when the BOOT-SW voltage falls to 4.85V. Once the BOOT UVLO is triggered, the SW pin is pulled down by an internal MOSFET, such that the boot capacitor can be recharged. The maximum pull-down current is 60mA. When the BOOT-SW voltage is charged above 5.6 V, the pull-down circuit is disabled.

Linear Regulator LED Current Control Overview

Figure 17 shows the TPS92660 linear regulator control circuit. The voltage drop across the current sense resistor R_{SNSLN} is applied on the LNCS pin. An internal operational amplifier compares this voltage with the linear regulator reference voltage. The output of the operational amplifier drives the gate of an external N-channel MOSFET. This MOSFET operates in the linear region when the LED current is in regulation.

The gate-drive voltage controls the drain-to-source voltage of the MOSFET by changing the MOSFET on-resistance. Applications must minimize the voltage difference between the linear regulator input voltage and the LED string forward voltage in order to limit the power dissipation on the MOSFET.

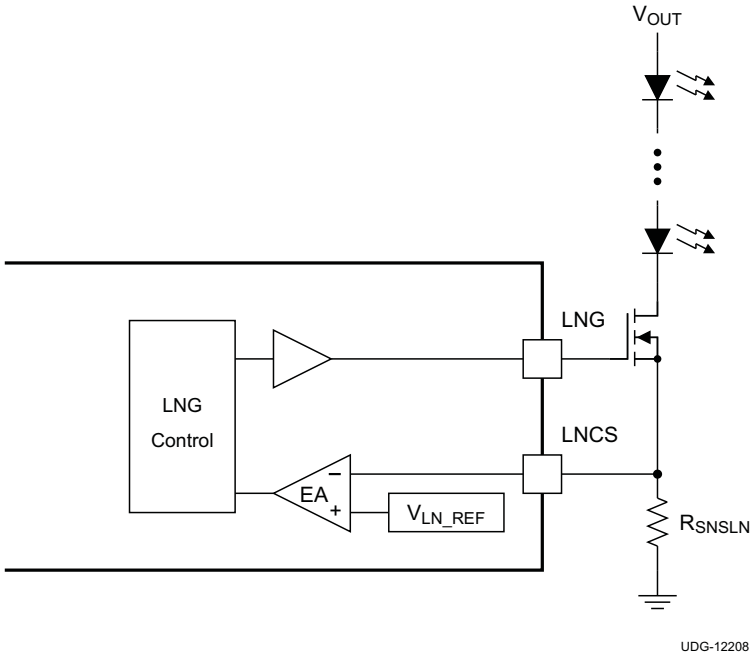


Figure 17. Linear Regulator Control

SADJ and LADJ Pins for Dimming

The SADJ pin controls the switching regulator dimming and the LADJ pin controls the linear regulator dimming. There are two different types of dimming that can be performed on those two pins.

Analog to PWM Dimming

When a DC voltage is applied on the SADJ pin, the switching regulator LED current is PWM dimmed at a fixed frequency of approximately 500 Hz. As shown in Figure 18, the PWM dimming duty cycle is linearly dependent on the input voltage level, from 0% duty cycle at 0.1 V to 100% duty cycle at 2.5 V. Similarly when a DC voltage is applied on the LADJ pin, the linear regulator LED current is PWM dimmed in the same way.

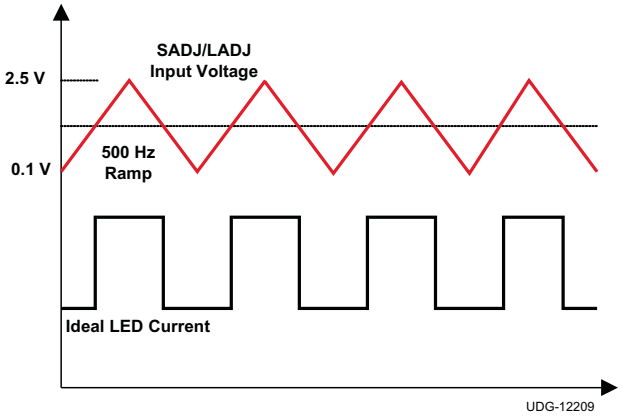


Figure 18. SADJ/LADJ Input to PWM Dimming

PWM Dimming

During PWM dimming, the signal applied on the pin is a PWM signal instead of a DC voltage. The LED current is PWM dimmed at the same frequency and duty cycle as the input PWM signal. To implement PWM dimming, the rising edges of two consecutive pulses of the input PWM signal must be less than 10ms. Once the device detects two consecutive rising edges, the regulator goes into PWM dimming mode. It turns on when the input PWM signal rises above the 2.7-V threshold and turns off when the PWM signal falls below the 2.2V threshold. For the switching regulator, when the input PWM signal is low, the regulator turns off the gate of the MOSFET and the COMP pin capacitor is disconnected. When the input PWM signal is high, the regulator starts again and the COMP pin capacitor is reconnected.

A low gate charge MOSFET is recommended for the linear regulator to prevent LED current overshoot during PWM dimming.

Input Undervoltage Lockout (UVLO)

The TPS92660 enable pin (EN/UVLO) can also be used to implement input undervoltage lockout. The input UVLO voltage is set by a resistor divider from V_{IN} to ground and is compared against a 1.2 V threshold shown in Figure 19. As soon as the input voltage is above the preset UVLO rising threshold, the internal circuitry becomes active and a 1-µA current source at the UVLO pin is turned on. This extra current provides hysteresis to create a lower input UVLO falling threshold.

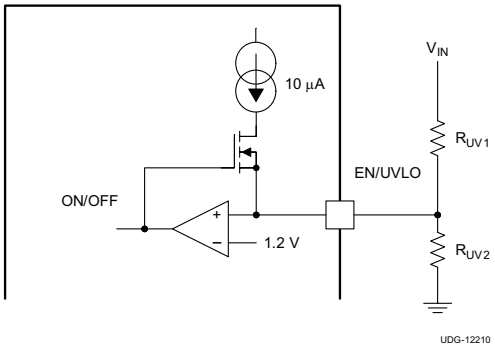


Figure 19. Input UVLO Circuit

The V_{IN} turn-on threshold is defined by Equation 9.

$$V_{IN\_ON} = \frac{1.2\,V \times (R_{UV1} + R_{UV2})}{R_{UV2}} \quad (9)$$

$$V_{HYS} = R_{UV1} \times 10\,\mu A \quad (10)$$

I²C OTP ROM LED Current Trim

I²C Compatible Interface

Interface Bus Overview

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bi-directional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). These lines should be connected to a positive supply, via a pull-up resistor, and remain HIGH even when the bus is idle. Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock (SCL).

Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the high period, the data should remain stable. Any changes on the SDA line during the high state of SCL and in the middle of a transaction aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

I^2C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.

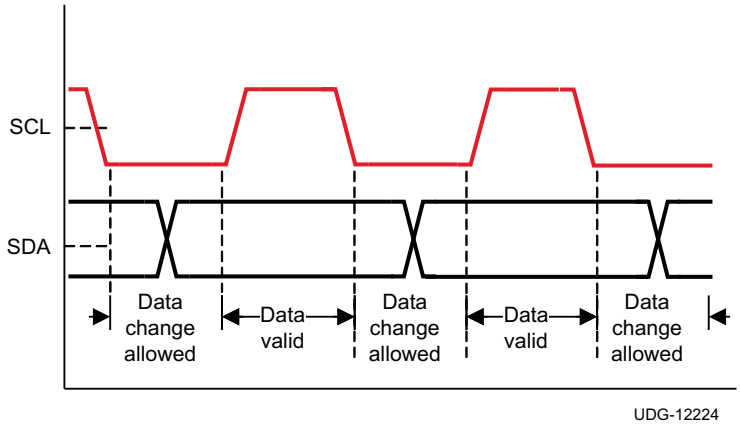


Figure 20. I^2C Signals: Data Validity

I^2C Start and Stop Conditions

START and STOP bits classify the beginning and the end of the I^2C session. START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I^2C master always generates START and STOP bits. Consider the I^2C bus as busy after a START condition and free after a STOP condition. During data transmission, the I^2C master can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

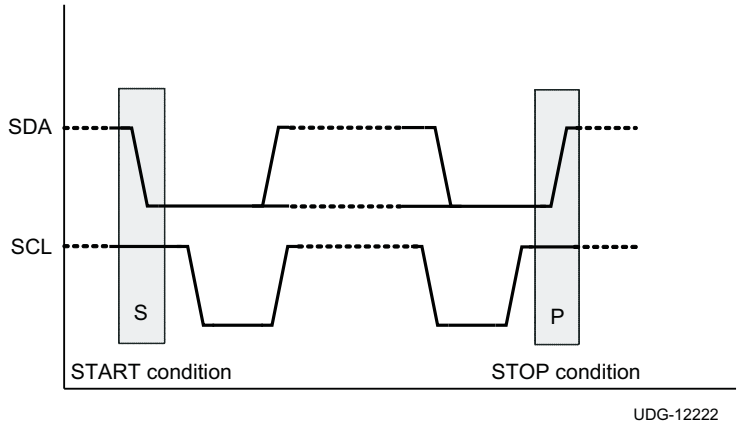


Figure 21. I^2C Start and Stop Conditions

I²C Addresses and Transferring Data

Every data value put on the SDA line must be eight bits long with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The master generates the clock pulse for the acknowledge bit. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledgement. A receiver which has been addressed must generate an acknowledge bit after each byte has been received. After the START condition, the I²C master sends a slave address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The I²C slave address (7 bits) for TPS92660 is 28H. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

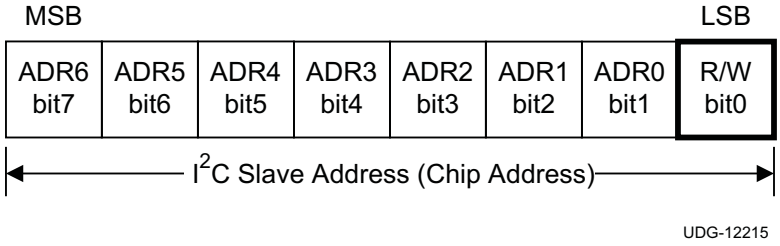
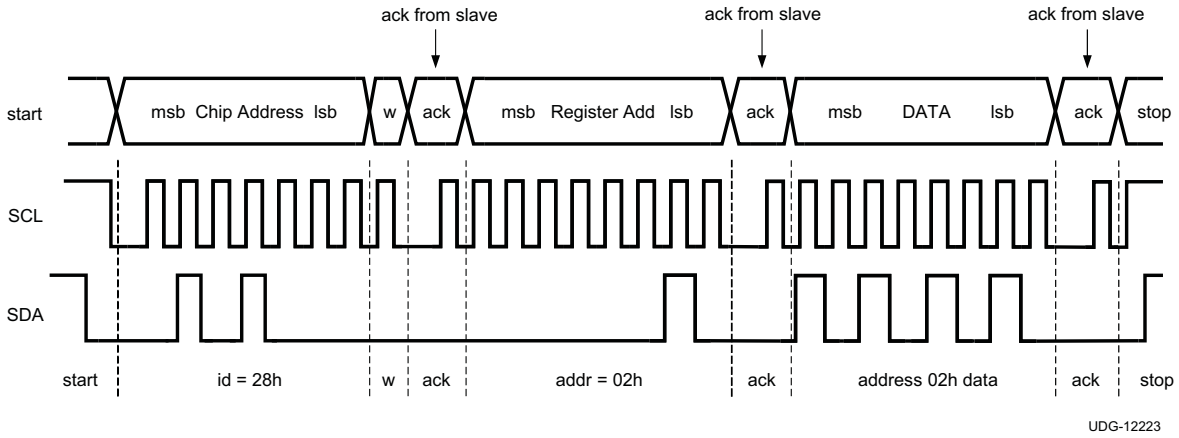


Figure 22. I²C Chip Address

Register changes take effect at the SCL rising edge during the last ACK from the slave as shown in Figure 23.



w = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = 7-bit chip address, 28H for TPS92660.

Figure 23. I²C Write Cycle

A WRITE function must precede the READ function, as shown in the read cycle waveform in Figure 24.

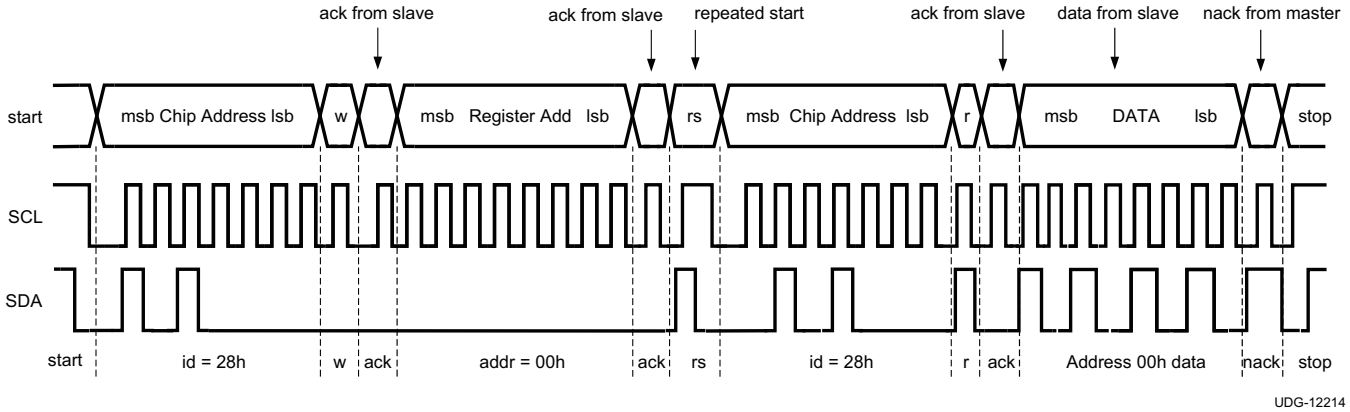


Figure 24. I²C Read Cycle

I²C Timing Parameters (V_{SVDD} = 5 V)

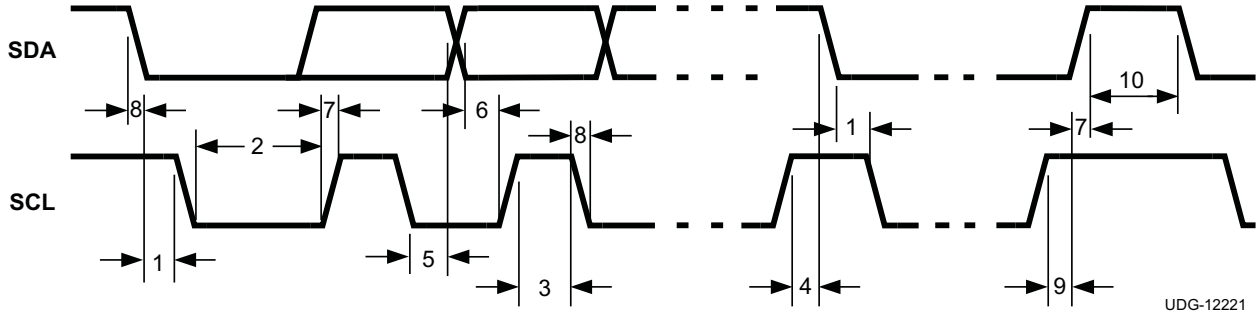


Figure 25. I²C Timing Diagram

TIME PERIOD	PARAMETER(1)	LIMIT		UNITS
		MIN	MAX	
1	Hold time (repeated) START condition	0.6		µs
2	Clock low time	1.3		µs
3	Clock high time	600		ns
4	Setup time for a repeated START condition	600		ns
5	Data hold time (output direction)	300		ns
5	Data hold time (input direction)	0		ns
6	Data setup time	100		ns
7	Rise time of SDA and SCL	20+0.1Cb	300	ns
8	Fall time of SDA and SCL	15+0.1Cb	300	ns
9	Set-up time for STOP condition	600		ns
10	Bus free time between a STOP and a START condition	1.3		µs
Cb	Capacitive load for each bus line	10	200	pF

(1) Data specified by design. Not production tested.

I²C Register Details

The I²C bus interacts with the TPS92660 to realize the features of LED current trim. The operation of these functions requires the writing and reading of the internal registers of the TPS92660. Table 1 is the master register map of the device.

Table 1. Master Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
01h	STRIM	RSV	RSV	STRIM[5:0]						0001 1111
02h	LTRIM	RSV	RSV	RSV	RSV	LTRIM[3:0]				0000 0111
FFh	OTP ROM	RSV	RSV	RSV	BURNED	RSV	WRITE	RSV	READ	0000 1000

Register Definitions

STRIM Register Definition

ADDR	REG	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
01h	**STRIM**	RSV	RSV	STRIM[5:0]						0001_1111

Bits **Description**

5:0 The STRIM register is meant to be programmed with possible trim values. When the best values have been found, the contents of this register may then be made permanent by burning them to OTP ROM using the OTP ROM write cycle (described below).

Upon power-up, the values in OTP ROM are loaded into this register.

Switching Regulator LED Current Trim Table

STRIM[5:0]	CURRENT CHANGE	STRIM[5:0]	CURRENT CHANGE	STRIM[5:0]	CURRENT CHANGE	STRIM[5:0]	CURRENT CHANGE
XX11 1111	–20.0%	XX10 1111	–10.0%	XX01 1111	0%	XX00 1111	10.0%
XX11 1110	–19.4%	XX10 1110	–9.38%	XX01 1110	0.625%	XX00 1110	10.6%
XX11 1101	–18.8%	XX10 1101	–8.75%	XX01 1101	1.25%	XX00 1101	11.3%
XX11 1100	–18.1%	XX10 1100	–8.13%	XX01 1100	1.88%	XX00 1100	11.9%
XX11 1011	–17.5%	XX10 1011	–7.50%	XX01 1011	2.50%	XX00 1011	12.5%
XX11 1010	–16.9%	XX10 1010	–6.88%	XX01 1010	3.13%	XX00 1010	13.1%
XX11 1001	–16.3%	XX10 1001	–6.25%	XX01 1001	3.75%	XX00 1001	13.8%
XX11 1000	–15.6%	XX10 1000	–5.63%	XX01 1000	4.38%	XX00 1000	14.4%
XX11 0111	–15.0%	XX10 0111	–5.00%	XX01 0111	5.00%	XX00 0111	15.0%
XX11 0110	–14.4%	XX10 0110	–4.38%	XX01 0110	5.63%	XX00 0110	15.6%
XX11 0101	–13.8%	XX10 0101	–3.75%	XX01 0101	6.25%	XX00 0101	16.3%
XX11 0100	–13.1%	XX10 0100	–3.13%	XX01 0100	6.88%	XX00 0100	16.9%
XX11 0011	–12.5%	XX10 0011	–2.50%	XX01 0011	7.50%	XX00 0011	17.5%
XX11 0010	–11.9%	XX10 0010	–1.88%	XX01 0010	8.13%	XX00 0010	18.1%
XX11 0001	–11.3%	XX10 0001	–1.25%	XX01 0001	8.75%	XX00 0001	18.8%
XX11 0000	–10.6%	XX10 0000	–0.625%	XX01 0000	9.38%	XX00 0000	19.4%

LTRIM Register Definition

ADDR	REG	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
02h	**LTRIM**	RSV	RSV	RSV	RSV	LTRIM[3:0]				0000_0111

Bits **Description**

3:0 The LTRIM register is meant to be programmed with possible trim values. When the best values have been found, the contents of this register may then be made permanent by burning them to OTP ROM using the OTP ROM write cycle (described below).

Upon power-up, the values in OTP ROM are loaded into this register.

Linear Regulator LED Current Trim Table

LTRIM[3:0]	CURRENT CHANGE	LTRIM[3:0]	CURRENT CHANGE	LTRIM[3:0]	CURRENT CHANGE	LTRIM[3:0]	CURRENT CHANGE
XXXX 1111	-25.0%	XXXX 1011	–12.5%	XXXX 0111	0%	XXXX 0011	12.5%
XXXX 1110	-21.9%	XXXX 1010	–9.38%	XXXX 0110	3.13%	XXXX 0010	15.6%
XXXX 1101	-18.8%	XXXX 1001	–6.25%	XXXX 0101	6.25%	XXXX 0001	18.8%
XXXX 1100	-15.6%	XXXX 1000	–3.13%	XXXX 0100	9.38%	XXXX 0000	21.9%

OTP ROM Register Definition

ADDR	REG	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
FFh	**OTP ROM**	RSV	RSV	RSV	BURNED	RSV	WRITE	RSV	READ	0000_1000

Bits	Description
7:5	Reserved. These bits are reserved for future use. When writing to the OTP ROM register, always write ‘0’s to these bits.
4	BURNED – This bit indicates that OTP ROM has been burned (when “BURNED” = 1). After burning OTP ROM, an OTP ROM read cycle must take place in order for the BURNED bit to be updated. This happens automatically upon power-up, or it can be accomplished manually by issuing an OTP ROM read command (see bit 0).
3	RSV
2	WRITE – Burning the LTRIM and STRIM register values to OTP ROM is accomplished by writing this bit to a ‘1’, waiting at least 25ms, and then writing this bit back to ‘0’.
1	RSV
0	READ – To reload the STRIM and LTRIM registers from OTP ROM, write this bit to a ‘1’. This bit always reads back as a ‘0’. Writing this bit to a ‘1’ temporarily enables the 500 kHz oscillator to perform the OTP ROM read. When the OTP ROM read is finished, the oscillator is disabled.

OTP ROM Programming

The programming of both the STRIM and the LTRIM registers to OTP ROM is performed in a single sequence as follows

1. Write the STRIM and LTRIM registers with the desired values.
2. Write a ‘1’ to the WRITE bit of the OTP ROM register (this switches the internal EVDD from 5V to 8V).
3. Wait at least 25 ms.
4. Write a ‘0’ to the WRITE bit (this returns EVDD to 5 V).

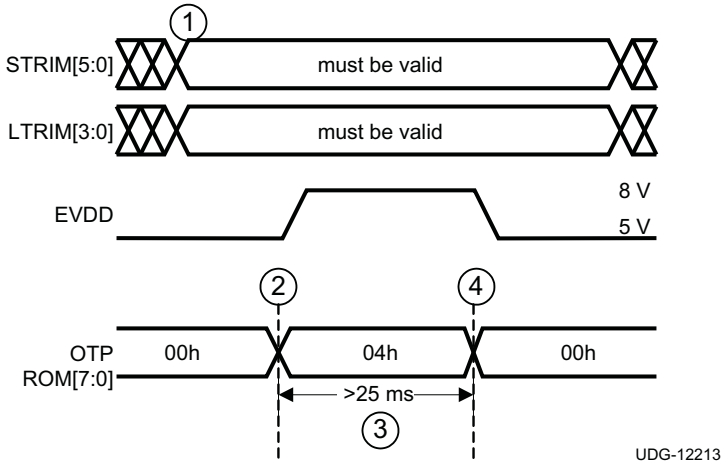


Figure 26. OTP ROM Programming Sequence

OTP ROM Reading

The EPROM is read under either of the following conditions:

- Power-on reset. Note that power-on reset starts when both EN pin and VCC voltages cross the UVLO threshold. It takes apprimately 50µs to read the OTP ROM contents into the TRIM registers.
- Writing a '1' to the READ bit of the OTP ROM register. It is not necessary to clear the READ bit after writing it to a '1'.

The device temporarily enables the 500-kHz oscillator during the OTP ROM read cycle. This operation is necessary because the digital counters generate the timing for the OTP ROM read cycle. After the OTP ROM read cycle is finished, the oscillator is disabled.

Figure 27 shows a power-on OTP ROM read cycle. The device reads all OTP ROM registers simultaneously. All timing values are approximate and based on a 500-kHz internal oscillator.

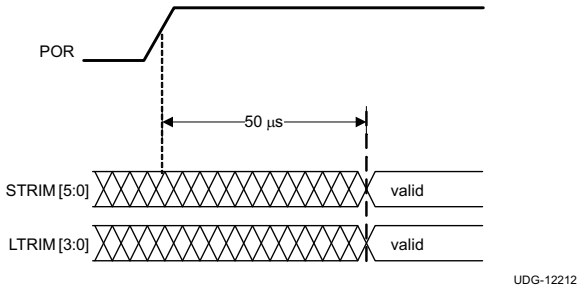


Figure 27. Power-ON OTP ROM Read Timing

Reference Voltage

The TPS92660 provides a 3.0V reference voltage which can be used in the AC/DC main power supply secondary-side control circuit.

Thermal Shutdown

Internal thermal shutdown circuitry protects the device in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 165°C with a 25°C hysteresis. Thermal shutdown protection disables the MOSFET drivers.

DESIGN EXAMPLE

Specifications

Switching Regulator

- Switching Regulator: (f_{SW}): 200 kHz
- Input voltage (V_{IN}): 60 V
- Output voltage (V_{OUT}): 48 V
- Charge current (I_{LED}): 500 mA
- Output overvoltage protection threshold (V_{OVP}): 60 V

Linear Regulator

- Input voltage (V_{IN}): 30 V
- Output voltage (V_{OUT}): 24 V
- Charge current (I_{LED}): 20 mA

Design Procedure

Step 1: Select Overvoltage and Timing Components R_{OV1}, R_{OV2}, R_T and C_T

$$V_{OVP} \times \frac{R_{VO2}}{(R_{VO1} + R_{VO2})} = 2.5\,V \tag{11}$$

- V_{OVP} = 60 V
- Choose R_{VO2} = 1.00 kΩ
- The calculated R_{VO1} = 23 kΩ, the standard resistor with the closest value (± 1%) is 23.2 kΩ

$$f_{SW} = \frac{(R_{VO1} + R_{VO2})}{R_{VO2} \times R_T \times C_T} \tag{12}$$

- f_{SW} = 200 KHz
- $R_T \times C_T = 121 \times 10^{-6}$, choose C_T = 1000 pF
- the calculated R_T = 121 kΩ

Step 2: Select Current Sense Resistors R_{SNS} and R_{SNS_LN}

The current sense resistor of the switching regulator R_{SNS} = 202 mV/500 mA = 0.404 Ω.

The current sense resistor of the linear regulator R_{SNS_LN} = 200 mV/20 mA = 10 Ω.

Step 3: Select Inductor

Choose inductor current ripple ΔI_{L_PP} = 0.15 A (30% of I_{LED})

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} = \frac{48\,V}{60\,V \times 200\,kHz} = 4\,\mu s \tag{13}$$

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{\Delta I_{L(P-P)}} = \frac{(60\,V - 48\,V) \times 4\,\mu s}{0.15\,A} = 320\,\mu H \tag{14}$$

The closest standard inductor value is 330 µH.

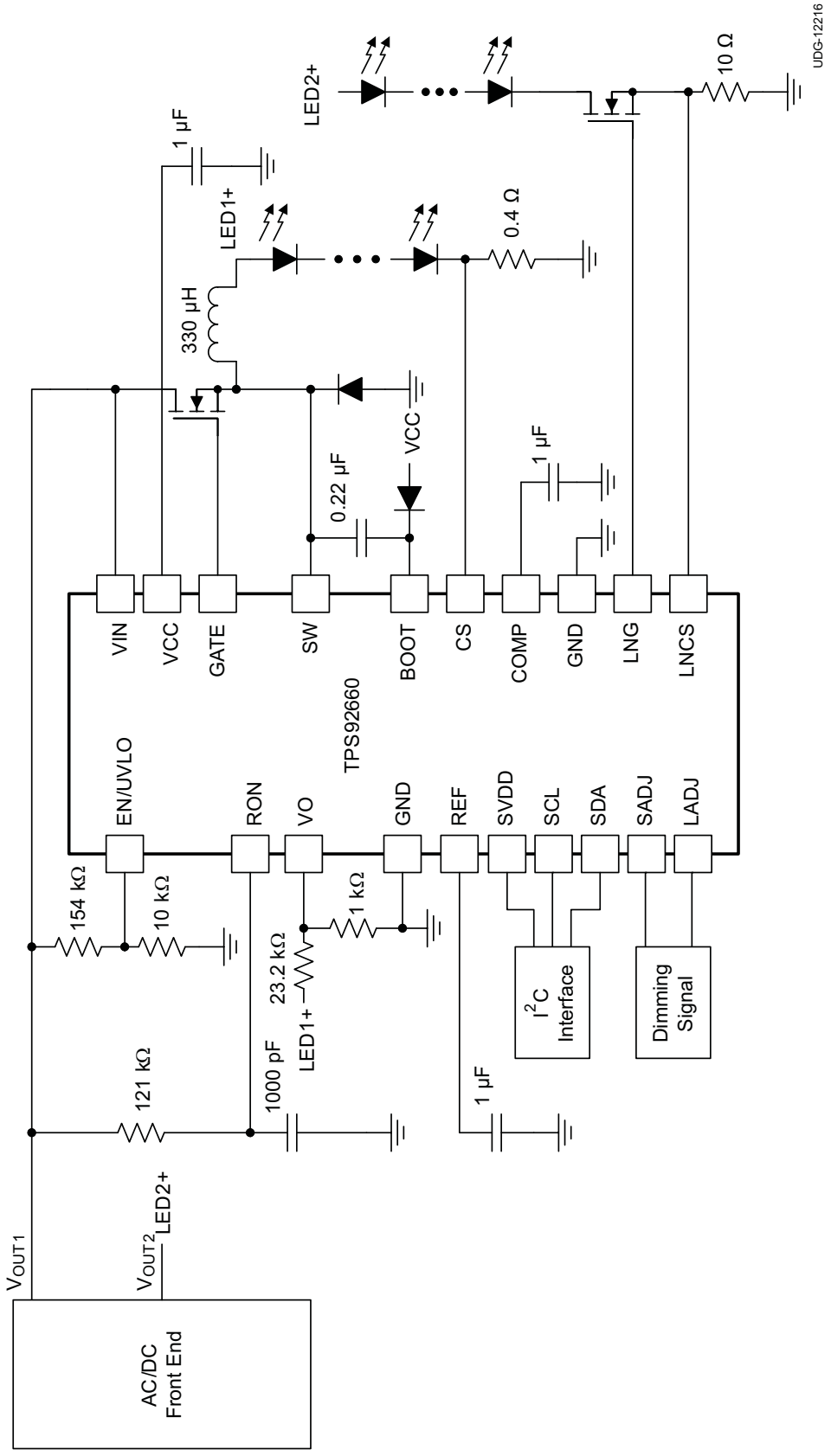


Figure 28. Design Example Application Schematic

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS92660PWP/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TP92660 PWP
TPS92660PWP/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TP92660 PWP
TPS92660PWPR/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TP92660 PWP
TPS92660PWPR/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TP92660 PWP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

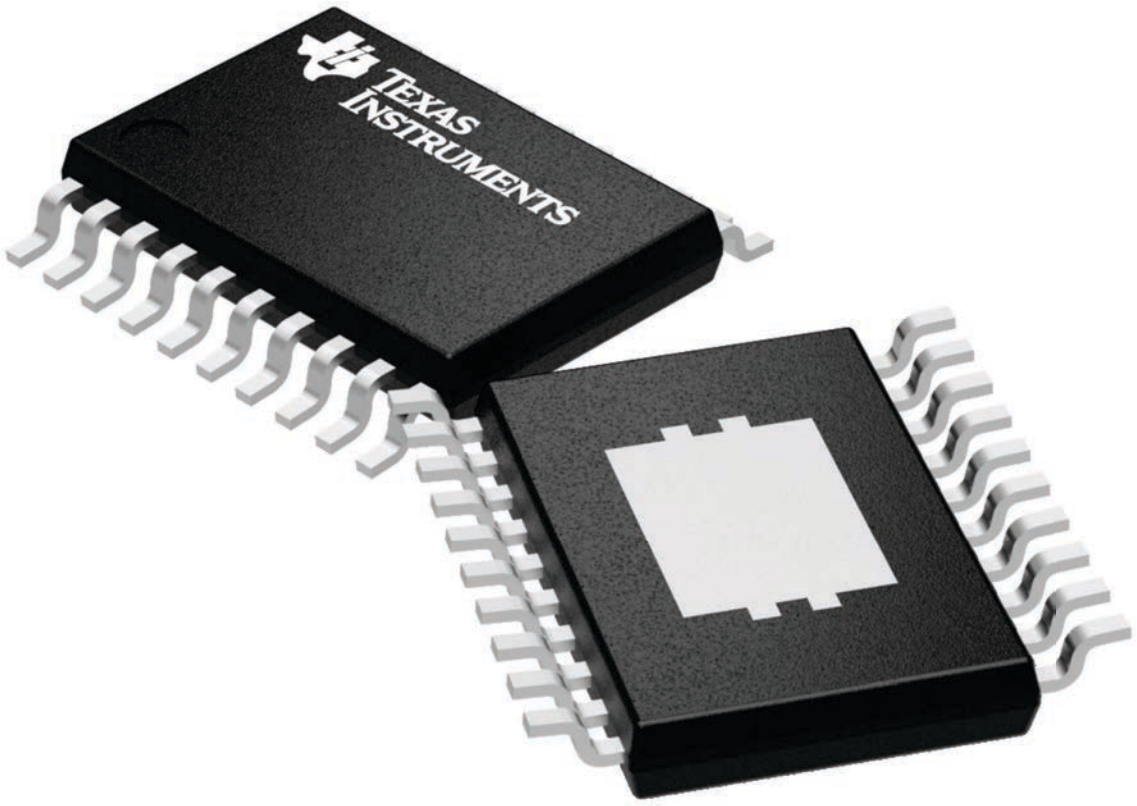
PWP 20

HTSSOP - 1.2 mm max height

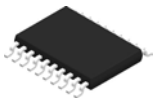
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

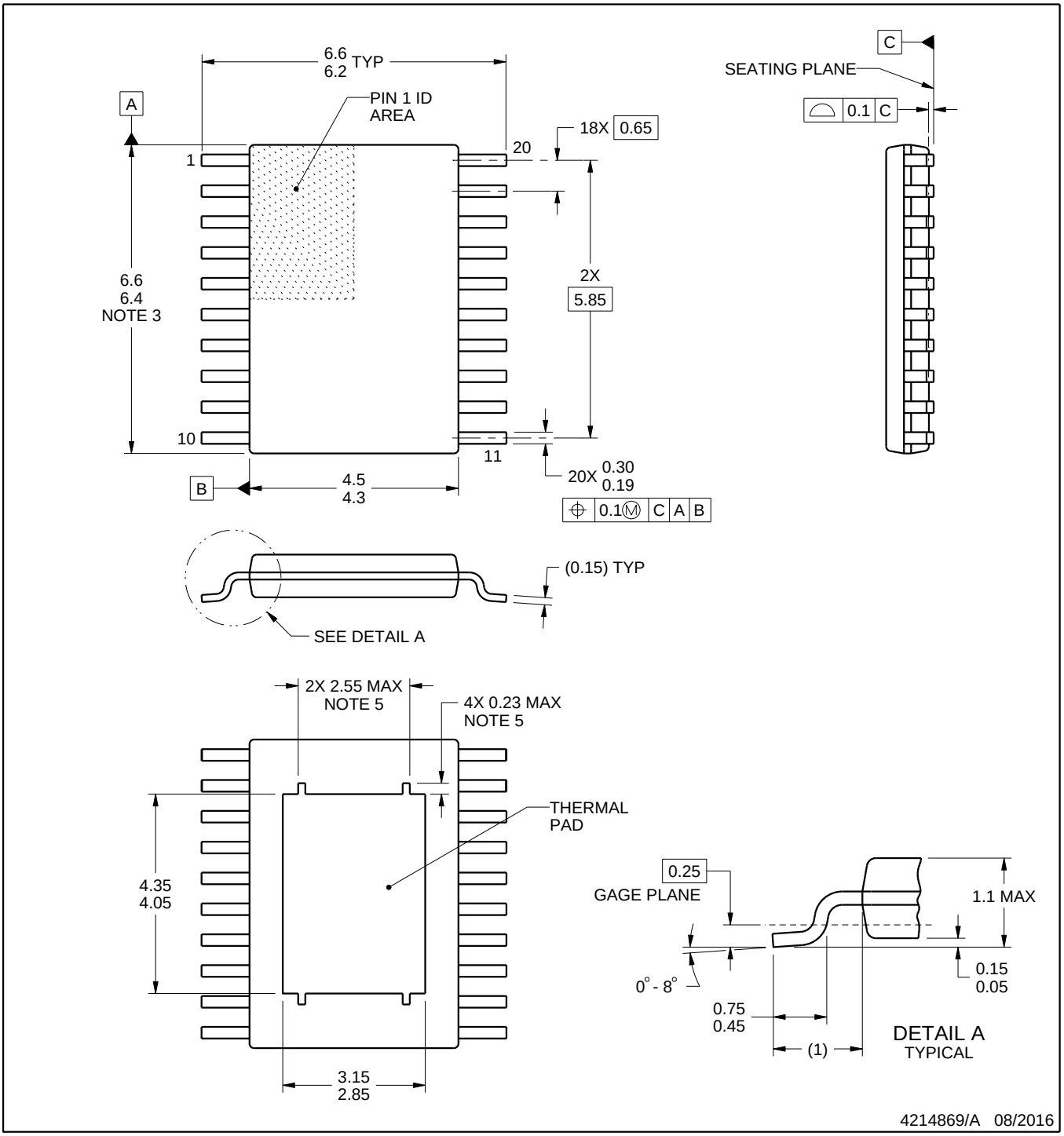


PACKAGE OUTLINE

PWP0020A

PowerPAD™ TSSOP - 1.1 mm max height

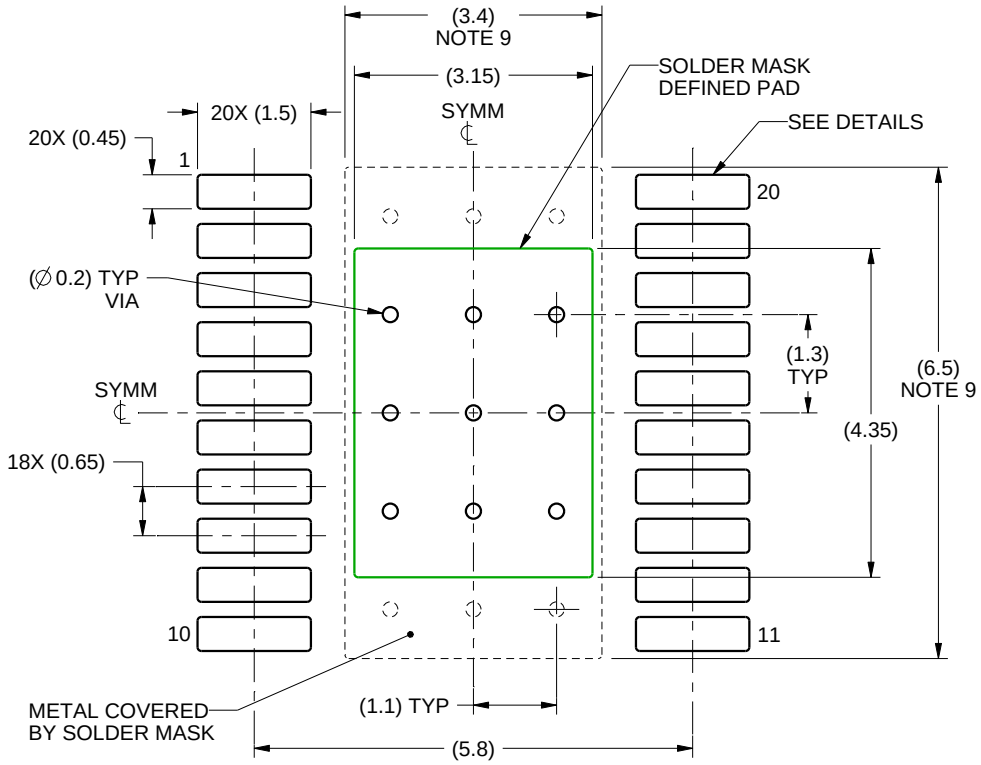
PLASTIC SMALL OUTLINE



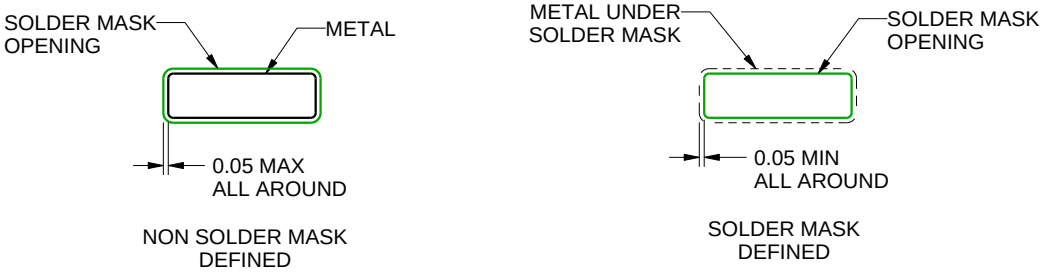
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-20

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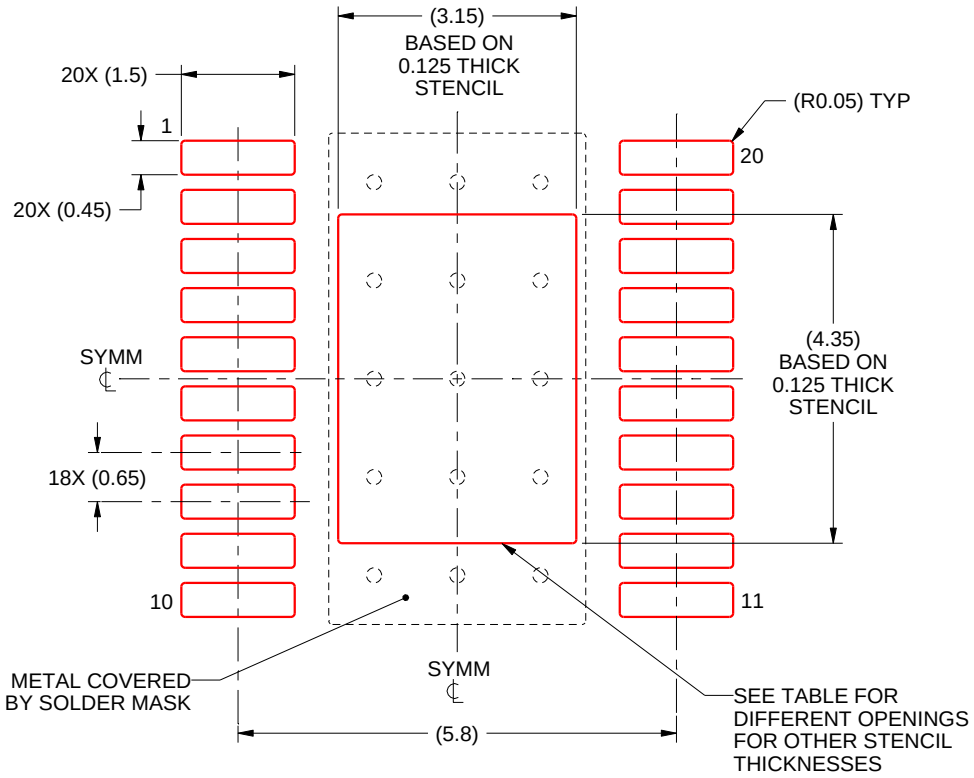
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.52 X 4.86
0.125	3.15 X 4.35 (SHOWN)
0.15	2.88 X 3.97
0.175	2.66 X 3.68

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月