4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

Check for Samples: TS3DV421

FEATURES

- **Compatible With HDMI v1.3 DVI 1.0 High-Speed Digital Interface**
  - **Wide Bandwidth of Over 3.8 Gbps**
  - **Serial Data Stream at 10× Pixel Clock Rate**
  - **Supports All Video Formats up to 1080p and SXGA (1280 × 1024 at 75 Hz)**
  - **High Bandwidth of 4.95 Gbps (Single Link)**
  - **HDCP Compatible**
- **Low Crosstalk (X_{TALK} = −50 dB Typ at 1.65 Gbps)**
- **Off Isolation (O_{IRR} = −50 dB Typ at 1.65 Gbps)**
- **Low Bit-to-Bit Skew ($t_{sk(o)}$ = 0.1 ns Max)**
- **Low and Flat ON-State Resistance (r_{ON} = 12.5 Ω Max, $r_{ON(flat)}$ = 0.5 Ω Typ)**
- **Low Input/Output Capacitance (C_{ON} = 4.5 pF Max)**
- **Enables Application-Specific Operating Voltage Selection**
  - **V_{DD} Operating Range From 1.5 V to 2.1 V When V_{SS} = GND**
  - **V_{DD} Operating Range From 3.0 V to 3.6 V When V_{SS} = 1.5 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **For DisplayPort Applications: V_{DD} = 1.8 V , V_{SS} = GND**
- **For HDMI /DVI Applications: V_{DD} = 3.3 V , V_{SS} = 1.5 V**
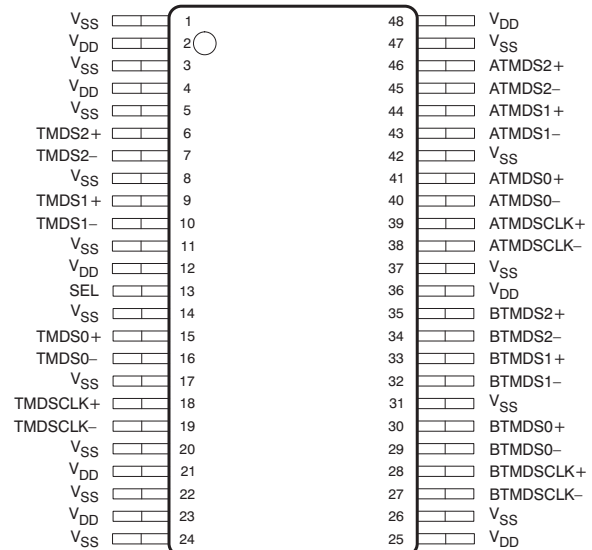
APPLICATIONS

- **DVI/HDMI Signal Switching**
- **Differential DVI, HDMI Signal Multiplexing for Audio/Video Receivers and High-Definition Televisions (HDTVs)**

RUA PACKAGE (TOP VIEW)
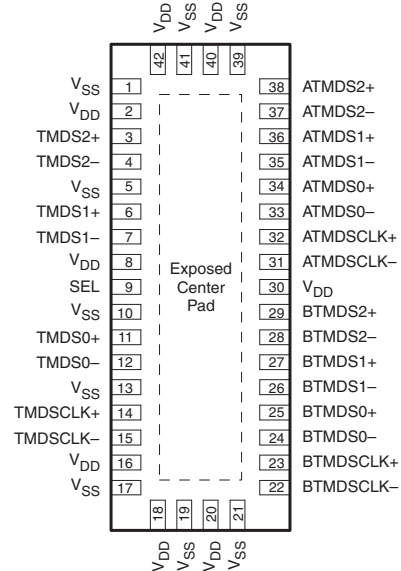
For RUA, the exposed center pad must be connected to V_{SS} or electronically open. For this part to be used in HDMI/TMDS applications, V_{SS} can be elevated to 1.5 V. See Figure 1.

DGV PACKAGE (TOP VIEW)

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TS3DV421

DESCRIPTION/ORDERING INFORMATION

The TS3DV421 is a 4-channel differential 2:1 multiplexer/demultiplexer digital video switch controlled with one select input (SEL). SEL controls the data path of the multiplexer/demultiplexer and can be connected to any GPIO in the system, using an external voltage divider system. The device provides high bandwidth necessary for DVI and HDMI applications. This device expands the high-speed physical link interface from a single HDMI port to two HDMI ports (A or B port). The unselected channel is set to a high-impedance state.

The most common application for the TS3DV421 is in the sink application. In this case, there are two sources (i.e., DVD, set-top box, or game console) that must be routed to one HDMI receiver. The TS3DV421 can route the signals where one HDMI receiver (in a DLP, LCD TV, PDP, or other high-definition display) can be expanded to three ports.

The HDMI application calls for a 100-Ω differential impedance between the differential lines (TMDSn+ and TMDSn–). Additionally, because the TS3DV421 is a high-bandwidth, low-r_{ON} pass transistor-type switch, a properly designed board retains a 100-Ω differential impedance through the switch. The unselected port is in the high-impedance mode, such that the receiver receives information from only one source. HDCP encryption is passed through the switch for the HDMI receiver to decode.

Table 1. ORDERING INFORMATION

T_A	PACKAGE[1] [2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RUA	Tape and reel	TS3DV421RUAR	SD421
	TVSOP – DGV	Tape and reel	TS3DV421DGVR	SD421

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TYPICAL APPLICATION
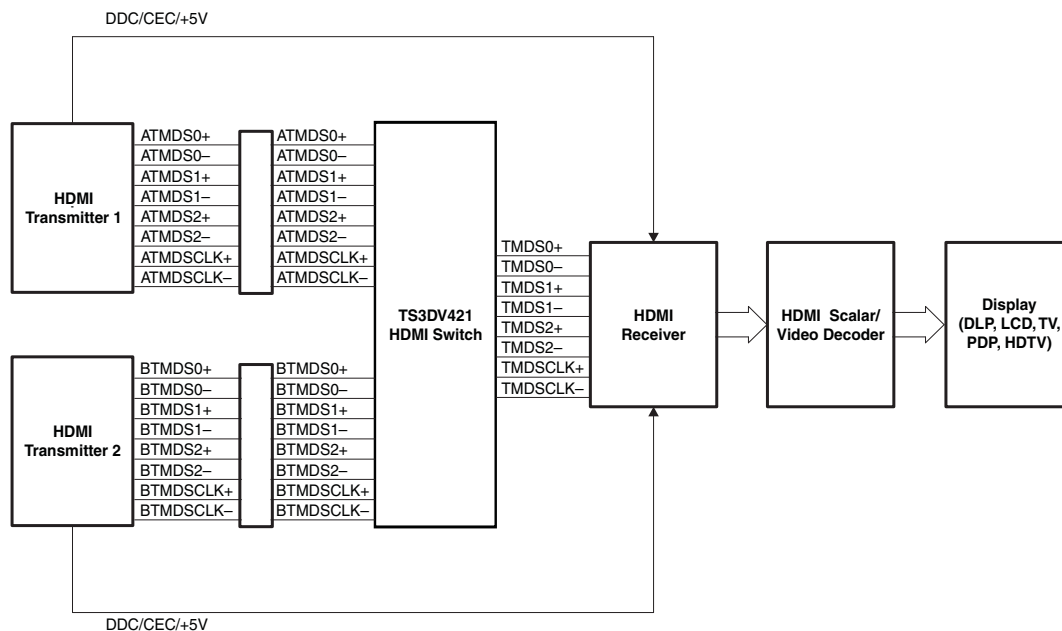
Table 2. FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn– = ATMDSn– TMDSCLK+ = ATMDSCLK+ TMDSCLK– = ATMDSCLK– BTMDSn+ = High impedance BTMDSn– = High impedance BTMDSCLK+ = High impedance BTMDSCLK– = High impedance	TMDSn+ TMDSn– TMDSCLK+ TMDSCLK–
H	TMDSn+ = BTMDSn+ TMDSn– = BTMDSn– TMDSCLK+ = BTMDSCLK+ TMDSCLK– = BTMDSCLK– ATMDSn+ = High impedance ATMDSn– = High impedance ATMDSCLK+ = High impedance ATMDSCLK– = High impedance	TMDSn+ TMDSn– TMDSCLK+ TMDSCLK–

FUNCTIONAL DIAGRAM
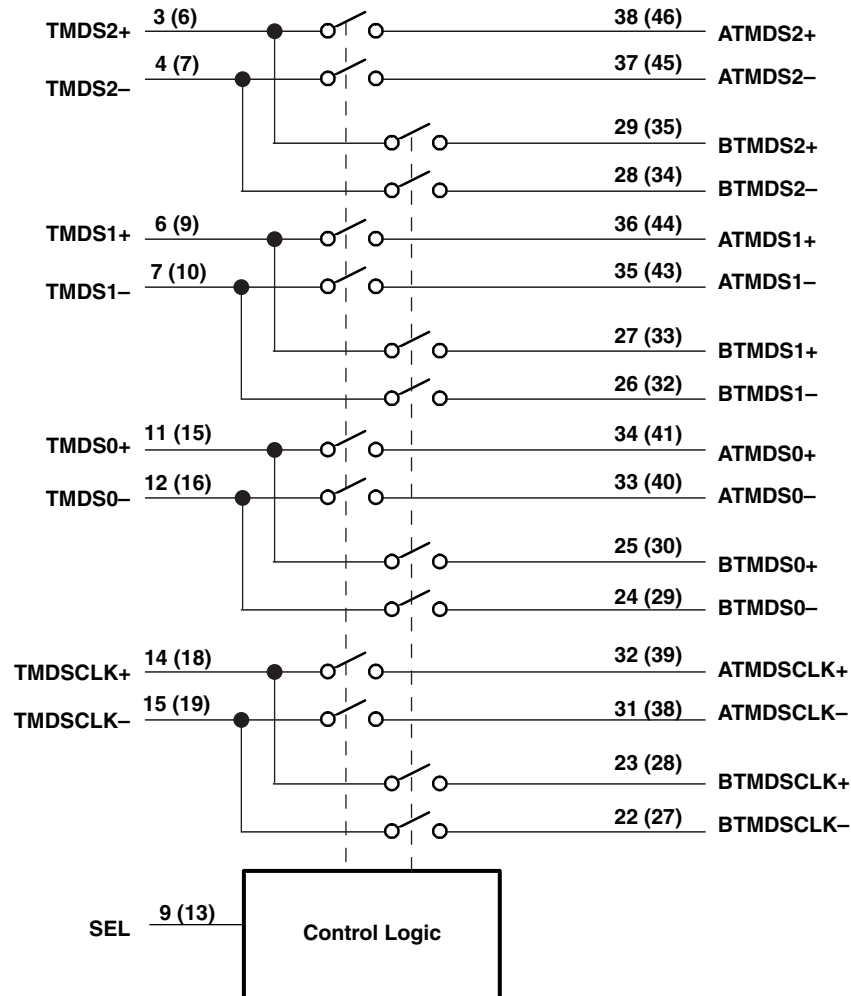
A.   TVSOP package pin identification in parenthesis.

Product Folder Link(s): TS3DV421

TS3DV421

TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	QFN (RUA)	TVSOP (DGV)		
ATMDS0–	33	40	I/O	Port A, channel 0, TMDS negative signal
ATMDS0+	34	41	I/O	Port A, channel 0, TMDS positive signal
ATMDS1–	35	43	I/O	Port A, channel 1, TMDS negative signal
ATMDS1+	36	44	I/O	Port A, channel 1, TMDS positive signal
ATMDS2–	37	45	I/O	Port A, channel 2, TMDS negative signal
ATMDS2+	38	46	I/O	Port A, channel 2, TMDS positive signal
ATMDSCLK–	31	38	I/O	Port A TMDS negative clock
ATMDSCLK+	32	39	I/O	Port A TMDS positive clock
BTMDS0–	24	29	I/O	Port B, channel 0, TMDS negative signal
BTMDS0+	25	30	I/O	Port B, channel 0, TMDS positive signal
BTMDS1–	26	32	I/O	Port B, channel 1, TMDS negative signal
BTMDS1+	27	33	I/O	Port B, channel 1, TMDS positive signal
BTMDS2–	28	34	I/O	Port B, channel 2, TMDS negative signal
BTMDS2+	29	35	I/O	Port B, channel 2, TMDS positive signal
BTMDSCLK–	22	27	I/O	Port B TMDS negative clock
BTMDSCLK+	23	28	I/O	Port B TMDS positive clock
SEL	9	13	I	Select pin to choose between port A or port B. Referenced to V_{SS}
TMDS0–	12	16	I/O	TMDS channel 0 negative signal
TMDS0+	11	15	I/O	TMDS channel 0 positive signal
TMDS1–	7	10	I/O	TMDS channel 1 negative signal
TMDS1+	6	9	I/O	TMDS channel 1 positive signal
TMDS2–	4	7	I/O	TMDS channel 2 negative signal
TMDS2+	3	6	I/O	TMDS channel 2 positive signal
TMDSCLK–	15	19	I/O	TMDS negative clock
TMDSCLK+	14	18	I/O	TMDS positive clock
V_{DD}	2, 8, 16, 18, 20, 30, 40, 42	2, 4, 12, 21, 23, 25, 36, 48	Power	Positive power supply voltage
V_{SS}	1, 5, 10, 13, 17, 19, 21, 39, 41	1, 3, 5, 8, 14, 17, 20, 22, 24, 26, 31, 37, 42, 47	Power	Negative power supply voltage

Product Folder Link(s): *TS3DV421*

ABSOLUTE MINIMUM AND MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted), - All voltages are with respect to V_{SS}

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		−0.5	2.5	V
V_{IN}	Control input voltage range[2]		−0.5	2.5	V
$V_{I/O}$	Switch I/O voltage range[2] [3]		−0.5	2.5	V
I_{IK}	Control input clamp current	$V_{IN} < V_{SS}$		50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < V_{SS}$		50	mA
$I_{I/O}$	ON-state switch current[4]			100	mA
I_{DD}	Continuous current through V_{DD}			100	mA
I_{SS}	Continuous current through V_{SS}			100	mA
$θ_{JA}$	Package thermal impedance[5]	DGV package		58.0	°C/W
		RUA package		51.2	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(4) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	V_{SS} = GND	1.5	1.8	2.1	V
		V_{SS} = 1.5 V	3	3.3	3.6	
V_{IH}	High-level input voltage	3 V < V_{DD} < 3.6 V, V_{SS} = 1.5 V	$0.65(V_{DD} - V_{SS})$ + V_{SS}			V
V_{IL}	Low-level input voltage	1.5 V < V_{DD} < 2.1 V, V_{SS} = 0 V			$0.35(V_{DD} - V_{SS})$ + V_{SS}	V
V_{IO}	Switch input/output voltage		0		V_{DD}	V
T_A	Operating free-air temperature		0		85	°C

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY[1]

V_{DD} = 1.5 V to 2.1 V, V_{SS} = 0 V, T_A = −40°C to 85°C (unless otherwise noted)

| PARAMETER		TEST CONDITIONS				MIN	TYP[2]	MAX	UNIT
V_{IK}	SEL	V_{DD} = 2.1 V,	I_{IN} = −18 mA				−0.7	−1.2	V
I_{IH}	SEL	V_{DD} = 2.1 V,	V_{IN} = V_{DD}					±1	µA
I_{IL}	SEL	V_{DD} = 2.1 V,	V_{IN} = V_{SS}					±1	µA
I_{off}		V_{DD} = 0,	V_O = 0 to 2.1 V,	V_I = 0				1	µA
I_{CC}		V_{DD} = 2.1 V,	$I_{I/O}$ = 0,	Switch ON or OFF			230	450	µA
C_{IN}	SEL	f = 1 MHz,	V_{IN} = 0				0.7	1	pF
C_{OFF}	B port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		1	1.5	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		4	4.5	pF
r_{on}		V_{DD} = 1.8 V,	V_{SS} ≤ V_I ≤ V_{DD},	I_O = −40 mA			12.5	20	Ω
$r_{on(flat)}$ [3]		V_{DD} = 1.8 V,	V_I = 1.65 V to 1.8 V	I_O = −40 mA			0.5		Ω
Δr_{on} [4]		V_{DD} = 1.8 V,	V_{SS} ≤ V_I ≤ V_{DD},	I_O = −40 mA			−0.1	0.2	Ω
Dynamic									
X_{TALK}		R_L = 50 Ω,	f = 825 MHz	See Figure 7			−50		dB
O_{IRR}		R_L = 50 Ω,	f = 825 MHz	See Figure 8			−50		dB
BW				See Figure 6			1.9		GHz
Max data rate				See Figure 6			3.8		Gbps

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from centerports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 1.5 V to 2.1 V, V_{SS} = 0 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP[1]	MAX	UNIT
t_{pd} [2]	TMDSn or xTMDSn	xTMDSn or TMDSn		0.25		ns
t_{PZH}, t_{PZL}	SEL	TMDSn or xTMDSn	0.5		9	ns
t_{PHZ}, t_{PLZ}	SEL	TMDSn or xTMDSn	0.5		5	ns
$t_{sk(o)}$ [3]	TMDSn or xTMDSn	xTMDSn or TMDSn		0.06		ns
$t_{sk(p)}$ [4]				0.06	0.1	ns

(1) All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port to any other port
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$
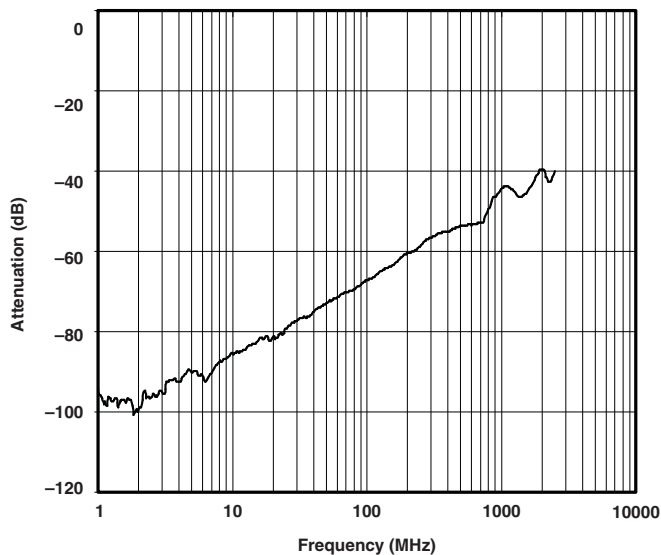
Product Folder Link(s): *TS3DV421*
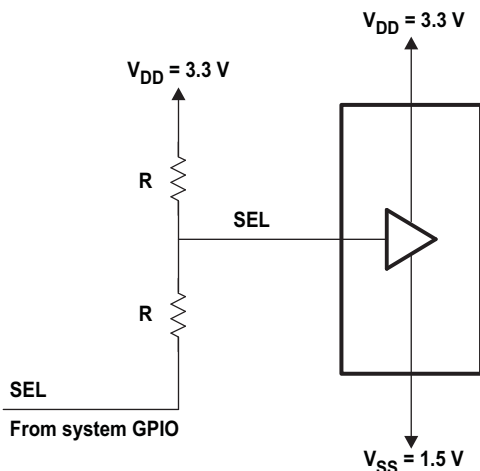
This example circuit shows connecting control inputs to GPIOs of an application using V_{SS} = 1.5 V, which allows the device to pass TMDS signal levels

Figure 1. Example Voltage Divider Circuit

TYPICAL CHARACTERISTICS
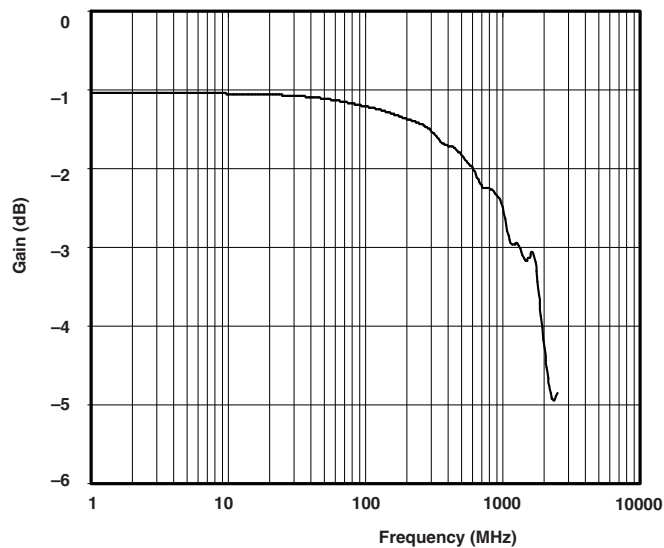
Figure 2. Insertion Loss

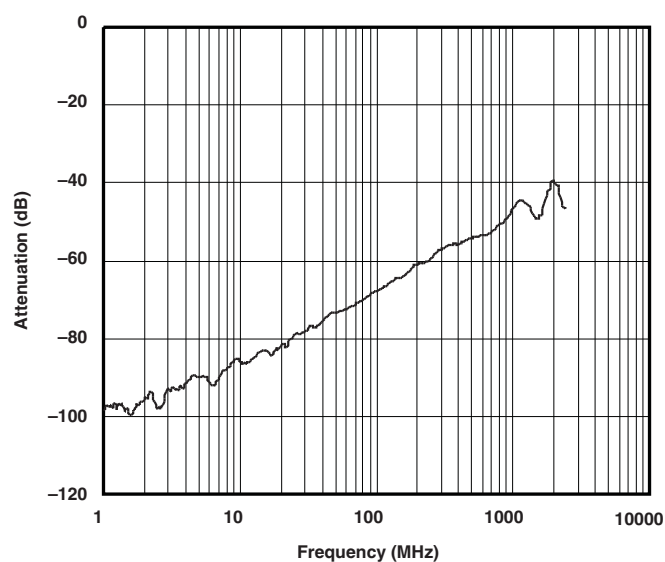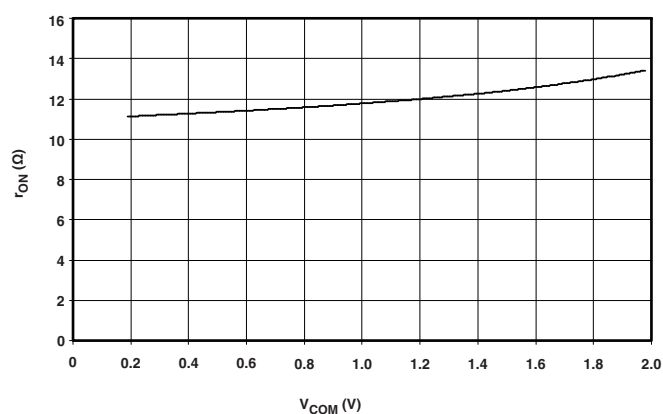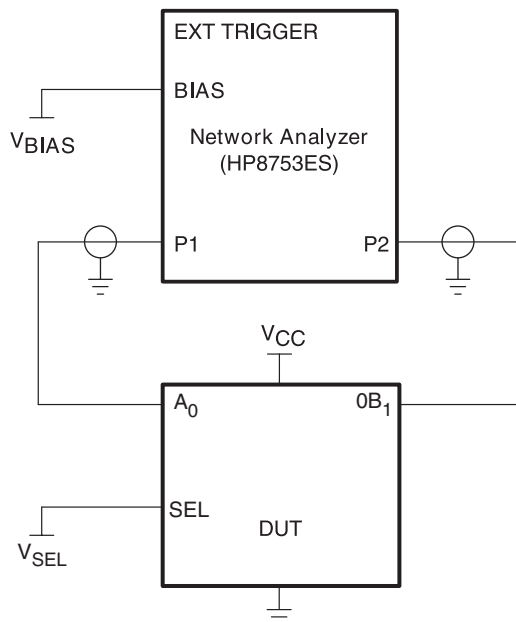**Figure 3. Crosstalk**

TYPICAL CHARACTERISTICS (continued)

Figure 4. Off Isolation vs Frequency

Figure 5. r_{ON} vs V_{COM}

Product Folder Link(s): TS3DV421

PARAMETER MEASUREMENT INFORMATION

Figure 6. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.
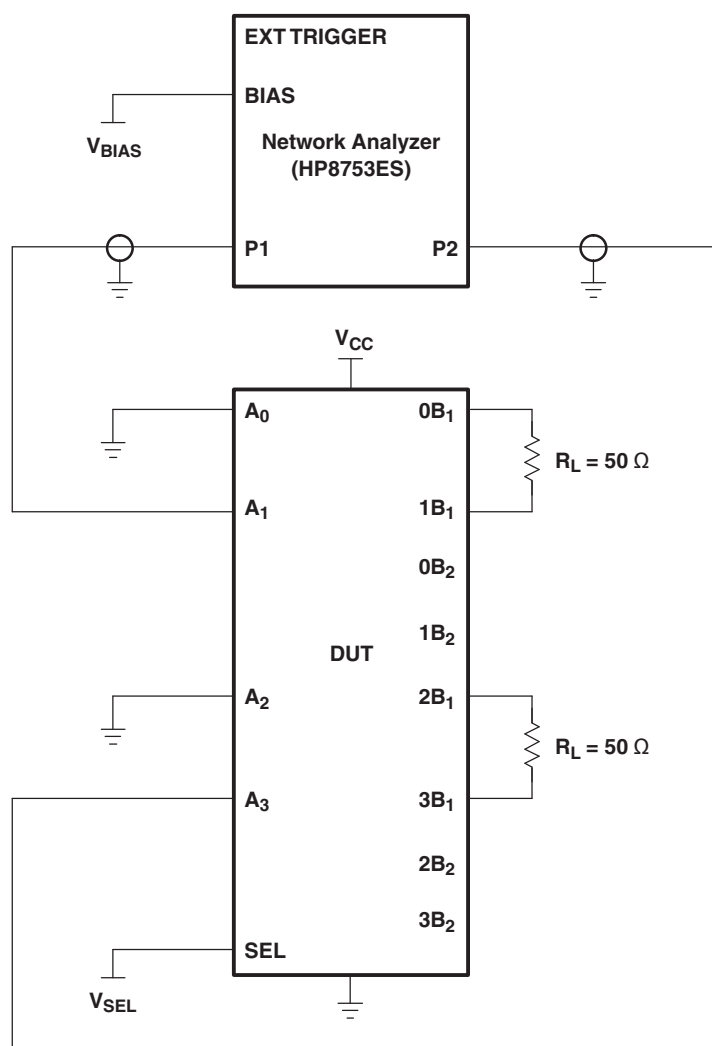
HP8753ES setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

Figure 7. Test Circuit for Crosstalk (X$_{TALK}$)

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V$_{SEL}$ is low and A$_0$ is the input, the output is measured at 1B$_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50-Ω pulldown resistors.
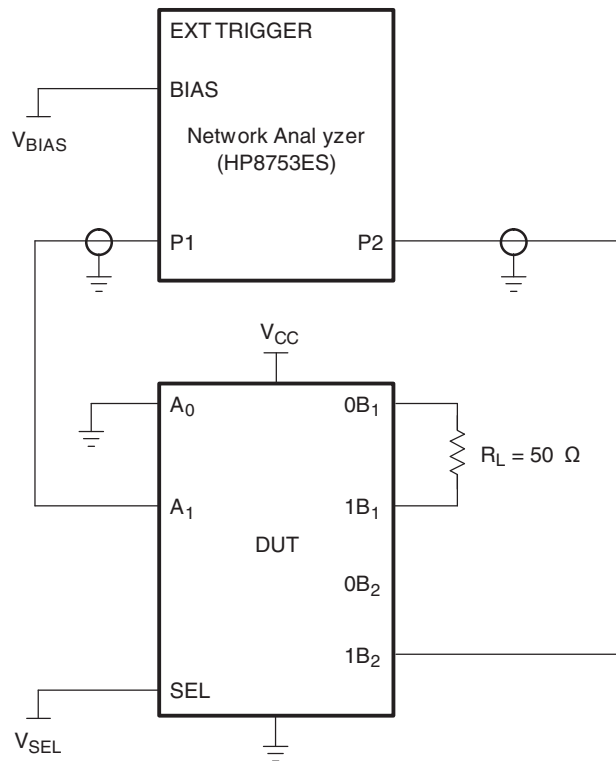
HP8753ES setup

Average = 4

RBW = 3 kHz

V$_{BIAS}$ = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

Figure 8. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $0B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2

P1 = 0 dBM

TS3DV421

TEXAS INSTRUMENTS

APPLICATION INFORMATION
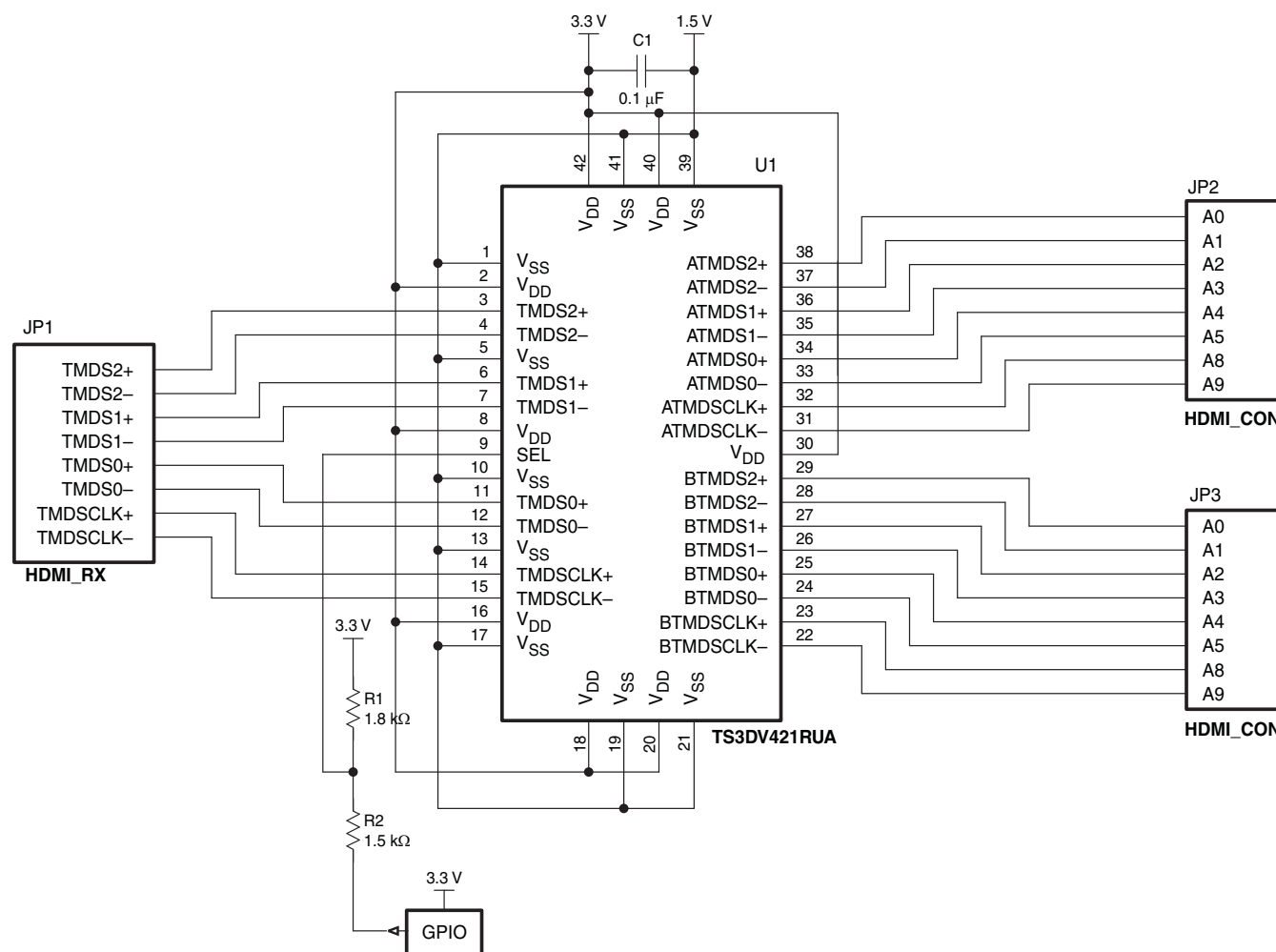
Figure 9. Reference Circuit for HDMI Application

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Product Folder Link(s): *TS3DV421*

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3DV421DGVR	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD421
TS3DV421DGVR.A	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD421
TS3DV421RUAR	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	FULL NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	SD421
TS3DV421RUAR.A	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SD421

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

K0 ← P1 →

B0 W

Cavity → A0 ←

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

| Q1 | Q2 | Q1 | Q2 |
| Q3 | Q4 | Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV421DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
TS3DV421RUAR	WQFN	RUA	42	3000	330.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV421DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
TS3DV421RUAR	WQFN	RUA	42	3000	346.0	346.0	35.0

DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

| | PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
DIM								
A MAX		3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN		3,50	3,50	4,90	4,90	7,70	9,60	11,20

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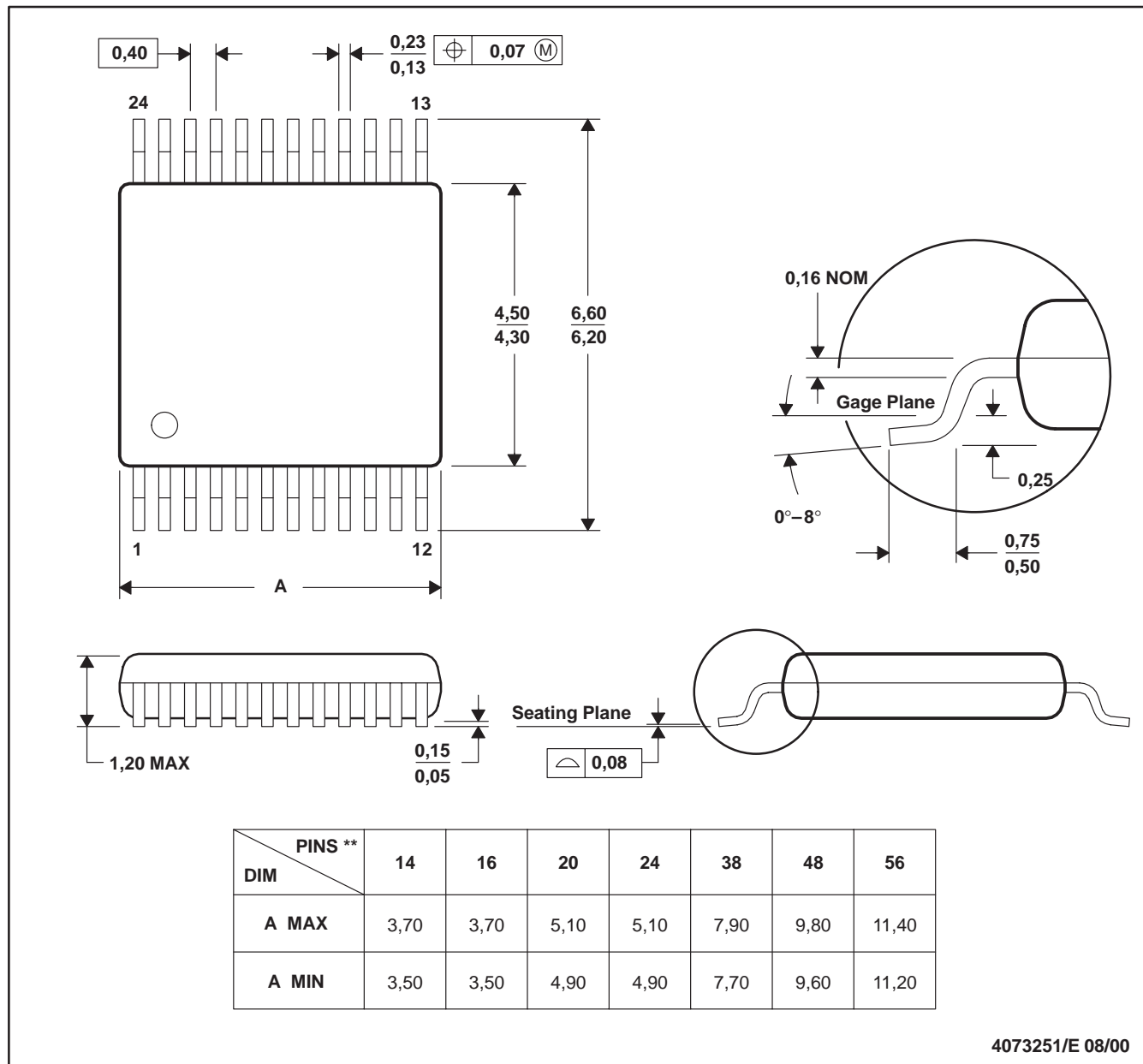
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
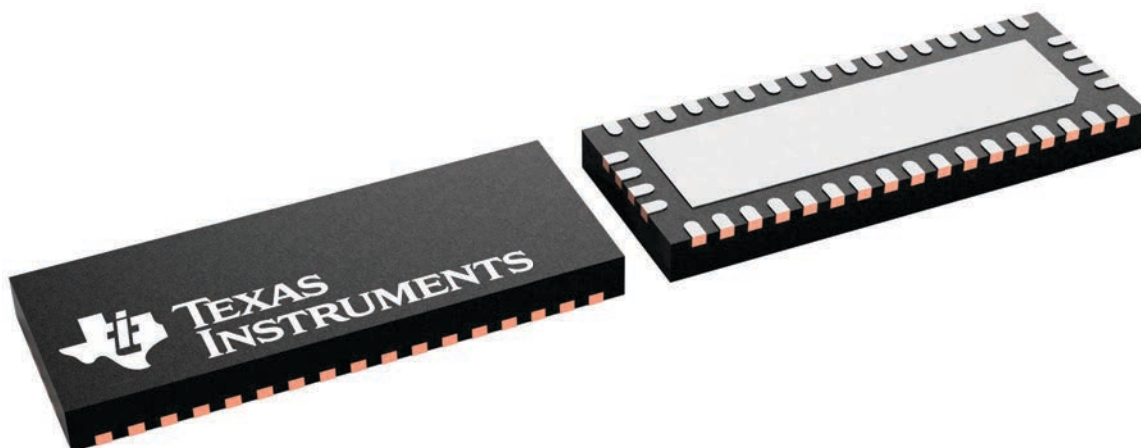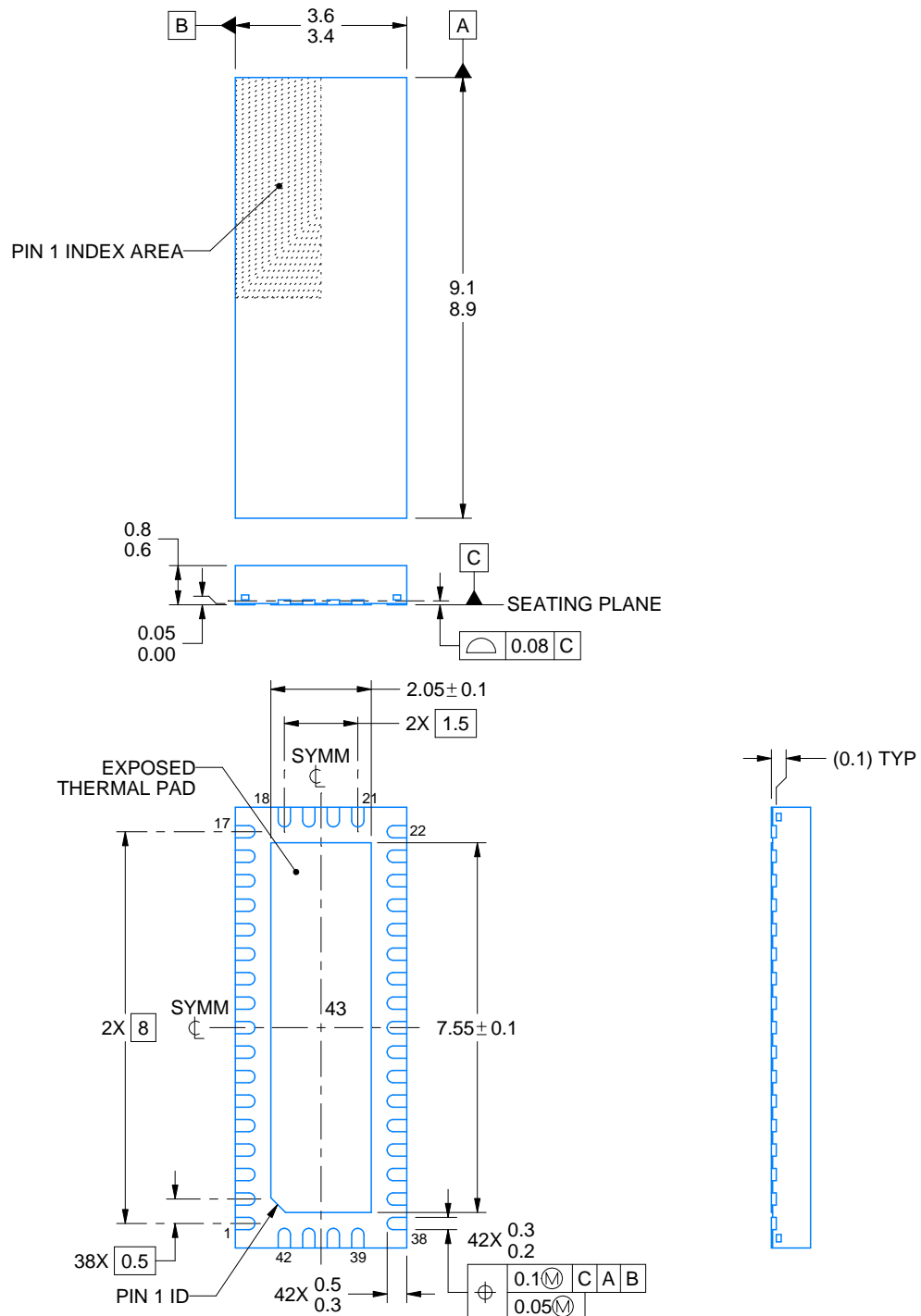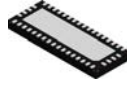14/16/20/56 Pins – MO-194

RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4226504/A

B | 3.6 / 3.4 | A

PIN 1 INDEX AREA

9.1 / 8.9

0.8 / 0.6

0.05 / 0.00

C

SEATING PLANE

$\boxed{0.08}$ C

2.05 ± 0.1

2X $\boxed{1.5}$

SYMM

EXPOSED THERMAL PAD

18   21

17   22

SYMM

2X $\boxed{8}$

43

7.55 ± 0.1

(0.1) TYP

1

38X $\boxed{0.5}$

PIN 1 ID

42   39

38

42X $\begin{array}{c}0.5\\0.3\end{array}$

42X $\begin{array}{c}0.3\\0.2\end{array}$
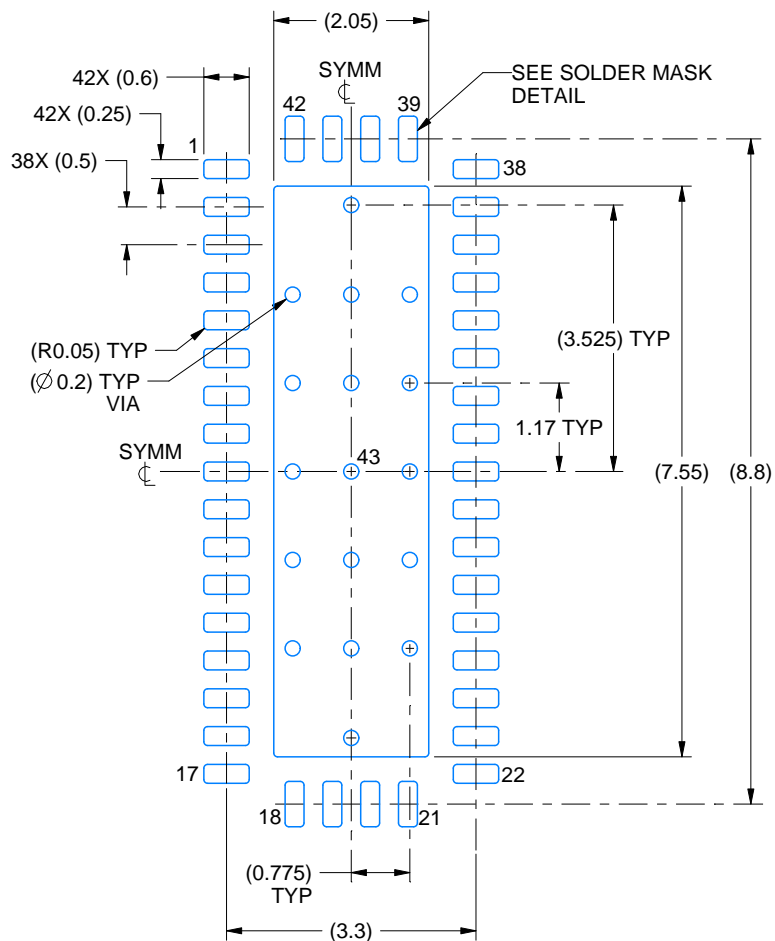
$\oplus$ | 0.1 Ⓜ | C | A | B
0.05 Ⓜ

4219139/A   03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
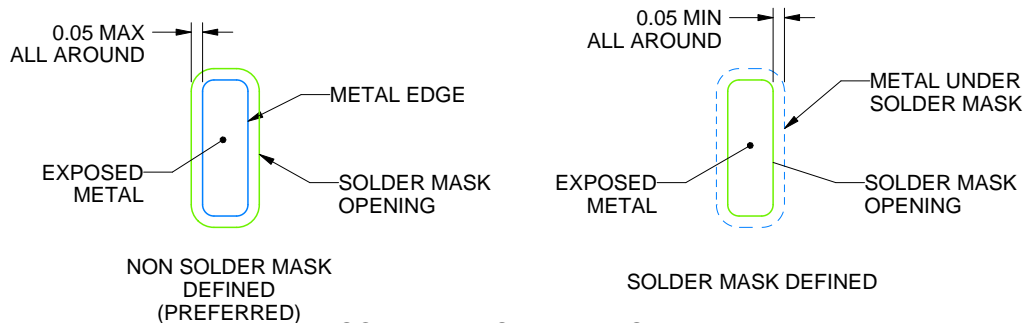
(2.05)

SYMM

42X (0.6)

42X (0.25)

38X (0.5)

SEE SOLDER MASK
DETAIL

42

39

1

38

(R0.05) TYP

(⌀ 0.2) TYP
VIA

(3.525) TYP

1.17 TYP

SYMM

43

(7.55)   (8.8)

17

22

18   21

(0.775)
TYP

(3.3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

0.05 MAX
ALL AROUND

METAL EDGE

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED

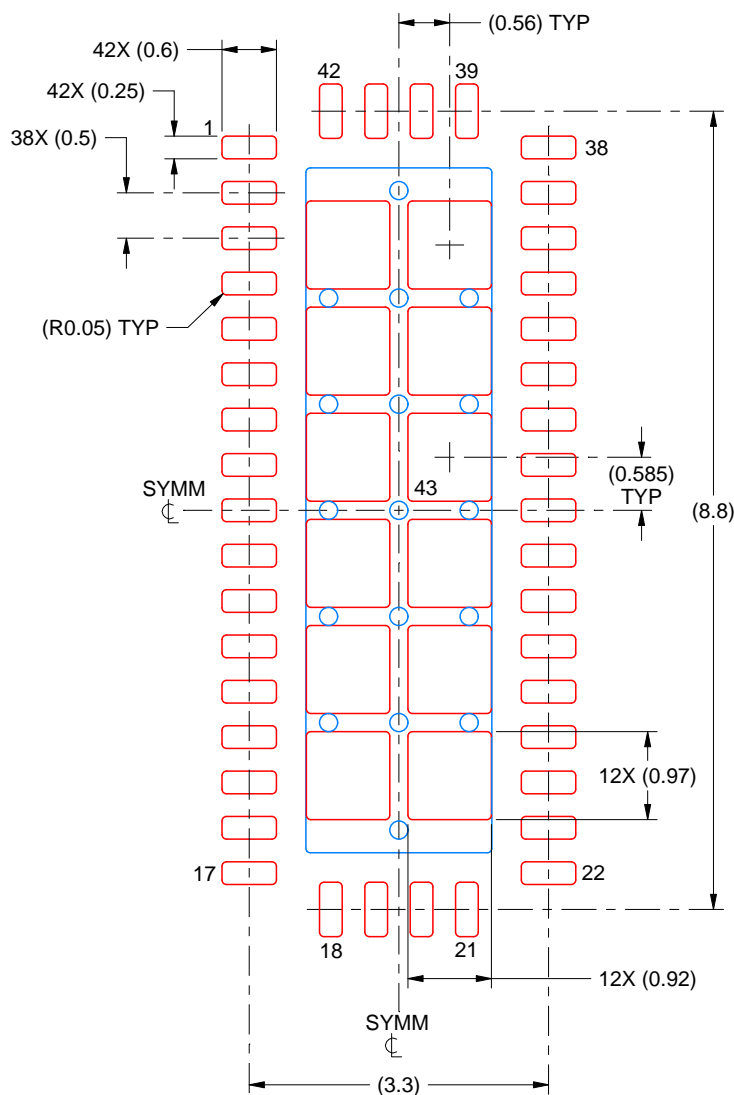SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

42X (0.6)

42X (0.25)

38X (0.5)

1

(0.56) TYP

42   39

38

(R0.05) TYP

SYMM

43

(0.585)
TYP

(8.8)

12X (0.97)

17   22

18   21

12X (0.92)

SYMM

(3.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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