

## 7-CHANNEL VIDEO SWITCH

Check for Samples: [TS3V712E](#)

### FEATURES

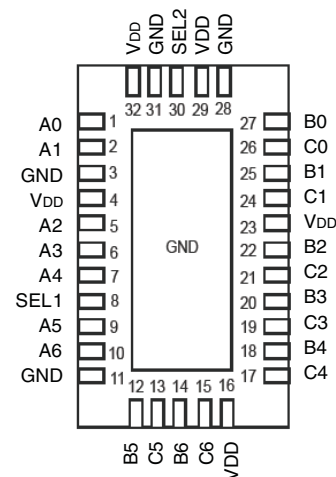
- High Bandwidth (BW = 1.36 GHz)
- Designed for 7-Channel VGA Signals (R,G,B, H<sub>sync</sub>, V<sub>sync</sub>, DDC Dat, and DDC CLK)
- Separate Control Logic for Data and Control Signals
- Operating Voltage: 3.3 V ±10%
- Low and Flat ON-State Resistance
  - $r_{ON} = 3 \Omega$
  - $r_{ON(flat)} = 500 \text{ m}\Omega$
- Low Crosstalk ( $X_{TALK} = -49.76 \text{ dB Typ at } 250 \text{ MHz}$ )
- Low Input/Output Capacitance
  - $C_{ON} = 7 \text{ pF, Typ}$
- ESD Performance Tested
  - 4-kV IEC61000-4-2, Contact Discharge on Switch IOs
  - 3-kV Human Body Model Per JESD22-A114E
  - 6-kV Human Body Model (Switch Pins to GND)
- Suitable for Both RGB and Composite-Video Switching

- 32-Pin Quad Flat Pack No-Lead QFN(RTG) Package

### APPLICATIONS

- Notebook Computers
- Analog VGA Peripheral Ports

RTG PACKAGE  
(TOP VIEW)



The exposed center pad must be connected to GND.

### DESCRIPTION/ORDERING INFORMATION

The TS3V712E is a high-bandwidth, 7-channel video multiplexer/demultiplexer for switching between multiple VGA sources or end points. The device is designed for ensuring video signal integrity and minimizing the video signal attenuation by providing high bandwidth of 1.36 GHz.

The video signals are protected against high ESD with integrated diodes to V<sub>DD</sub> and GND that will support up to 6-kV of ESD HBM and 4-kV contact protection.

The TS3V712E is available in a 32-pin QFN package and is characterized for operation over the free-air temperature range of –40°C to 85°C.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup> (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RTG	Tape and reel	TS3V712ERTGR	TF712E

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

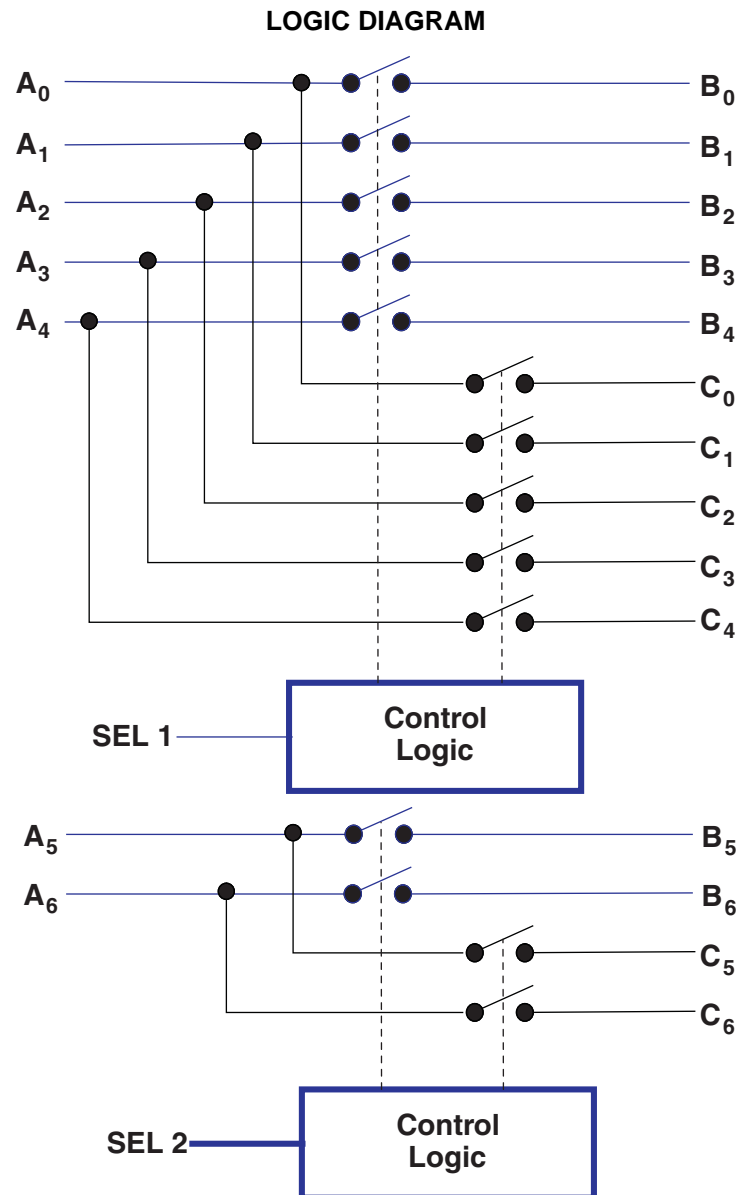


Table 1. FUNCTION TABLE

SEL1	SEL2	FUNCTION		
		A0–A4	A5, A6	Hi-Z
L	L	B0–B4	B5, B6	Cn
L	H	B0–B4	C5, C6	C0–C4, B5, B6
H	L	C0–C4	B5, B6	B0–B4, C5, C6
H	H	C0–C4	C5, C6	Bn

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage range		−0.5	4.6	V
V <sub>IN</sub>	Control input voltage range <sup>(2) (3)</sup>	SEL	−0.5	7	V
V <sub>I/O</sub>	Switch I/O voltage range <sup>(2) (3) (4)</sup>	All I/O ports	−0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0 V		−50	mA
I <sub>I/OK</sub>	I/O port clamp current	V <sub>I/O</sub> < 0 V		−50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>	ON-state switch		±128	mA
	Continuous current through V <sub>DD</sub> or GND			±100	mA
θ <sub>JA</sub>	Package thermal impedance	RTG package <sup>(6)</sup>		39.2	°C/W
T <sub>stg</sub>	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.
- (6) The package thermal impedance is calculated in accordance with JESD 51-5 (High K with via).

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage		3	3.6	V
V <sub>IN</sub>	Control input voltage (SEL)		0	5.5	V
V <sub>IH</sub>	High-level control input voltage (SEL)		2		V
V <sub>IL</sub>	Low-level control input voltage (EN, IN)		−0.5	0.8	V
V <sub>I/O</sub>	I/O voltage (all ports)		0	V <sub>DD</sub>	V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>DD</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

for high-frequency switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$	SEL n	$V_{DD} = 3.6 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$			-0.7	-1.2		V
$I_{IH}$	SEL n	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = V_{DD}$				$\pm 1$		$\mu\text{A}$
$I_{IL}$	SEL n	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = \text{GND}$				$\pm 1$		$\mu\text{A}$
$I_{OFF}$		$V_{DD} = 0 \text{ V}$ ,	$V_O = 0 \text{ to } 3.6 \text{ V}$ ,	$V_I = 0$ ,	$V_{IN} = 0$			1	$\mu\text{A}$
$I_{CC}$		$V_{DD} = 3.6 \text{ V}$ ,	$I_{IO} = 0$ ,	$V_{IN} = V_{DD}$ or GND,	Switch ON or OFF		200	500	$\mu\text{A}$
$C_{IN}$	SEL n	$f = 10 \text{ MHz}$	$V_{IN} = 0$ ,				2.7	3	pF
$C_{OFF}$	3 ports	$f = 10 \text{ MHz}$	$V_{IN} = 0$ ,	Output open,	Switch OFF		3	4	pF
$C_{ON}$	3 ports	$f = 10 \text{ MHz}$	$V_{IN} = 0$ ,	Output open,	Switch ON		7		pF
$r_{ON}$		$V_{DD} = 3 \text{ V}$ ,	$0 \text{ V} \leq V_I \leq 1.2 \text{ V}$ ,	$I_{IO} = -40 \text{ mA}$			3	4	$\Omega$
$r_{ON(\text{flat})}$ <sup>(3)</sup>		$V_{DD} = 3 \text{ V}$ ,	$V_I = 0 \text{ V and } 1.2 \text{ V}$	$I_{IO} = -40 \text{ mA}$			0.5	1	$\Omega$
$\Delta r_{ON}$ <sup>(4)</sup>		$V_{DD} = 3 \text{ V}$ ,	$0 \text{ V} \leq V_I \leq 1.2 \text{ V}$ ,	$I_{IO} = -40 \text{ mA}$			0.1	1	$\Omega$

(1)  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.

(2) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3)  $r_{ON(\text{flat})}$  is the difference of  $r_{ON}$  in a given channel at specified voltages.

(4)  $\Delta r_{ON}$  is the difference of  $r_{ON}$  from center port to any other ports.

## DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $R_L = 50 \Omega$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP <sup>(1)</sup>	UNIT
$X_{TALK}$	$R_L = 50 \Omega$ ,	$f = 250 \text{ MHz}$ ,	See <a href="#">Figure 7</a>	-49.76	dB
$O_{IRR}$	$R_L = 50 \Omega$ ,	$f = 250 \text{ MHz}$ ,	See <a href="#">Figure 8</a>	-37.51	dB
BW	See <a href="#">Figure 6</a>			1.36	GHz

(1) All typical values are at  $V_{CC} = 5 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $R_L = 50 \Omega$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted) (see [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
$t_{pd}$ <sup>(1)</sup>	An or Bn/Cn	Bn/Cn or An		0.25		ns
$t_{PZH}$ , $t_{PZL}$ <sup>(2)</sup>	SEL	Bn or Cn	0.5		12	ns
$t_{PHZ}$ , $t_{PLZ}$ <sup>(3)</sup>	SEL	Bn or Cn	0.5		11	ns
$t_{sk(o)}$ <sup>(4)</sup>	An, Bn, Cn			0.05	0.1	ns
$t_{sk(p)}$ <sup>(5)</sup>	An, Bn, Cn			0.05	0.1	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

(2) Line enable time: SEL to input, output; also called as SEL to switch turn on time.

(3) Line disable time: SEL to input, output; also called as SEL to switch turn off time.

(4) Output skew between center port to any other ports.

(5) Skew between opposite transitions of the same output.  $|t_{PHL} - t_{PLH}|$

### TYPICAL CHARACTERISTICS

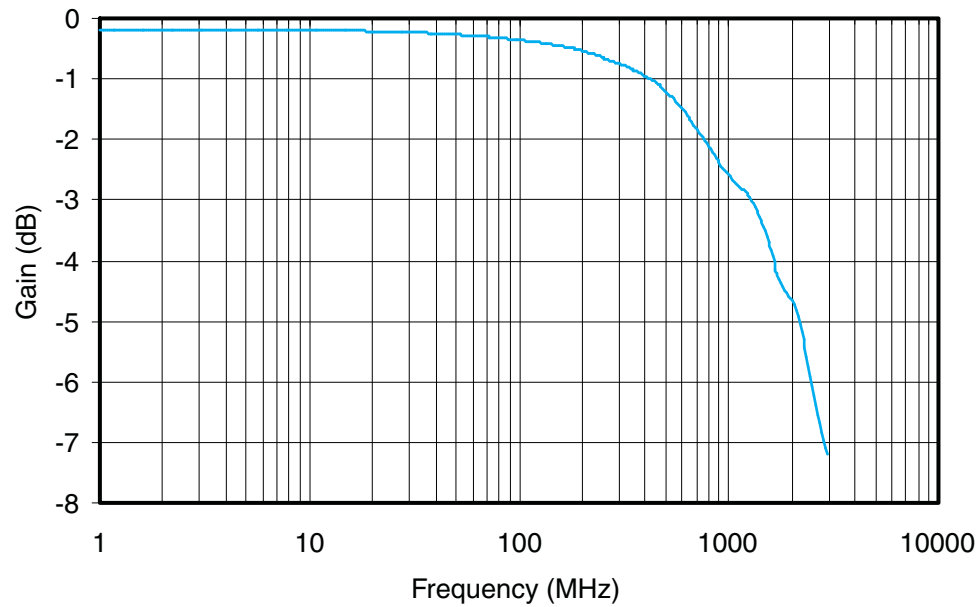


Figure 1. Gain vs Frequency

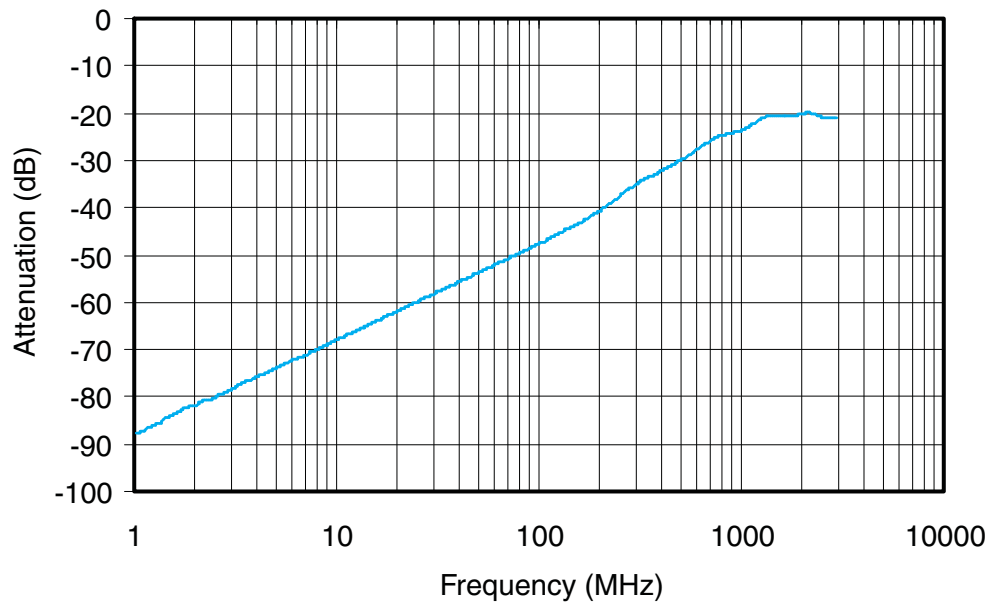


Figure 2. Off Isolation vs Frequency

## TYPICAL CHARACTERISTICS (continued)

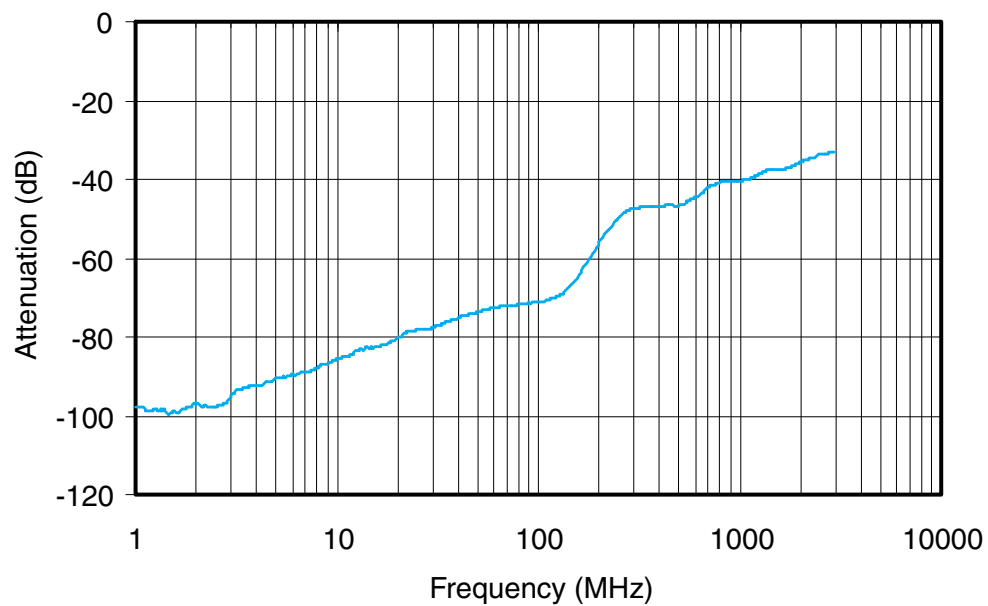
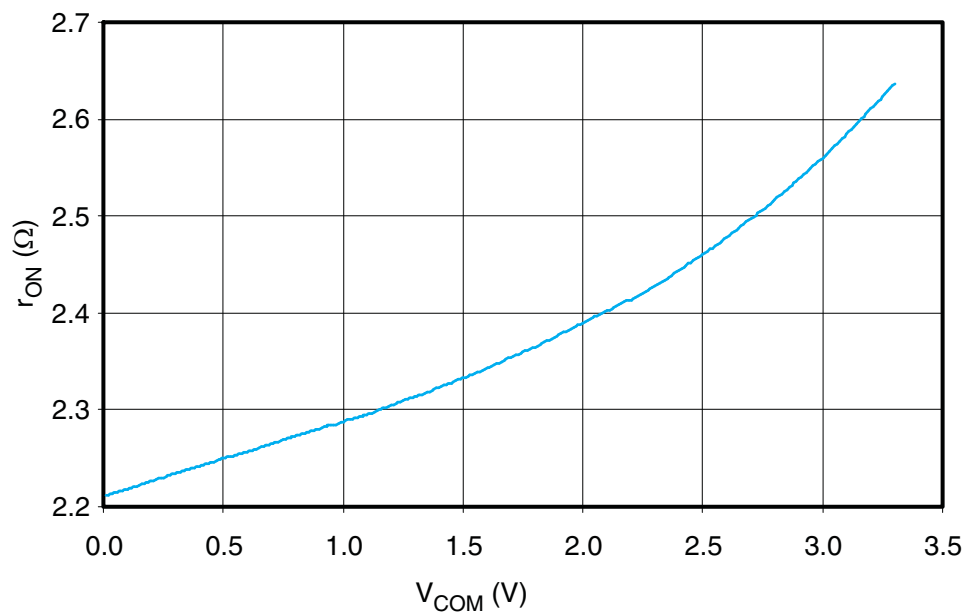
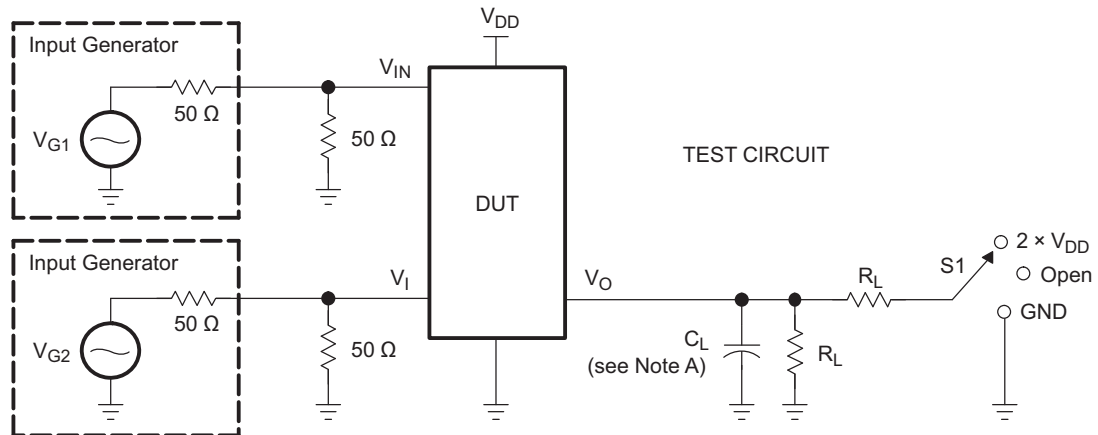


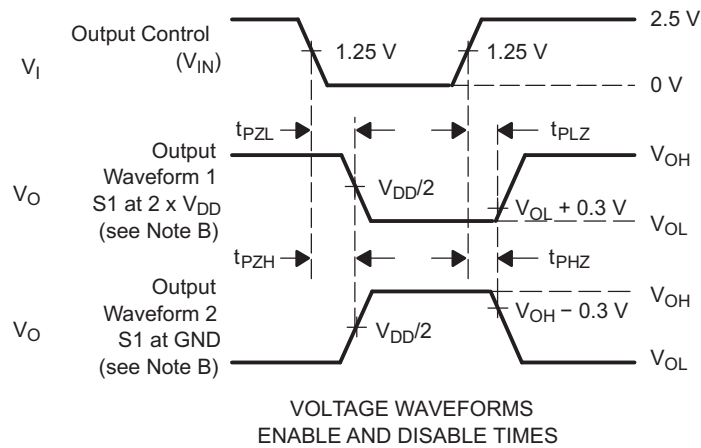
Figure 3. Crosstalk vs Frequency

Figure 4. . r<sub>ON</sub>(Ω) vs V<sub>COM</sub>(V)

## PARAMETER MEASUREMENT INFORMATION

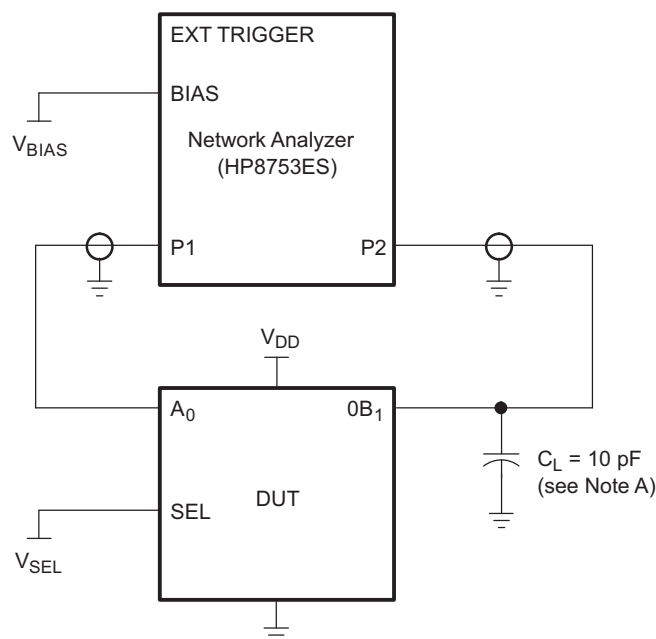


TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>in</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V	2 × V <sub>DD</sub>	200 Ω	GND	10 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V	GND	200 Ω	V <sub>DD</sub>	10 pF	0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
 F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

Figure 5. Test Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)****Figure 6. Test Circuit for Frequency Response (BW)**

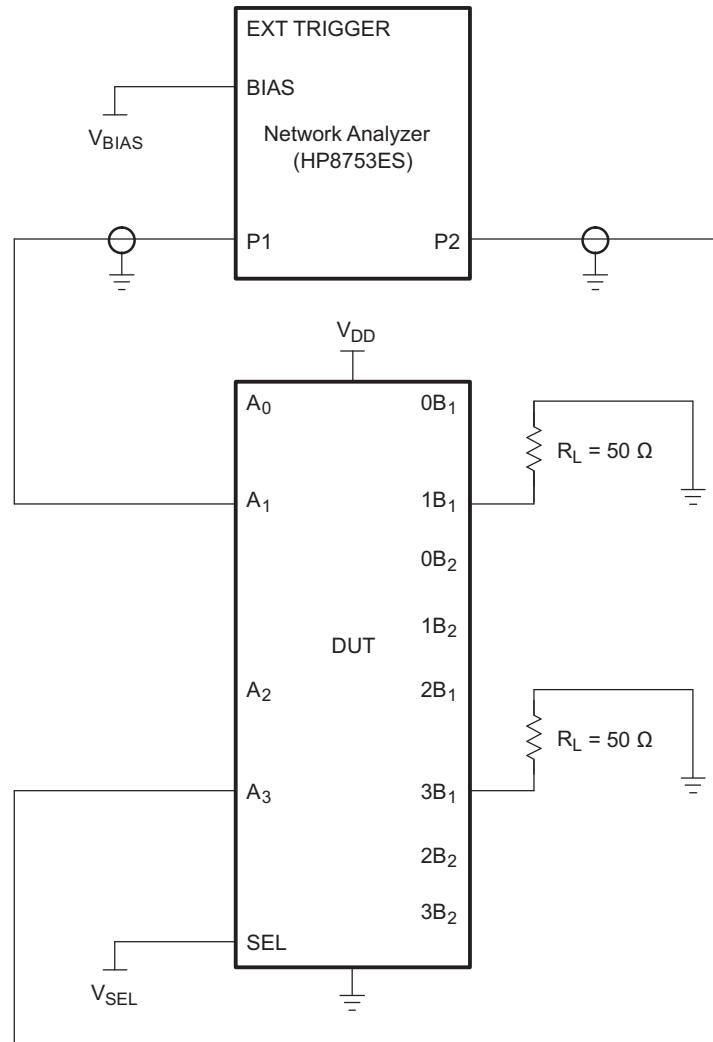
Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL} = 0$  and  $A_0$  is the input, the output is measured at  $0B1_1$ . All unused analog I/O ports are left open.

**HP8753ES Setup**

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35\text{ V}$   
 ST = 2 s  
 P1 = 0 dBm



## PARAMETER MEASUREMENT INFORMATION (continued)

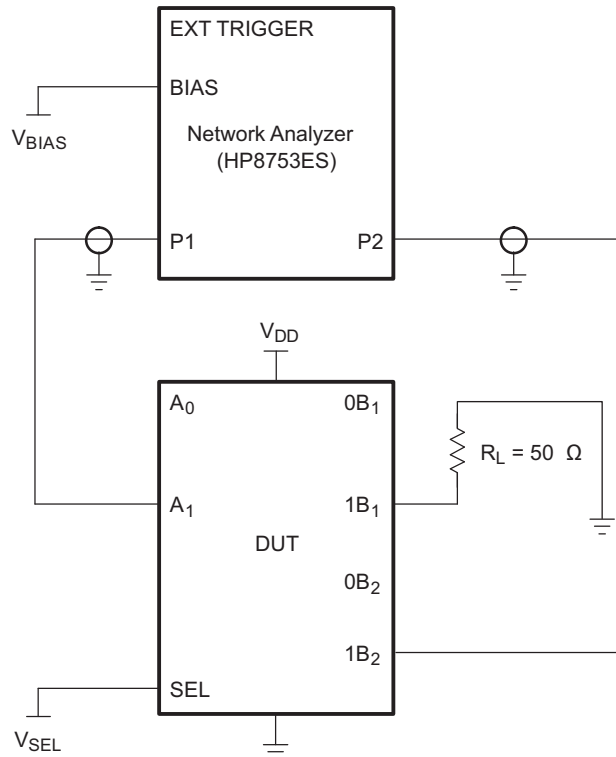


**Figure 7. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{IN} = 0$ ,  $V_{EN} = 0$ , and  $D_A$  is the input, the output is measured at  $S1_B$ . All unused analog input (D) ports and output (S) ports are connected to GND through 10- $\Omega$  and 50- $\Omega$  pulldown resistors, respectively.

### HP8753ES Setup

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

**PARAMETER MEASUREMENT INFORMATION (continued)****Figure 8. Test Circuit for Off Isolation ( $O_{IRR}$ )**

Off isolation is measured at the output of the OFF channel. For example, when  $V_{IN} = V_{CC}$ ,  $V_{EN} = 0$ , and  $D_A$  is the input, the output is measured at  $S1_A$ . All unused analog input (D) ports are left open, and output (S) ports are connected to GND through 50- $\Omega$  pulldown resistors.

**HP8753ES Setup**

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35\text{ V}$   
 ST = 2 s  
 P1 = 0 dBm

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TS3V712ERTGR</a>	Active	Production	WQFN (RTG)   32	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TF712E
TS3V712ERTGR.B	Active	Production	WQFN (RTG)   32	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TF712E
TS3V712ERTGRG4	Active	Production	WQFN (RTG)   32	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TF712E
TS3V712ERTGRG4.B	Active	Production	WQFN (RTG)   32	3000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TF712E

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3V712ERTGR	WQFN	RTG	32	3000	330.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1
TS3V712ERTGRG4	WQFN	RTG	32	3000	330.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



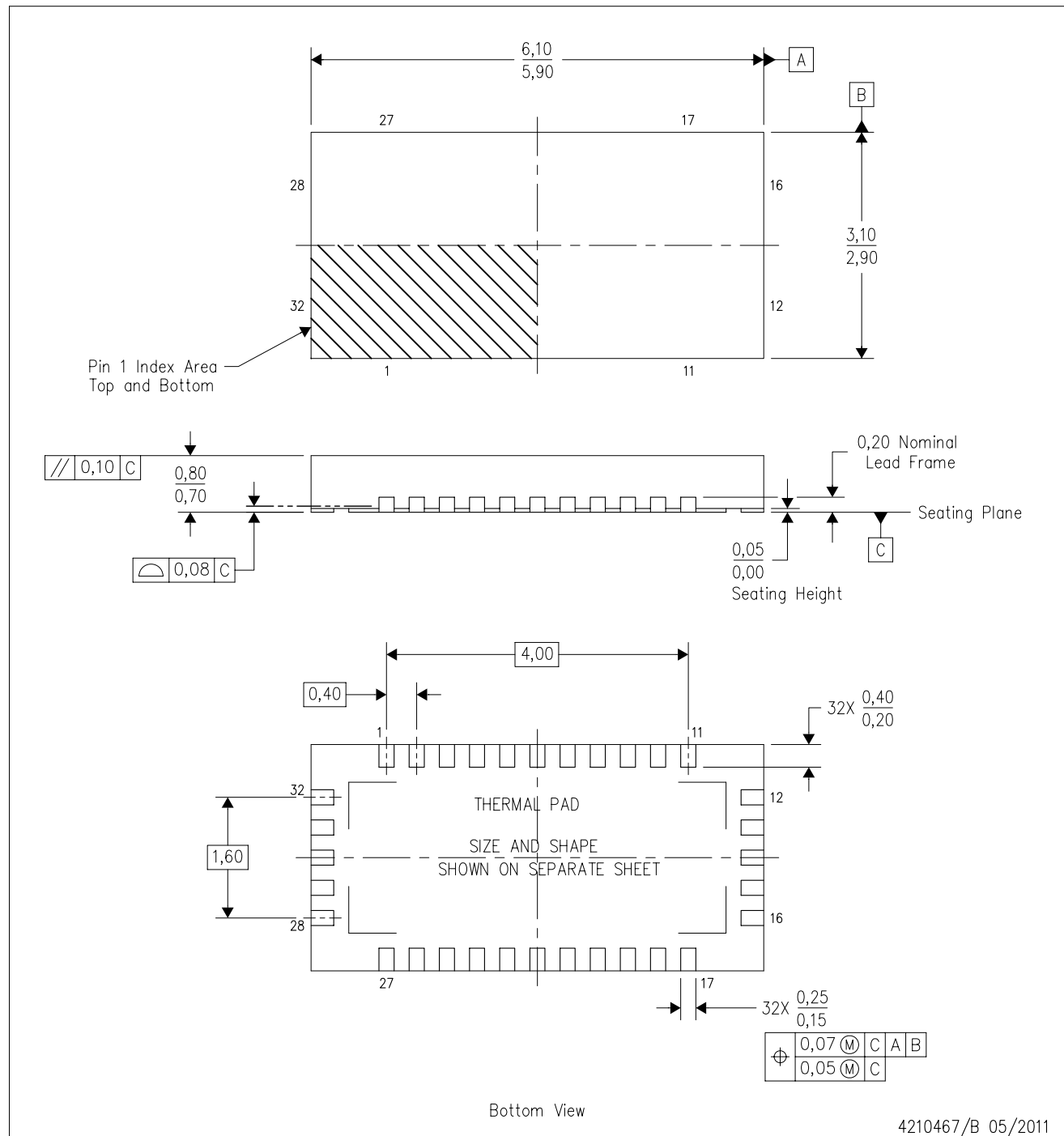
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3V712ERTGR	WQFN	RTG	32	3000	353.0	353.0	32.0
TS3V712ERTGRG4	WQFN	RTG	32	3000	353.0	353.0	32.0

# MECHANICAL DATA

RTG (R-PWQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Reference JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RTG (R-PWQFN-N32)

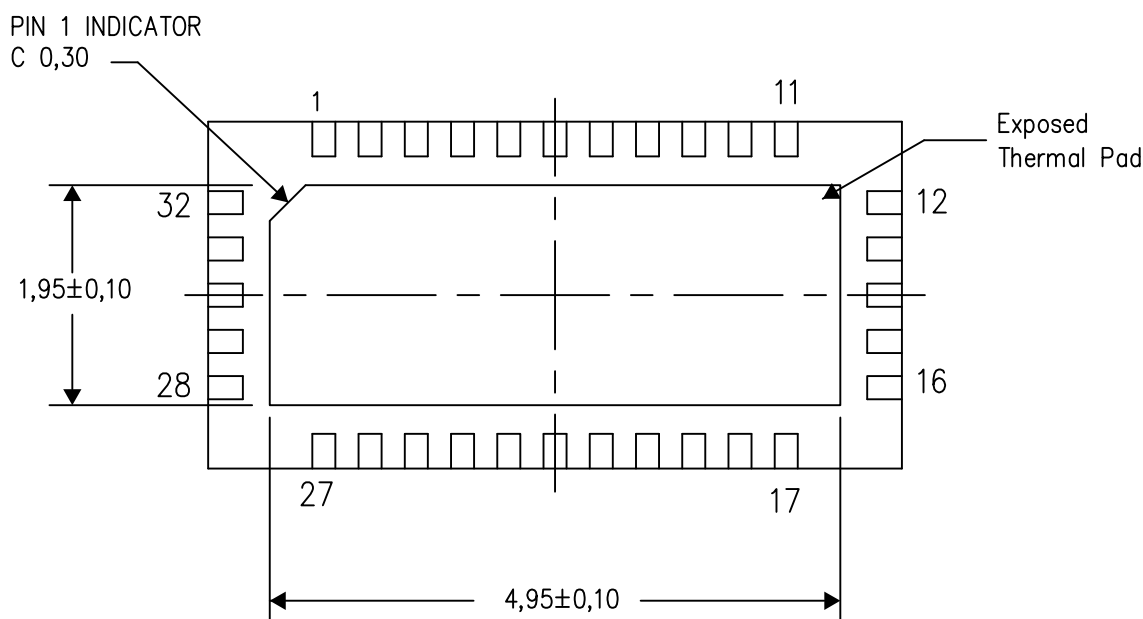
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

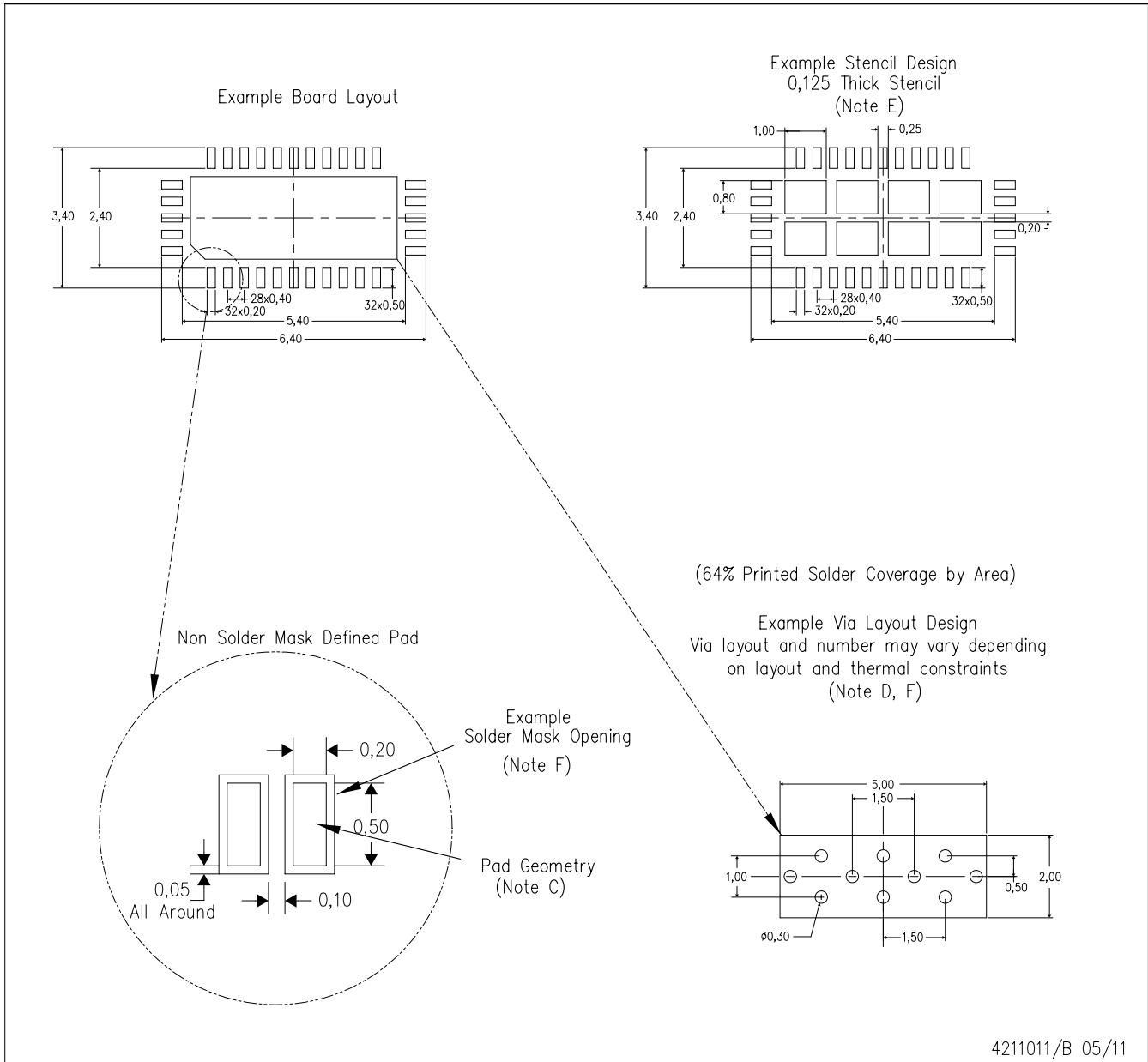
Exposed Thermal Pad Dimensions

4210534-2/D 12/13

NOTE: All linear dimensions are in millimeters

RTG (R-PWQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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