3.3-V IEEE 1394-1995 Backplane PHY

FEATURES

- **Provides a Backplane 1394 Environment That Supports an Asynchronous Transfer Rate of 50 or 100 Mbits/s Across 2 Etches**
- **Single 3.3-V Supply Operation With 5-V Tolerance on the Transceiver Receive Interface**
- **Allows Utilization of 3-State Drivers as Well as Open-Collector Drivers**
- **Software Compatible With the TSB14CO1APM**
- **Enhanced Compatibility With the 1394 Cable Link Layer. Compatible With 1394–1995 and 1394a–2000 Link Layers; PHY/link Interface is 1394a Compliant[1]**
- **Supports Provisions of IEEE 1394–1995[2][3]**
- **Extensive Testability and Debug Functions Added. Expanded Register Set Including Automatic Saving of ID and Priority for Last Node Winning Arbitration**
- **100 MHz or 50 MHz Oscillator Provides Transmit, Receive Data, and Link Layer Controller (LLC) Clocks**
- **Logic Performs System Initialization Arbitration Functions. Encode And Decode Functions Included for Data-Strobe Bit Level Encoding. Incoming Data Resynchronized to Local Clock.**
- **Operates Over the Extended Temperature Ranges of 0°C to 70°C (no suffix), –40°C to 85°C (I suffix), and –40°C to 105°C (T suffix)**
- **Packaged in the Very Compact 48-Pin 7 x 7 x 1 mm PFB Package**

(1) IEEE Std 1394a–2000, *IEEE Standard for a High Performance Serial Bus – Amendment 1*

(2) IEEE Std 1394–1995, *IEEE Standard for a High Performance Serial Bus*

(3) Implements technology covered by one or more patents of Apple Computer, Inc. and ST Microelectronics.

DESCRIPTION

The TSB14AA1A (TSB14AA1A refers to all three devices: TSB14AA1A, TSB14AA1AI, and TSB14AA1AT) is the second-generation 1394 backplane physical layer device. It is recommended for use in all new designs instead of the first generation TSB14C01A. It provides the physical layer functions needed to implement a single port node in a backplane based 1394 network. The TSB14AA1A provides two pins for transmitting, two for receiving, and two pins to externally control the transceivers for data and strobe. In addition to supporting open-collector drivers, the TSB14AA1A can also support 3-state(1) (high-impedance) drivers. The TSB14AA1A is not designed to drive the backplane directly; this function must be provided externally. The TSB14AA1A is designed to interface with a link-layer controller (LLC), such as the TSB12LV01B, TSB12LV32, TSB12LV21B, etc.

The TSB14AA1A requires an external 98.304-MHz reference oscillator input for S100 asynchronous only operation or 49.152-MHz for S50 asynchronous only operation. Two clock select pins (CLK_SEL0, CLK_SEL1) select the speed mode for the TSB14AA1A. For S100 operation, the 98.304-MHz reference signal is internally divided to provide the 49.152-MHz system clock signals used to control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. For S50 operation, a 49.152-MHz reference signal is used. This reference signal is internally divided to provide the 24.576-MHz system clock signals for S50 operations.

During packet transmit, data bits to be transmitted are received from the LLC on two parallel paths and are latched internally in the TSB14AA1A in synchronization with the system clock. These bits are combined serially, encoded, and transmitted as the outbound data-strobe information stream. During transmit, the encoded data information is transmitted on TDATA, and the encoded strobe information is transmitted on TSTRB.

(1) 3-State means a driver may drive high, low, or may be placed in a high-impedance state

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During packet reception, the data information is received on RDATA and strobe information is received on RSTRB. The received data and strobe information is decoded to recover the received clock signal and the serial data bits, which are resynchronized to the local system clock. The serial data bits are split into two parallel streams and sent to the associated LLC. The PHY-Link interface has been made compliant to IEEE 1394a–2000 including timing and transfer of register 0 to the link-layer automatically after every 1394 bus reset.

The TSB14AA1A is a 3.3 V device that provides LVCMOS level outputs. The TSB14AA1A is an asynchronous only device.

NOTE:

This product is for high-volume applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSB14AA1AIPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-	TSB14AA1AI
TSB14AA1AIPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TSB14AA1AI
TSB14AA1AIPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TSB14AA1AI
TSB14AA1AIPFBG4.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TSB14AA1AI
TSB14AA1APFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TSB14AA1A
TSB14AA1APFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TSB14AA1A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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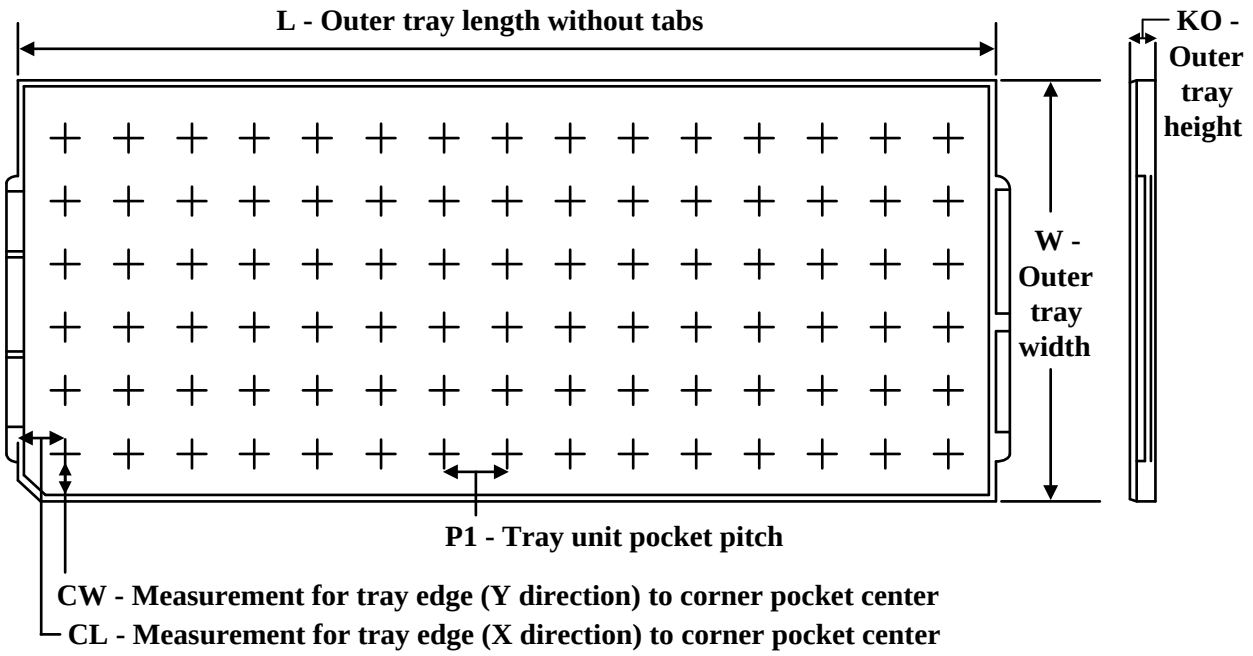
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

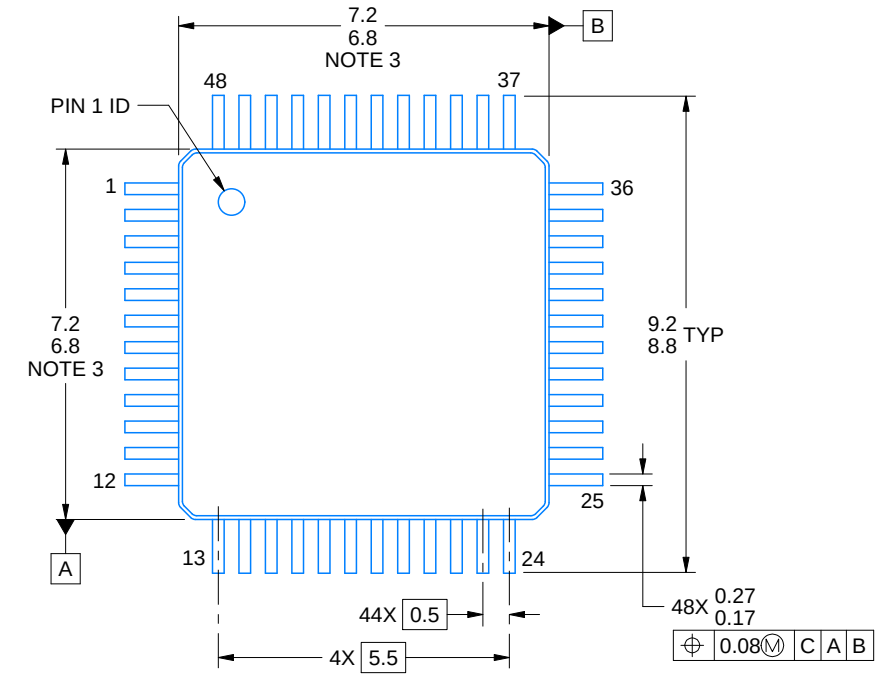
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TSB14AA1AIPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TSB14AA1AIPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TSB14AA1AIPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TSB14AA1AIPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TSB14AA1APFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TSB14AA1APFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

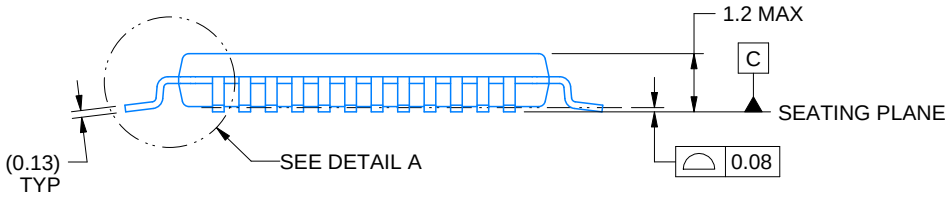
PACKAGE OUTLINE

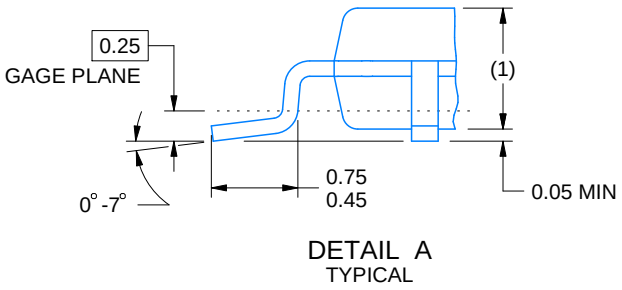
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK







DETAIL A
TYPICAL

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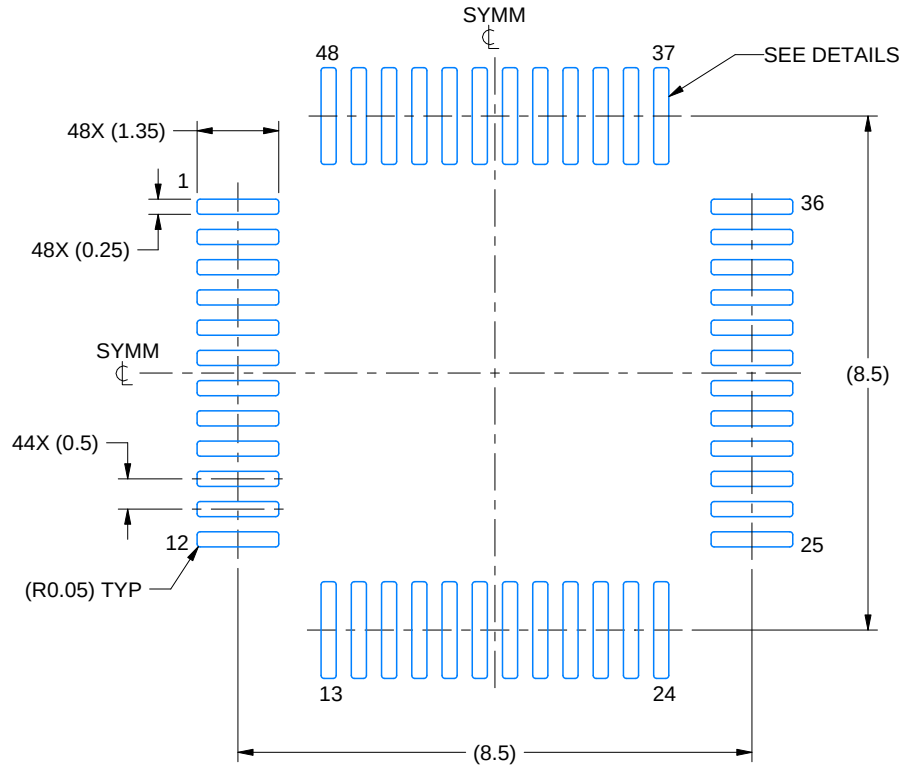
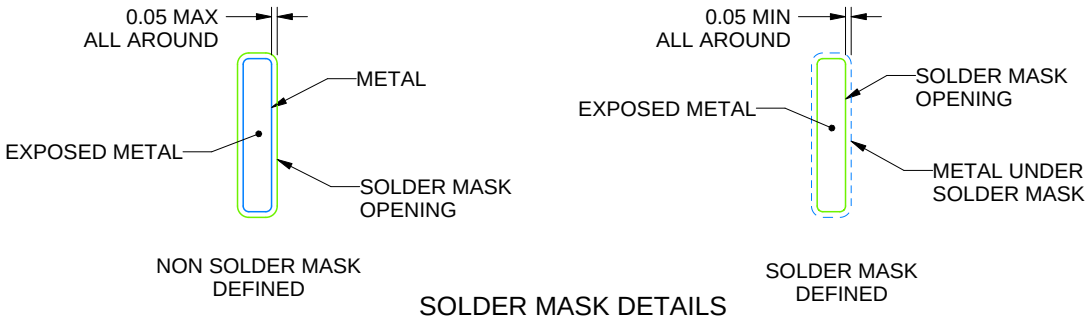
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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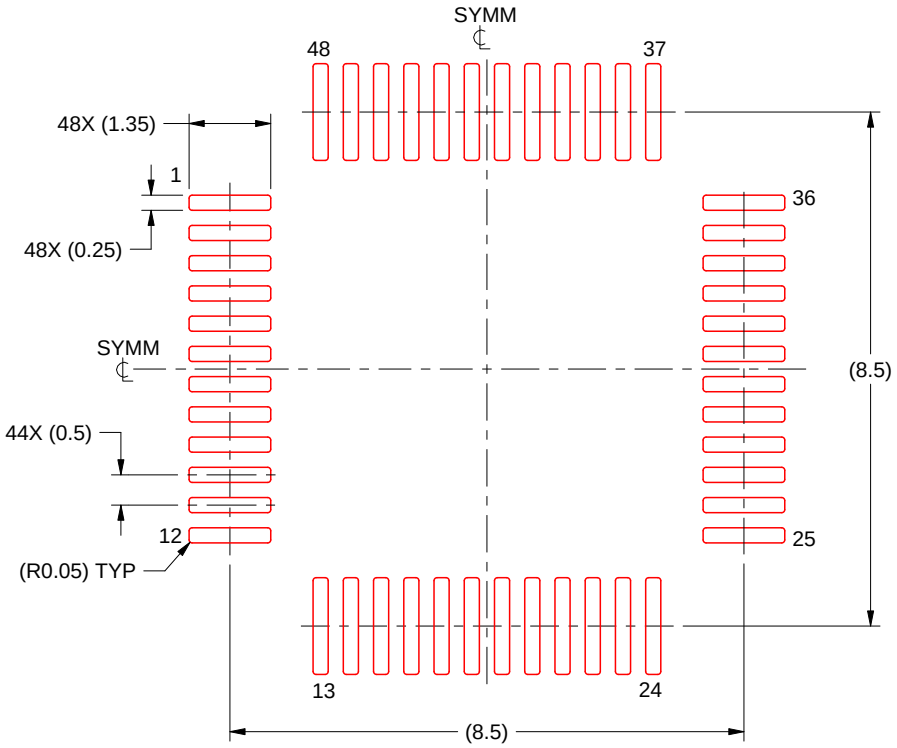
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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