TUSB212-Q1 USB 2.0 高速信号调节器

1 特性

- 符合汽车应用 要求：
  - 器件温度等级 2 级：环境工作温度范围为 –40°C 至 105°C
  - 器件 HBM 分类等级 H1C
  - 器件 CDM 分类等级 C3
- 与 USB 2.0、OTG 2.0 和 BC 1.2 兼容
- 引脚搭接或可通过 I^2C 进行配置
- 支持 LS、FS 和 HS 信号传输
- 超低 USB 断开和关断功耗
- 在高损耗应用中通过菊花链设备实现可选信号 增益
- D1P/M 和 D2P/M 可互换且主机/设备不可知
- 支持长达 5 米的通道前或 2 米的通道后电缆长度
  - 通过外部下拉电阻器实现四种可选交流升压设置
  - 直流升压与交流升压，可实现最佳信号完整性

2 应用

- 车用信息娱乐
- 笔记本电脑
- 台式机
- 扩展坞
- 平板电脑
- 手机
- 有源电缆、电缆扩展器
- 背板
- 电视

3 说明

TUSB212-Q1 是一款 USB 高速 (HS) 信号调节器，专为补偿传输通道中的 ISI 信号损失而设计。

TUSB212-Q1 采用了对 USB 低速 (LS) 和全速 (FS) 信号无感知的设计，该设计正在申请专利。LS 和 FS 信号特征不受 TUSB212-Q1 的影响，但该器件会对 HS 信号进行补偿。

借助可编程信号交流升压和直流升压，可精调器件性能，从而优化连接器上的高速信号。这有助于通过 USB 高速电气合规性测试。

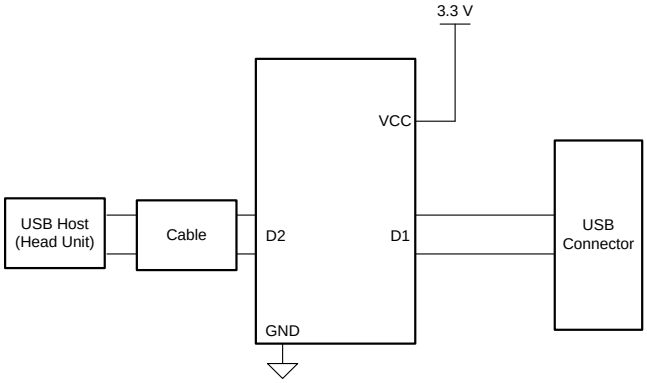
此外，TUSB212-Q1 符合 USB On-The-Go (OTG) 和电池充电 (BC) 协议。

器件信息 (1)

部件号	封装	封装尺寸（标称值）
TUSB212-Q1	X2QFN (12)	1.60mm x 1.60mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



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显示屏



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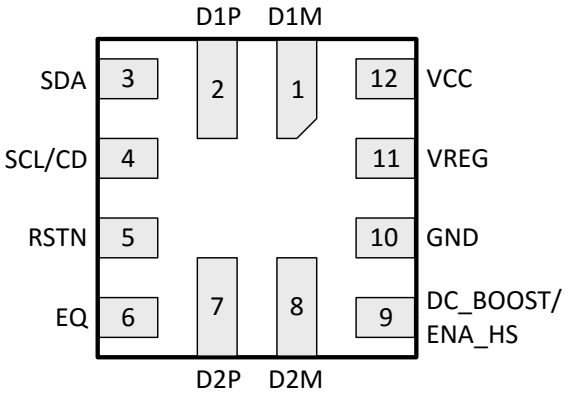
4 修订历史记录

日期	修订版本	注意
2017 年 8 月	*	初始发行版。

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5 Pin Configuration and Functions

RWB Package
12 Pin (X2QFN)
Top View



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
D1M	1	I/O	N/A	USB High Speed negative port..
D1P	2	I/O	N/A	USB High Speed positive port.
SDA(1)	3	I/O	RSTN asserted: 500 kΩ PD	I2C Mode: Bidirectional I2C data pin [I2C address = 0x2C]. In non I2C mode: Reserved for TI test purpose.
SCL(1)/CD	4	I/O	RSTN asserted: 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.
RSTN	5	I	500 kΩ PU	Device disable/enable. Low – Device is at reset and in shutdown, and High – Normal operation. Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
EQ	6	I	N/A	USB High Speed AC boost select via external pull down resistor. Sampled upon de-assertion of RSTN. Does not recognize real time adjustments. Auto selects max AC Boost when left floating.
D2P	7	I/O	N/A	USB High Speed positive port.
D2M	8	I/O	N/A	USB High Speed negative port.
DC_BOOST(2)/ ENA_HS	9	I/O		In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal DC_BOOST. USB High Speed DC signal boost selection. H (pin is pulled high) – 80 mV M (pin is left floating) – 60 mV L (pin is pulled low) – 40 mV After reset: Output signal ENA_HS. Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs].
GND	10	P	N/A	Ground
VREG	11	O	N/A	1.8-V LDO output. Only enabled when operating in High Speed mode. Requires 0.1-µF external capacitor to GND to stabilize the core.
VCC	12	P	N/A	Supply power

(1) Pull-up resistors for SDA and SCL pins in I^2C mode should be 2 kΩ (5%). If both SDA and SCL are pulled up at reset the device enters into I^2C mode.
(2) Pull-down and pull-up (to 3.3 V) resistors for DC_BOOST pins must be between 22 kΩ to 47 kΩ in non I^2C mode.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	VCC	-0.3	3.8	V
Voltage Range on I/O pins	DxP, DxM, RSTN, EQ, SCL, SDA, DC_BOOST, VREG	-0.3	3.8	V
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
T_A	Ambient temperature	TUSB212Q1	-40		105	°C
T_J	Junction temperature	TUSB212Q1	-40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		RWB (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High-speed active curent	USB channel = HS mode; 480 Mbps traffic; V_{CC} = 3.3V; V_{CC} supply stable; DC Boost = 60 mV		22	30	mA
I_{IDLE_HS}	High-speed idle current	USB channel = HS mode; no traffic; V_{CC} = 3.3V; V_{CC} supply stable; DC Boost = 60 mV		14	22	mA
$I_{SUSPEND_HS}$	High-speed suspend current	USB channel = HS suspend mode; V_{CC} = 3.3V; V_{CC} supply stable		0.55	1.5	mA
I_{FS_LS}	Full/Low speed current	USB channel = FS mode or LS mode; V_{CC} = 3.3V		0.6	1.5	mA
$I_{DISCONNECT}$	Disconnect current	Host side application; No device attachment; V_{CC} = 3.3V		0.7	1.5	mA
I_{RSTN}	Disable current	RSTN driven low; V_{CC} supply stable; V_{CC} = 3.3V		13	80	µA
I_{LKG_FS}	Pin fail-safe leakage current for SDA, SCL, DC_BOOST, DxP/N, RSTN	V_{CC} = 0 V; Pin at 3.6 V			40	µA
RSTN						
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{IH}	High-level input current	V_{IH} = 3.6 V	-4		4	µA
I_{IL}	Low-level input current	V_{IL} = 0 V	-11		11	µA
EQ						
R_{EQ}	External pull-down resistor on EQ pin.	AC Boost Level 0			160	Ω
		AC Boost Level 1	1.4		2	kΩ
		AC Boost Level 2	3.7		3.9	kΩ
		AC Boost Level 3	6			kΩ
CD, ENA_HS						
V_{OH}	High-level output voltage	I_O = -50µA	2.4			V
V_{OL}	Low-level output voltage	I_O = 50µA			0.4	V
SCL, SDA						
C_{I2CBUS}	I2C Bus capacitance		4		150	pF
DC_BOOST						
V_{IH}	High-level input voltage		2.4		3.6	V
V_{IM}	Mid-level input voltage			1.6		V
V_{IL}	Low-level input voltage		0		0.4	V
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with LCR meter and device powered down. 1 MHz sinusoid, 30 mVpp ripple		2.4		pF

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{BR_DXX}	DxP/M Bit Rate	USB channel = HS mode; 480 Mbps traffic; VCC supply stable			480.24	Mbps
t_{RISE_DXX}	DxP/M rise time		100			ps
t_{FALL_DXX}	DxP/M fall time		100			ps
$t_{RSTN_PULSE_WIDTH}$	Minimum width to detect a valid RSTN signal assert when the pin is actively driven	V_{CC} = 3.0 V; Refer to 图 1	20			µs
t_{STABLE}	VCC stable before RSTN de-assertion	Refer to 图 1	100			µs
t_{VCC_RAMP}	VCC ramp time		0.2		100	ms

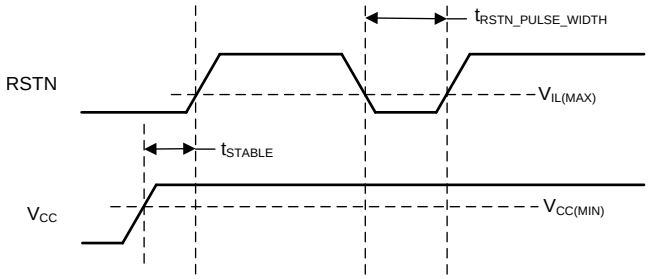


图 1. Power On and Reset Timing

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6.7 Typical Characteristics

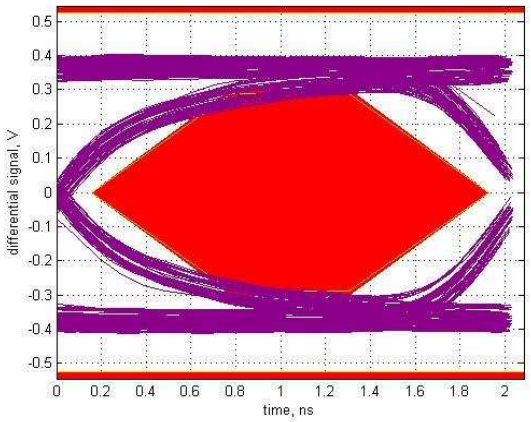


图 2. USB2.0 HS Eye Diagram, Host far-end with 2m cable post-channel loss without TUSB212-Q1

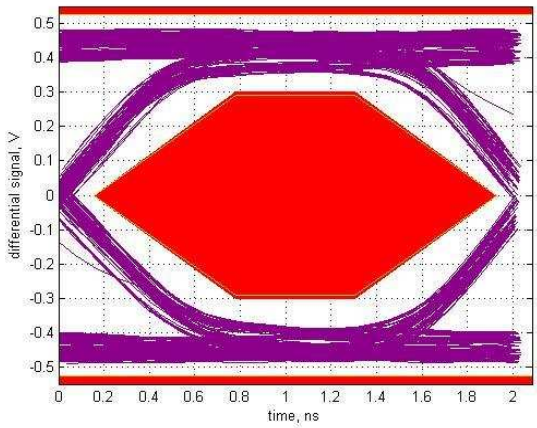


图 3. USB 2.0 HS Eye Diagram, Host far-end with 2m cable post-channel loss with TUSB212-Q1

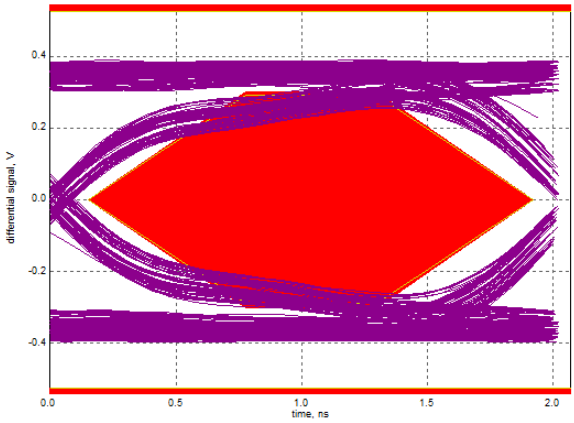


图 4. USB2.0 HS Eye Diagram, Host far-end with 5m cable pre-channel loss without TUSB212-Q1

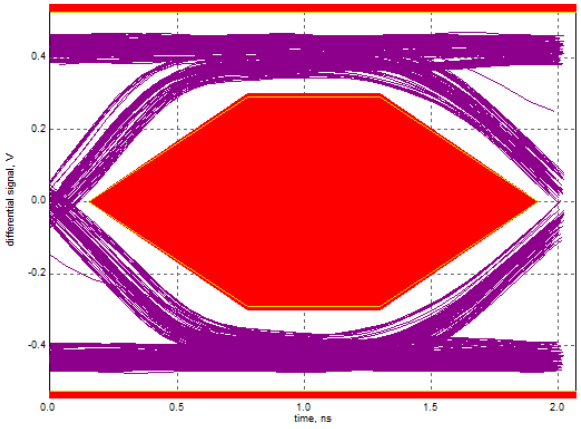


图 5. USB2.0 HS Eye Diagram, Host far-end with 5m cable pre-channel loss with TUSB212-Q1

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7 Detailed Description

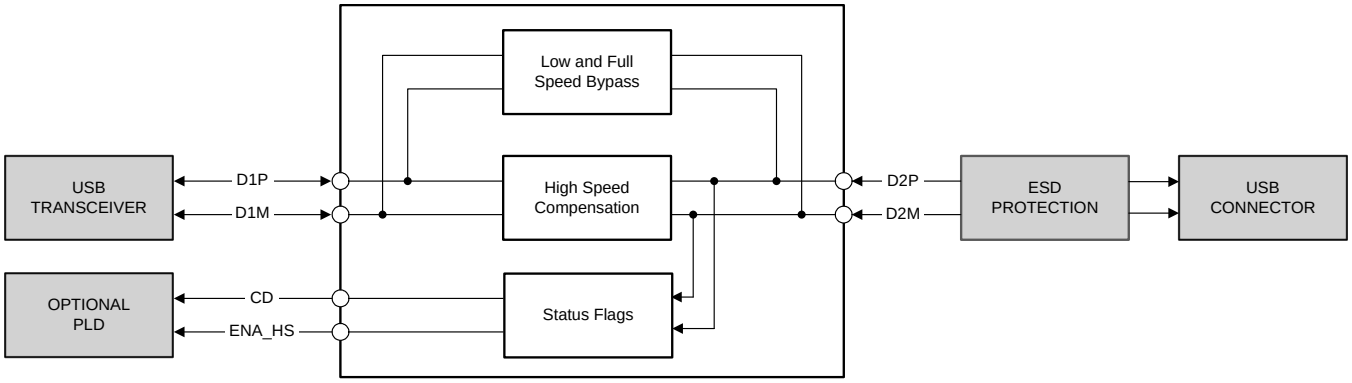
7.1 Overview

The TUSB212-Q1 is a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel. TUSB212-Q1 has a patent-pending design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals and does not alter their signal characteristics, while HS signals are compensated. In addition, the design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals helping to pass USB HS electrical compliance tests at the connector. Additional DC boost configurable by three level input DC_BOOST helps overcoming the cable losses.

The footprint of TUSB212-Q1 allows a board layout using this device such that it does not break the continuity of the DP/DM signal traces. This permits risk free system design of a complete USB channel with flexible use of one or multiple TUSB212-Q1 devices as needed for optimal signal integrity. This allows system designers to plan for this device and use it only if signal integrity analysis and/or lab measurements sow a need. If such a need is not warranted, the device can be left unpopulated without any board rework.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 EQ

The EQ pin of the TUSB212-Q1 is used to configure the AC boost of the device. The four levels are set through different values of an external pulldown resistor at this pin.

7.3.2 DC BOOST

The DC_BOOST pin of the TUSB212-Q1 is a tri-level pin, used to set the DC gain of the device according to 表 1.

表 1. DC Boost Settings

DC BOOST SETTING VIA PIN STRAP	
DC_BOOST	**DC Boost Setting (mV)**
V_{IL}	40
V_{IM}	60
V_{IH}	80

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7.4 Device Functional Modes

7.4.1 Low Speed (LS) Mode

TUSB212-Q1 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high.

7.4.2 Full Speed (FS) Mode

TUSB212-Q1 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high.

7.4.3 High Speed (HS) Mode

TUSB212-Q1 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the DC_BOOST pin and the external pulldown resistance on its EQ pin. CD pin is asserted high.

7.4.4 Shutdown Mode

TUSB212-Q1 is disabled when its RSTN pin is asserted low. In shutdown mode the USB channel is still fully operational, but there is neither signal compensation nor any indication from the CD pin as to the status of the channel.

7.4.5 I^2C Mode

TUSB212-Q1 supports 100 kHz I^2C for device configuration, status readback and test purposes. This controller is enabled after SCL and SDA pins are sampled high shortly after de-assertion of RSTN. In this mode, the register as described in 表 2 can be accessed by I^2C read/write transaction to 7-bit slave address 0x2C. It is necessary to set CFG_ACTIVE bit and reset it to zero after making changes to the EQ and DC Boost level registers to restart the state machine.

注

All registers or fields in 表 2 which are not specifically mentioned are considered reserved. The default value of these reserved registers or fields must not be changed. It is suggested to perform a read-modify-write operation to maintain the default value of the reserved fields.

表 2. Register definition

Offset	Bit(s)	Name	Type	Default	Description
0x01	6:4	ACB_LVL	RW	XXX (Sampled from EQ pin at reset)	Sets the level of AC Boost 000 : Level 0 AC Boost programmed [MIN] 001 : Level 1 AC Boost programmed 011 : Level 2 AC Boost programmed 111 : Level 3 AC Boost programmed [MAX]
0x03	0	CFG_ACTIVE	RW	1b	Configuration mode 0 : Normal mode. State machine enabled. 1 : Configuration mode: State machine disabled. After reset, if I2C mode is true (SCL and SDA are both pulled high) it is maintained until it is cleared by an I2C write, but, if I2C mode is not true, it is cleared automatically.
0x0E	2:0	DCB_LVL	RW	XXX (Sampled from DC_BOOST pin at reset)	Sets the level of DC Boost 011 : 40mV (DC_Boost = L) 101 : 60mV (DC_Boost = M, default) 111 : 80mV (DC_Boost = H)

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

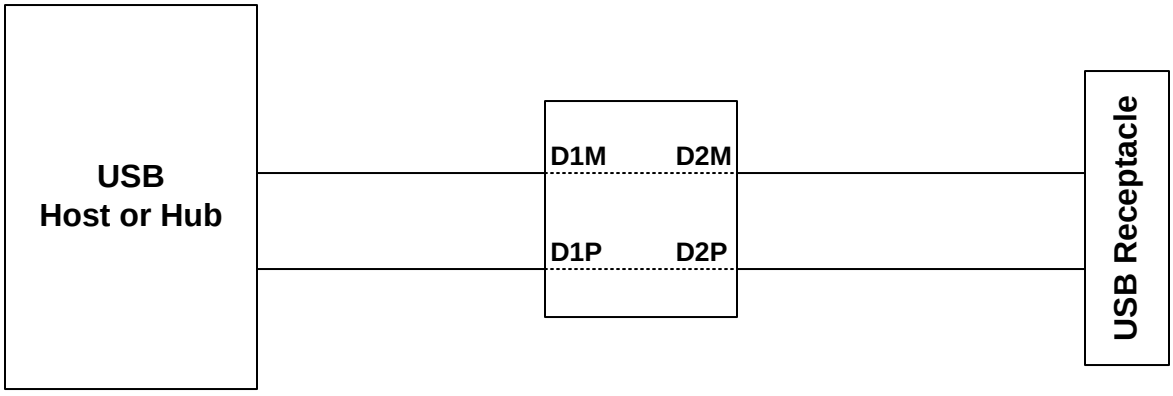
8.1 Application Information

The primary purpose of the TUSB212-Q1 is to re-store the signal integrity of a USB High Speed channel up to the USB receptacle. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB212-Q1 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB212-Q1 to control other blocks on the customer platform if so desired.

8.2 Typical Application

A typical application is shown in 图 6. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. If desired, the orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].



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图 6. Typical Application

8.2.1 Design Requirements

For this design example, use parameters shown in the table below.

表 3. Design Parameters

PARAMETER			VALUE
VCC (3.0V to 3.6V)			3.3V
I^2C support required in system (Yes/No)			No
AC Boost	R_{EQ}	Level	AC Boost Level 2: R_{EQ} = 3.83K
	0-ohms	0	
	1.69k +/- 1%	1	
	3.83k +/- 1%	2	
	DNI	3	

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Typical Application (接下页)

表 3. Design Parameters (接下页)

PARAMETER				VALUE
DC Boost	R_{DC1}	R_{DC2}	Level	Mid DC Level: R_{DC1} = DNI R_{DC2} = DNI
	22k - 47k ohms	Do Not Install (DNI)	40mV Low DC Boost	
	DNI	DNI	60mV Mid DC Boost	
	DNI	22k - 47k ohms	80mV High DC Boost	

8.2.2 Detailed Design Procedure

TUSB212-Q1 requires a valid reset signal as described in the power supply recommendations section. The capacitor at RSTN pin is not required if a microcontroller drives the RSTN pin according to recommendations.

VREG pin is the internal LDO output that requires a 0.1-μF external capacitor to GND to stabilize the core.

The ideal AC/DC Boost setting is dependent upon the signal chain loss characteristics of the target platform. The general recommendation is to start with AC Boost level 0, and then increment to AC Boost level 1, etc. when needed. Same applies to the DC boost setting where it is recommended to plan for the required pad to change boost settings.

In order for the TUSB212-Q1 to recognize any change to the AC or DC boost settings, the RSTN pin must be toggled. This is because the EQ and DC_BOOST pins are latched on power up and the pins are ignored thereafter.

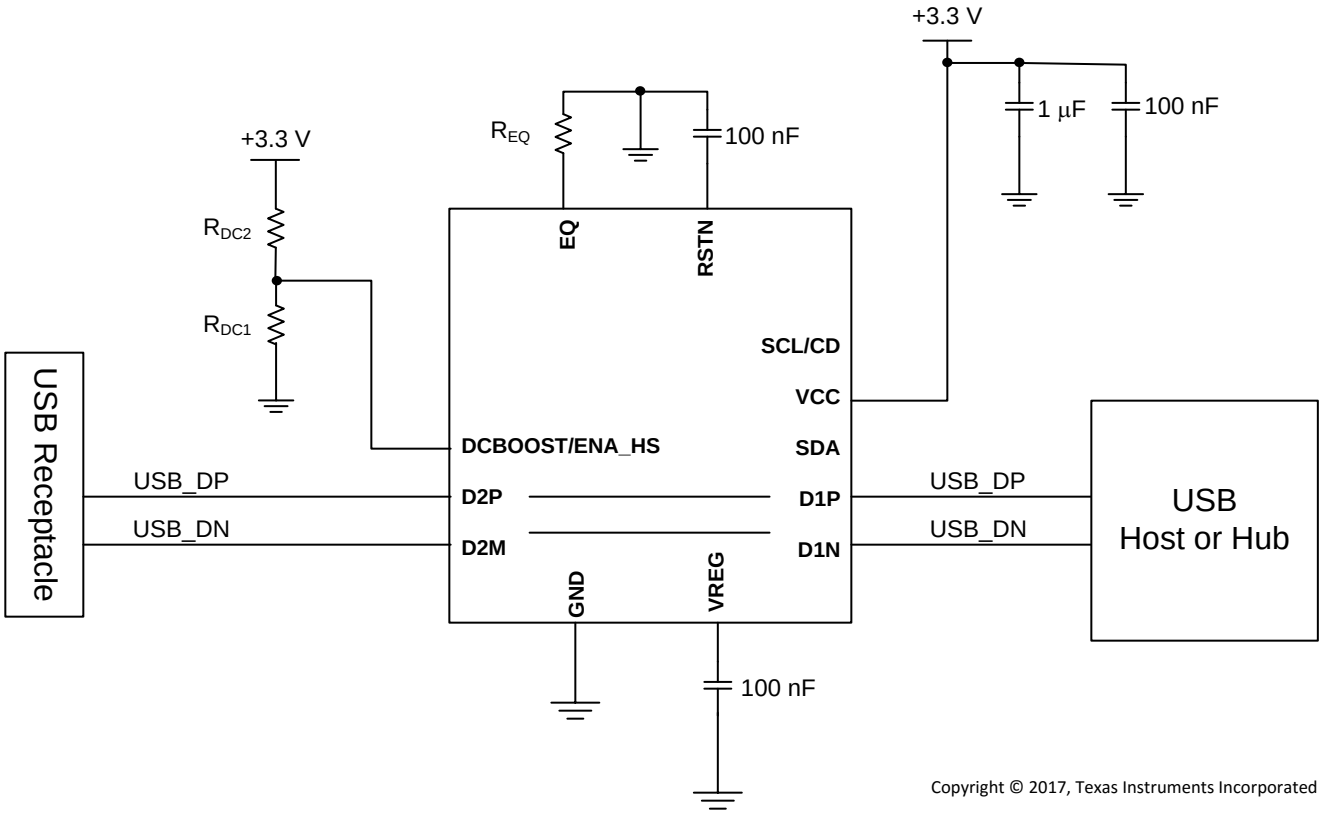
Further D1P has to be shorted to D2P and D1M shorted to D2M on the board for correct functionality of the device.

Placement of the device is also dependent on the application goal. 表 4 summarizes our recommendations.

表 4. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB212-Q1 PLACEMENT
Pass USB Near End Mask	Close to measurement point
Pass USB Far End Eye Mask	Close to USB PHY
Cascade multiple TUSB212-Q1 to improve device enumeration	Midway between each USB interconnect

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D2P must be shorted to D1P on PCB.

D2N must be shorted to D1N on PCB.

图 7. Reference Schematic

8.2.2.1 Test Procedure to Construct USB High Speed Eye Diagram

注

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the 'Electricals' section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB212-Q1 to the desired AC and DC boost settings.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB212-Q1
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB212-Q1
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB212-Q1 with different AC and DC boost settings.

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB212-Q1 to the desired AC and DC boost settings.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB212-Q1

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3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB212-Q1. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB212-Q1 with different AC and DC boost settings.

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8.2.3 Application Curves

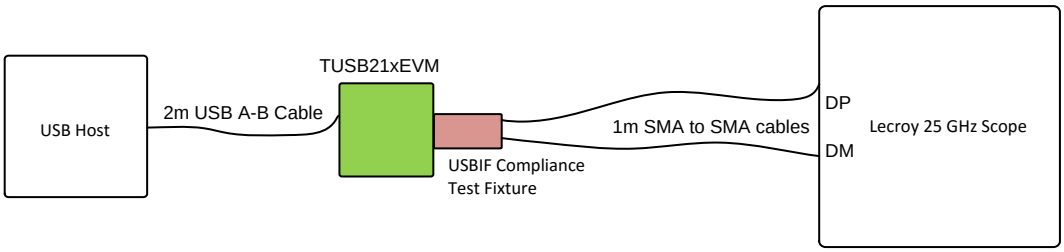


图 8. Eye Diagram Bench Setup

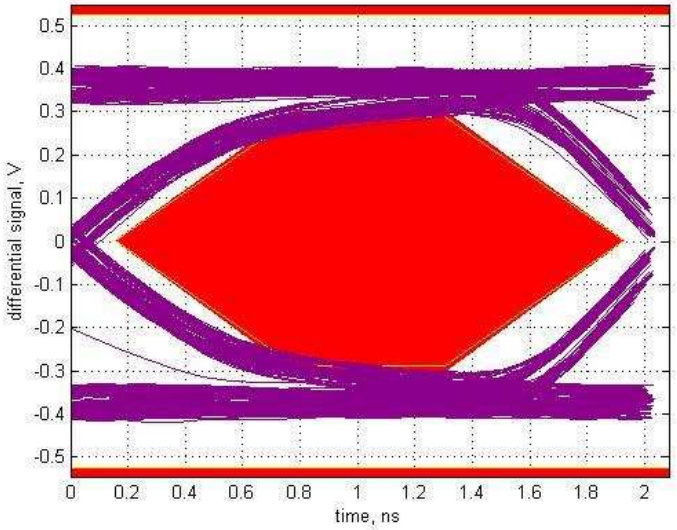


图 9. No TUSB212-Q1

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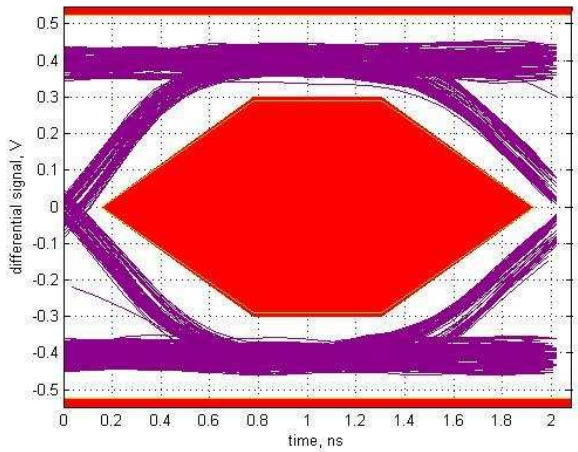


图 10. Low DC Boost, AC Boost Level 0

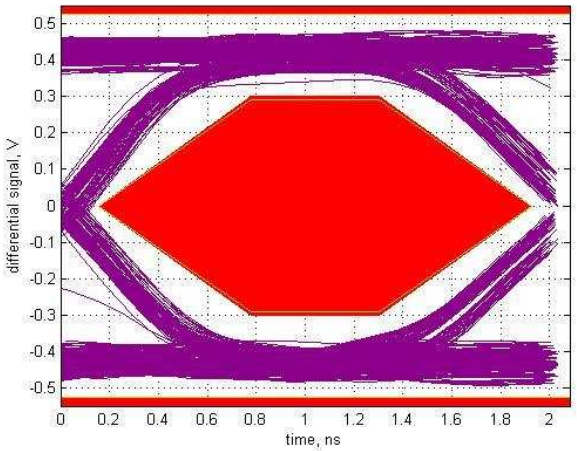


图 11. Mid DC Boost, AC Boost Level 0

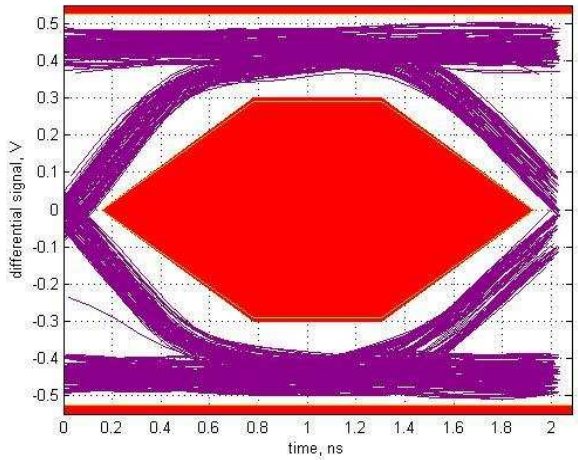


图 12. High DC Boost, AC Boost Level 0

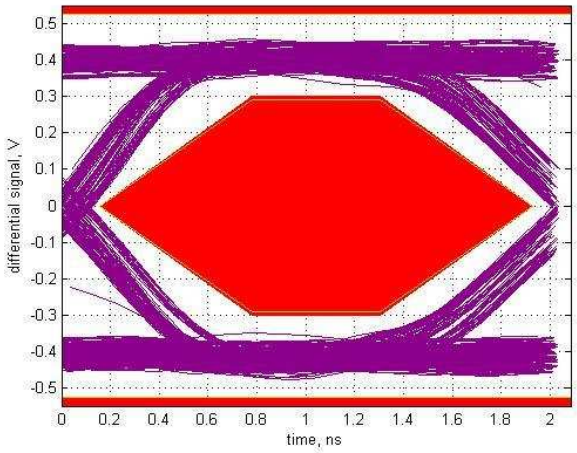


图 13. Low DC Boost, AC Boost Level 1

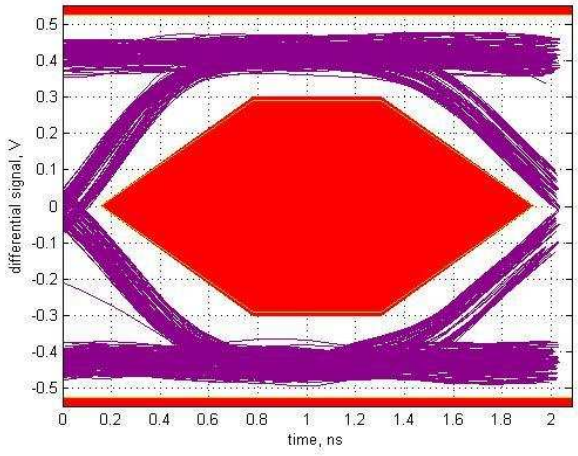


图 14. Mid DC Boost, AC Boost Level 1

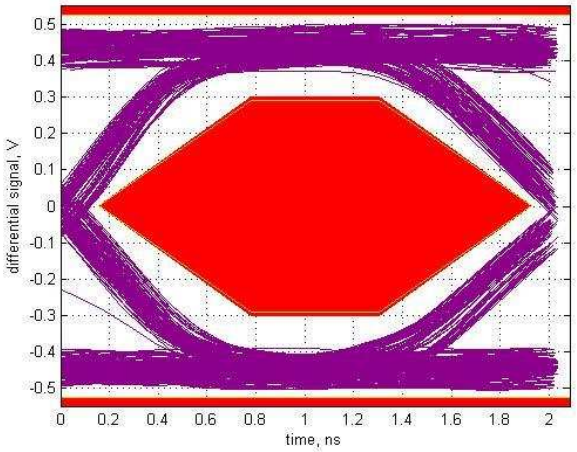


图 15. High DC Boost, AC Boost Level 1

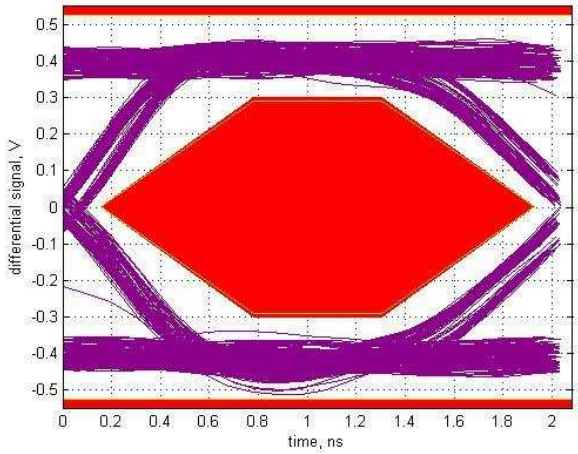


图 16. Low DC Boost, AC Boost Level 2

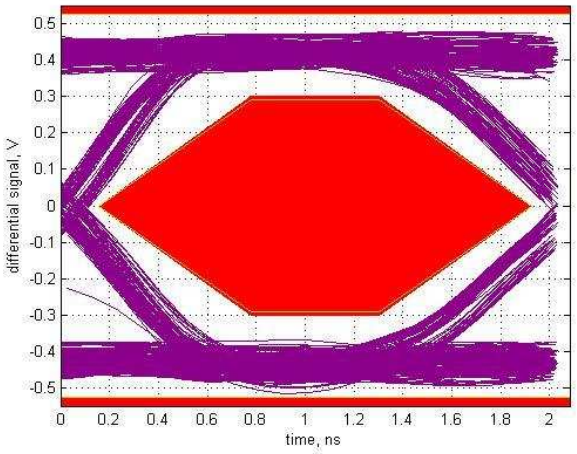


图 17. Mid DC Boost, AC Boost Level 2

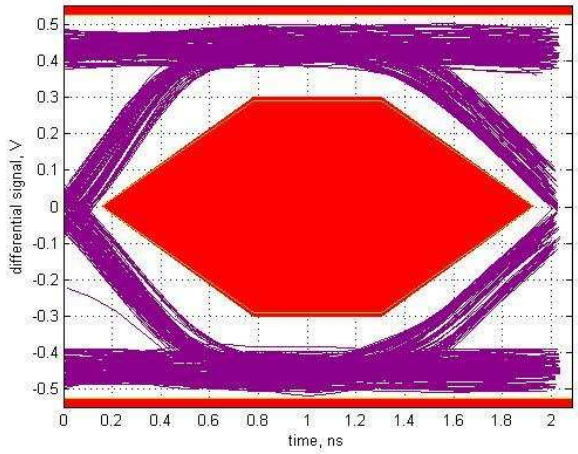


图 18. High DC Boost, AC Boost Level 2

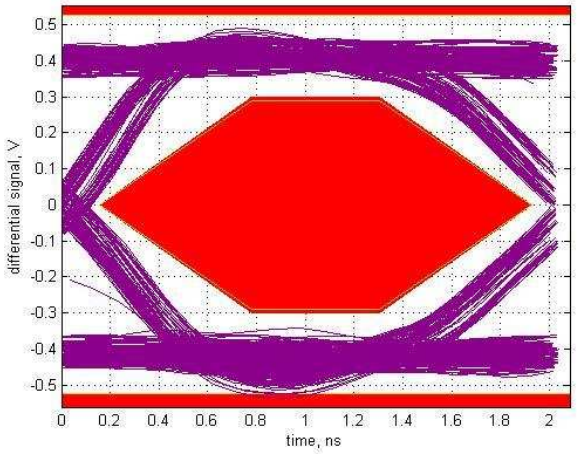


图 19. Low DC Boost, AC Boost Level 3

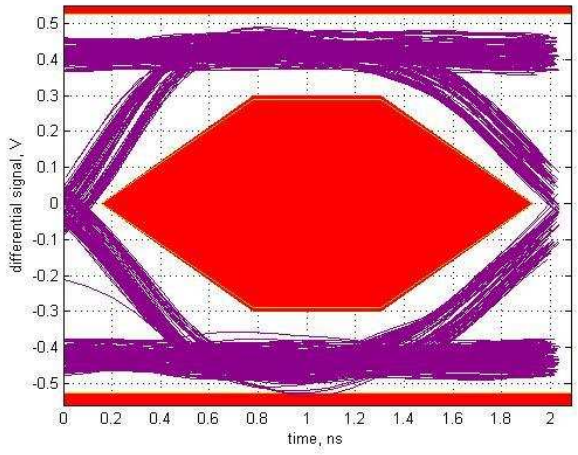


图 20. Mid DC Boost, AC Boost Level 3

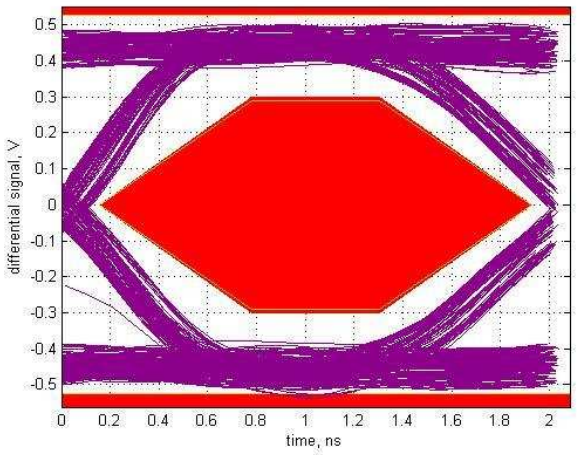


图 21. High DC Boost, AC Boost Level 3

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9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to 3 V or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

[Ramp Time x 5] ÷ [500 kΩ] (1)

10 Layout

10.1 Layout Guidelines

The USB signal trace must not be broken when placing TUSB212-Q1. Thus, even with the TUSB212-Q1 powered down, or not populated, the USB link is still fully operational. To avoid the need for signal vias, it is highly recommend to route the High Speed traces directly underneath the TUSB212-Q1 package, as illustrated in the PCB land pattern shown in 图 22.

Although the land pattern shown below has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. It is recommended to maintain 90 Ω differential routing underneath the device.

All dimensions are in millimetres (mm).

10.2 Layout Example

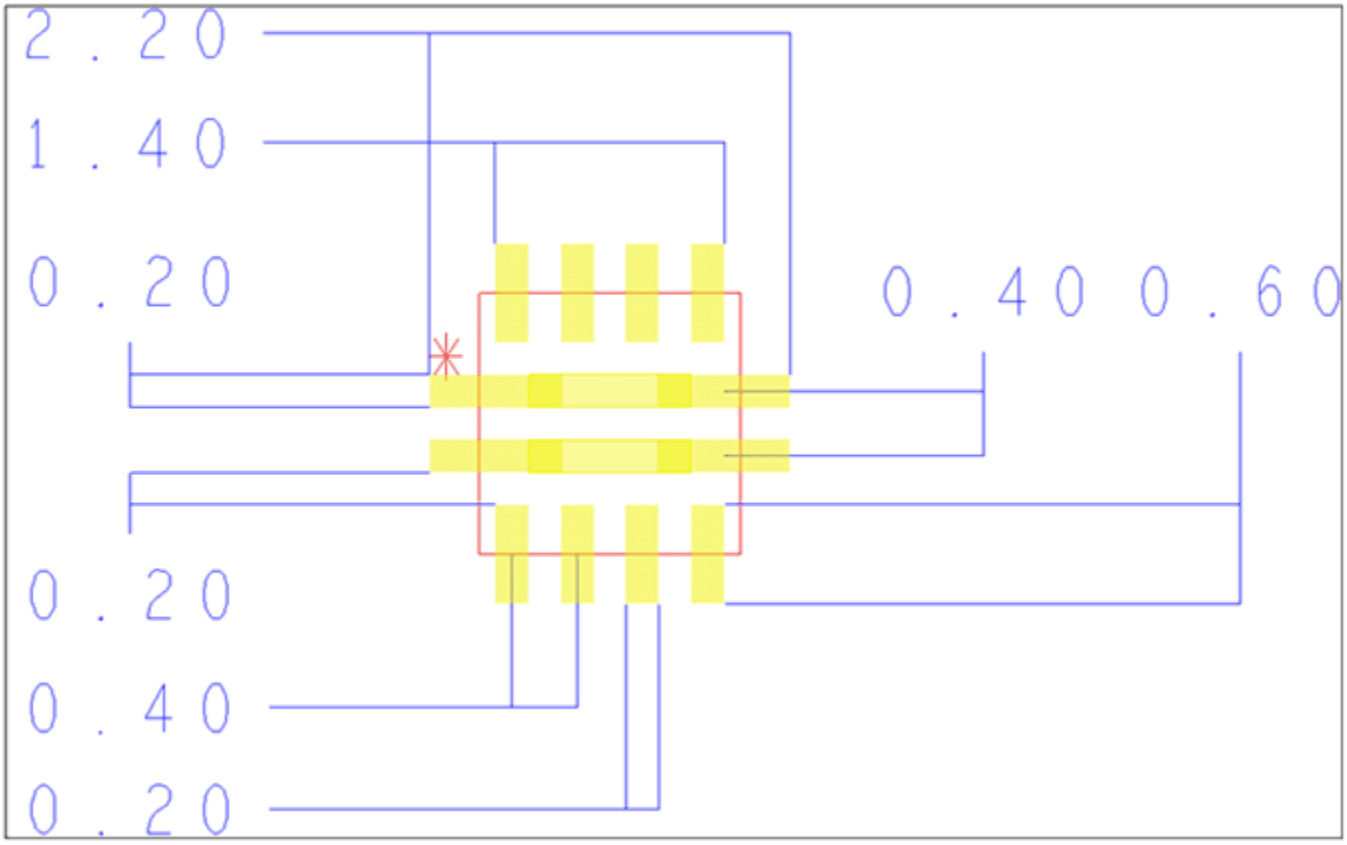


图 22. DP and DM Routing Underneath Device Package

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11 器件和文档支持

11.1 文档支持

11.2 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB212QRWBRQ1	Active	Production	X2QFN (RWB) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22
TUSB212QRWBRQ1.A	Active	Production	X2QFN (RWB) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22
TUSB212QRWBTQ1	Active	Production	X2QFN (RWB) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22
TUSB212QRWBTQ1.A	Active	Production	X2QFN (RWB) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TUSB212-Q1 :

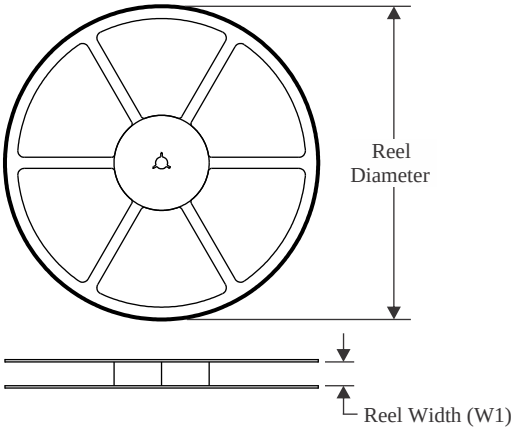
- Catalog : TUSB212

NOTE: Qualified Version Definitions:

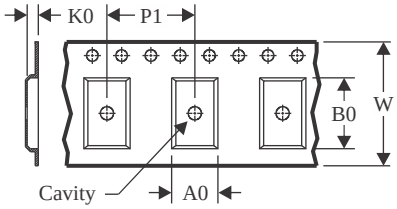
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

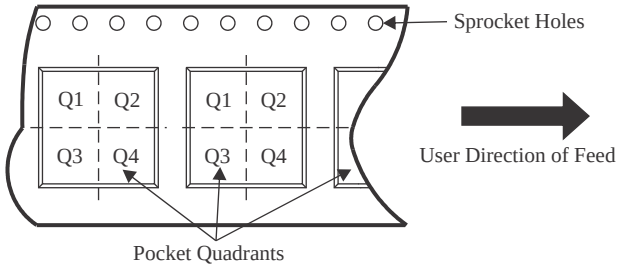


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

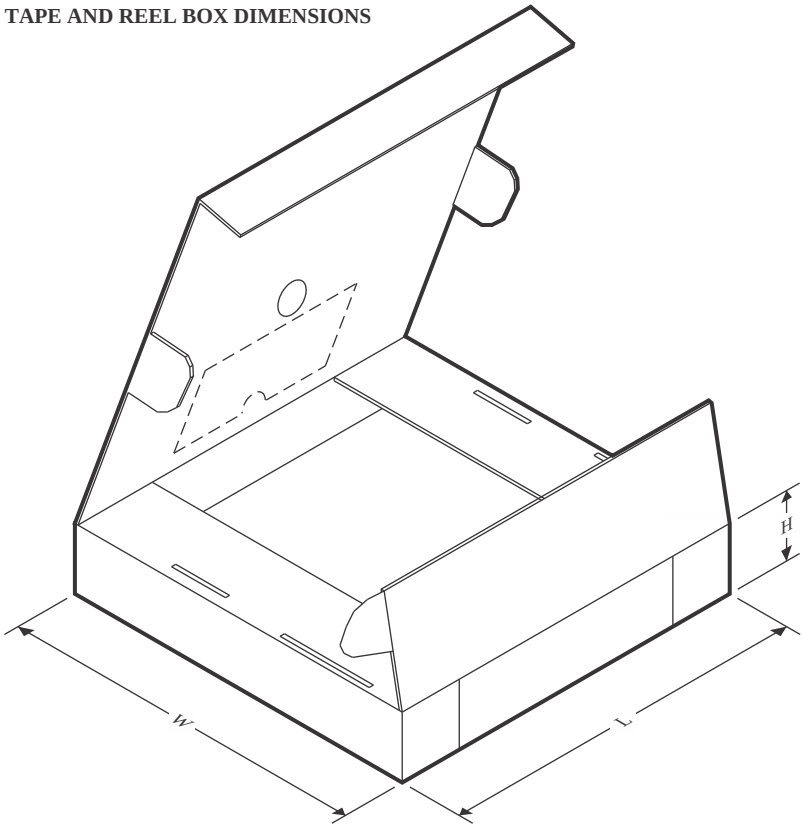
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB212QRWBRQ1	X2QFN	RWB	12	3000	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1
TUSB212QRWBTQ1	X2QFN	RWB	12	250	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

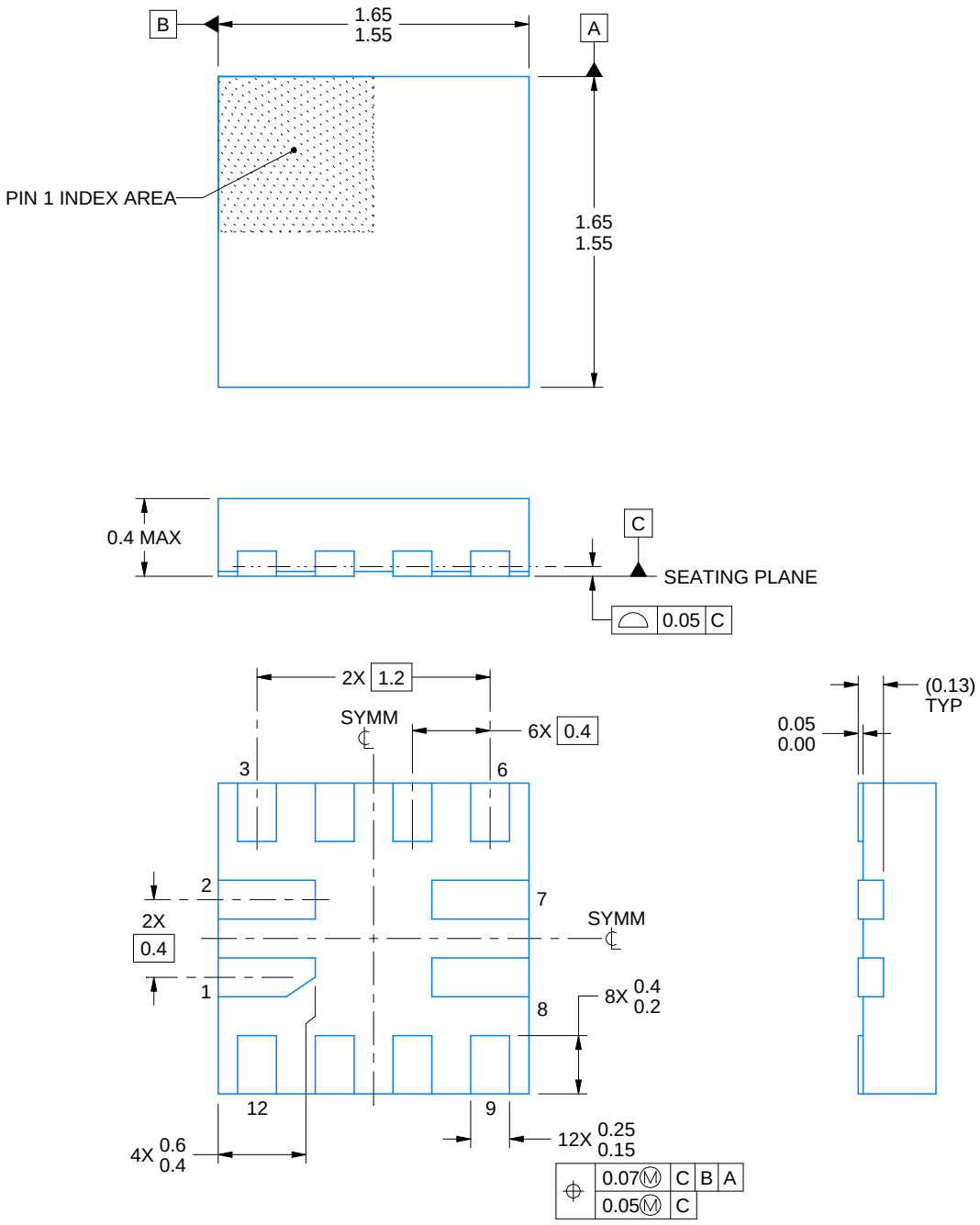
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB212QRWBRQ1	X2QFN	RWB	12	3000	189.0	185.0	36.0
TUSB212QRWBTQ1	X2QFN	RWB	12	250	189.0	185.0	36.0

PACKAGE OUTLINE

RWB0012A

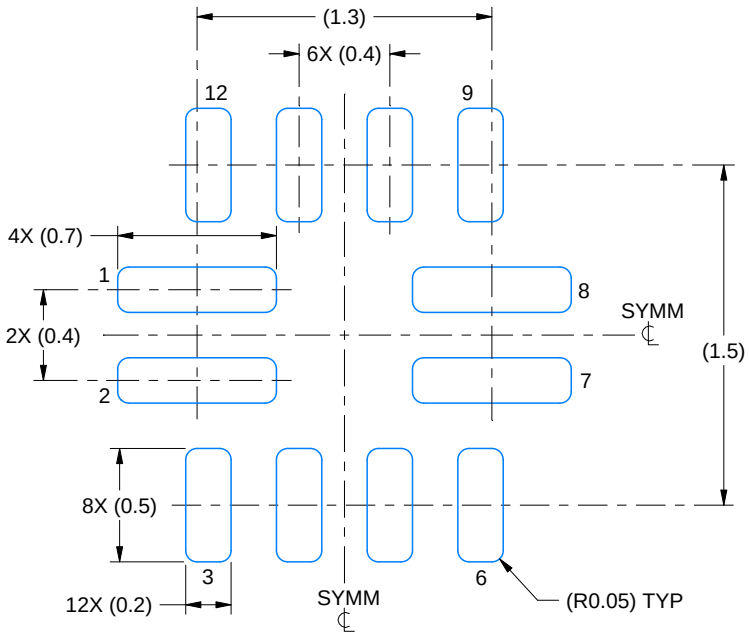
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

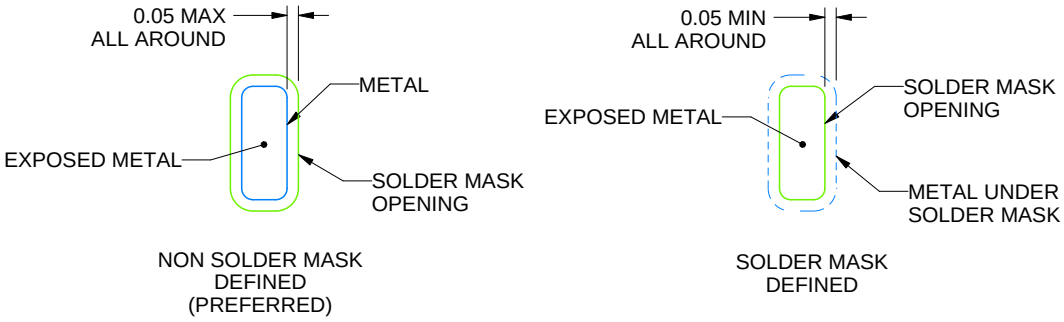


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

NOTES: (continued)

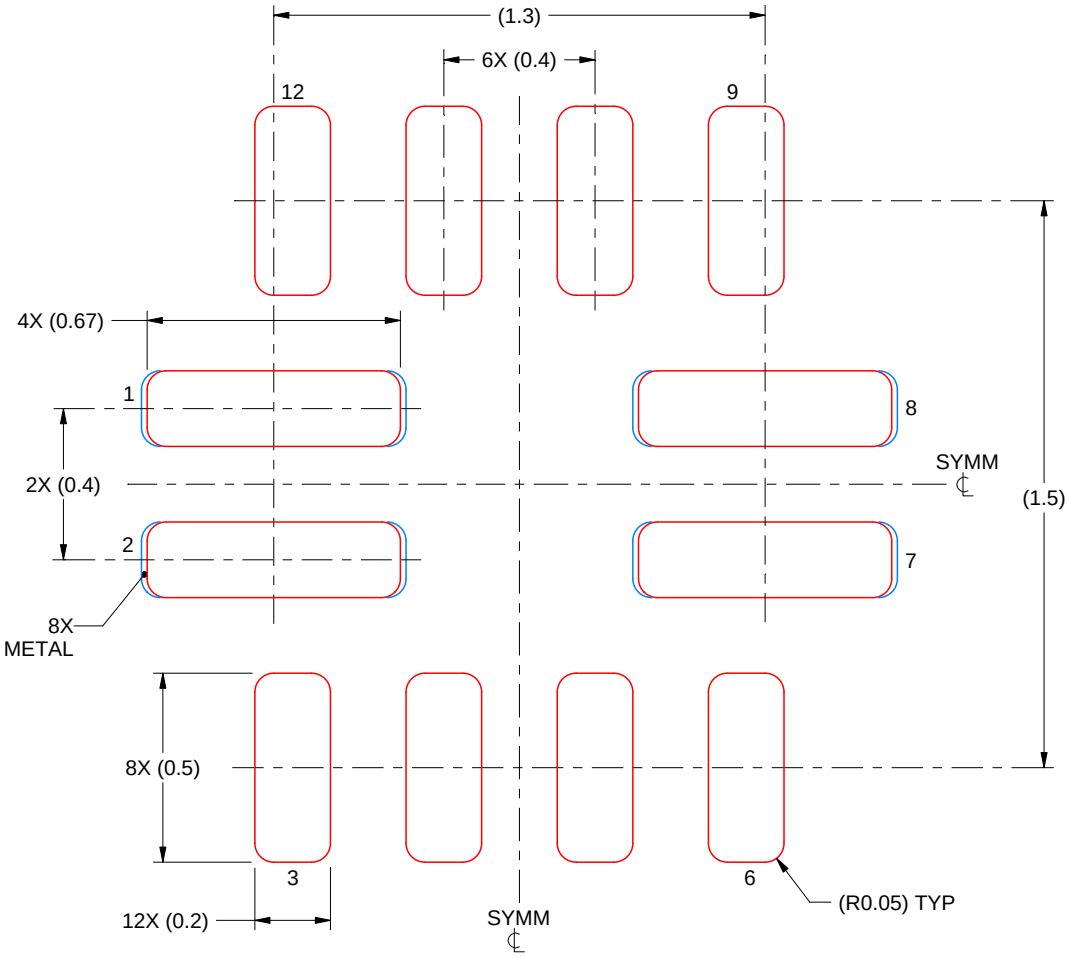
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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