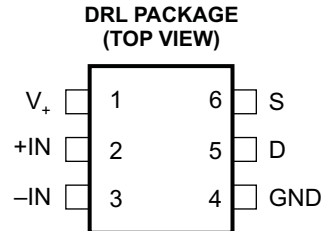


COMPARATOR WITH OUTPUT VOLTAGE-LEVEL TRANSLATION

FEATURES

- **Low Supply Current:** 8 μ A (Max)
- **Supply Voltage:** 2.5 V to 5.5 V
- **Output FET Provides Down Translation**
- **Small Package:** SOT-563
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance**
 - 2500-V Human-Body Model (JESD-A114E)
 - 250-V Machine Model (EIA/JESD A115-A)
 - 1500-V Charged-Device Model (JESD22-C101-A Level III)



DESCRIPTION/ORDERING INFORMATION

The TXS03121 is a comparator designed for battery monitoring applications. It can be operated with a voltage of 2.5 V to 5.5 V. The reference voltage is applied to the –IN terminal, whereas the voltage to be monitored is connected to +IN. When the voltage at +IN is greater than the voltage at –IN, the output FET is turned On. When the voltage at +IN is less than the voltage at –IN, the output FET is turned Off. The source (S) of the output FET can be connected to 1.1 V to 3.6 V, which allows the output signal to be level translated to another voltage value. The voltage at V₊ must be greater than or equal to the voltage at S. The voltage at S must be greater than or equal to the voltage at D ($V_+ \geq V_S \geq V_D$).

ORDERING INFORMATION

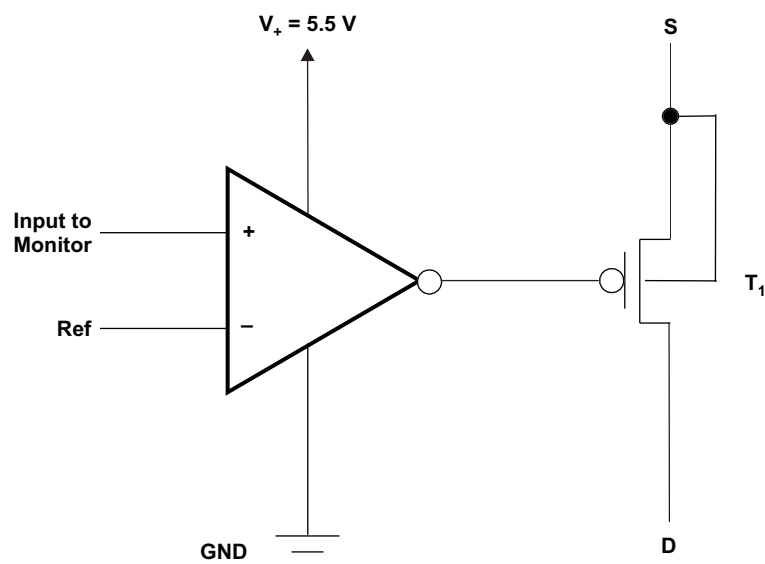
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOT-563 – DRL	Tape and reel	TXS03121DRLR	2FR

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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APPLICATION BLOCK DIAGRAM



PIN ASSIGNMENTS

NO.	NAME	DESCRIPTION
1	V_+	Comparator supply voltage
2	+IN	Comparator positive input
3	-IN	Comparator negative input
4	GND	Ground
5	D	Drain of output FET
6	S	Source of output FET

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range ⁽²⁾		–0.5	6.5	V
$+IN$, $-IN$	Input voltage range		–0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current (On-state switch current)			–50	mA
	Continuous current through V_+ or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DRL package		171.6	°C/W
T_{stg}	Storage temperature range			150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Comparator supply voltage	2.5	5.5	V
V_S , V_D ⁽¹⁾	Output FET source or drain voltage	1.1	3.6	V
T_A	Operating free-air temperature	–40	85	°C

- (1) V_+ must be greater than or equal to V_S , and V_S must be greater than or equal to V_D ($V_+ \geq V_S \geq V_D$).

COMPARATOR ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

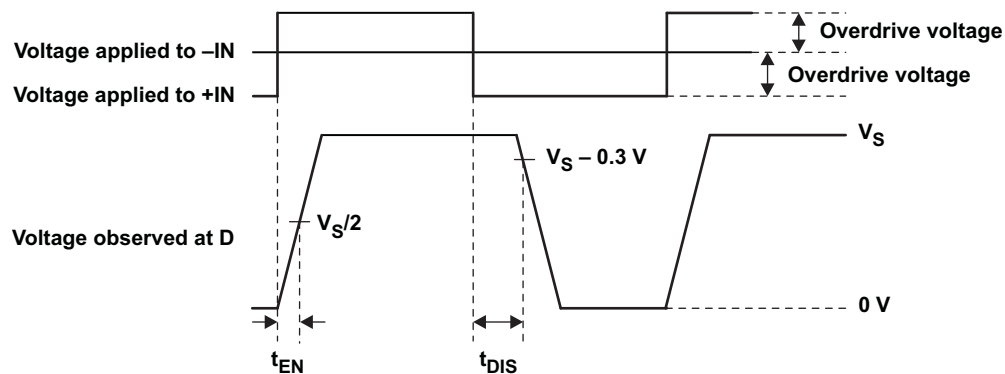
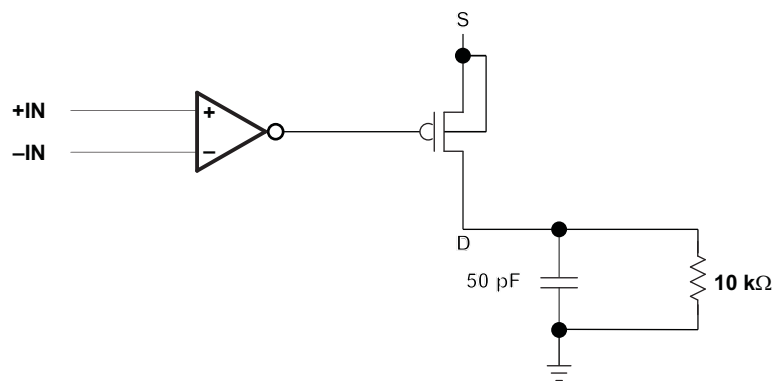
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OS}	Input offset voltage	V ₊ = 2.5 V to 5.5 V	V _{CM} = 0.8 V, I _O = 0	–10	0.5	10	mV
			V _{CM} = V ₊ , I _O = 0				
V _{CM}	Common-mode voltage range	V ₊ = 2.5 V to 5.5 V		0.8		V ₊	V
I _{+IN}	Input leakage current	V ₊ = 2.5 V to 5.5 V	V _{+IN} = 0 V to V ₊			0.5	μA
I _{–IN}			V _{–IN} = 0 V to V ₊				
I ₊	Supply current	V ₊ = 2.5 V to 5.5 V				8	μA
C _{IN}	Capacitance of +IN, –IN pins				2	2.5	pF

OUTPUT FET ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{DS(ON)}$	On leakage current	$V_S = 1.1\text{ V to }3.6\text{ V}$, Switch ON				0.5	μA
$I_{DS(OFF)}$	Off leakage current	$V_S = 1.1\text{ V to }3.6\text{ V}$, $V_D = \text{Open}$, Switch OFF				0.5	μA
$C_{(ON)}$	On capacitance			4	5.1	6	pF
$C_{(OFF)}$	Off capacitance, S and D terminals			1.5	3.4	5	pF
r_{ON}	On resistance of output FET	$V_+ \geq V_S$, $I_D = -100\text{ }\mu\text{A}$	$V_S = 1.1\text{ V}$			150	Ω
			$V_S = 1.4\text{ V}$			65	
			$V_S = 1.65\text{ V}$			61	
			$V_S = 2.3\text{ V}$			50	
			$V_S = 3\text{ V}$			44	
t_{EN}	Enable time	20-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		1.7	μs
				$V_+ = 3\text{ V}$		3.9	
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		1	
				$V_+ = 3\text{ V}$		3.9	
		50-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		1.2	
				$V_+ = 3\text{ V}$		2.7	
				$V_+ = 2.5\text{ V}$		6.2	
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		1	
		100-mV overdrive		$V_+ = 3\text{ V}$		2.4	
				$V_+ = 2.5\text{ V}$		5.3	
			$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		0.8	
				$V_+ = 3\text{ V}$		1.4	
				$V_+ = 2.5\text{ V}$		5	
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		0.7	
				$V_+ = 3\text{ V}$		1.3	
				$V_+ = 2.5\text{ V}$		4.7	
t_{DIS}	Disable time	20-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		4.4	μs
				$V_+ = 3\text{ V}$		12	
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		3.5	
				$V_+ = 3\text{ V}$		6.1	
		50-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		4.1	
				$V_+ = 3\text{ V}$		9.6	
				$V_+ = 2.5\text{ V}$		5.3	
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		2.5	
		100-mV overdrive		$V_+ = 3\text{ V}$		3.2	
				$V_+ = 2.5\text{ V}$		5.2	
			$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		4.6	
				$V_+ = 3\text{ V}$		6.7	
				$V_+ = 2.5\text{ V}$		5.2	
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		1.9	
				$V_+ = 3\text{ V}$		2.8	
				$V_+ = 2.3\text{ V}$		4.9	

PARAMETER MEASUREMENT INFORMATION



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS03121DRLR	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2FR
TXS03121DRLR.B	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2FR

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

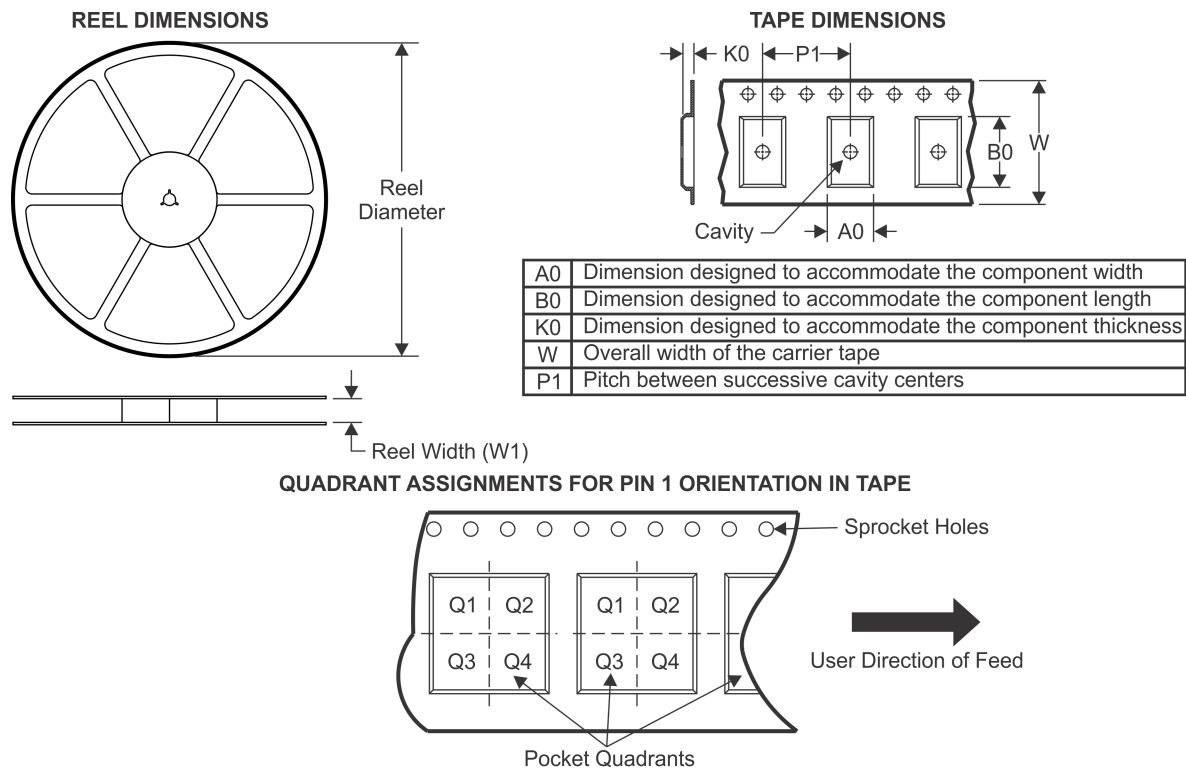
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

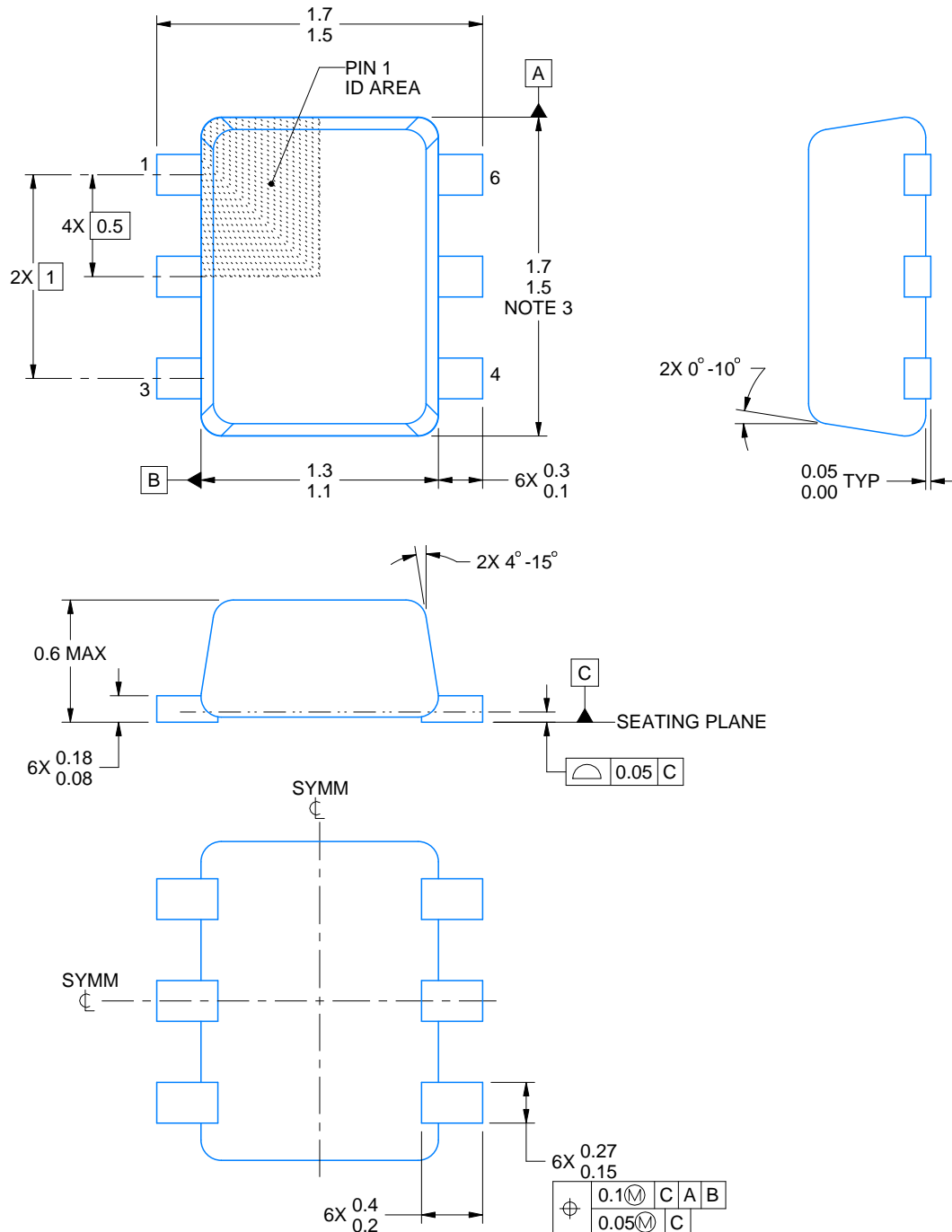
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS03121DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS03121DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0



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NOTES:

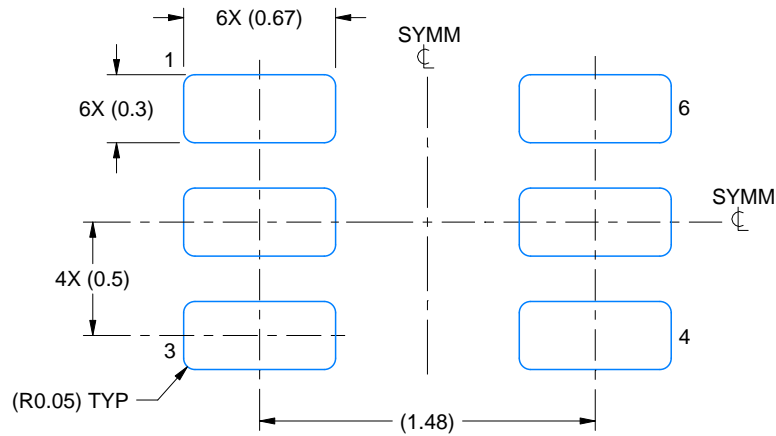
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

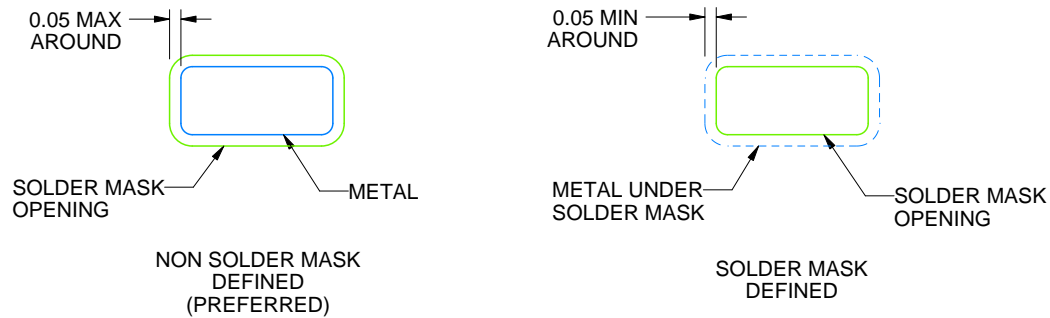
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

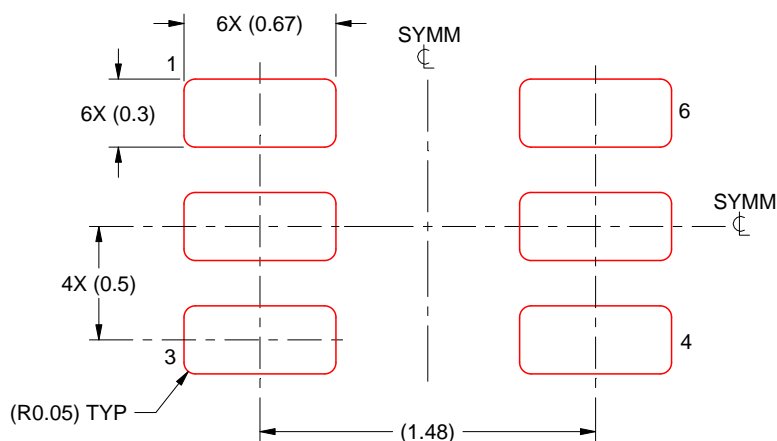
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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