双通道高速差分线路驱动器

查询样品: uA9638C-EP

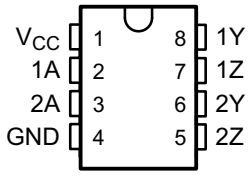
特性

- 符合或者优于**ANSI**标准**EIA/TIA-422-B**
- 单一**5V**电源供电下运行
- 驱动负载低至**50** Ω高达**15Mbps**
- **TTL-** 和 **CMOS-**输入兼容性
- 输出短路保护
- 可与 美国国家半导体公司 **(National Semiconductor)**的™ **DS9638**互换

支持国防，航空航天，和医疗应用

- 可控基线
- 一个组装**/**测试场所
- 一个制造场所
- 额定温度为**–40°C** 至 **85°C**
- 延长的产品生命周期
- 延长产品的变更通知周期
- 产品可追溯性

D PACKAGE
(TOP VIEW)

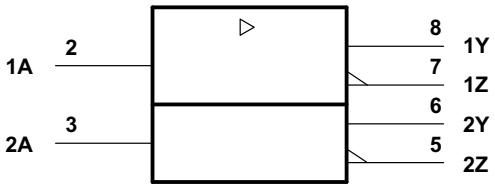


说明

uA9638C是一款双通道高速差分线路驱动器，设计满足ANSI标准EIA/TIA-422-B。 此输入是TTL和CMOS兼容的并且具有输入钳位二极管。 肖特基(Schottky)钳位二极管晶体管用于大大减少传播延迟时间。 这个器件由一个单一5V电源供电并采用一个8引脚封装。

uA9638提供高速驱动低阻抗负载所需的电流。 通常使用双绞线和差分接收器，在设计正确的系统中，基带数据速率传输可高达甚至超过14Mbps。 uA9637A双线路接收器通常用作接收器。 要在同样的引脚配置下获得更快的开关速度，请见SN75ALS191。

uA9638C额定运行温度为-40°C 至 85°C。



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 1. Logic Symbol

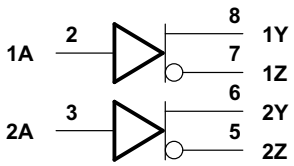


Figure 2. Logic Diagram

ORDERING INFORMATION(1)

$T_A = T_J$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 85°C	SOIC - D	Reel of 2500	UA9638CIDREP	9638I	V62/12606-10XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

SCHEMATICS OF INPUTS AND OUTPUTS

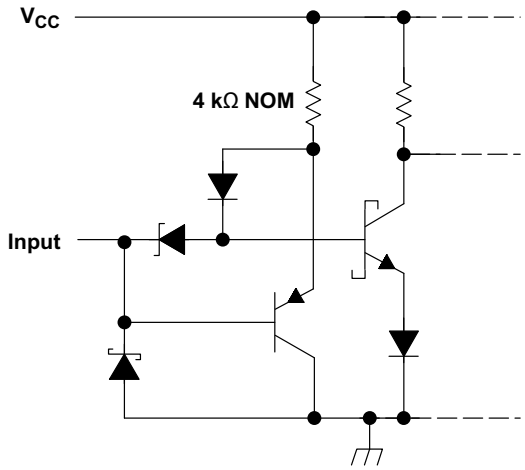


Figure 3. Equivalent of Each Input

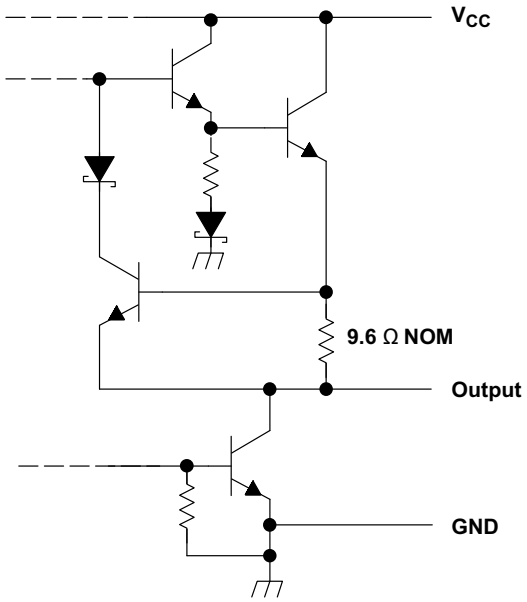


Figure 4. Typical of All Inputs

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range(2)	–0.5 V to 7 V
V_I	Input voltage range	–0.5 V to 7 V
	Continuous total power dissipation	See Dissipation Ratings Table
	Lead temperature 1,6 mm (1/16 inch) from 10 seconds	260°C
T_A	Operating free-air temperature range	–40°C to 85°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Voltage values except differential output voltages are with respect to network GND.
(2) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		uA9638C D 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	114.3	°C/W
θ_{JC}	Junction-to-case thermal resistance	59.1	
θ_{JB}	Junction-to-board thermal resistance(3)	55.3	
ψ_{JT}	Junction-to-top characterization parameter(4)	12.7	
ψ_{JB}	Junction-to-board characterization parameter(5)	54.7	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定在一个 JEDEC 标准 high-K 测试电路板上进行仿真，从而获得自然对流条件下的结到外部热阻。
(3) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结到电路板热阻。
(4) 结到顶部的表征参数 (ψ_{JT}) 估算真实系统中器件的结温，并使用 JESD51-2a (第 6 章和第 7 章) 中描述的程序从从得到 θ_{JA}的仿真数据中提取出该参数。
(5) 结到电路板的表征参数 (ψ_{JB}) 估算真实系统中器件的结温，并使用 JESD51-2a (第 6 章和第7 章) 中描述的程序从从得到 θ_{JA} 的仿真数据中提取出该参数。

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A = 25°C (mW)	DERATING FACTOR T_A > 70°C (mW/°C)	POWER RATING T_A = 85°C (mW)
D	725	8.75	199

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-50	mA
I_{OL}	Low-level output current			50	mA
T_A	Operating free-air temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA			-1	-1.2	V
V_{OH}	High level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2			
V_{OL}	Low level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.5	V
$\lvert V_{OD1}\rvert$	Magnitude of differential output voltage	V_{CC} = 5.25 V, I_O = 0 A			1.25 x V_{OD2}		V
$\lvert V_{OD2}\rvert$	Magnitude of differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5		2			V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage(2)	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5				±0.4	V
V_{OC}	Common-mode output voltage(3)	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5				3	V

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level or vice versa.
(3) In Standard EIA-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage(2)	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5				±0.4	V
I_O	Output current with power off	V_{CC} = 0 V	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		-0.1	-100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V				-200	μA
I_{OS}	Short-circuit output current(4)	V_{CC} = 5.25 V, V_O = 0 V		-50		-150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25 V, No load, All inputs at 0 V			45	65	mA

(4) Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 6		10		ns
$t_{t(OD)}$	Differential output transition time	C_L = 15 pF, R_L = 100 Ω, See Figure 6		10		ns
$t_{sk(o)}$	Output skew	See Figure 6		1		ns

PARAMETER MEASUREMENT INFORMATION

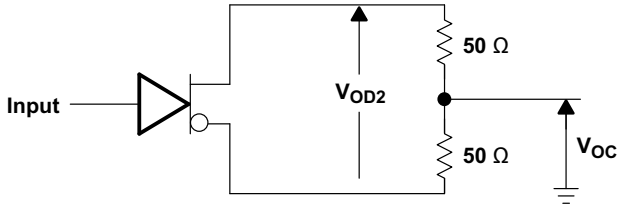
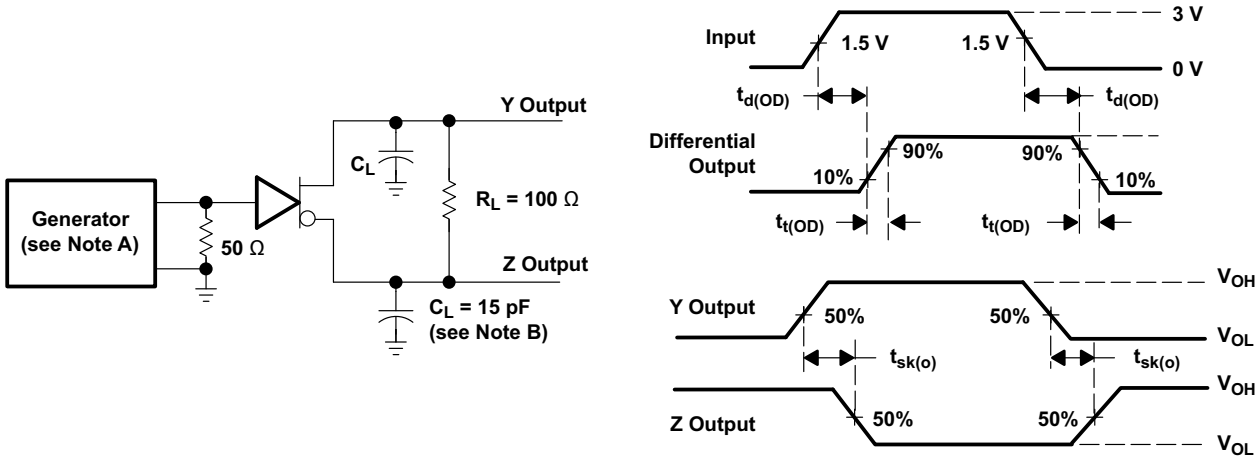


Figure 5. Differential and Common-Mode Output Voltages



TEST CIRCUIT **VOLTAGE WAVEFORMS**

A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.

B. C_L includes probe and jig capacitance.

Figure 6. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA9638CIDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I
UA9638CIDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I
V62/12606-01XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

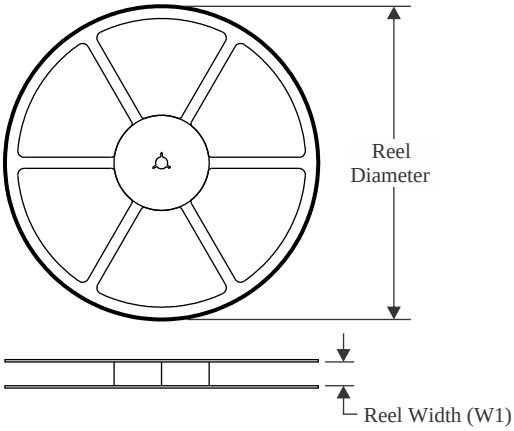
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

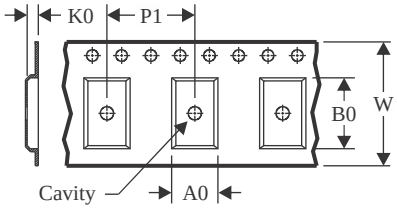
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

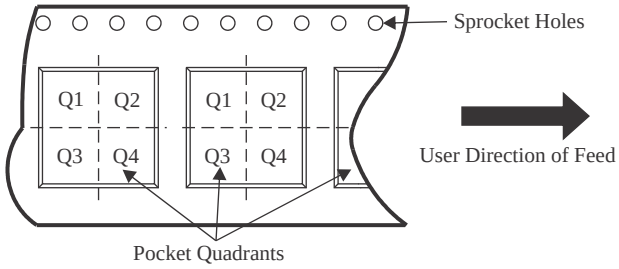


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

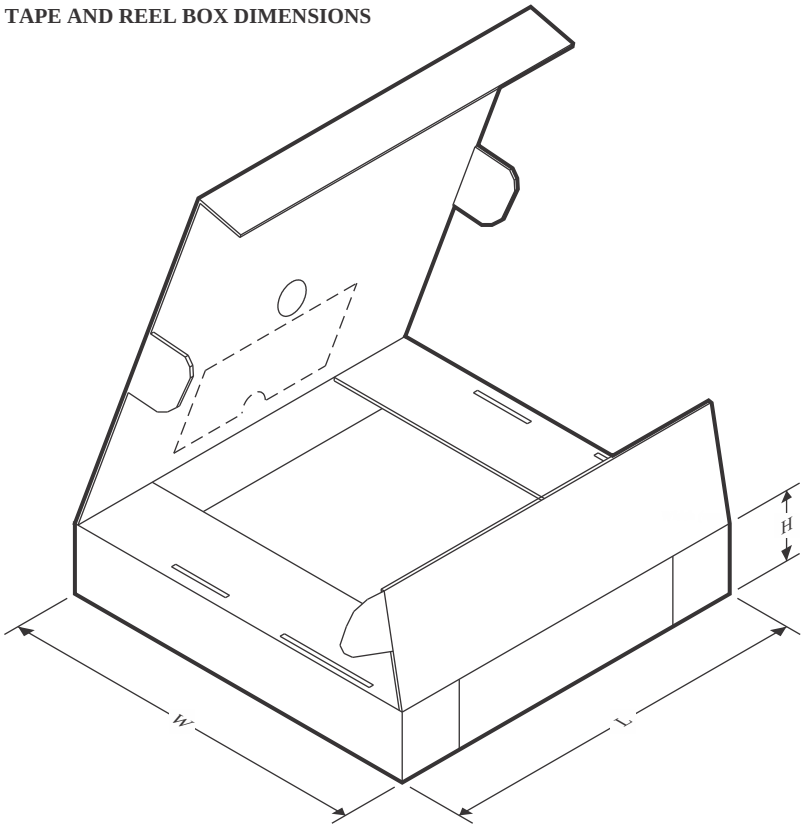
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

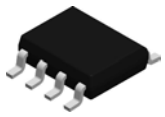
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9638CIDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9638CIDREP	SOIC	D	8	2500	353.0	353.0	32.0

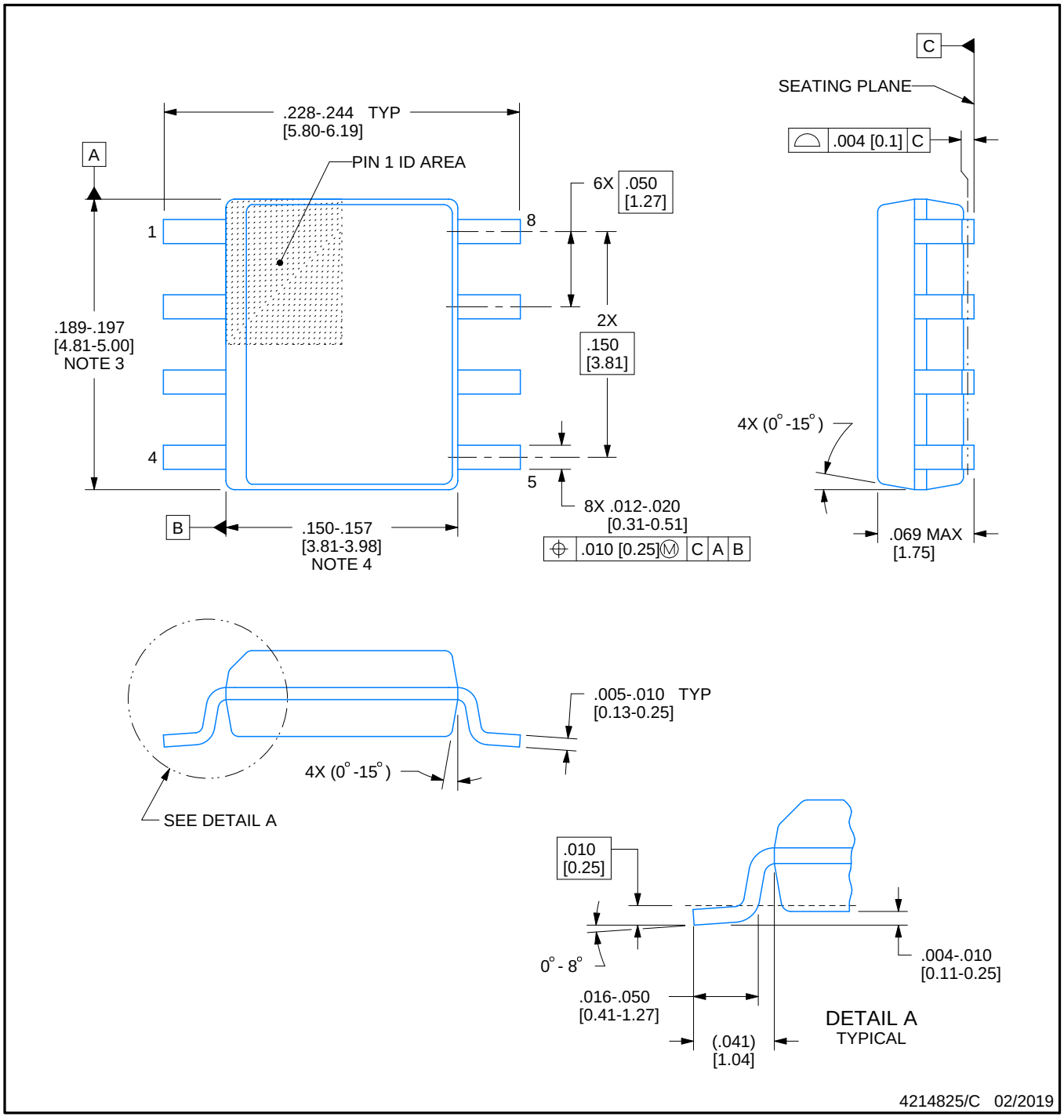


PACKAGE OUTLINE

D0008A

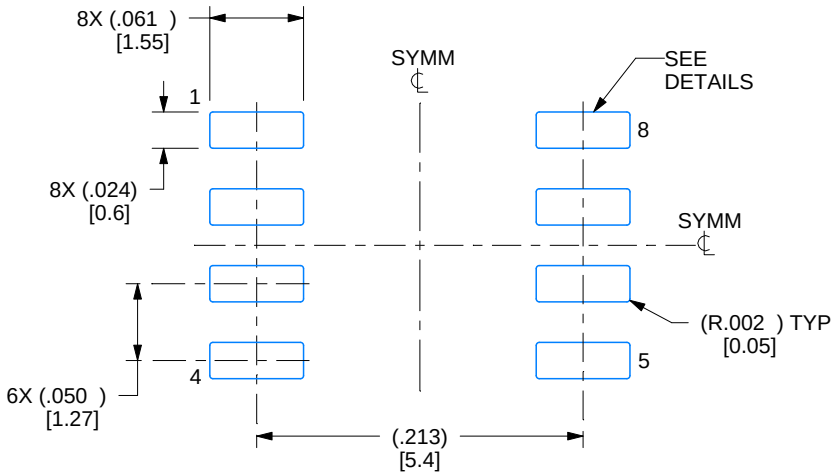
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

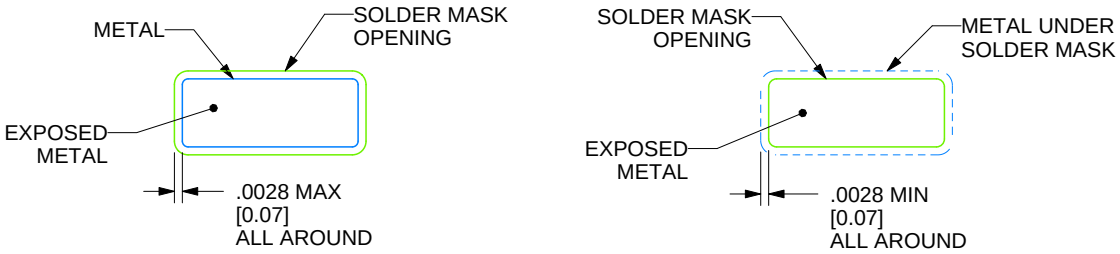


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

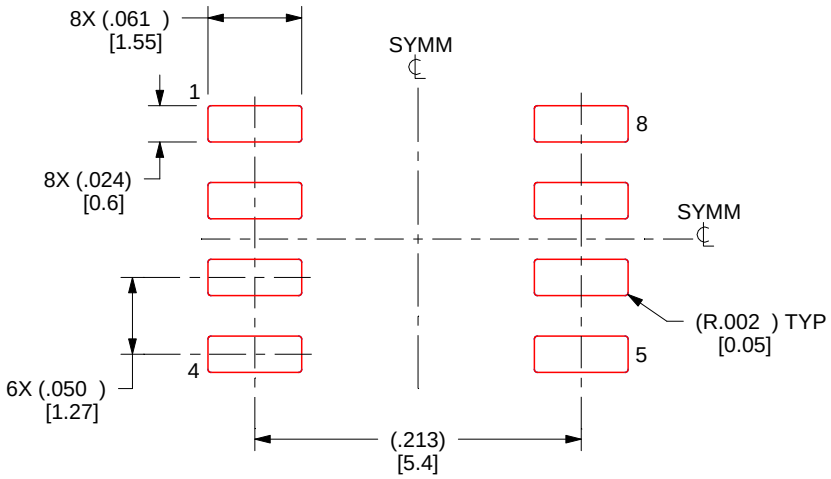
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月