

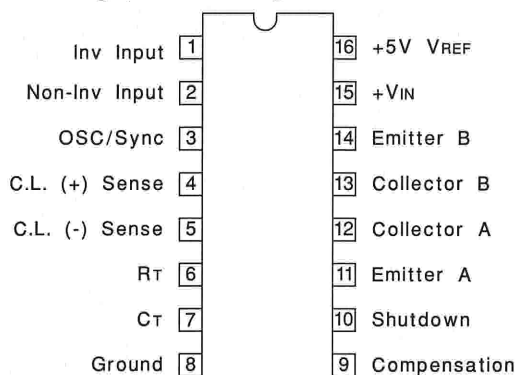


### ABSOLUTE MAXIMUM RATINGS

|   |                 |
|---|-----------------|
| Supply Voltage (V <sub>IN</sub> )           | 40V             |
| Collector Supply Voltage (V <sub>C</sub> )  | 60V             |
| Output Current (each Output)                | 200mA           |
| Maximum Forced Voltage (Pin 9, 10)          | -3 to +5V       |
| Maximum Forced Current (Pin 9, 10)          | ±10mA           |
| Reference Output Current                    | 50mA            |
| Oscillator Charging Current                 | 5mA             |
| Power Dissipation at T <sub>A</sub> = +25°C | 1000mW          |
| Power Dissipation at T <sub>C</sub> = +25°C | 2000mW          |
| Operating Temperature Range                 | -55°C to +125°C |
| Storage Temperature Range                   | -65°C to +150°C |
| Lead Temperature, (Soldering, 10 seconds)   | +300°C          |

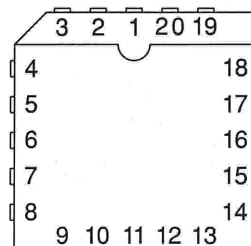
Note: Consult packaging section of Databook for thermal limitations and considerations of package.

### DIL-16, SOIC-16 (TOP VIEW) J or N Package, DW Package



### CONNECTION DIAGRAMS

#### PLCC-20, LCC-20 (TOP VIEW) Q or L Package



| PACKAGE PIN FUNCTION |     |
|----------------------|-----|
| FUNCTION             | PIN |
| N/C                  | 1   |
| Inv. Input           | 2   |
| Non-Inv. Input       | 3   |
| OSC/SYNC             | 4   |
| C.L. (+) sense       | 5   |
| N/C                  | 6   |
| C.L. (-) sense       | 7   |
| R <sub>T</sub>       | 8   |
| C <sub>T</sub>       | 9   |
| Ground               | 10  |
| N/C                  | 11  |
| Compensation         | 12  |
| Shutdown             | 13  |
| Emitter A            | 14  |
| Collector A          | 15  |
| N/C                  | 16  |
| Collector B          | 17  |
| Emitter B            | 18  |
| +V <sub>IN</sub>     | 19  |
| +5V V <sub>REF</sub> | 20  |

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for T<sub>A</sub> = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V<sub>IN</sub> = V<sub>C</sub> = 20V, T<sub>A</sub> = T<sub>J</sub>.

| PARAMETER                      | TEST CONDITIONS                                     | UC1524A / UC2524A |      |      | UC3524A |      |      | UNITS             |
|--------------------------------|---|-------------------|------|------|---------|------|------|-------------------|
|                                |   | MIN               | TYP  | MAX  | MIN     | TYP  | MAX  |                   |
| <b>Turn-on Characteristics</b> |   |                   |      |      |         |      |      |                   |
| Input Voltage                  | Operating Range after Turn-on                       | 8                 |      | 40   | 8       |      | 40   | V                 |
| Turn-on Threshold              |   | 6.5               | 7.5  | 8.5  | 6.5     | 7.5  | 8.5  | V                 |
| Turn-on Current                | V <sub>IN</sub> = 6V                                |                   | 2.5  | 4    |         | 2.5  | 4    | mA                |
| Operating Current              | V <sub>IN</sub> = 8 to 40V                          |                   | 5    | 10   |         | 5    | 10   | mA                |
| Turn-on Hysteresis*            |   |                   | 0.5  |      |         | 0.5  |      | V                 |
| <b>Reference Section</b>       |   |                   |      |      |         |      |      |                   |
| Output Voltage                 | T <sub>J</sub> = 25°C                               | 4.95              | 5.00 | 5.05 | 4.90    | 5.00 | 5.10 | V                 |
|                                | Over Operating Range                                | 4.9               |      | 5.1  | 4.85    |      | 5.15 | V                 |
| Line Regulation                | V <sub>IN</sub> = 10 to 40V                         |                   | 10   | 20   |         | 10   | 30   | mV                |
| Load Regulation                | I <sub>L</sub> = 0 to 20 mA                         |                   | 20   | 25   |         | 20   | 35   | mV                |
| Temperature Stability*         | Over Operating Range*                               |                   | 20   | 25   |         | 20   | 35   | mV                |
| Short Circuit Current          | V <sub>REF</sub> = 0, 25°C ≤ T <sub>J</sub> ≤ 125°C |                   | 80   | 100  |         | 80   | 100  | mA                |
| Output Noise Voltage*          | 10Hz ≤ f ≤ 10kHz, T <sub>J</sub> = 25°C             |                   | 40   |      |         | 40   |      | μV <sub>rms</sub> |
| Long Term Stability*           | T <sub>J</sub> = 125°C, 1000 Hrs.                   |                   | 20   | 50   |         | 20   | 50   | mV                |

\* These parameters are ensured by design but not 100% tested in production.

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1524A,  $-40^{\circ}$  to  $+85^{\circ}\text{C}$  for the UC2524A, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3524A;  $V_{IN} = V_C = 20\text{V}$ ,  $T_A = T_J$ .

| PARAMETER   | TEST CONDITIONS   | UC1524A / UC2524A |      |      | UC3524A |      |      | UNITS                        |
|---|---|-------------------|------|------|---------|------|------|------------------------------|
|   |   | MIN               | TYP  | MAX  | MIN     | TYP  | MAX  |                              |
| <b>Oscillator Section</b> (Unless otherwise specified, $R_T = 2700\Omega$ , $C_T = 0.01\text{ mfd}$ ) |   |                   |      |      |         |      |      |                              |
| Initial Accuracy  | $T_J = 25^{\circ}\text{C}$  | 41                | 43   | 45   | 39      | 43   | 47   | kHz                          |
|   | Over Operating Range  | 40.2              |      | 45.9 | 38.2    |      | 47.9 | kHz                          |
| Temperature Stability*  | Over Operating Temperature Range  |                   | 1    | 2    |         | 1    | 2    | %                            |
| Minimum Frequency   | $R_T = 150\text{k}\Omega$ , $C_T = 0.1\text{ mfd}$                            |                   |      | 140  |         |      | 120  | Hz                           |
| Maximum Frequency   | $R_T = 2.0\text{k}\Omega$ , $C_T = 470\text{pF}$                              | 500               |      |      | 500     |      |      | kHz                          |
| Output Amplitude*   |   | 3                 | 3.5  |      | 3       | 3.5  |      | V                            |
| Output Pulse Width*   |   | 0.29              | 0.5  | 1.0  | 0.3     | 0.5  | 1.0  | $\mu\text{s}$                |
| Ramp Peak   |   | 3.3               | 3.5  | 3.7  | 3.3     | 3.5  | 3.7  | V                            |
| Ramp Valley   | $T_J = 25^{\circ}\text{C}$  | 0.7               | 0.8  | 0.9  | 0.7     | 0.8  | 0.9  | V                            |
| Ramp Valley T.C.  |   |                   | -1.0 |      |         | -1.0 |      | $\text{mV}/^{\circ}\text{C}$ |
| <b>Error Amplifier Section</b> (Unless otherwise specified, $V_{CM} = 2.5\text{V}$ )                  |   |                   |      |      |         |      |      |                              |
| Input Offset Voltage  |   |                   | 0.5  | 5    |         | 2    | 10   | mV                           |
| Input Bias Current  |   |                   | 1    | 5    |         | 1    | 10   | $\mu\text{A}$                |
| Input Offset Current  |   |                   | .05  | 1    |         | 0.5  | 1    | $\mu\text{A}$                |
| Common Mode Rejection Ratio   | $V_{CM} = 1.5$ to $5.5\text{V}$   | 70                | 80   |      | 70      | 80   |      | dB                           |
| Power Supply Rejection Ratio  | $V_{IN} = 10$ to $40\text{V}$   | 70                | 80   |      | 70      | 80   |      | dB                           |
| Output Swing (Note 1)   |   | 5.0               |      | 0.5  | 5.0     |      | 0.5  | V                            |
| Open Loop Voltage Gain  | $\Delta V_O = 1$ to $4\text{V}$ , $R_L \geq 10\text{M}\Omega$                 | 72                | 80   |      | 64      | 80   |      | dB                           |
| Gain-Bandwidth*   | $T_J = 25^{\circ}\text{C}$ , $A_V = 0\text{dB}$                               | 1                 | 3    |      | 1       | 3    |      | MHz                          |
| DC Transconductance*§   | $T_J = 25^{\circ}\text{C}$ , $30\text{k}\Omega \leq R_L \leq 1\text{M}\Omega$ | 1.7               | 2.3  |      | 1.7     | 2.3  |      | $\text{mS}$                  |
| <b>P.W.M. Comparator</b> ( $R_T = 2\text{k}\Omega$ , $C_T = 0.01\text{ mfd}$ )                        |   |                   |      |      |         |      |      |                              |
| Minimum Duty Cycle  | $V_{COMP} = 0.5\text{V}$  |                   |      | 0    |         |      | 0    | %                            |
| Maximum Duty Cycle  | $V_{COMP} = 3.8\text{V}$  | 45                |      |      | 45      |      |      | %                            |
| <b>Current Limit Amplifier</b> (Unless otherwise specified, $\text{Pin } 5 = 0\text{V}$ )             |   |                   |      |      |         |      |      |                              |
| Input Offset Voltage  | $T_J = 25^{\circ}\text{C}$ , E/A Set for Maximum Output                       | 190               | 200  | 210  | 180     | 200  | 220  | mV                           |
|   | Over Operating Temperature Range  | 180               |      | 220  | 170     |      | 230  | mV                           |
| Input Bias Current  |   |                   | -1   | -10  |         | -1   | -10  | $\mu\text{A}$                |
| Common Mode Rejection Ratio   | $V_{(\text{pin } 5)} = -0.3\text{V}$ to $+5.5\text{V}$                        | 50                | 60   |      | 50      | 60   |      | dB                           |
| Power Supply Rejection Ratio  | $V_{IN} = 10$ to $40\text{V}$   | 50                | 60   |      | 50      | 60   |      | dB                           |
| Output Swing (Note 1)   | Minimum Total Range   | 5.0               |      | 0.5  | 5.0     |      | 0.5  | V                            |
| Open-Loop Voltage Gain  | $\Delta V_O = 1$ to $4\text{V}$ , $R_L \geq 10\text{M}\Omega$                 | 70                | 80   |      | 70      | 80   |      | dB                           |
| Delay Time*   | $\text{Pin } 4$ to $\text{Pin } 9$ , $\Delta V_{IN} = 300\text{mV}$           |                   | 300  |      |         | 300  |      | ns                           |
| <b>Output Section</b> (Each Output)   |   |                   |      |      |         |      |      |                              |
| Collector Emitter Voltage   | $I_C = 100\mu\text{A}$  | 60                | 80   |      | 60      | 80   |      | V                            |
| Collector Leakage Current   | $V_{CE} = 50\text{V}$   |                   | .1   | 20   |         | .1   | 20   | $\mu\text{A}$                |

\* These parameters are ensured by design but not 100% tested in production.

§ DC transconductance ( $g_m$ ) relates to DC open-loop voltage gain according to the following equation:  $A_V = g_m R_L$  where  $R_L$  is the resistance from pin 9 to the common mode voltage.

The minimum  $g_m$  specification is used to calculate minimum  $A_V$  when the error amplifier output is loaded.

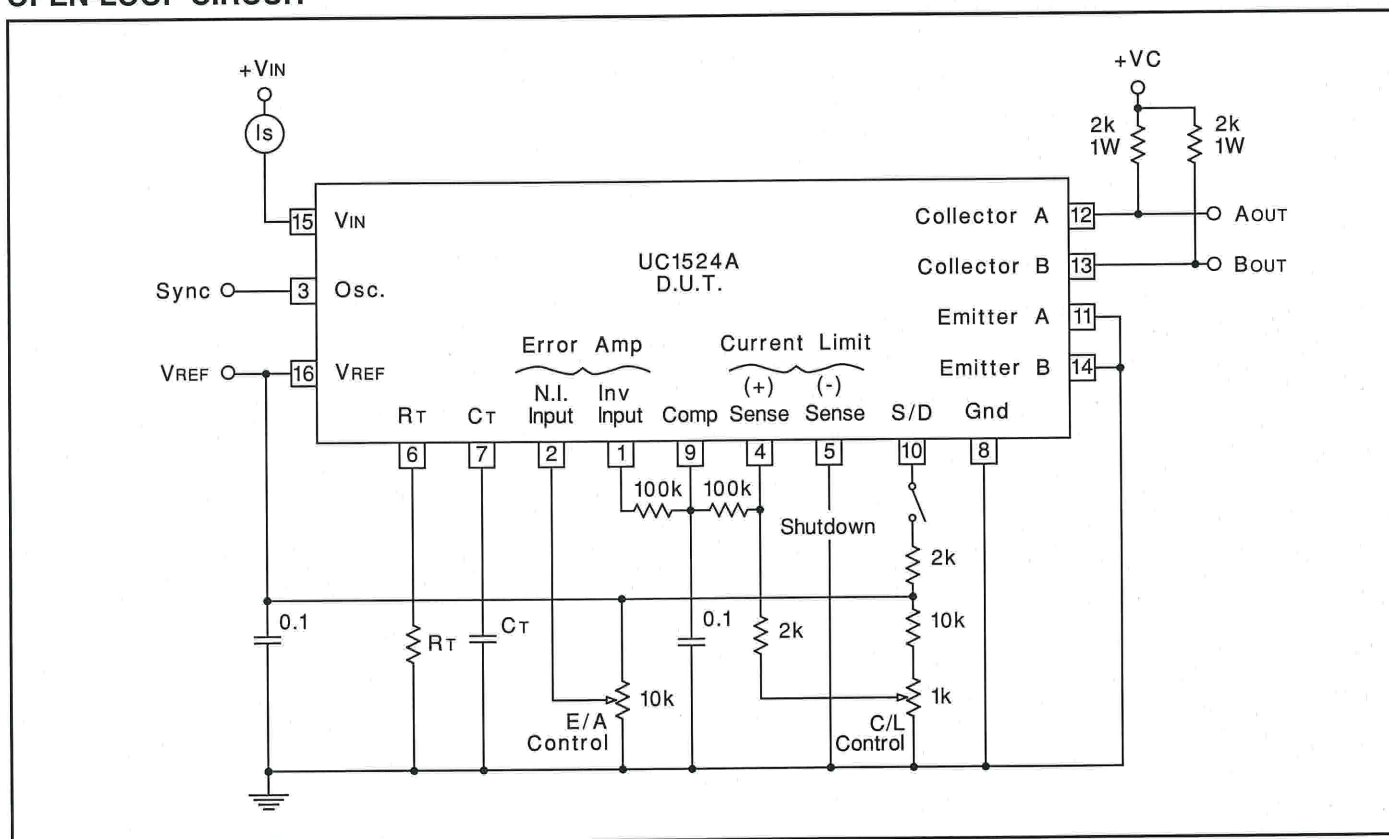
Note 1: Min Limit applies to output high level, max limit applies to output low level.

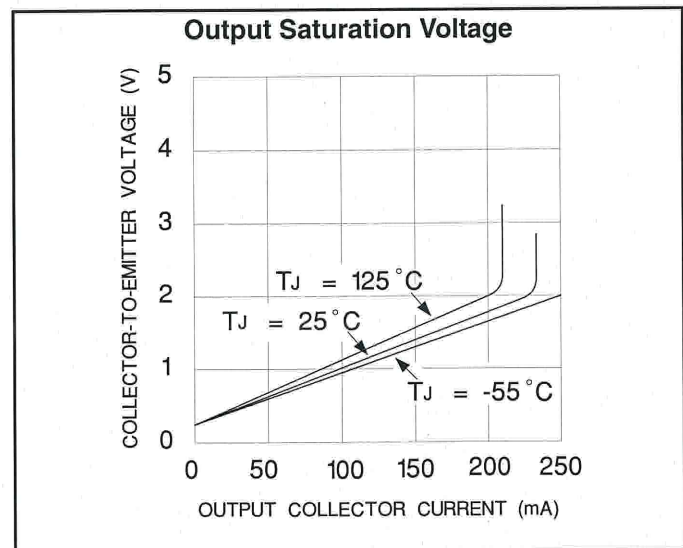
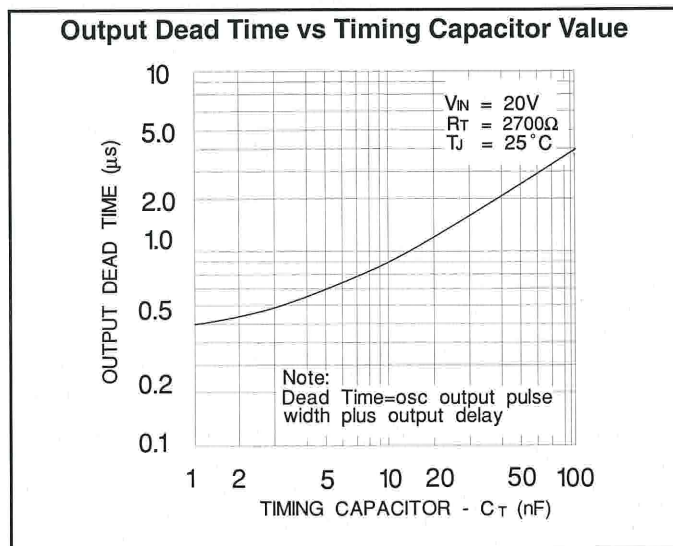
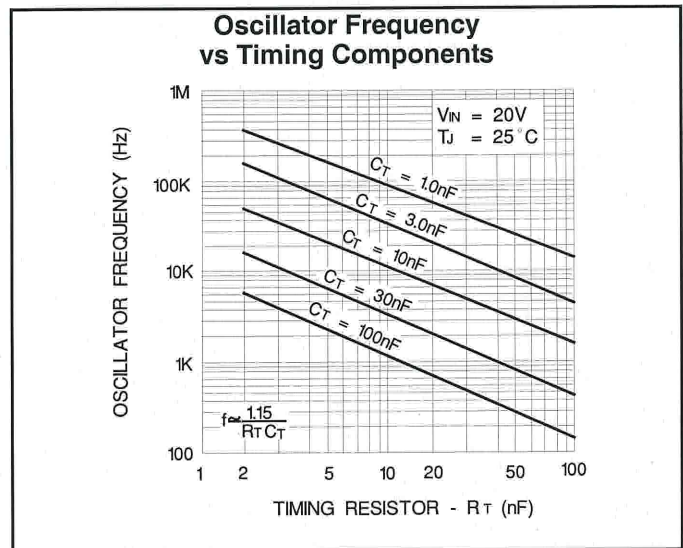
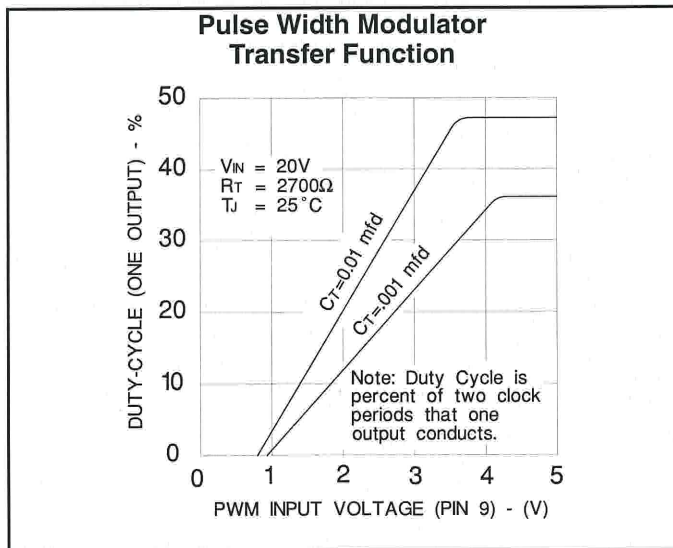
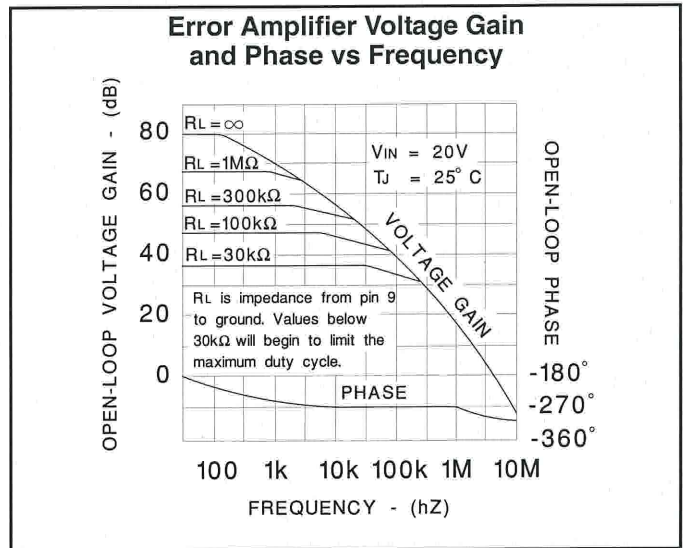
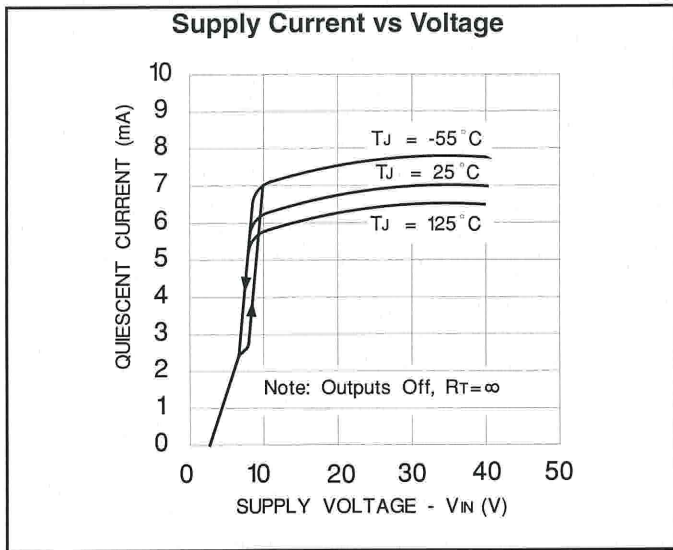
**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1524A,  $-40^{\circ}$  to  $+85^{\circ}\text{C}$  for the UC2524A, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3524A;  $V_{IN} = V_C = 20\text{V}$ .  $T_A = T_J$ .

| PARAMETER                                    | TEST CONDITIONS                                      | UC1524A / UC2524A |         |           | UC3524A |         |           | UNITS              |
|--|--|-------------------|---------|-----------|---------|---------|-----------|--------------------|
|  |  | MIN               | TYP     | MAX       | MIN     | TYP     | MAX       |                    |
| <b>Output Section ( cont.) (Each Output)</b> |  |                   |         |           |         |         |           |                    |
| Saturation Voltage                           | $I_C = 20\text{mA}$<br>$I_C = 200\text{mA}$          |                   | .2<br>1 | .4<br>2.2 |         | .2<br>1 | .4<br>2.2 | V<br>V             |
| Emitter Output Voltage                       | $I_E = 50\text{mA}$                                  | 17                | 18      |           | 17      | 18      |           | V                  |
| Rise Time*                                   | $T_J = 25^{\circ}\text{C}$ , $R = 2\text{k}\Omega$   |                   | 120     | 400       |         | 120     | 400       | ns                 |
| Fall Time*                                   | $T_J = 25^{\circ}\text{C}$ , $R = 2\text{k}\Omega$   |                   | 25      | 200       |         | 25      | 200       | ns                 |
| Comparator Delay*                            | $T_J = 25^{\circ}\text{C}$ , Pin 9 to output         |                   | 300     |           |         | 300     |           | ns                 |
| Shutdown Delay*                              | $T_J = 25^{\circ}\text{C}$ , Pin 10 to output        |                   | 200     |           |         | 200     |           | ns                 |
| Shutdown Threshold                           | $T_J = 25^{\circ}\text{C}$ , $R_C = 2\text{k}\Omega$ | 0.6               | .7      | 1.0       | 0.6     | .7      | 1.0       | V                  |
| S/D Threshold Over Temp.                     | Over Operating Temperature Range                     | 0.4               |         | 1.2       | 0.4     |         | 1.0       | V                  |
| Thermal Shutdown*                            |  |                   | 165     |           |         | 165     |           | $^{\circ}\text{C}$ |

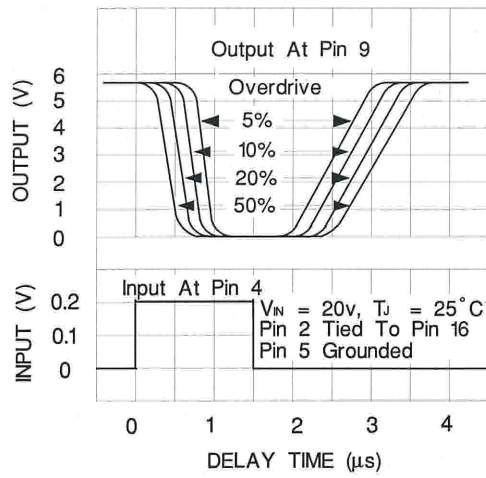
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### OPEN-LOOP CIRCUIT

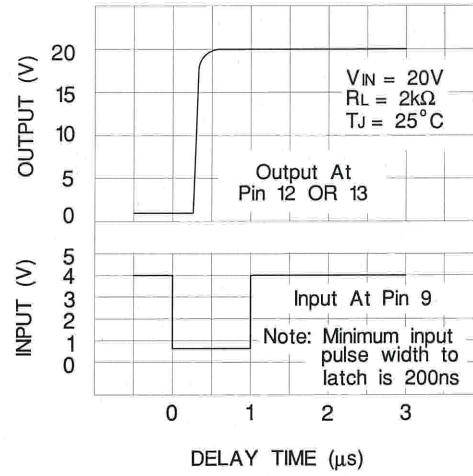




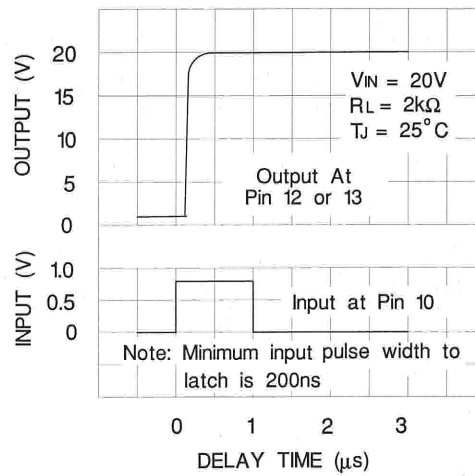
**Current Limit Amplifier Delay**



**Shutdown Delay From PWM Comparator - Pin 9**



**Turn-Off Delay From Shutdown - Pin 10**



**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">5962-8764502EA</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8764502EA      |
| 5962-8764502EA.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8764502EA      |
| <a href="#">UC1524AJ</a>       | NRND          | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AJ            |
| UC1524AJ.A                     | NRND          | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AJ            |
| <a href="#">UC1524AJ883B</a>   | NRND          | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AJ/883B       |
| UC1524AJ883B.A                 | NRND          | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AJ/883B       |
| <a href="#">UC1524AL</a>       | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AL            |
| UC1524AL.A                     | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AL            |
| <a href="#">UC1524AL883B</a>   | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AL/<br>883B   |
| UC1524AL883B.A                 | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1524AL/<br>883B   |
| <a href="#">UC2524ADW</a>      | NRND          | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2524ADW           |
| UC2524ADW.A                    | NRND          | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2524ADW           |
| UC2524ADWG4                    | NRND          | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2524ADW           |
| <a href="#">UC2524ADWTR</a>    | NRND          | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2524ADW           |
| UC2524ADWTR.A                  | NRND          | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2524ADW           |
| <a href="#">UC2524AJ</a>       | NRND          | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -40 to 85    | UC2524AJ            |
| UC2524AJ.A                     | NRND          | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -40 to 85    | UC2524AJ            |
| <a href="#">UC2524AN</a>       | NRND          | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2524AN            |
| UC2524AN.A                     | NRND          | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2524AN            |
| <a href="#">UC3524ADW</a>      | NRND          | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524ADW           |
| UC3524ADW.A                    | NRND          | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524ADW           |
| <a href="#">UC3524ADWTR</a>    | NRND          | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524ADW           |
| UC3524ADWTR.A                  | NRND          | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524ADW           |
| <a href="#">UC3524AJ</a>       | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | 0 to 70      | UC3524AJ            |
| UC3524AJ.A                     | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | 0 to 70      | UC3524AJ            |
| <a href="#">UC3524AN</a>       | NRND          | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3524AN            |
| UC3524AN.A                     | NRND          | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3524AN            |
| UC3524ANG4                     | NRND          | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3524AN            |

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1524A, UC2524A, UC2524AM, UC3524A, UC3524AM :**

- Catalog : [UC3524A](#), [UC2524A](#), [UC3524AM](#), [UC3524A](#)
- Military : [UC2524AM](#), [UC1524A](#), [UC1524A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

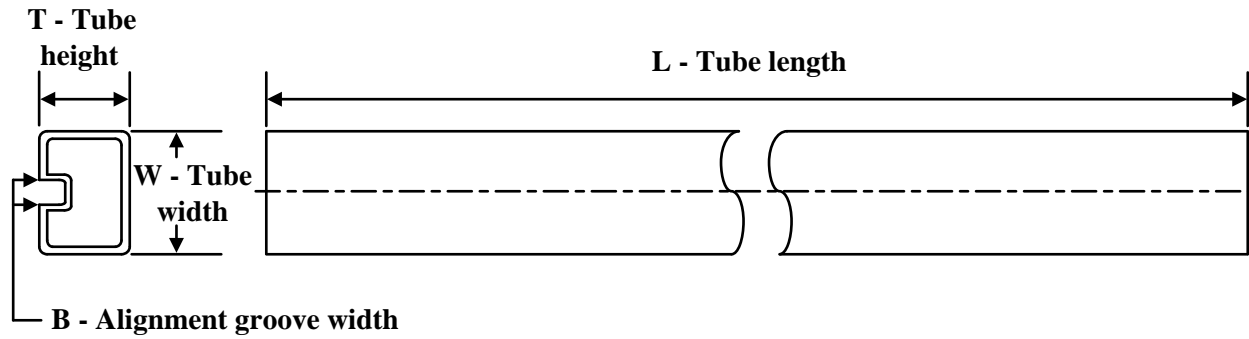

\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC2524ADWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| UC3524ADWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC2524ADWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| UC3524ADWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| UC1524AL       | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1524AL.A     | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1524AL883B   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1524AL883B.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC2524ADW      | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2524ADW.A    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2524ADWG4    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2524AN       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2524AN.A     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3524ADW      | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3524ADW.A    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3524AN       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3524AN.A     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3524ANG4     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

## GENERIC PACKAGE VIEW

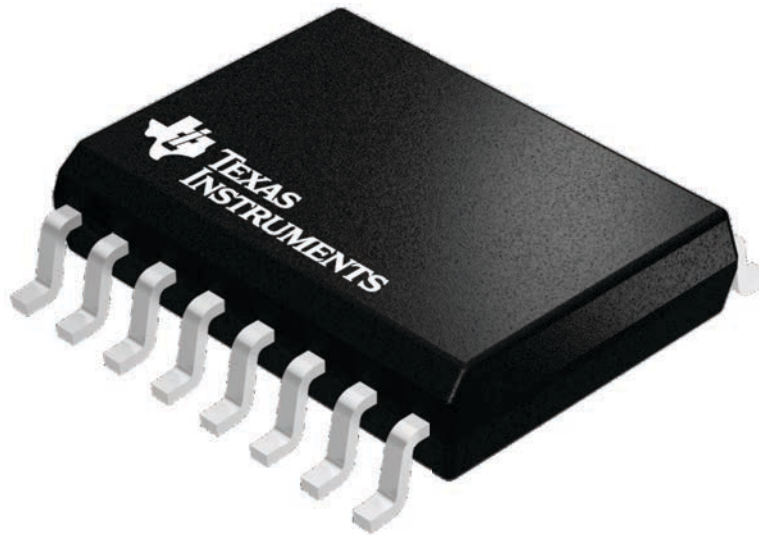
**DW 16**

**SOIC - 2.65 mm max height**

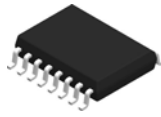
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



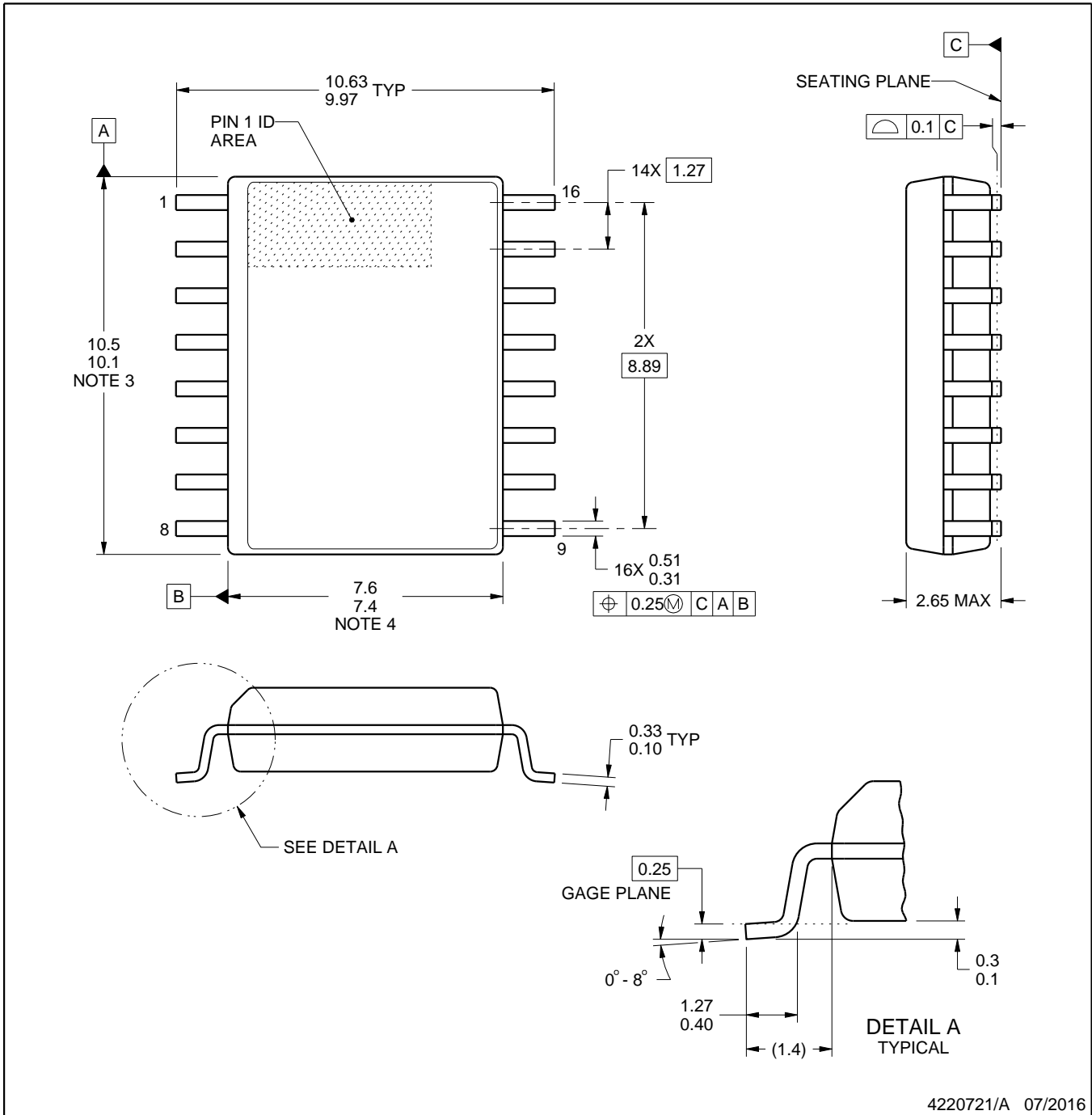
4224780/A



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

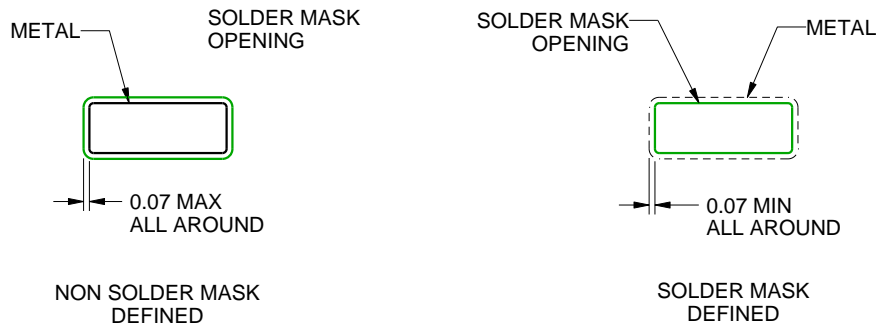
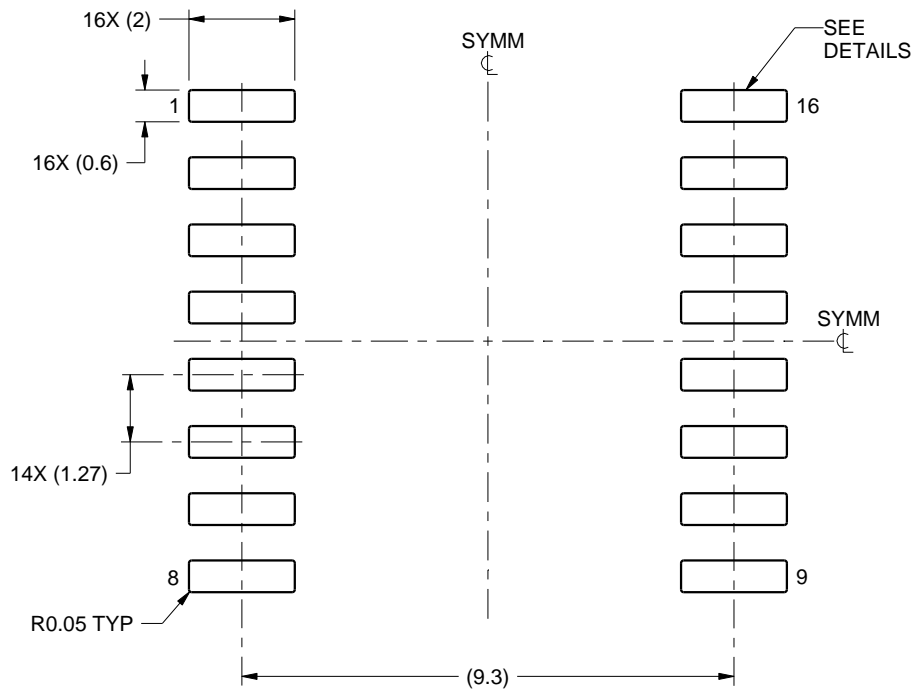
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

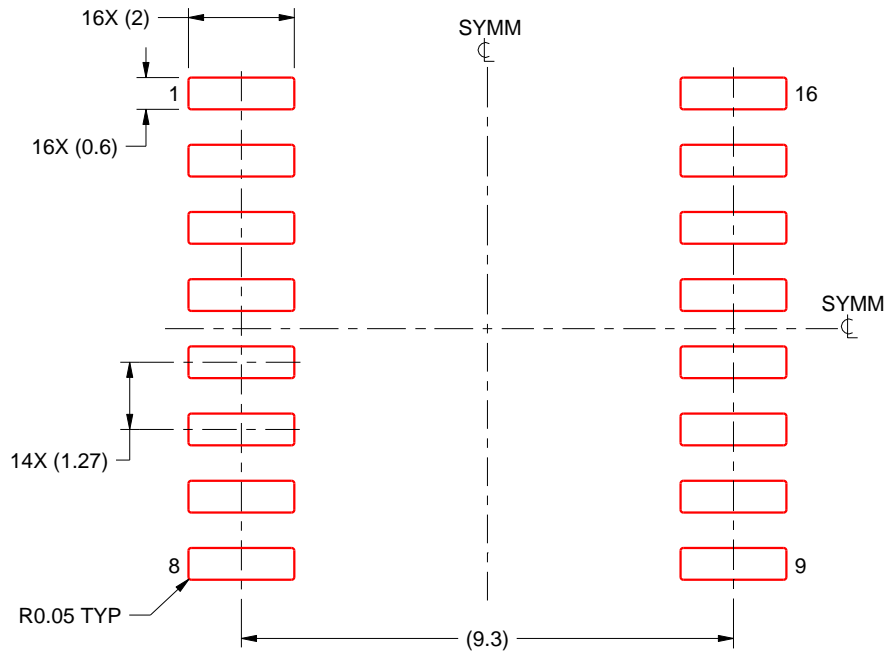
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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