



Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-current, Off-line Start Circuit
- Voltage Feed Forward or Current Mode Control
- Guaranteed Duty Cycle Clamp
- PWM Latch for Single Pulse per Period
- Pulse-by-Pulse Current Limiting Plus Shutdown for Over-Current Fault
- No Start-up or Shutdown Transients
- Slow Turn-on Both Initially and After Fault Shutdown
- Shutdown Upon Over- or Under-Voltage Sensing
- Latch Off or Continuous Retry After Fault
- PWM Output Switch Usable to 1A Peak Current
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL Package

DESCRIPTION

The UC1841 family of PWM controllers has been designed to increase the level of versatility while retaining all of the performance features of the earlier UC1840 devices. While still optimized for highly-efficient bootstrapped primary-side operation in forward or flyback power converters, the UC1841 is equally adept in implementing both low and high voltage input DC to DC converters. Important performance features include a low-current starting circuit, linear feed-forward for constant volt-second operation, and compatibility with either voltage or current mode topologies.

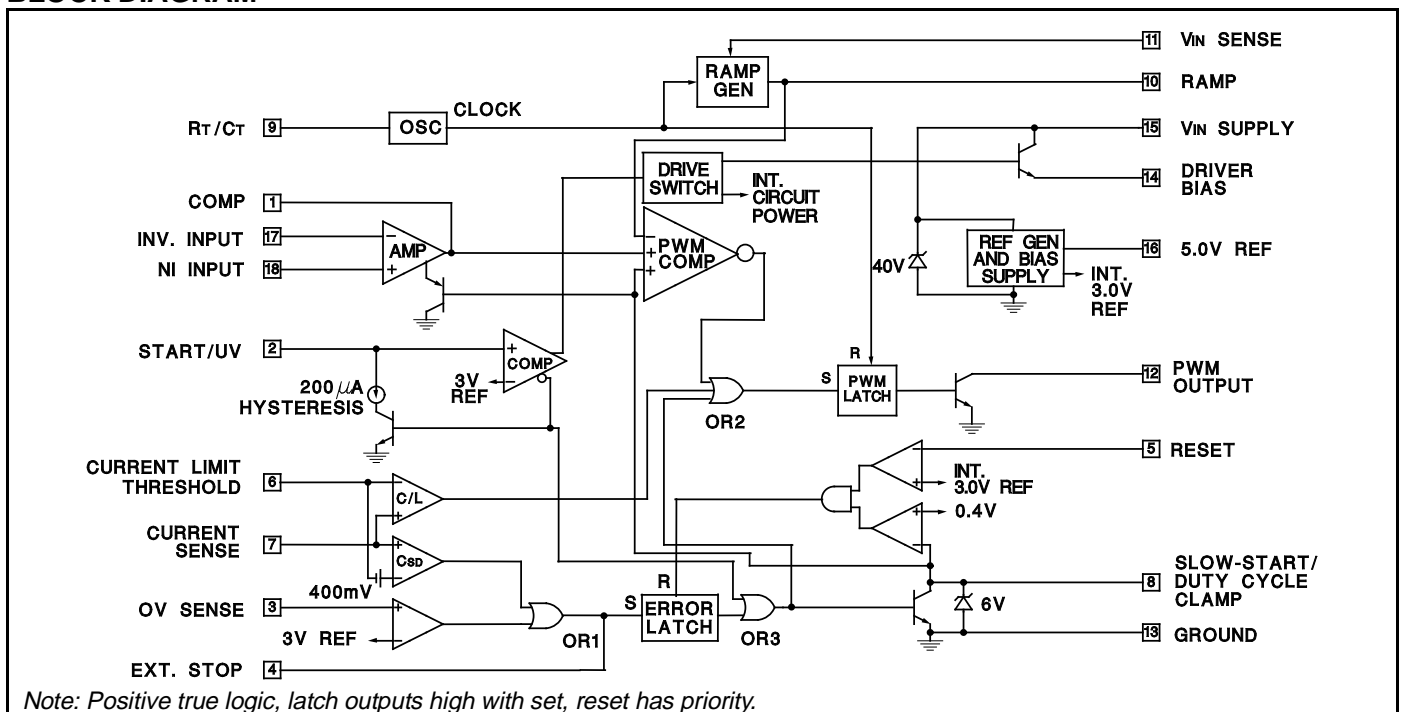
In addition to start-up and normal regulating PWM functions, these devices include built in protection from over-voltage, under-voltage, and over-current fault conditions with the option for either latch-off or automatic restart.

While pin compatible with the UC1840 in all respects except that the polarity of the External Stop has been reversed, the UC1841 offers the following improvements:

1. Fault latch reset is accomplished with slow start discharge rather than recycling the input voltage to the chip.
2. The External Stop input can be used for a fault delay to resist shutdown from short duration transients.
3. The duty-cycle clamping function has been characterized and specified.

The UC1841 is characterized for -55°C to +125°C operation while the UC2841 and UC3841 are designed for -25°C to +85°C and 0° to +70°C, respectively.

BLOCK DIAGRAM



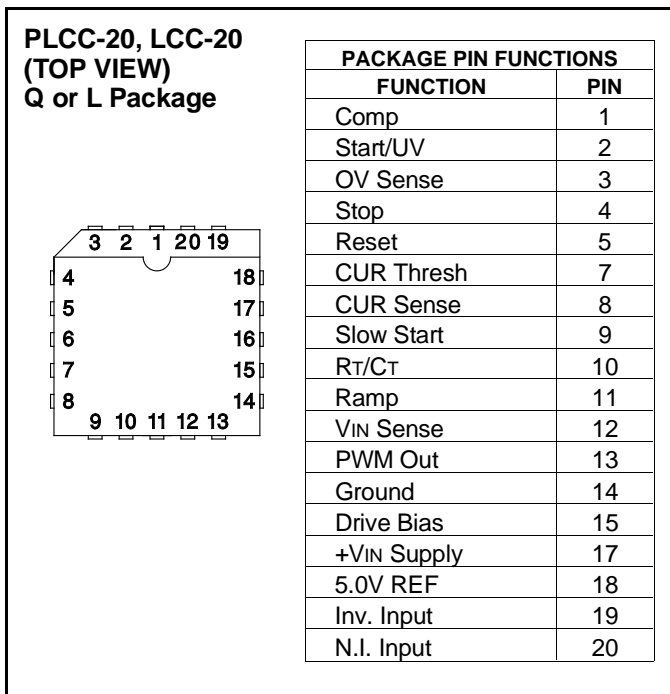
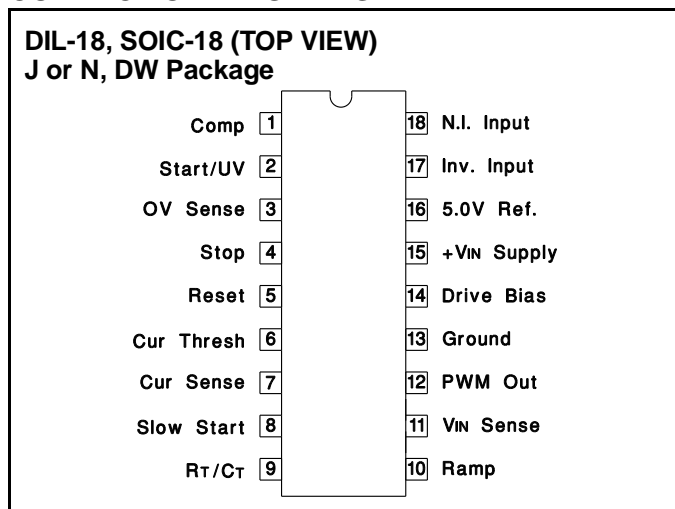
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V_{IN} (Pin 15) (Note 2)
 Voltage Driven +32V
 Current Driven, 100mA maximum. Self-limiting
 PWM Output Voltage (Pin 12) 40V
 PWM Output Current, Steady-State (Pin 12) 400mA
 PWM Output Peak Energy Discharge 20μJoules
 Driver Bias Current (Pin 14) -200mA
 Reference Output Current (Pin 16) -50mA
 Slow-Start Sink Current (Pin 8) 20mA
 V_{IN} Sense Current (Pin 11) 10mA
 Current Limit Inputs (Pins 6 & 7) -0.5 to +5.5V
 Stop Input (Pin 4) -0.3 to +5.5V
 Comparator Inputs
 (Pins 1, 7, 9-11, 16) Internally clamped at 12V
 Power Dissipation at T_A = 25°C (Note 3) 1000mW
 Power Dissipation at T_C = 25°C (Note 3) 2000mW

Operating Junction Temperature -55°C to +150°C
 Storage Temperature Range. -65°C to +150°C
 Lead Temperature (Soldering, 10 sec) +300°C

Note 1: All voltages are with respect to ground, Pin 13.
 Currents are positive-into, negative-out of the specified terminal.
 Note 2: All pin numbers are referenced to DIL-18 package.
 Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

| PARAMETER | TEST CONDITIONS | UC1841 / UC2841 | | | UC3841 | | | UNITS |
|--------------------------|----------------------------------------------|-----------------|-----|------|--------|-----|------|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Power Inputs | | | | | | | | |
| Start-Up Current | V _{IN} = 30V, Pin 2 = 2.5V | | 4.5 | 6 | | 4.5 | 6 | mA |
| Operating Current | V _{IN} = 30V, Pin 2 = 3.5V | | 10 | 14 | | 10 | 14 | mA |
| Supply OV Clamp | I _{IN} = 20mA | 33 | 40 | 45 | 33 | 40 | 45 | V |
| Reference Section | | | | | | | | |
| Reference Voltage | T _J = 25°C | 4.95 | 5.0 | 5.05 | 4.9 | 5.0 | 5.1 | V |
| Line Regulation | V _{IN} = 8 to 30V | | 10 | 15 | | 10 | 20 | mV |
| Load Regulation | I _L = 0 to 10mA | | 10 | 20 | | 10 | 30 | mV |
| Temperature Stability | Over Operating Temperature Range | 4.9 | | 5.1 | 4.85 | | 5.15 | V |
| Short Circuit Current | V _{REF} = 0, T _J = 25°C | | -80 | -100 | | -80 | -100 | mA |
| Oscillator | | | | | | | | |
| Nominal Frequency | T _J = 25°C | 47 | 50 | 53 | 45 | 50 | 55 | kHz |
| Voltage Stability | V _{IN} = 8 to 30V | | 0.5 | 1 | | 0.5 | 1 | % |
| Temperature Stability | Over Operating Temperature Range | 45 | | 55 | 43 | | 57 | kHz |
| Maximum Frequency | R _T = 2kΩ, C _T = 330pF | 500 | | | 500 | | | kHz |

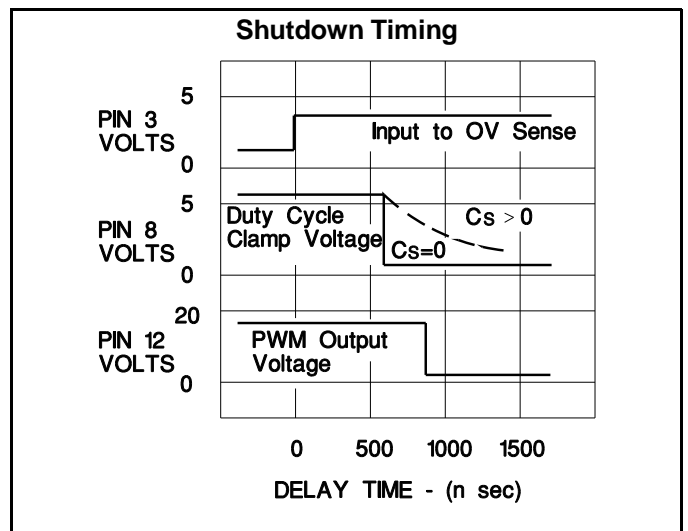
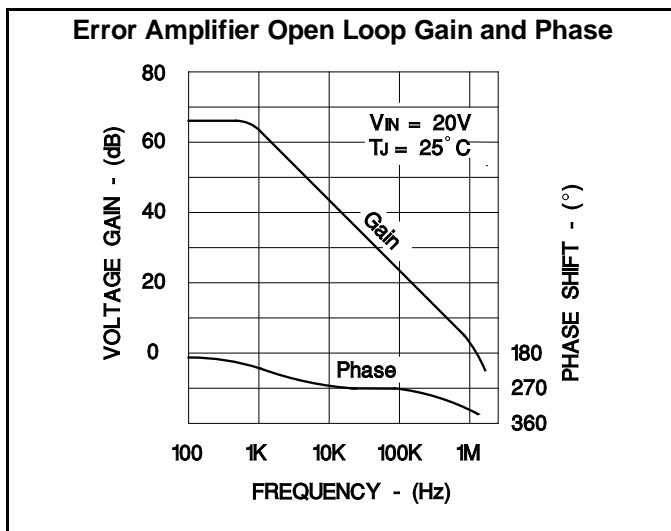
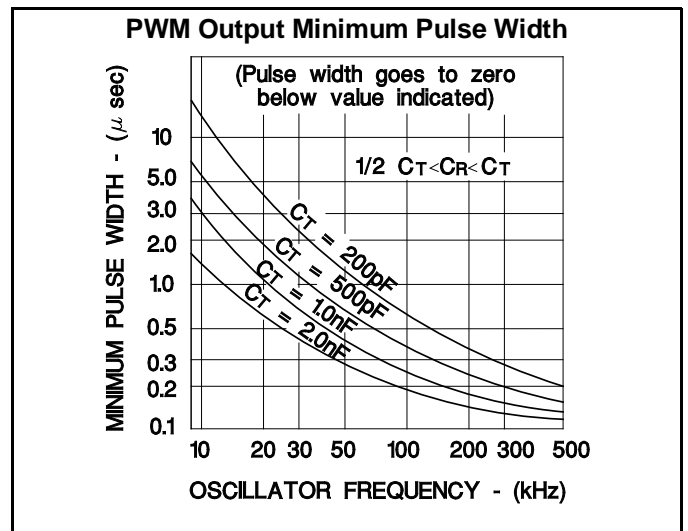
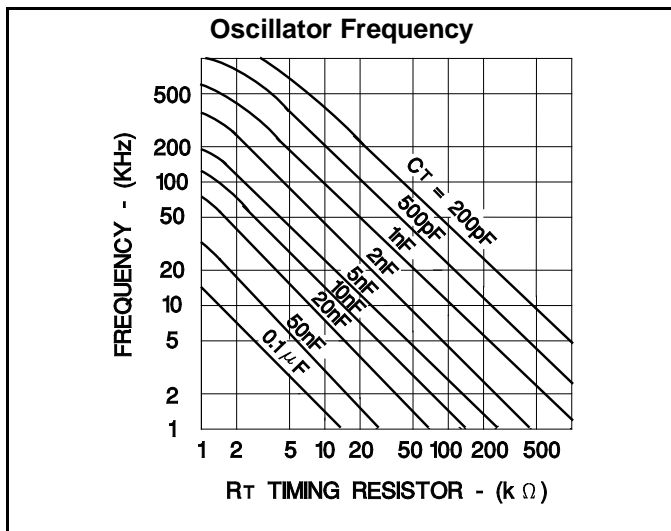
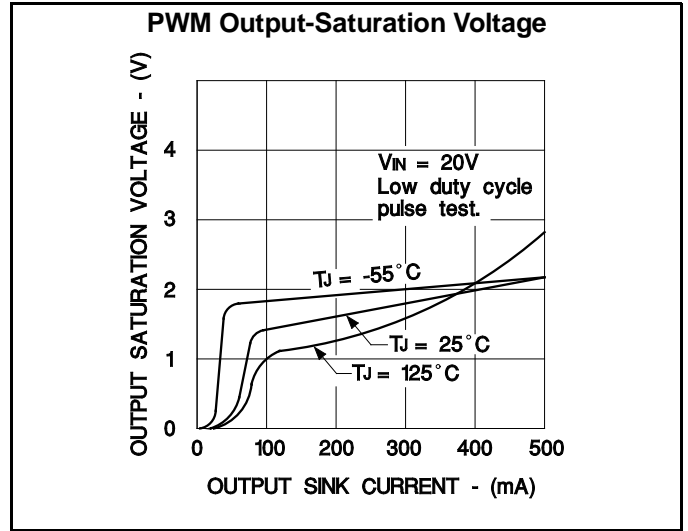
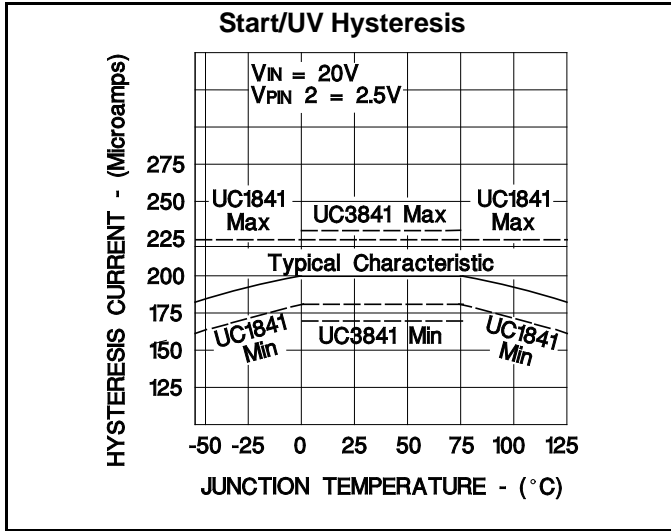
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1841, -25°C to $+85^\circ\text{C}$ for the UC2841, and 0°C to $+70^\circ\text{C}$ for the UC3841; $V_{IN} = 20\text{V}$, $R_T = 20\text{k}\Omega$, $C_T = .001\text{mfd}$, $R_R = 10\text{k}\Omega$, $C_R = .001\text{mfd}$, Current Limit Threshold = 200mV , $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1841 / UC2841 | | | UC3841 | | | UNITS |
|---------------------------------------------------------------|---------------------------------------------------------------------|-----------------|------|------|--------|------|------|------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Ramp Generator | | | | | | | | |
| Ramp Current, Minimum | $I_{SENSE} = -10\mu\text{A}$ | | -11 | -14 | | -11 | -14 | μA |
| Ramp Current, Maximum | $I_{SENSE} = 1.0\text{mA}$ | -0.9 | -95 | | -0.9 | -95 | | mA |
| Ramp Valley | | 0.3 | 0.4 | 0.6 | 0.3 | 0.4 | 0.6 | V |
| Ramp Peak | Clamping Level | 3.9 | 4.2 | 4.5 | 3.9 | 4.2 | 4.5 | V |
| Error Amplifier | | | | | | | | |
| Input Offset Voltage | $V_{CM} = 5.0\text{V}$ | | 0.5 | 5 | | 2 | 10 | mV |
| Input Bias Current | | | 0.5 | 2 | | 1 | 5 | μA |
| Input Offset Current | | | | 0.5 | | | 0.5 | μA |
| Open Loop Gain | $\Delta V_O = 1$ to 3V | 60 | 66 | | 60 | 66 | | dB |
| Output Swing (Max. Output \leq Ramp Peak - 100mV) | Minimum Total Range | 0.3 | | 3.5 | 0.3 | | 3.5 | V |
| CMRR | $V_{CM} = 1.5$ to 5.5V | 70 | 80 | | 70 | 80 | | dB |
| PSRR | $V_{IN} = 8$ to 30V | 70 | 80 | | 70 | 80 | | dB |
| Short Circuit Current | $V_{COMP} = 0\text{V}$ | | -4 | -10 | | -4 | -10 | mA |
| Gain Bandwidth* | $T_J = 25^\circ\text{C}$, $A_{VOL} = 0\text{dB}$ | 1 | 2 | | 1 | 2 | | MHz |
| Slew Rate* | $T_J = 25^\circ\text{C}$, $A_{VCL} = 0\text{dB}$ | | 0.8 | | | 0.8 | | $\text{V}/\mu\text{s}$ |
| PWM Section | | | | | | | | |
| Continuous Duty Cycle Range* (other than zero) | Minimum Total Continuous Range, Ramp Peak $< 4.2\text{V}$ | 4 | | 95 | 4 | | 95 | % |
| 50% Duty Cycle Clamp | R_{SENSE} to $V_{REF} = 10\text{k}$ | 42 | 47 | 52 | 42 | 47 | 52 | % |
| Output Saturation | $I_{OUT} = 20\text{mA}$ | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| | $I_{OUT} = 200\text{mA}$ | | 1.7 | 2.2 | | 1.7 | 2.2 | V |
| Output Leakage | $V_{OUT} = 40\text{V}$ | | 0.1 | 10 | | 0.1 | 10 | μA |
| Comparator Delay* | Pin 8 to Pin 12, $T_J = 25^\circ\text{C}$, $R_L = 1\text{k}\Omega$ | | 300 | 500 | | 300 | 500 | ns |
| Sequencing Functions | | | | | | | | |
| Comparator Thresholds | Pins 2, 3, 5 | 2.8 | 3.0 | 3.2 | 2.8 | 3.0 | 3.2 | V |
| Input Bias Current | Pins 3, 5 = 0V | | -1.0 | -4.0 | | -1.0 | -4.0 | μA |
| Input Leakage | Pins 3, 5 = 10V | | 0.1 | 2.0 | | 0.1 | 2.0 | μA |
| Start/UV Hysteresis Current | Pin 2 = 2.5V | 170 | 200 | 220 | 170 | 200 | 230 | μA |
| Ext. Stop Threshold | Pin 4 | 0.8 | 1.6 | 2.4 | 0.8 | 1.6 | 2.4 | V |
| Error Latch Activate Current | Pin 4 = 0V , Pin 3 $> 3\text{V}$ | | -120 | -200 | | -120 | -200 | μA |
| Driver Bias Saturation Voltage, $V_{IN} - V_{OH}$ | $I_B = -50\text{mA}$ | | 2 | 3 | | 2 | 3 | V |
| Driver Bias Leakage | $V_B = 0\text{V}$ | | -0.1 | -10 | | -0.1 | -10 | μA |
| Slow-Start Saturation | $I_S = 10\text{mA}$ | | 0.2 | 0.5 | | 0.2 | 0.5 | V |
| Slow-Start Leakage | $V_S = 4.5\text{V}$ | | 0.1 | 2.0 | | 0.1 | 2.0 | μA |
| Current Control | | | | | | | | |
| Current Limit Offset | | | 0 | 5 | | 0 | 10 | mV |
| Current Shutdown Offset | | 370 | 400 | 430 | 360 | 400 | 440 | mV |
| Input Bias Current | Pin 7 = 0V | | -2 | -5 | | -2 | -5 | μA |
| Common Mode Range* | | -0.4 | | 3.0 | -0.4 | | 3.0 | V |
| Current Limit Delay* | $T_J = 25^\circ\text{C}$, Pin 7 to 12, $R_L = 1\text{k}$ | | 200 | 400 | | 200 | 400 | ns |

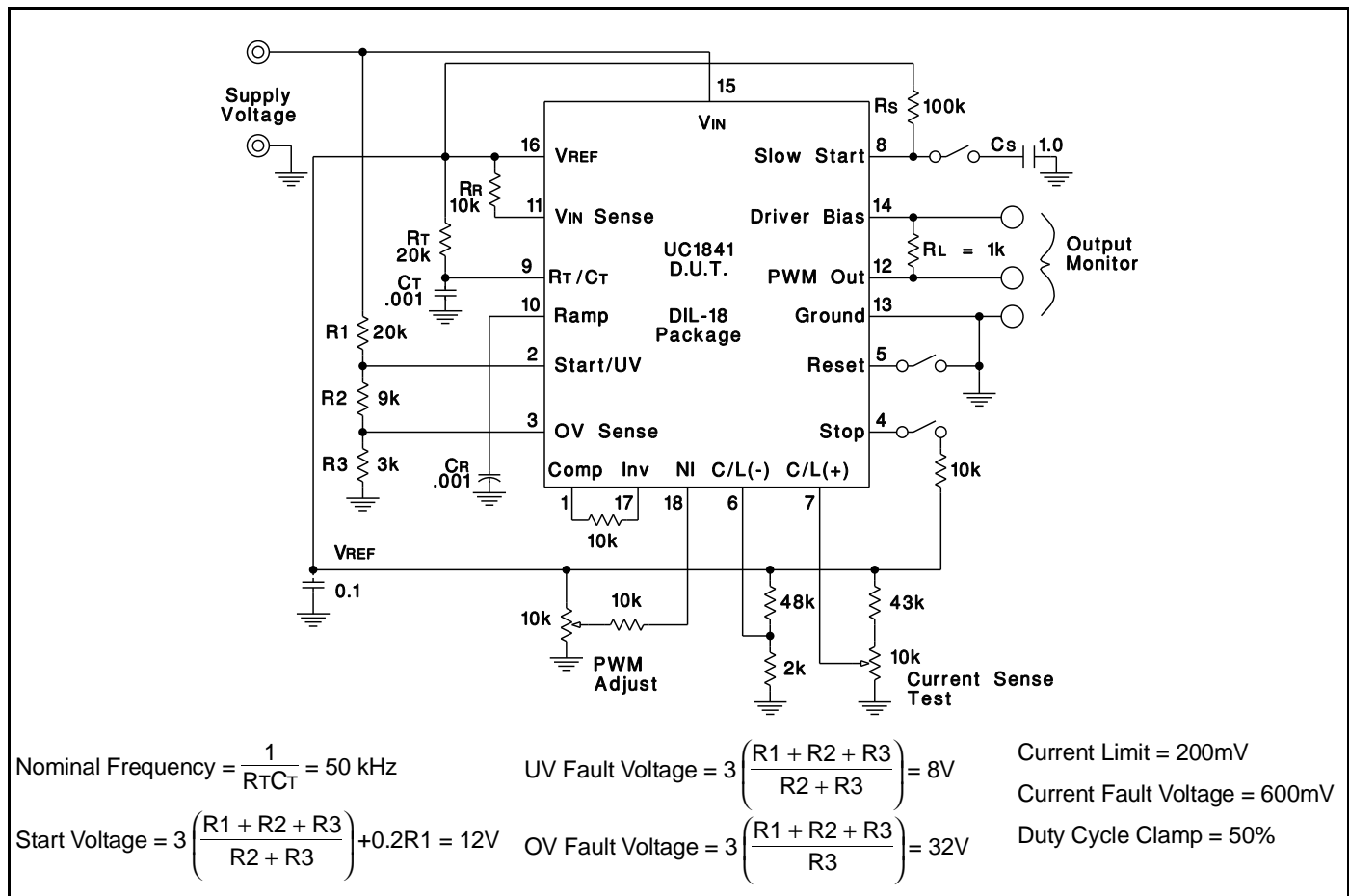
* These parameters are guaranteed by design but not 100% tested in production.

FUNCTIONAL DESCRIPTION

| PWM CONTROL | |
|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1. Oscillator | Generates a fixed-frequency internal clock from an external R_T and C_T . Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first order correction factor $\approx 0.3 \log(C_T \times 10^{12})$. |
| 2. Ramp Generator | Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. Limiting the minimum value for I_{SENSE} will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control. |
| 3. Error Amplifier | Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot. |
| 4. Reference Generator | Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm 2\%$. 40V clamp zener for chip OV protection, 100mA maximum current. |
| 5. PWM Comparator | Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs. |
| 6. PWM Latch | Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse. |
| 7. PWM Output Switch | Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp. |
| SEQUENCING FUNCTIONS | |
| 1. Start/UV Sense | With an increasing voltage, it generates a turn-on signal and releases the slow-start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200 μ A hysteresis current. |
| 2. Drive Switch | Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold. |
| 3. Driver Bias | Supplies drive current to external power switch to provide turn-on bias. |
| 4. Slow Start | Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider. |
| PROTECTION FUNCTIONS | |
| 1. Error Latch | When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (typically 3V) b. Stop > 2.4V (typically 1.6V) c. Current Sense 400mV over threshold (typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin 5 < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set. |
| 2. Current Limiting | Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch. |
| 3. External Stop | A voltage over 1.2V will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a typical delay of 13ms/ μ F. |



OPEN-LOOP TEST CIRCUIT



FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling – a task made even easier with the UC1841's feed-forward line regulation.

An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output.

Not shown, are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Q_s , or the application; however, one example of power transistor interfacing is provided on the following page.

REGULATOR APPLICATION (B)

With the addition of a level shifting transistor, Q1, the UC1841 is an ideal control circuit for DC to DC converters such as the buck regulator shown in Figure B opposite. In addition to providing constant current drive pulses to the PIC661 power switch, this circuit has full fault protection and high speed dynamic line regulation due to its feed-forward capability. An additional feature is the ability to

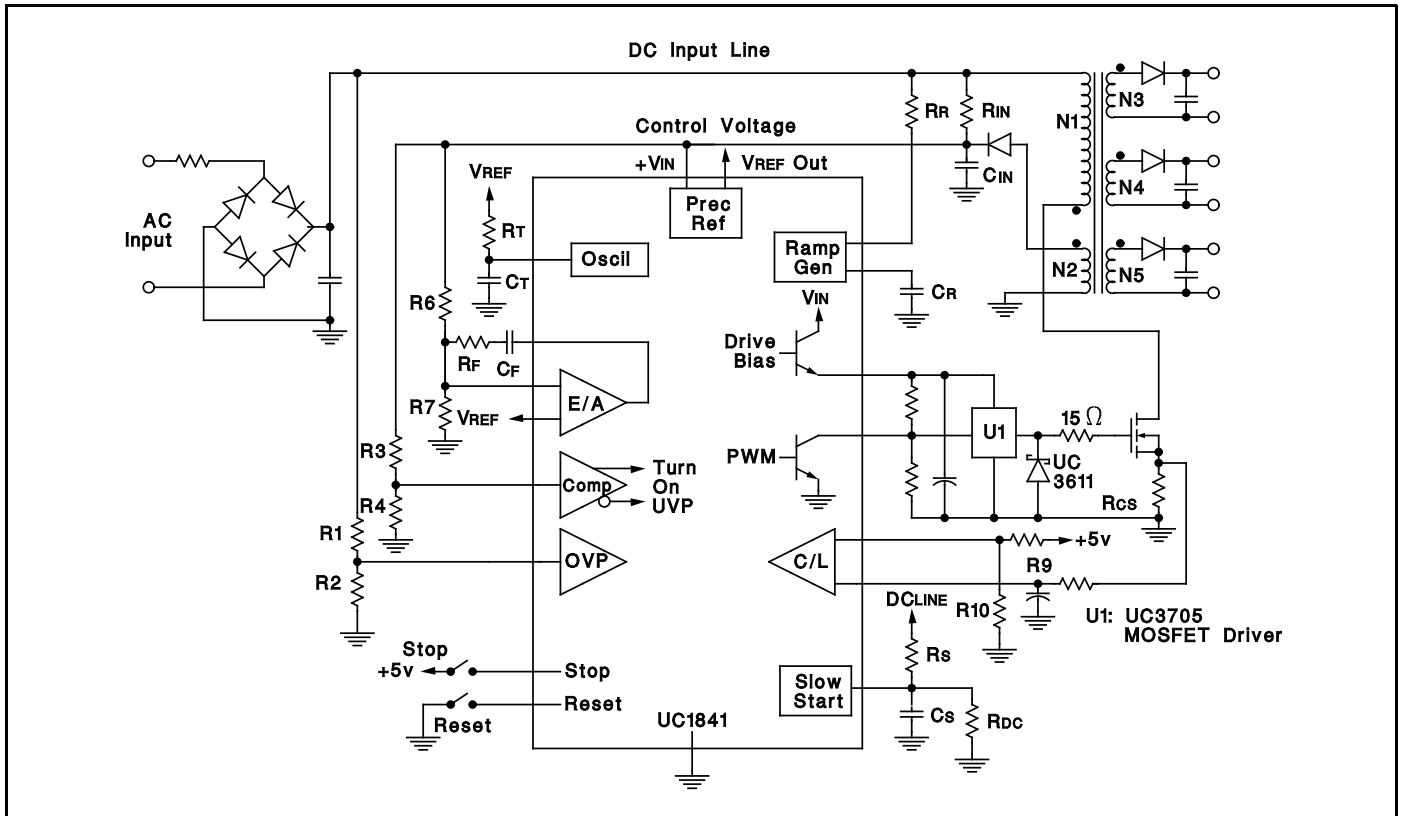


Figure A. UC1841 Programmable PWM Controller In A Simplified Flyback Regulator

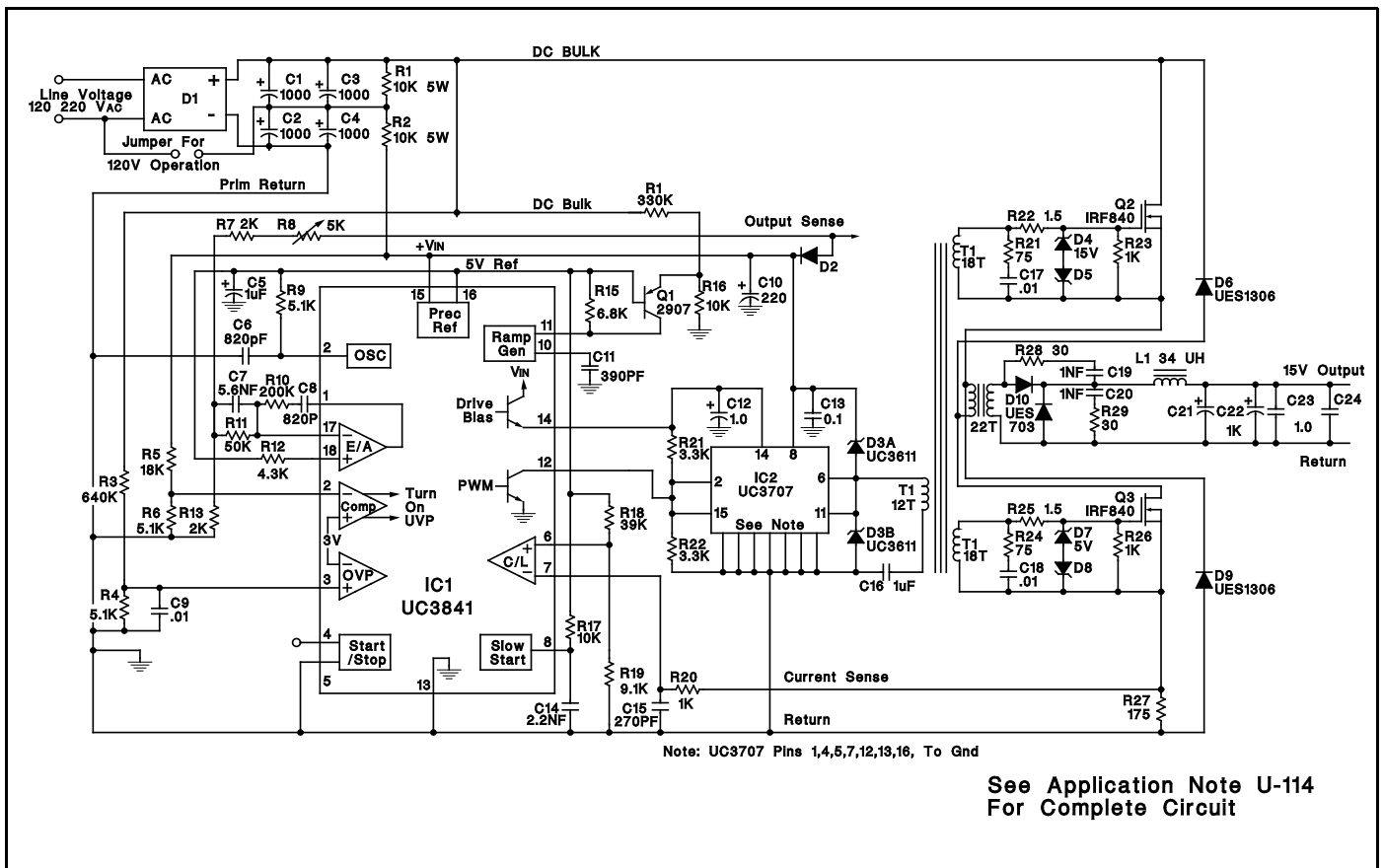
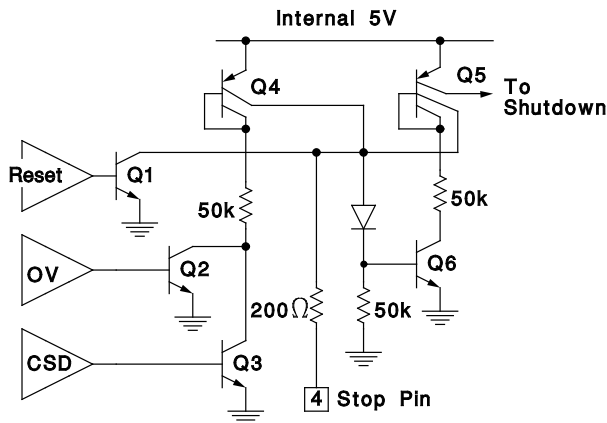


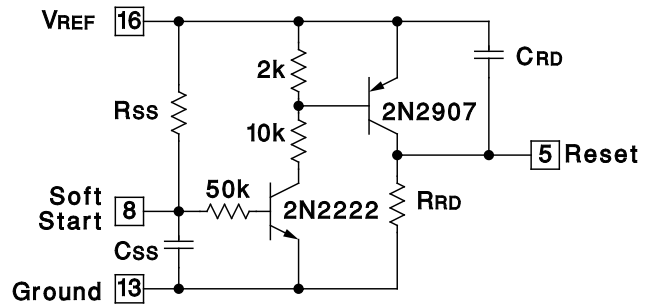
Figure B. Overall Schematic For A 300 Watt, Off-line Power Converter Using The UC3841 For Control

ERROR LATCH INTERNAL CIRCUITRY



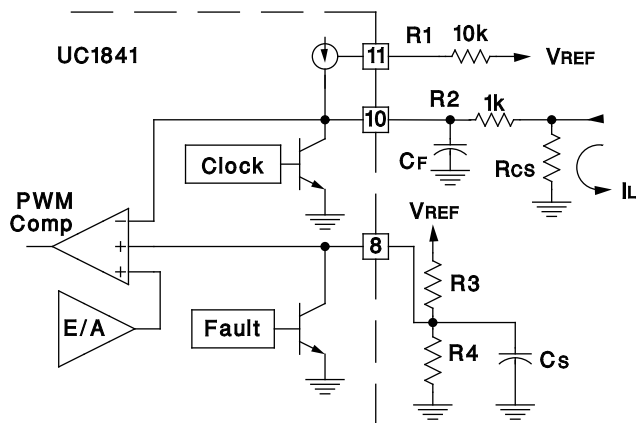
The Error Latch consists of Q5 and Q6 which, when both on, turns off the PWM Output and pulls the Slow-Start pin low. This latch is set by either the Over-Voltage or Current Shutdown comparators, or by a high signal on Pin 4. Reset is accomplished by either the Reset comparator or a low signal on Pin 4. An activation time delay can be provided with an external capacitor on Pin 4 in conjunction with the $\approx 100\mu\text{A}$ collector current from Q4.

PROGRAMMABLE SOFT START AND RESTART DELAY CIRCUIT



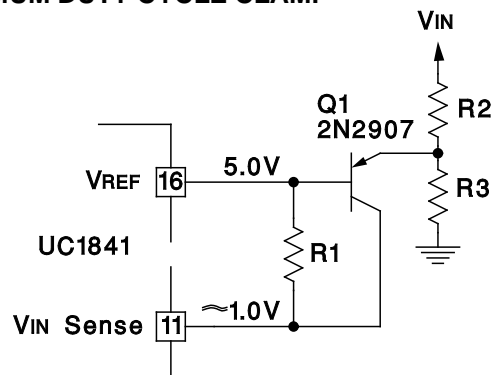
$$\text{Restart Delay} = (.51)(\text{RRD})(\text{CRD})$$

CURRENT MODE CONTROL



Since Pin 10 is a direct input to the PWM comparator, this point can also serve as a current sense port for current mode control. In this application, current sensing is ground referenced through R_{cs} . Resistor R_1 sets a 400mV offset across R_2 (assuming $R_2 > R_{cs}$) so that both the Error Amplifier and Fault Shutdown can force the current completely to zero. R_2 is also used along with C_f as a small filter to attenuate leading-edge spikes on the load current waveform. In this mode, current limiting can be accomplished by divider R_3/R_4 which forms a clamp overriding the output of the Error Amplifier.

VOLTAGE FEED-FORWARD COMBINED WITH MAXIMUM DUTY-CYCLE CLAMP



In this circuit, R_1 is used in conjunction with C_R (not shown) to establish a minimum ramp charging current such that the ramp voltage reaches 4.2V at the required maximum output pulse width.

The purpose of Q_1 is to provide an increasing ramp current above a threshold established by R_2 and R_3 such that the duty cycle is further reduced with increasing V_{IN} .

The minimum ramp current is:

$$I_{R(\text{MIN})} = \frac{V_{\text{REF}} - V_{\text{IN SENSE}}}{R_1} \approx \frac{4V}{R_1}$$

The threshold where V_{IN} begins to add extra ramp current is:

$$V_{IN} \approx 5.6V \left(\frac{R_2 + R_3}{R_3} \right)$$

Above the threshold, the ramp current will be:

$$I_{R(\text{VARIAB})} \approx \frac{4}{R_1} + \frac{V_{IN} - 5.6}{R_2} - \frac{5.6}{R_3}$$

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| UC2841DW | NRND | Production | SOIC (DW) 18 | 40 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -20 to 85 | UC2841DW |
| UC2841DW.A | NRND | Production | SOIC (DW) 18 | 40 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -20 to 85 | UC2841DW |
| UC2841N | NRND | Production | PDIP (N) 18 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -20 to 85 | UC2841N |
| UC2841N.A | NRND | Production | PDIP (N) 18 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -20 to 85 | UC2841N |
| UC3841N | NRND | Production | PDIP (N) 18 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | UC3841N |
| UC3841N.A | NRND | Production | PDIP (N) 18 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | UC3841N |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| UC2841DW | DW | SOIC | 18 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2841DW.A | DW | SOIC | 18 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2841N | N | PDIP | 18 | 20 | 506 | 13.97 | 11230 | 4.32 |
| UC2841N.A | N | PDIP | 18 | 20 | 506 | 13.97 | 11230 | 4.32 |
| UC3841N | N | PDIP | 18 | 20 | 506 | 13.97 | 11230 | 4.32 |
| UC3841N.A | N | PDIP | 18 | 20 | 506 | 13.97 | 11230 | 4.32 |

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