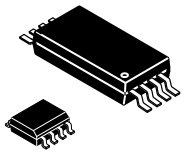


SLUS232E – DECEMBER 19, 2002 – REVISED JULY 2011

LOAD SHARE CONTROLLER

FEATURES

- **2.7-V to 20-V Operation**
- **8-Pin Package**
- **Requires Minimum Number of External Components**
- **Compatible with Existing Power Supply Designs Incorporating Remote Output Voltage Sensin**
- **Differential Share Bus**
- **Precision Current Sense Amplifier (40 Gain)**
- **UVLO (Undervoltage Lockout) Circuitry**
- **User Programmable Share Loop Compensation**

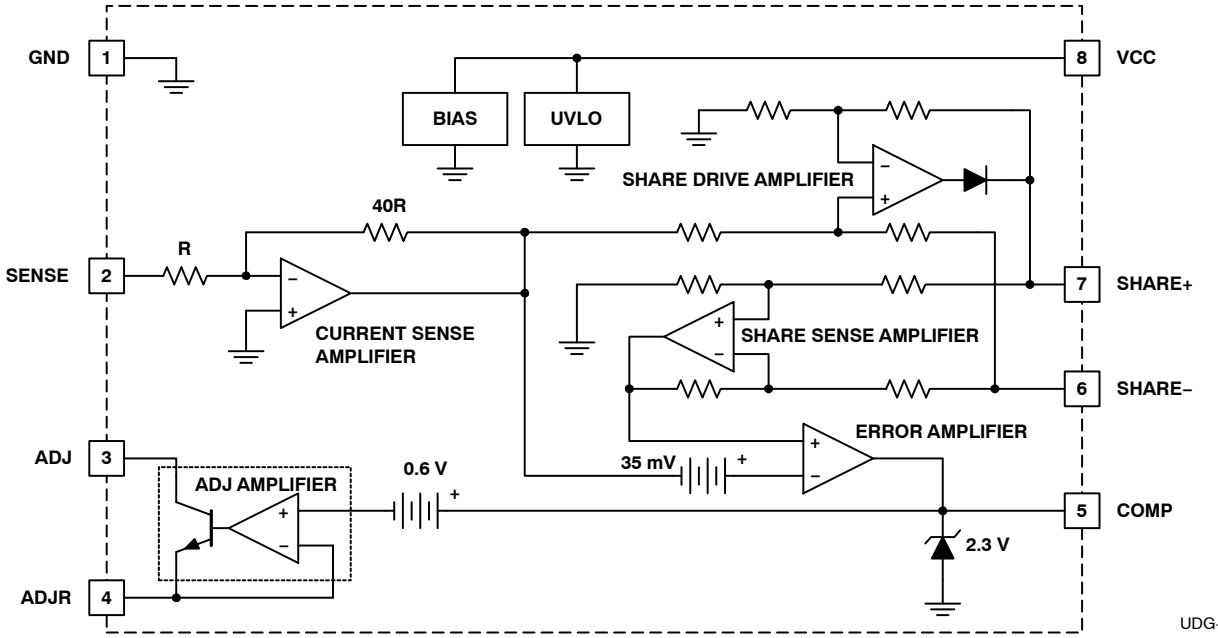
APPLICATIONS

- **Paralelled Power Supplies**

DESCRIPTION

The UC3902 load share controller is an 8-pin device that balances the current drawn from independent, paralleled power supplies. Load sharing is accomplished by adjusting each supplies' output current to a level proportional to the voltage on a share bus.

The master power supply, which is automatically designated as the supply that regulates to the highest voltage, drives the share bus with a voltage proportional to its output current. The UC3902 trims the output voltage of the other paralleled supplies so that they each support their share of the load current. Typically, each supply is designed for the same current level although that is not necessary for use with the UC3902. By appropriately scaling the current sense resistor, supplies with different output current capability can be paralleled with each supply providing the same percentage of their output current capability for a particular load.



DESCRIPTION (continued)

A differential line is used for the share bus to maximize noise immunity and accommodate different voltage drops in each power converter's ground return line. Trimming of each converter's output voltage is accomplished by injecting a small current into the output voltage sense line, which requires a small resistance (typically 20 Ω to 100 Ω) to be inserted.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UC2902 UC3902	UNIT
Input voltage range, V_I	VCC, ADJ	–0.3 to 20	V
	SENSE	–5 to 5	
	ADJR, COMP	–0.3 to 4	
	SHARE–, SHARE+	–0.3 to 10	
Output current, I_O	SHARE+	–100 mA to 10 mA	mA
	ADJ	–1 mA to 30 mA	mA
Operating free-air temperature range, T_A		–40 to 100	°C
Junction temperature range, T_J		–55 to 105	
Storage temperature, T_{stg}		–65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Voltages are with respect to GND. Currents are positive into, and negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power SUPPLY SUPPLY CURRENT						
I_{CC}	Supply current	SHARE+ = 1 V, SENSE = 0 V		4	6	mA
		V_{CC} = 20 V		6	10	
UNDERVOLTAGE LOCKOUT						
V_{CC}	Startup voltage	SHARE+ = 0.2 V, SENSE = 0 V, COMP = 1 V	2.3	2.5	2.7	V
	Hysteresis	SHARE+ = 0.2 V, SENSE = 0 V, COMP = 1 V	60	100	140	mV
CURRENT SENSE AMPLIFIER						
V_{IO}	Input offset voltage	0.1 V ≤ $V_{(SHARE+)}$ ≤ 1.1 V	–2.5	–0.5	1.5	mV
	SENSE to SHARE gain	0.1 V ≤ $V_{(SHARE+)}$ ≤ 1.1 V	–41	–40	–39	V
R_{IN}	Input resistance		0.6	1	1.5	V
SHARE DRIVE AMPLIFIER						
V_{OH}	High-level output voltage, SHARE+	V_{CC} = 2.5 V, $V_{(SENSE)}$ = –50 mV, $I_{(SHARE+)}$ = –1 mA	1.2	1.4		V
		V_{CC} = 12 V, $V_{(SENSE)}$ = –250 mV, $I_{(SHARE+)}$ = –1 mA	9.6	10.0	10.4	
		V_{CC} = 20 V, $V_{(SENSE)}$ = –250 mV, $I_{(SHARE+)}$ = –1 mA	9.6	10.0	10.4	
V_{OL}	Low-level output voltage, SHARE+	V_{CC} = 2.5 V, $V_{(SENSE)}$ = 10 mV, $I_{(SHARE+)}$ = –1 mA		20	50	mV
		V_{CC} = 12 V, $V_{(SENSE)}$ = 10 mV, $I_{(SHARE+)}$ = –1 mA		20	50	
		V_{CC} = 20 V, $V_{(SENSE)}$ = 10 mV, $I_{(SHARE+)}$ = –1 mA		20	50	
V_O	Output voltage, SHARE+	$V_{(SENSE)}$ = 0 mV, $R_{(SHARE+)}$ = 200 Ω (SHARE+ to GND)		20	40	
CMRR	Common mode rejection ratio	0 V ≤ $V_{(SHARE–)}$ ≤ 1 V, SENSE used as input to amplifier	50	90		dB
	Load regulation	Load on SHARE+, 1 mA ≤ I_{LOAD} ≤ –20 mA, $V_{(SENSE)}$ = –25 mV		0	20	mV
I_{SC}	Short circuit current	$V_{(SHARE+)}$ = 0 V, $V_{(SENSE)}$ = –25 mV	–85	–50	–20	mA
	Slew rate	$V_{(SENSE)}$ = 10 mV to –90 mV step, $R_{(SHARE+)}$ = 200 Ω (SHARE+ to GND)	0.12	0.26	0.38	V/μs
		$V_{(SENSE)}$ = –90 mV to 10 mV step, $R_{(SHARE+)}$ = 200 Ω (SHARE+ to GND)	0.12	0.26	0.38	

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 105°C, (unless otherwise noted)

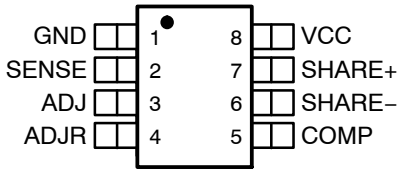
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHARE SENSE AMPLIFIER						
R_{IN}	Input impedance	$V_{(SHARE+)}$ = 1 V, $V_{(SHARE–)}$ = GND $V_{(SENSE)}$ = 10 mV	8	15		kΩ
		$R_{(SHARE+)}$ = 200 Ω (SHARE+ to GND) $V_{(SHARE–)}$ = 1 V, $V_{(SENSE)}$ = 10 mV	8	15		
$V_{(SHARE)}$	Threshold voltage	$V_{(SENSE)}$ = 0 V	41	70	100	mV
CMRR	Common mode rejection ratio	0 V ≤ $V_{(SHARE–)}$ ≤ 1 V, $V_{(SENSE)}$ = –2.5 mV	50	60		dB
AVOL	DESCRIPTION from SHARE+ to ADJR	$V_{(SENSE)}$ = –2.5 mV, 5 nF capacitor from COMP to GND, 1 kΩ resistor from ADJR to GND	50	68		
		$V_{(SENSE)}$ = –2.5 mV, 5 nF capacitor from COMP to GND, 150 Ω resistor from ADJR to GND	50	66		
	Slew rate	$V_{(SHARE+)}$ = 0 mV to 10 V step through a 200-Ω resistor, $R_{(COMP)}$ = 500 Ω, $V_{(SENSE)}$ = 10 mV, V_{CC} = 10 V	0.2	0.5	0.8	V/μs
ERROR AMPLIFIER						
g_M	Transconductance, SHARE+ to COMP	200-Ω resistor SHARE+ to GND	3.0	4.5	6.0	mS
I_{OH}	High-level output current	$V_{(COMP)}$ = 1.5 V, SHARE+ ≥ 300 mV $V_{(SENSE)}$ = –10 mV	–450	–325	–200	μA
I_{OL}	Low-level output current	200-Ω resistor SHARE+ to GND, $V_{(COMP)}$ = 1.5 V, $V_{(SENSE)}$ = 10 mV	80	150	250	
V_{IO}	Input offset voltage		15	35	65	mV
$\Delta V_{IO}/\Delta V_{(SENSE)}$		1-kΩ resistor ADJR to GND –2.5 mV ≤ $V_{(SENSE)}$ ≤ –25 mV	–6	0	6	mV/V
ADJ AMPLIFIER						
	ADJR low voltage	200-Ω resistor SHARE+ to GND, $V_{(SENSE)}$ = 10 mV	–1	0	1	mV
	ADJR high voltage	$V_{(SENSE)}$ = 10 mV, $V_{(SHARE+)}$ = 1 V	1.4	1.8	2.1	V
	Current gain ADJR to ADJ	$I_{(ADJR)}$ = –0.5 mA, $V_{(ADJ)}$ = 2.5 V, $V_{(SENSE)}$ = 10 mV, $V_{(SHARE+)}$ = 1 V	0.96	0.99	1.02	A/A
		$I_{(ADJR)}$ = –0.5 mA, $V_{(ADJ)}$ = 20 V, $V_{(SENSE)}$ = 10 mV, $V_{(SHARE+)}$ = 1 V	0.96	0.99	1.02	
		$I_{(ADJR)}$ = –10 mA, $V_{(ADJ)}$ = 2.5 V, $V_{(SENSE)}$ = 10 mV, $V_{(SHARE+)}$ = 1 V	0.96	0.99	1.02	
		$I_{(ADJR)}$ = –10 mA, $V_{(ADJ)}$ = 20 V, $V_{(SENSE)}$ = 10 mV, $V_{(SHARE+)}$ = 1 V	0.96	0.99	1.02	

ORDERING INFORMATION

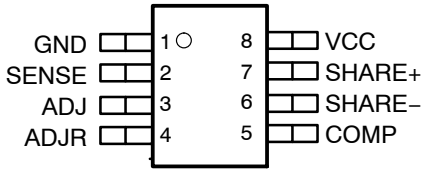
T_A	PACKAGE(2)	PART NUMBER
–40°C to 85°C	SOIC (D)	UC2902D
	Plastic DIP (N)	UC2902N
0°C to 70°C	SOIC (D)	UC3902D
	Plastic DIP (N)	UC3902N

(2) The D package is also available taped and reeled. Add an R suffix to the device type (i.e., bq24901DR) for quantities of 3,000 devices per reel.

D PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADJ	3	I	Current output of the adjust amplifier circuit (NPN collector)
ADJR	4	O	Current adjust amplifier range set (NPN emitter)
COMP	5	I/O	Output of the error amplifier, input of the adjust amplifier
GND	1	–	Local power supply return and signal ground
SENSE	2	I	Inverting input of the current sense amplifier
SHARE+	7	I/O	Positive input from share bus or drive-to-share bus
SHARE–	6	I	Reference for SHARE+ pin
VCC	8	I	Local power supply (positive)

APPLICATION INFORMATION

The values of five passive components must be determined to configure the UC3902 load share controller. The output and return lines of each converter are connected together at the load, with current sense resistor R_{SENSE} inserted in each negative return line. Another resistor, R_{ADJ}, is also inserted in each positive remote sense line. The differential share bus terminals (SHARE+ and SHARE−) of each UC3902 are connected together respectively, and the SHARE− node is also connected to the system ground. A typical application is illustrated in Figure 1.

The load share controller design can be executed by following the next few steps:

Step 1.

$$R_{SENSE} = \frac{V_{SHARE(max)}}{A_{CSA} \times I_{O(max)}} \quad (1)$$

- where A_{CSA} is 40, the gain of the current sense amplifier

At full load, the voltage drop across the R_{SENSE} resistor is $I_{O(max)} \times R_{SENSE}$. Taking into account the gain of the current sense amplifier, the voltage at full load on the current share bus,

$$V_{SHARE(max)} = \frac{A_{CSA} \times I_{O(max)}}{R_{SENSE}} \quad (2)$$

This voltage must stay 1.5-V below V_{CC} or below 10 V whichever is smaller. V_{SHARE} represents an upper limit but the designer should select the full scale share bus voltage keeping in mind that every volt on the load share bus increases the master controller's supply current by approximately 100 μA times the number of slave units connected parallel.

Step 2.

$$R_G = \frac{V_{ADJ(max)}}{I_{ADJ(max)}} \quad (3)$$

Care must be taken to ensure that $I_{ADJ(max)}$ is low enough so that both the drive current and power dissipation are within the device's capability. For most applications, an $I_{ADJ(max)}$ current between 5 mA and 10 mA is acceptable. In a typical application, a 360-Ω R_G resistor from the ADJR pin to ground sets $I_{ADJ(max)}$ to approximately 5 mA.

Step 3.

$$R_{ADJ} = \frac{\Delta V_{O(max)} - \left(I_{O(max)} \times R_{SENSE}\right)}{I_{ADJ(max)}} \quad (4)$$

R_{ADJ} must be low enough to not affect the normal operation of the converter's voltage feedback loop. Typical R_{ADJ} values are between 20 Ω to100 Ω depending on V_O, $\Delta V_{O(max)}$ and the selected $I_{ADJ(max)}$ value.

Step 4.

$$C_C = \frac{g_M}{2\pi \times f_C} \times \frac{R_{ADJ}}{R_G} \times \frac{R_{SENSE}}{R_{LOAD}} \times A_{CSA} \times A_{PWR} \quad \left(f_C\right) \quad (5)$$

The share loop compensation capacitor, C_C is calculated to produce the desired share loop unity gain crossover frequency, f_C. The share loop error amplifier's transconductance, g_M is nominally 4.5 ms. The values of the resistors are already known. Typically, f_C is set to at least one order of magnitude below the converter's closed loop bandwidth. The load share circuit is primarily intended to compensate for each converter's initial output voltage tolerance and temperature drift, not for differences in their transient response. The term $A_{PWR(fc)}$ is the gain of the power supply measured at the desired share loop crossover frequency, f_C. This gain can be measured by injecting the measurement signal between the positive output and the positive sense terminal of the power supply.

Step 5.

$$R_C = \frac{1}{2\pi \times f_C \times C_C} \tag{6}$$

A resistor in series with C_C is required to boost the phase margin of the load share loop. The zero is placed at the load share loop crossover frequency, f_C.

When the system is powered up, the converter with the highest output voltage tends to source the most current and take control of the share bus. The other converters increase their output voltages until their output currents are proportional to the share bus voltage minus 50 mV. The converter which in functioning as the master may change due to warmup drift and differences in load and line transient response of each converter.

ADDITIONAL INFORMATION

Please refer to the following topic for additional application information.

1. Application Note U−163, (TI Literature No. SLUA128) *The UC3902 Load Share Controller and Its Performance in Distributed Power Systems* by Laszlo Balogh

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2902D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2902D
UC2902D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2902D
UC2902DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2902D
UC2902DTR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2902D
UC2902DTR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2902D
UC2902N	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2902N
UC2902N.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2902N
UC3902D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3902D
UC3902D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3902D
UC3902DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3902D
UC3902DTR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3902D
UC3902DTR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3902D
UC3902N	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3902N
UC3902N.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3902N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

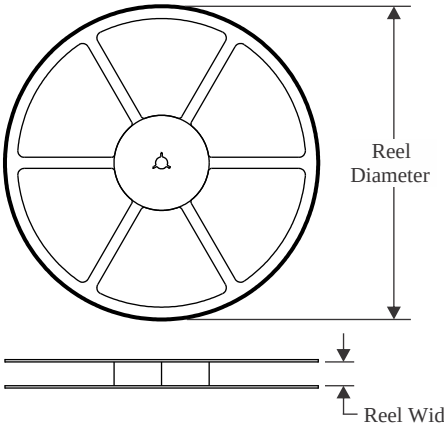
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

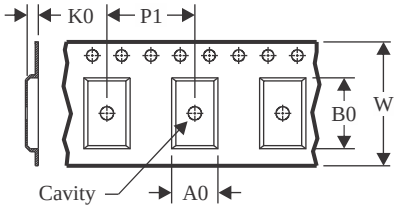
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

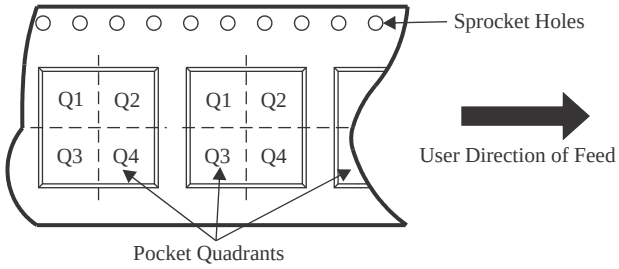


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

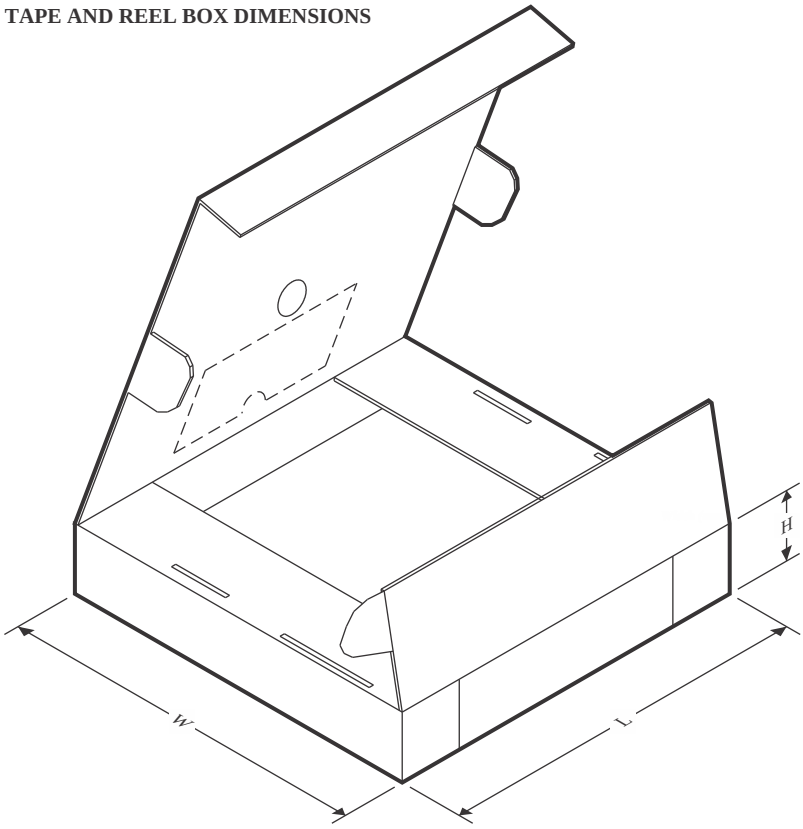
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2902DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3902DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

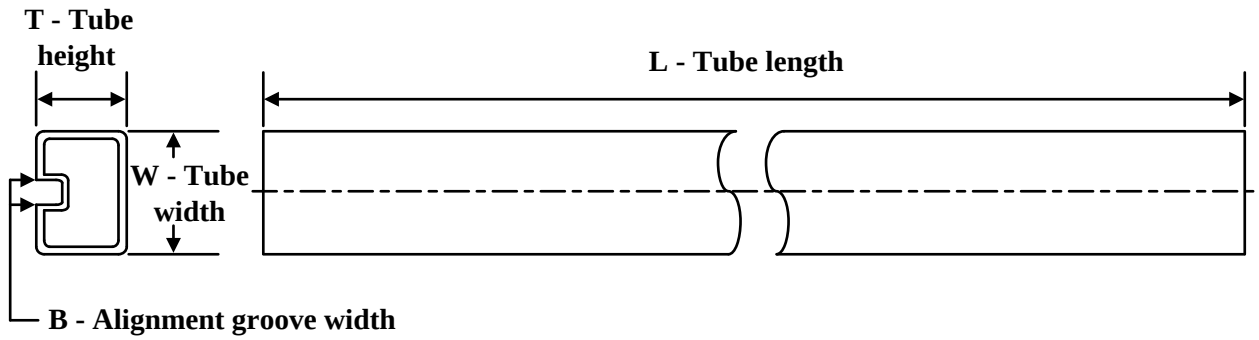
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

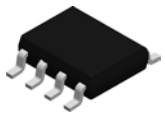
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2902DTR	SOIC	D	8	2500	353.0	353.0	32.0
UC3902DTR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2902D	D	SOIC	8	75	507	8	3940	4.32
UC2902D.A	D	SOIC	8	75	507	8	3940	4.32
UC2902DG4	D	SOIC	8	75	507	8	3940	4.32
UC2902N	P	PDIP	8	50	506	13.97	11230	4.32
UC2902N.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3902D	D	SOIC	8	75	507	8	3940	4.32
UC3902D.A	D	SOIC	8	75	507	8	3940	4.32
UC3902DG4	D	SOIC	8	75	507	8	3940	4.32
UC3902N	P	PDIP	8	50	506	13.97	11230	4.32
UC3902N.A	P	PDIP	8	50	506	13.97	11230	4.32

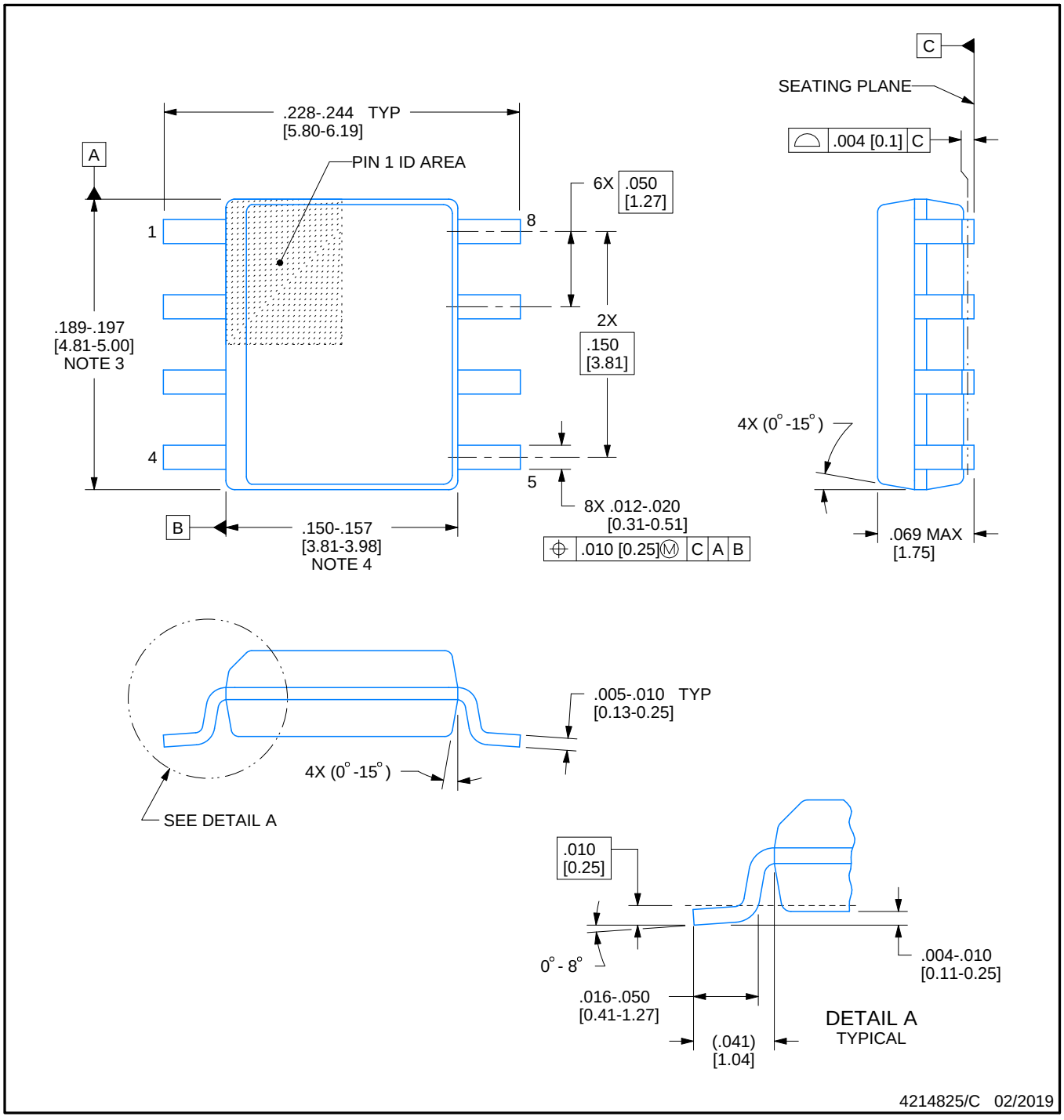


PACKAGE OUTLINE

D0008A

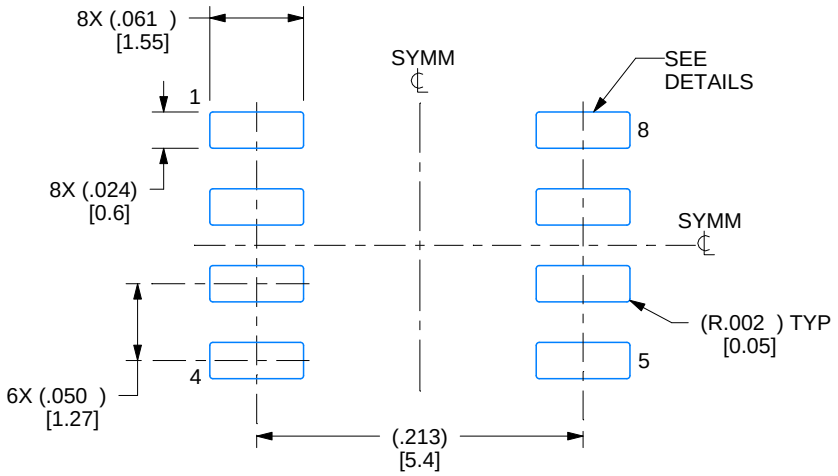
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

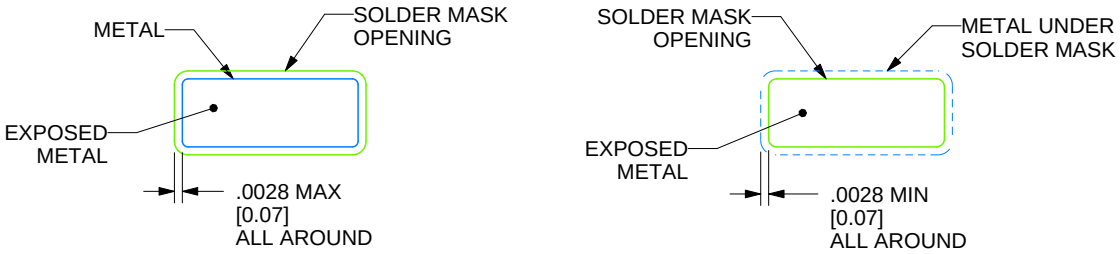


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

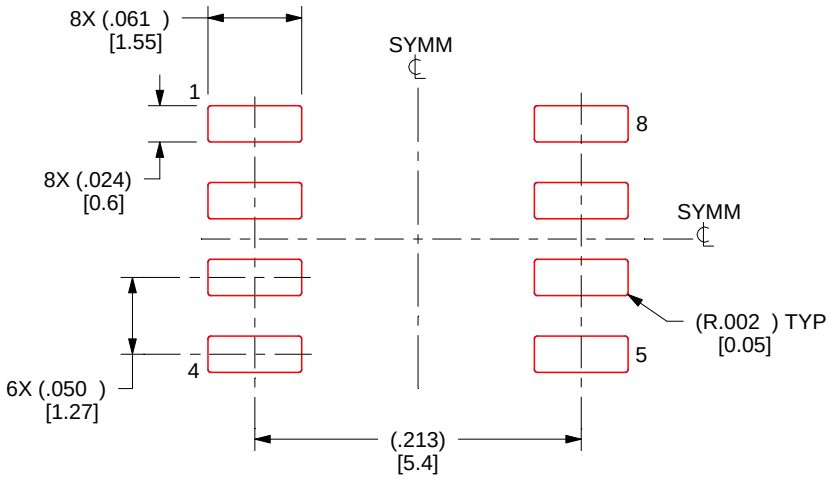
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



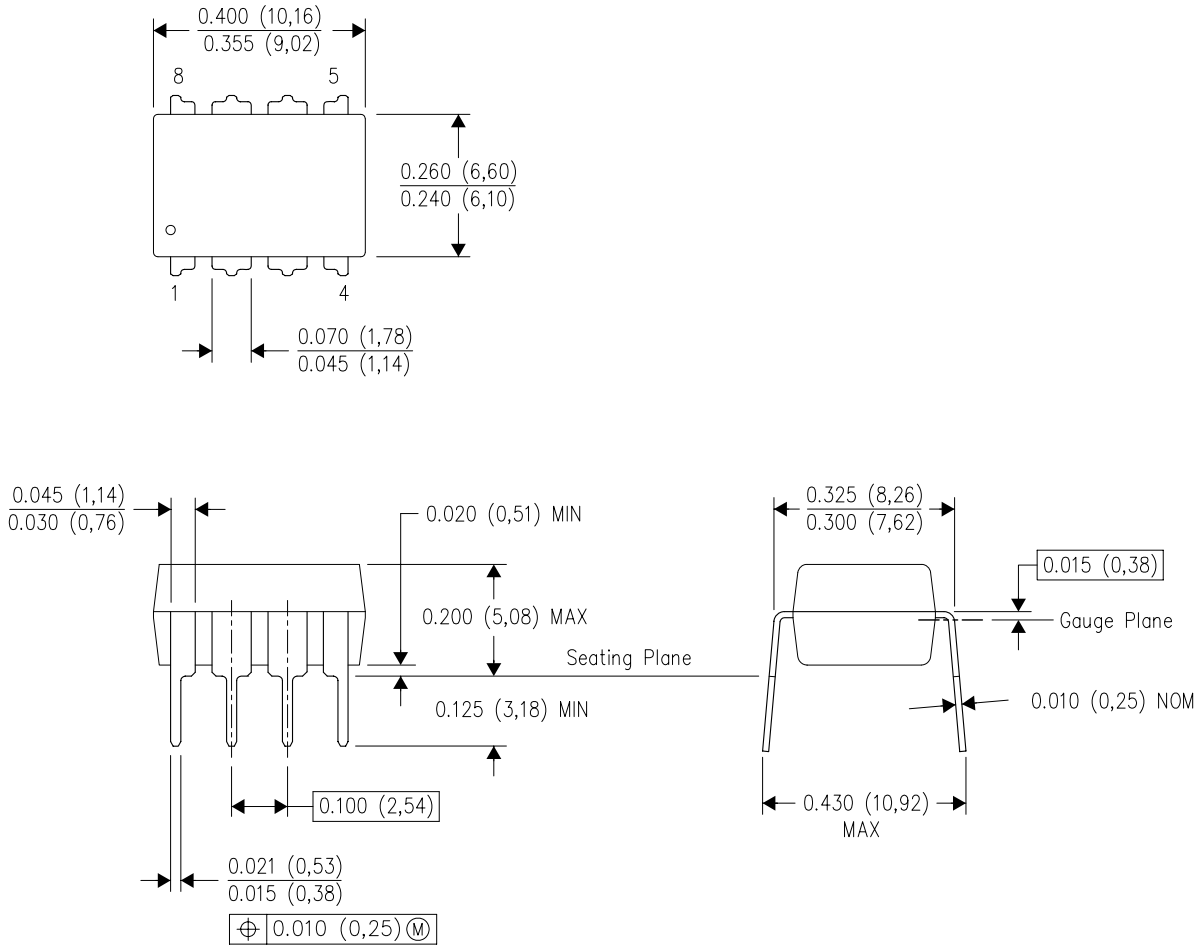
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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