UC1709, UC2709, UC3709
DUAL HIGH-SPEED FET DRIVER

SLUS196C – NOVEMBER 1996 – REVISED FEBRUARY 2008

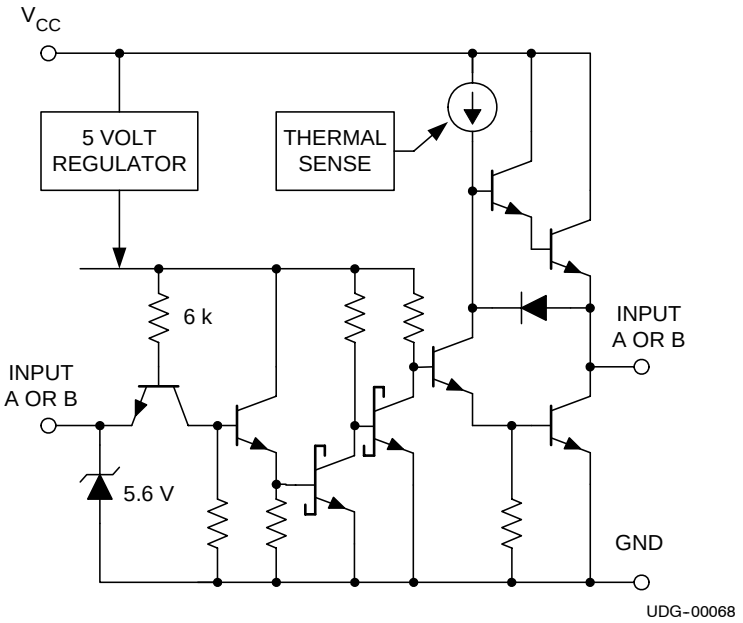
- **1.5 Amp Source/Sink Drive**
- **Pin Compatible with 0026 Products**
- **40 ns Rise and Fall into 1000pF**
- **Low Quiescent Current**
- **5 V to 40 V Operation**
- **Thermal Protection**

description

The UC3709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 A of either source or sink current from a totem–pole output stage configured for minimal cross-conduction current spike.

The UC3709 is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

simplified schematic (only one driver shown)



With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30 V. This design also includes thermal shutdown protection.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Parameter	DW PACKAGE	J PACKAGE	L PACKAGE	N PACKAGE	UNIT
Supply Voltage, V_{CC}	40	40	40	40	V
Output Current (Source or Sink)					
. . . . . Steady–State	±500	±500	±500	±500	mA
. . . . . Peak Transient	±1.5	±1.0	±1.0	±1.5	A
. . . . . Capacitive Discharge Energy	20	15	15	20	mJ
Digital Inputs‡	5.5	5.5	5.5	5.5	V
Power Dissipation at T_A = 25°C	1	1	1	1	W
Power Dissipation at T_C = 25°C	3	2	2	3	W
Operating Junction Temperature Range (T_J)	–55 to 125	–55 to 125	–55 to 125	–55 to 125	°C
Storage Temperature Range	–65 to 150	–65 to 150	–65 to 150	–65 to 150	°C
Lead Temperature (Soldering, 10 Seconds)	300	300	300	300	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All currents are positive into and negative out of the specified terminals. Digital drive can exceed 5.5V if input is limited to 10mA. Consult the Packaging Section of the Databook for thermal limitations and considerations of the package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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THERMAL RESISTANCE TABLE

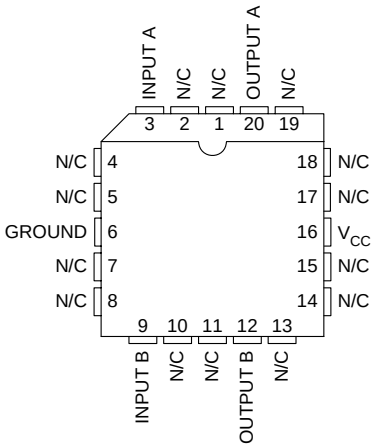
PACKAGE	θjc(°C/W)	θja(°C/W)
SOIC-16 (DW)	20 (1)	35 to 58 (3)
DIL-16 (J)	28 (2)	125 to 160
LCC-16 (L)	20 (2)	70 to 80
DIL-16 (N)	45	90 (3)

NOTES: (1) Specified thermal resistance is θjl (junction to lead)where noted.

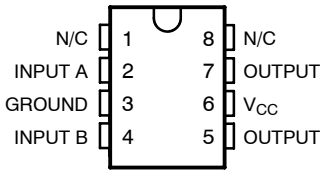
(2) θjc data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states, "The baseline values shown are worst case (mean +2s) for a 60x60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, .10°C/W; pin grid array, 10°C/W".

(3) Specified θja (junction to ambient) is for devices mounted to 5-inch^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 inch^2 aluminum PC board. Test PWB was 0.062 inch thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil x 100-mil probe land area at the end of each trace.

LCC-20 (TOP VIEW)
L PACKAGES

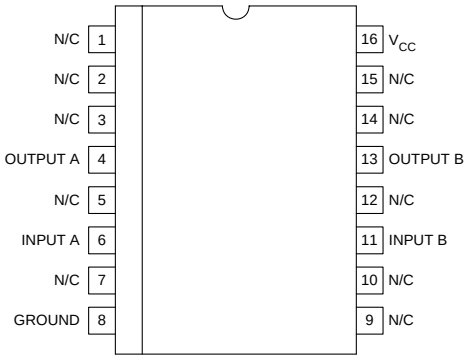


8 PIN DIL N OR J PACKAGE
(TOP VIEW)



N/C – No internal connection

SOIC-16 (TOP VIEW)
DW PACKAGE



electrical characteristics over recommended operating free-air temperature range, T_A = 55°C to 125°C for the UC1709, –40°C to 85°C for the UC2709, and 0°C to 70°C for the UC3709; V_{CC} = 20 V, T_A = T_J.

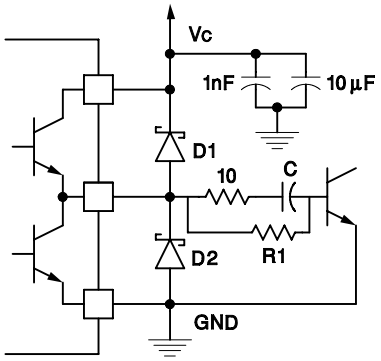
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	Both outputs low		10	12	mA
	Both outputs high		7	10	mA
Logic 0 input voltage				0.8	V
Logic 1 input voltage		2.2			V
Input current	V_I = 0		–0.6	–1.0	mA
Input leakage	V_I = 5 V		0.05	0.1	mA
Output high saturation V_{CC}-V_O	I_O = –50 mA		1.5	2.0	V
	I_O = –500 mA		2.0	2.5	V
Output low saturation V_O	I_O = 50 mA		0.1	0.4	V
	I_O = 500 mA		2.0	2.5	V
Thermal shutdown			155		mA

typical switching characteristics, V_{CC} = 20 V, T_A = 25°C, delays measured to 10% output change

PARAMETER	TEST CONDITIONS	OUTPUT C_L =		UNITS
		0 nF	2.2 nF	
Rise time delay		80	80	ns
10% to 90% rise		20	40	ns
Fall time delay		60	80	ns
10% to 90% fall		20	40	ns
VCC cross-conduction curent spike duration	Output rise	25		ns
	Output fall	0		ns

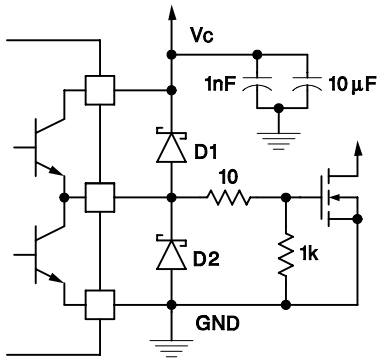
NOTE: Refer to UC1705 specifications for further information.

APPLICATION INFORMATION



D1, D2: UC3611 Schottky Diodes

Figure 1. Power bipolar drive circuit.



D1, D2: UC3611 Schottky Diodes

Figure 2. Power MOSFET drive circuit.

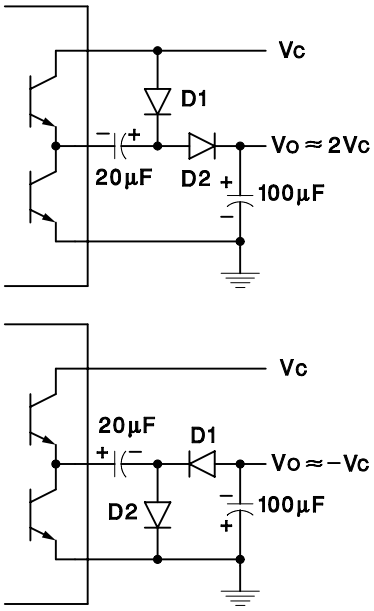
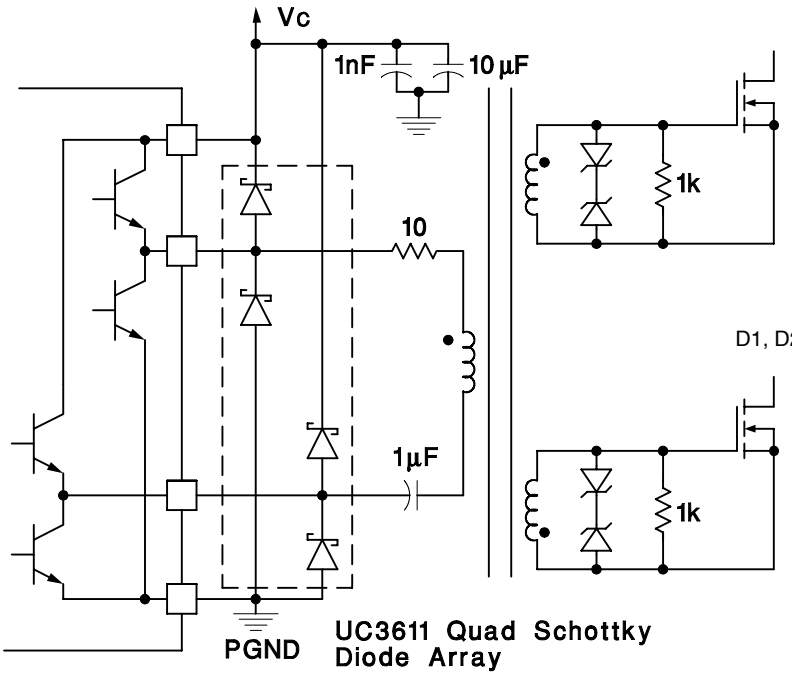
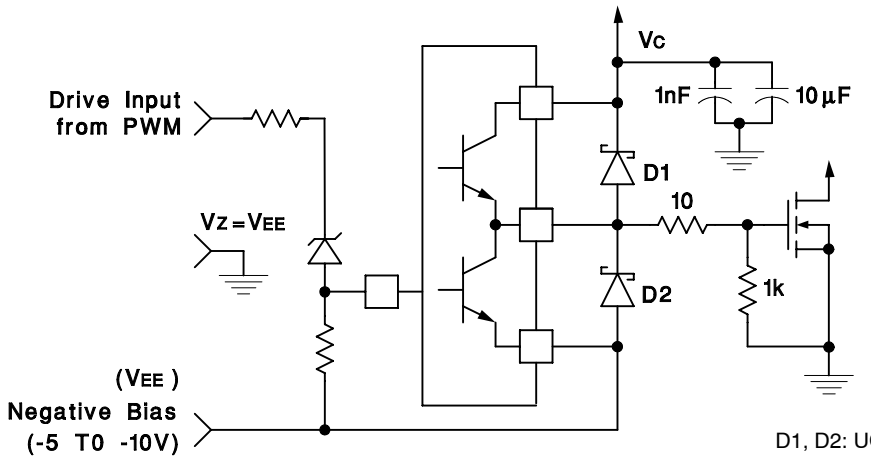


Figure 3. Charge pump circuits.



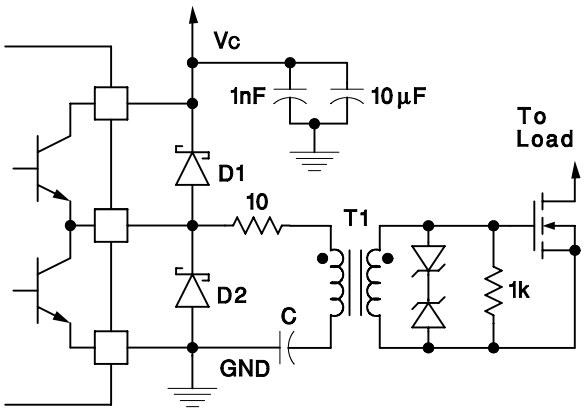
D1, D2: UC3611 Schottky Diodes

Figure 4. Transformer coupled push-pull MOSFET drive circuit.



D1, D2: UC3611 Schottky Diodes

Figure 5. Power MOSFET drive circuit using negative bias voltage and level shifting to ground referenced PWM



D1, D2: UC3611 Schottky Diodes

Figure 6. Transformer coupled MOSFET drive circuit.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0151201VPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	0151201VPA UC1709
5962-0151201VPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	0151201VPA UC1709
UC1709J	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709J
UC1709J.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709J
UC1709J883B	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709J/ 883B
UC1709J883B.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709J/ 883B
UC1709L	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709L
UC1709L.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709L
UC1709L883B	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709L/ 883B
UC1709L883B.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1709L/ 883B
UC2709DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2709DW
UC2709DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2709DW
UC2709N	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2709N
UC2709N.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2709N
UC3709DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3709DW
UC3709DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3709DW
UC3709N	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3709N
UC3709N.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3709N
UC3709NG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3709N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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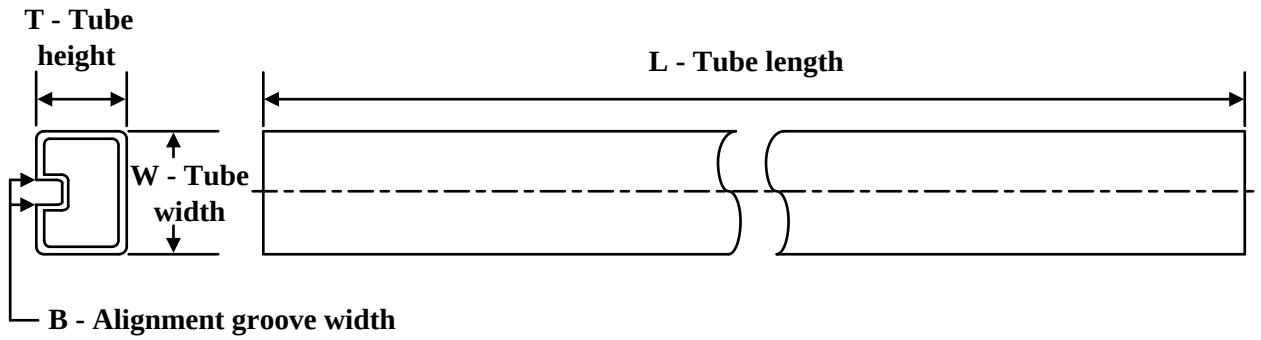
OTHER QUALIFIED VERSIONS OF UC1709, UC1709-SP, UC3709 :

- Catalog : UC3709, UC1709
- Military : UC1709
- Space : UC1709-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TUBE



*All dimensions are nominal

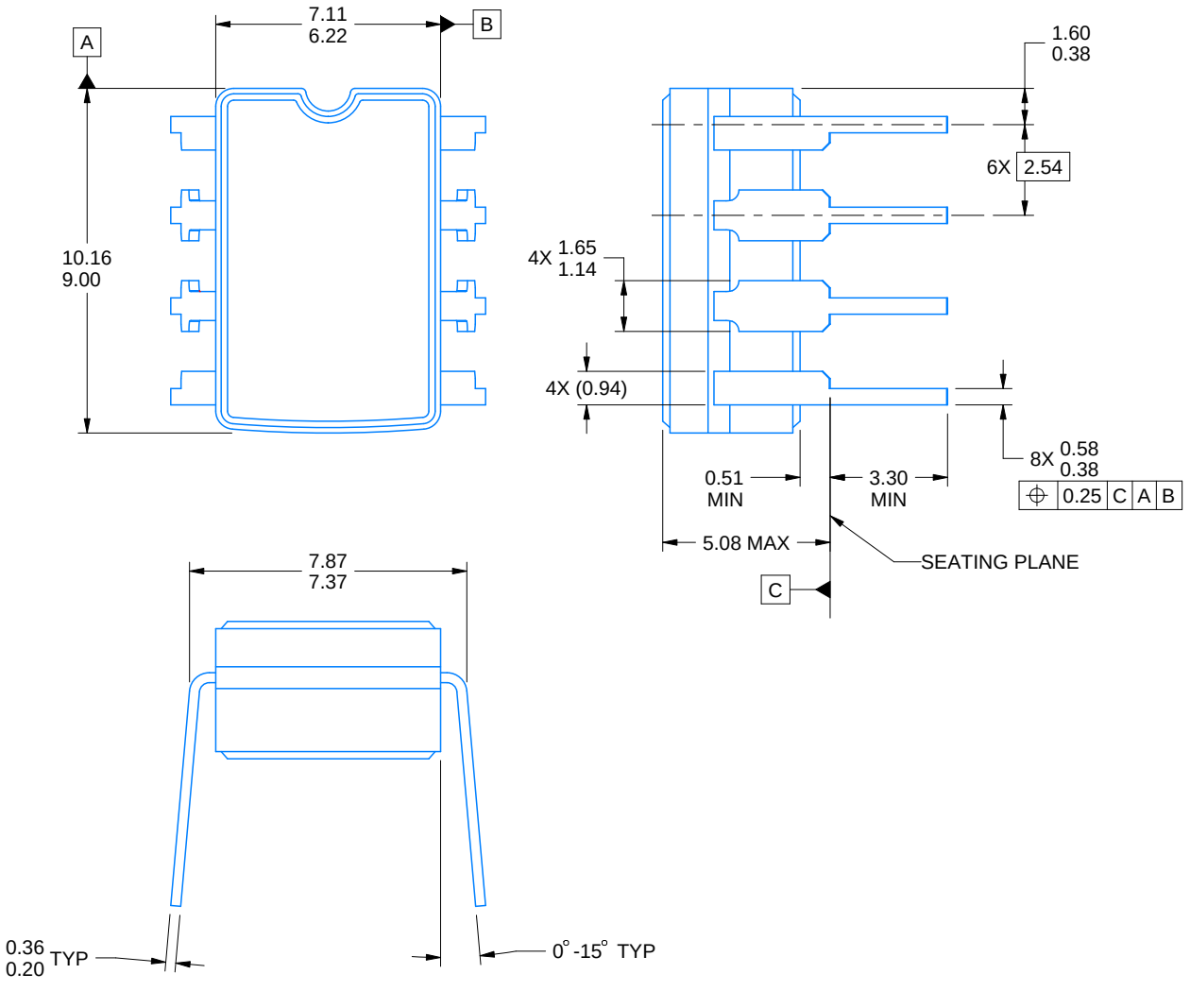
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC1709L	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1709L.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1709L883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1709L883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2709DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2709DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2709N	P	PDIP	8	50	506	13.97	11230	4.32
UC2709N.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3709DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3709DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3709N	P	PDIP	8	50	506	13.97	11230	4.32
UC3709N.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3709NG4	P	PDIP	8	50	506	13.97	11230	4.32

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

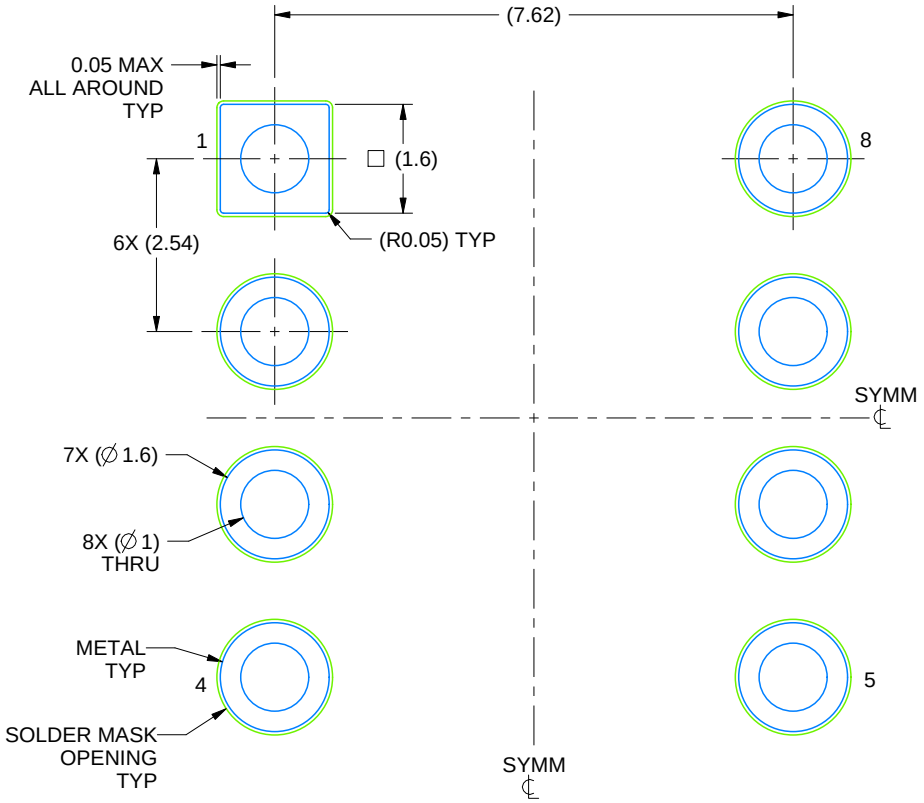
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

GENERIC PACKAGE VIEW

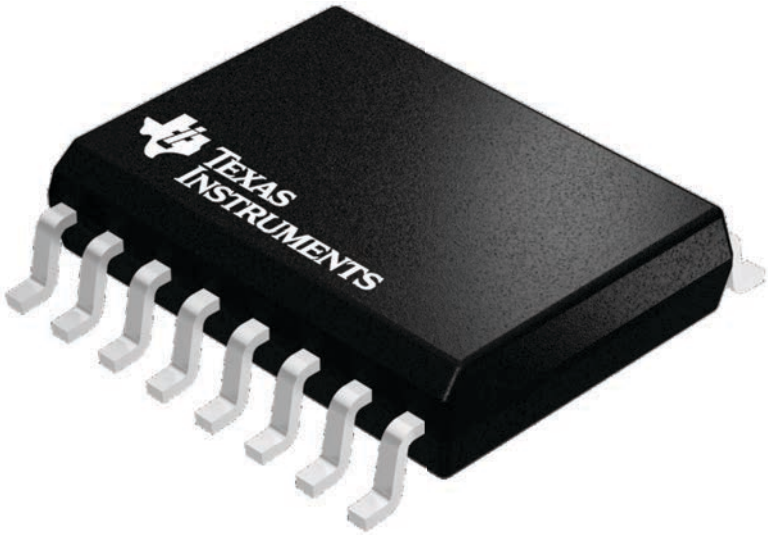
DW 16

SOIC - 2.65 mm max height

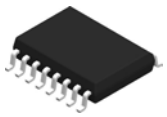
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

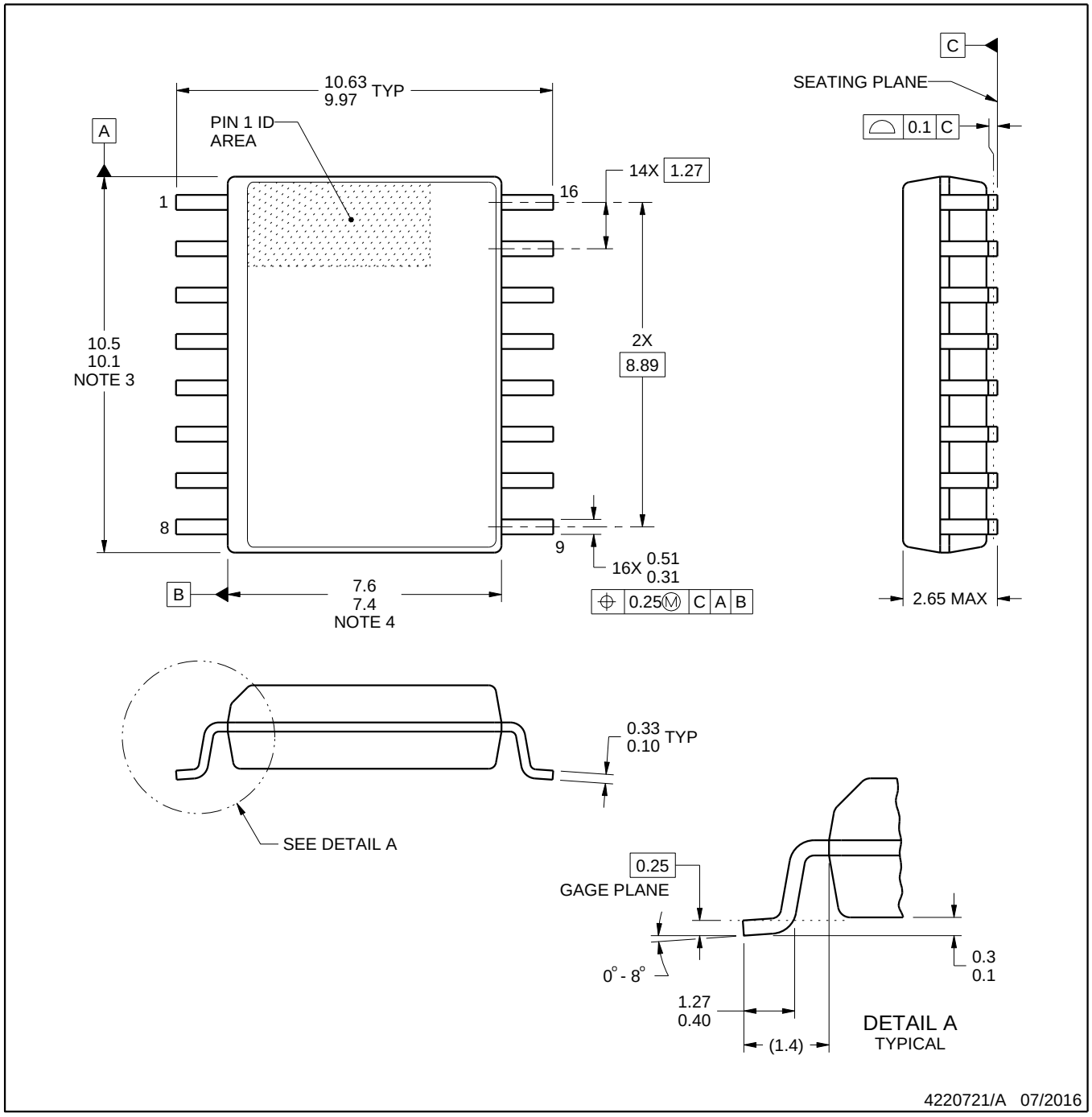


PACKAGE OUTLINE

DW0016A

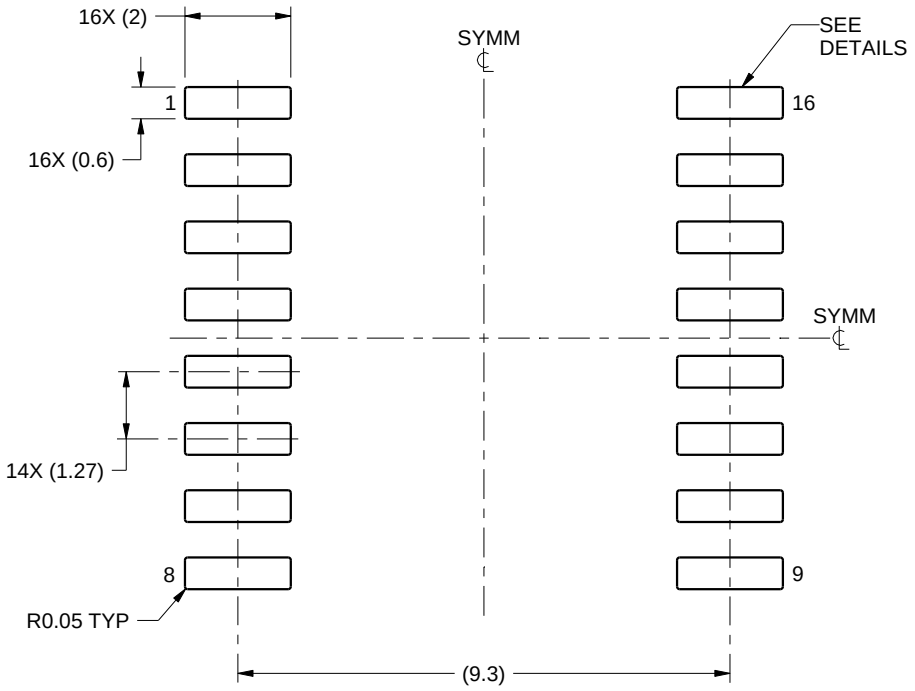
SOIC - 2.65 mm max height

SOIC

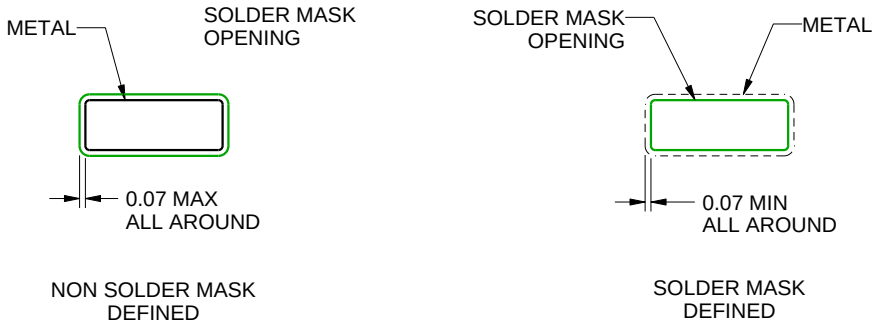


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

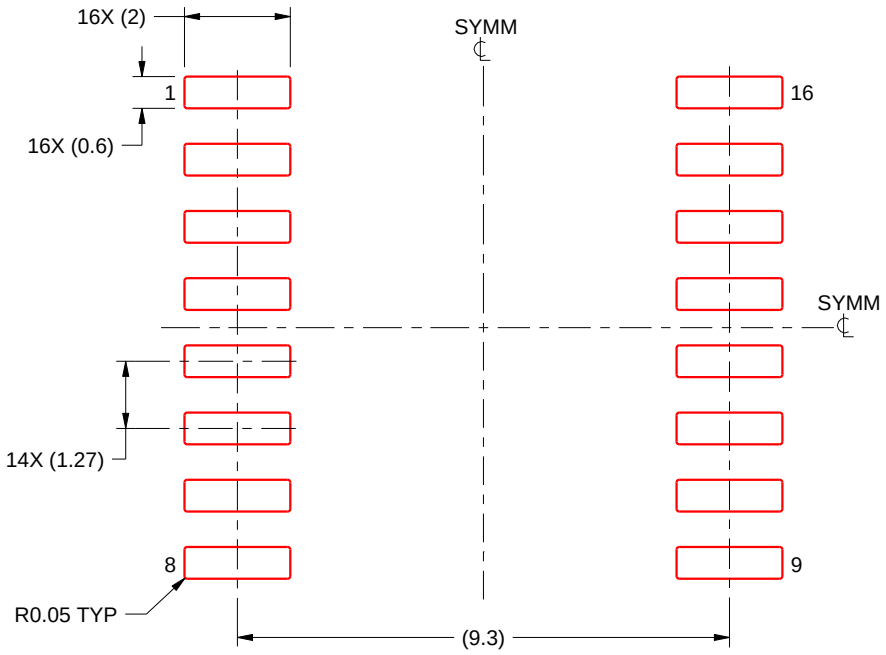


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

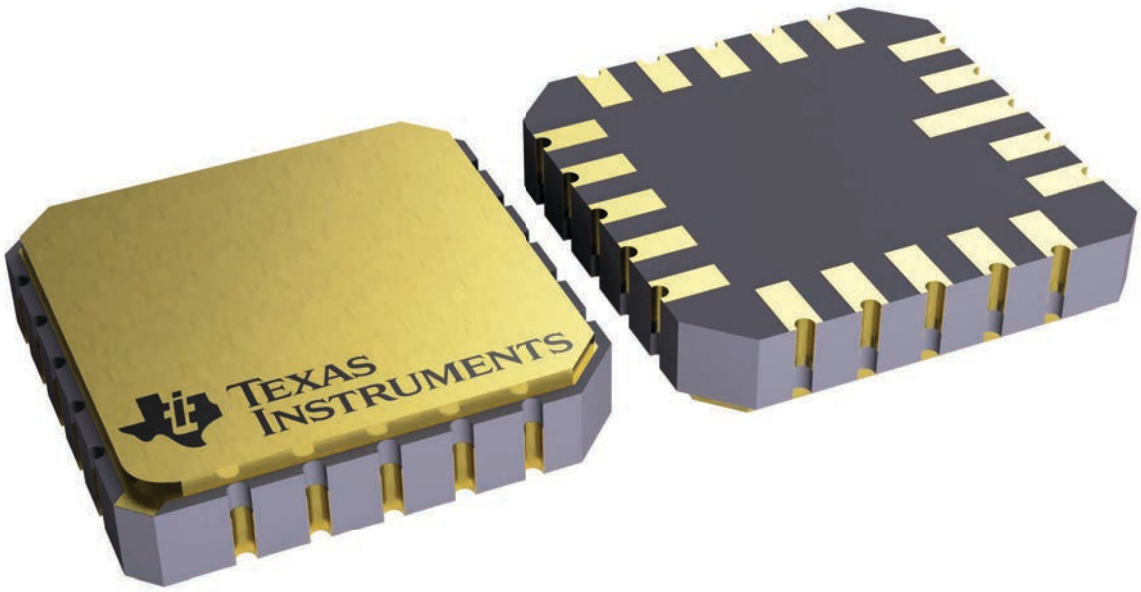
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

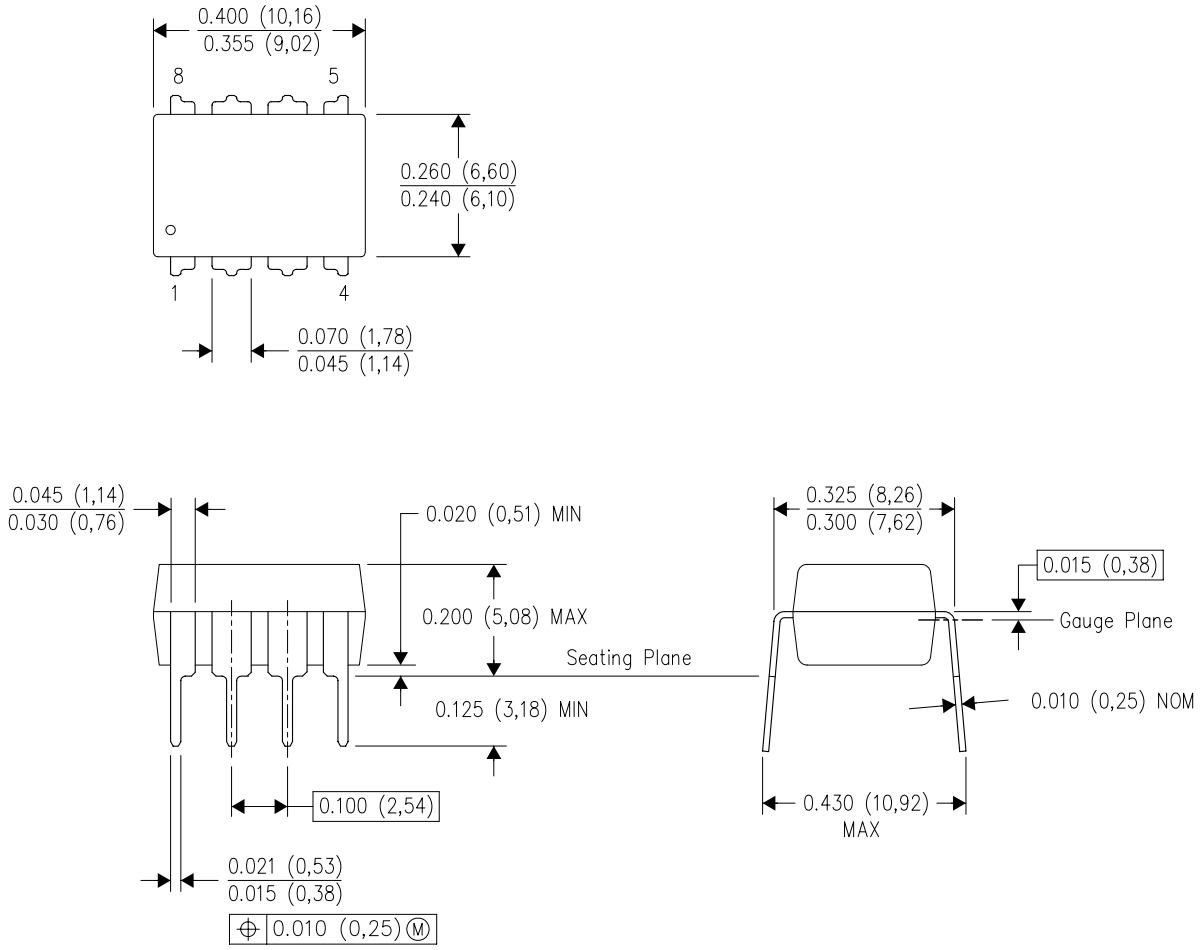
LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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