采用 LGA 封装的 UCC20225 2.5kV$_{RMS}$ 单输入隔离式双通道栅极驱动器

1 特性

- 单输入，双输出单输入，双输出，并具有可编程死区时间
- 节省空间的 5mm x 5mm LGA-13 封装
- 开关参数：
  - 19ns 典型传播延迟
  - 5ns 最大延迟匹配度
  - 6ns 最大脉宽失真度
- CMTI 大于 100V/ns
- 4A 峰值拉电流，6A 峰值灌电流输出
- TTL 和 CMOS 兼容输入
- 输入 VCCI 范围为 3V 至 18V
- VDD 高达 25V，带 8V UVLO
- 可编程死区时间
- 抑制短于 5ns 的输入瞬变
- 电源定序快速禁用
- 安全相关认证：
  - 符合 DIN V VDE V 0884-11:2017-01 标准的 3535V$_{PK}$ 隔离
  - 符合 UL 1577 标准且长达 1 分钟的 2500V$_{RMS}$ 隔离
  - 通过 GB4943.1-2011 CQC 认证

2 应用

- 服务器、电信、IT 和工业基础设施
- 交流/直流电源
- 电机驱动器和直流/交流光伏逆变器
- HEV 和 BEV 电池充电器

3 说明

UCC20225 是一款隔离式单输入、双输出栅极驱动器，可在 5mm x 5mm LGA-13 封装中提供 4A 峰值拉电流和 6A 峰值灌电流。该器件旨在以一流的传播延迟和脉宽失真度驱动功率晶体管，频率最高可达 5MHz。

输入侧通过一个 2.5kV$_{RMS}$ 隔离栅与两个输出驱动器隔离，共模瞬态抗扰度 (CMTI) 的最小值为 100V/ns。两个输出侧驱动器之间的内部功能隔离支持高达 700V$_{DC}$ 的工作电压。

UCC20225 通过 DT 引脚上的电阻器支持可编程死区时间 (DT)。禁用引脚在设为高电平时可同时关断两个输出，在保持开路或接地时允许器件正常运行。

该器件接受的 VDD 电源电压高达 25V。凭借 3V 至 18V 宽输入 VCCI 电压范围，该驱动器适用于连接数字和模拟控制器。所有电源电压引脚均具有欠压闭锁 (UVLO) 保护。

凭借上述所有高级 特性，UCC20225 在多种电力应用中实现了高功率密度、高效率 和鲁棒性。

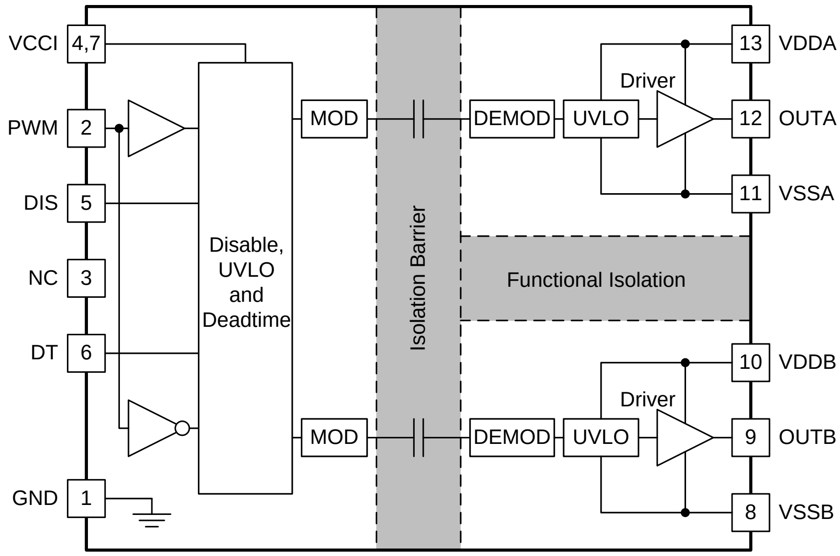
器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC20225NPL	NPL LGA (13)	5mm × 5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

English Data Sheet: SLUSCV8

功能方框图



Copyright © 2017, Texas Instruments Incorporated

目录

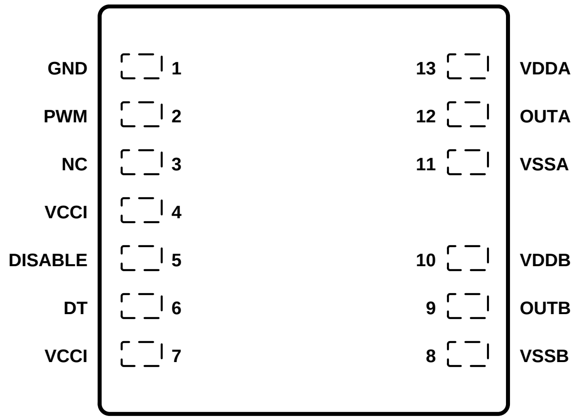
4 修订历史记录

Changes from Original (April 2017) to Revision A — **Page**

- 已更改 更改了有关特性、应用和 说明 部分的说明 ... 1
- 已更改 将 “特性” 部分中的 UL、VDE 和 CQC 安全相关认证说明从计划状态更改成了已完成状态 ... 1
- 已删除 从“安装相关认证” 部分中 删除了 CSA 认证说明 ... 1
- Changed detailed description for DISABLE Pin and DT Pin ... 4
- Changed the testing conditions for the power ratings ... 6
- Deleted test conditions for the material group on the insulation specification section ... 7
- Changed the overvoltage category on the insulation specification section ... 7
- Changed from VDE V 0884-10:2006-12 to VDE V 0884-11:2017-01 in safety-related certifications ... 7
- Changed V_{IOSM} in insulation specifications from 3535V_{PK} to 3500V_{PK} ... 7
- Changed from VDE V 0884-10 to VDE V 0884-11 in insulation specification and safety-related certification table ... 8
- Added certification number for for VDE, UL and CQC in safety-related certification table ... 8
- Added 320-V_{RMS} maximum working voltage in the safety-related certification table ... 8
- Changed table note to explain how safety-limiting values are calculated ... 8
- Added minimum specifications for propagation delay t_{PDHL} and t_{PDLH} ... 10
- Changed CMTI specification to be replaced by $|CM_H|$ and $|CM_L|$ ... 10
- 已添加 feature description for UVLO delay to OUTPUT ... 17
- 已添加 footnote on INPUT/OUTPUT logic table ... 21
- 已添加 bullet "It is recommended..." bullet to the component placement in the Layout Guidelines section ... 37
- 已添加 在认证部分中添加了 UL、VDE 和 CQC 在线认证目录 ... 40

5 Pin Configuration and Functions

NPL Package
13-Pin LGA
Top View



Not to scale

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
DISABLE	5	I	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting to a micro controller with distance.
DT	6	I	Programmable dead time function. Tying DT to VCCI disables the DT function with dead time ≈ 0ns. Leaving DT open sets the dead time to <15 ns. Placing a resistor (R_{DT}) between DT and GND adjusts dead time according to: DT (in ns) = 10 x R_{DT} (in kΩ). It is recommended to parallel a ceramic capacitor, 2.2nF or above, close to DT pin to achieve better noise immunity.
GND	1	G	Primary-side ground reference. All signals in the primary side are referenced to this ground.
NC	3	–	No internal connection.
OUTA	12	O	Output of driver A. Connect to the gate of the A channel FET or IGBT. Output A is in phase with PWM input with a propagation delay
OUTB	9	O	Output of driver B. Connect to the gate of the B channel FET or IGBT. Output B is always complementary to output A with a programmed dead time.
PWM	2	I	PWM input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open.
VCCI	4	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	7	P	Primary-side supply voltage. This pin is internally shorted to pin 4.
VDDA	13	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	10	P	Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible.
VSSA	11	G	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VSSB	8	G	Ground for secondary-side driver B. Ground reference for secondary side B channel.

(1) P =Power, G= Ground, I= Input, O= Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	VCCI to GND	–0.3	20	V
Driver bias supply	VDDA-VSSA, VDDB-VSSB	–0.3	30	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB	–0.3	V_{VDDA}+0.3, V_{VDDB}+0.3	V
	OUTA to VSSA, OUTB to VSSB, Transient for 200 ns	–2	V_{VDDA}+0.3, V_{VDDB}+0.3	V
Input signal voltage	PWM, DIS, DT to GND	–0.3	V_{VCCI}+0.3	V
	PWM Transient for 50ns	–5	V_{VCCI}+0.3	V
Channel to channel voltage	VSSA-VSSB, VSSB-VSSA		700	V
Junction temperature, T_J (2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for T_J, see the Thermal Information.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCCI	VCCI Input supply voltage	3	18	V
VDDA, VDDB	Driver output bias supply	9.2	25	V
T_A	Ambient Temperature	–40	125	°C
T_J	Junction Temperature	–40	130	°C

6.4 Thermal Information

THERMAL METRIC[1]		UCC20225 LGA (13)[2]	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	78.9	
ψ_{JT}	Junction-to-top characterization parameter	26.2	
ψ_{JB}	Junction-to-board characterization parameter	76.8	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Standard JESD51-9 Area Array SMT Test Board (2s2p) in still air, with 12-mil dia. 1-oz copper vias connecting VSSA and VSSB to the plane immediately below (three vias for VSSA, three vias for VSSB).

6.5 Power Ratings

			VALUE	UNIT
P_D	Power dissipation by UCC20225NPL	VCCI = 18 V, VDDA/B = 12 V, PWM = 3.3 V, 3.5 MHz 50% duty cycle square wave 1-nF load	1.25	W
P_{DI}	Power dissipation by primary side of UCC20225NPL		0.05	
P_{DA}, P_{DB}	Power dissipation by each driver side of UCC20225NPL		0.60	

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance(1)(2)	Shortest pin-to-pin distance through air	3.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	3.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group		I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-III	
		Rated mains voltage ≤ 300 V_{RMS}	I-II	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01(3)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	792	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test; (See 图 1)	560	V_{RMS}
		DC Voltage	792	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	3535	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	3500	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input/Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	<5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	<5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	<5	
C_{IO}	Barrier capacitance, input to output(6)	$V_{IO} = 0.4 \sin(2\pi ft)$, f =1 MHz	1.2	pF
R_{IO}	Isolation resistance, input to output	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S =150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 3000 V_{RMS}, t = 60 sec. (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 3000V_{RMS}, t = 1 sec (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Package dimension tolerance ± 0.05mm.
(3) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(4) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL	CQC
Certified according to DIN V VDE V 0884-11:2017-01	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 3535 V_{PK}; Maximum Repetitive Peak Voltage, 792 V_{PK}; Maximum Surge Isolation Voltage, 2719 V_{PK}	Single protection, 2500 V_{RMS}	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate 320-V_{RMS} maximum working voltage
Certification Number: 40016131	Certification Number: E181974	Certification Number: CQC18001186974

6.8 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current(1)	$R_{\theta JA}$ = 98.0ºC/W, VDDA/B = 12 V, T_A = 25°C, T_J = 150°C See 图 2	DRIVER A, DRIVER B			50	mA
		$R_{\theta JA}$ = 98.0ºC/W, VDDA/B = 25 V, T_A = 25°C, T_J = 150°C	DRIVER A, DRIVER B			24	mA
P_S	Safety supply power(1)	$R_{\theta JA}$ = 98.0ºC/W, T_A = 25°C, T_J = 150°C See 图 3	INPUT			0.05	W
			DRIVER A			0.60	
			DRIVER B			0.60	
			TOTAL			1.25	
T_S	Safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the ***Thermal Information*** table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCCI}	VCCI quiescent current	DISABLE = VCCI		1.5	2.0	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB quiescent current	DISABLE = VCCI		1.0	1.8	mA
I_{VCCI}	VCCI operating current	(f = 500 kHz) current per channel, C_{OUT} = 100 pF		2.5		mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB operating current	(f = 500 kHz) current per channel, C_{OUT} = 100 pF		2.5		mA
VCCI SUPPLY UNDERVOLTAGE LOCKOUT THRESHOLDS						
V_{VCCI_ON}	Rising threshold VCCI_ON		2.55	2.7	2.85	V
V_{VCCI_OFF}	Falling threshold VCCI_OFF		2.35	2.5	2.65	V
V_{VCCI_HYS}	Threshold hysteresis			0.2		V
VDD SUPPLY UNDERVOLTAGE LOCKOUT THRESHOLDS						
V_{VDDA_ON}, V_{VDDB_ON}	Rising threshold VDDA_ON, VDDB_ON		8.3	8.7	9.2	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling threshold VDDA_OFF, VDDB_OFF		7.8	8.2	8.7	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold hysteresis			0.5		V
PWM AND DISABLE						
V_{PWMH}, V_{DISH}	Input high voltage		1.6	1.8	2	V
V_{PWML}, V_{DISL}	Input low voltage		0.8	1	1.2	V
V_{PWM_HYS}, V_{DIS_HYS}	Input hysteresis			0.8		V
V_{PWM}	Negative transient, ref to GND, 50 ns pulse	Not production tested, bench test only	–5			V
OUTPUT						
I_{OA+}, I_{OB+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		4		A
I_{OA-}, I_{OB-}	Peak output sink current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		6		A
R_{OHA}, R_{OHB}	Output resistance at high state	I_{OUT} = –10 mA, T_A = 25°C, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in Switching Characteristics and Output Stage for details.		5		Ω
R_{OLA}, R_{OLB}	Output resistance at low state	I_{OUT} = 10 mA, T_A = 25°C		0.55		Ω
V_{OHA}, V_{OHB}	Output voltage at high state	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = –10 mA, T_A = 25°C		11.95		V
V_{OLA}, V_{OLB}	Output voltage at low state	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = 10 mA, T_A = 25°C		5.5		mV
DEADTIME AND OVERLAP PROGRAMMING						
Dead time		Pull DT pin to VCCI		0		ns
		DT pin is left open, min spec characterized only, tested for outliers		8	15	ns
		R_{DT} = 20 kΩ	160	200	240	ns

6.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = –40°C to +125°C, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, 20% to 80% measured points	C_{OUT} = 1.8 nF		6	16	ns
t_{FALL}	Output fall time, 90% to 10% measured points	C_{OUT} = 1.8 nF		7	12	ns
t_{PWmin}	Minimum pulse width	Output off for less than minimum, C_{OUT} = 0 pF			20	ns
t_{PDHL}	Propagation delay from INx to OUTx falling edges		14	19	30	ns
t_{PDLH}	Propagation delay from INx to OUTx rising edges		14	19	30	ns
t_{PWD}	Pulse width distortion $\|t_{PDLH} – t_{PDHL}\|$				6	ns
t_{DM}	Propagation delays matching between VOUTA, VOUTB				5	ns
$\|CM_H\|$	High-level common-mode transient immunity	PWM is tied to GND or VCCI; V_{CM}=1200V; (See CMTI Testing)	100			V/ns
$\|CM_L\|$	Low-level common-mode transient immunity		100			

6.11 Thermal Derating Curves

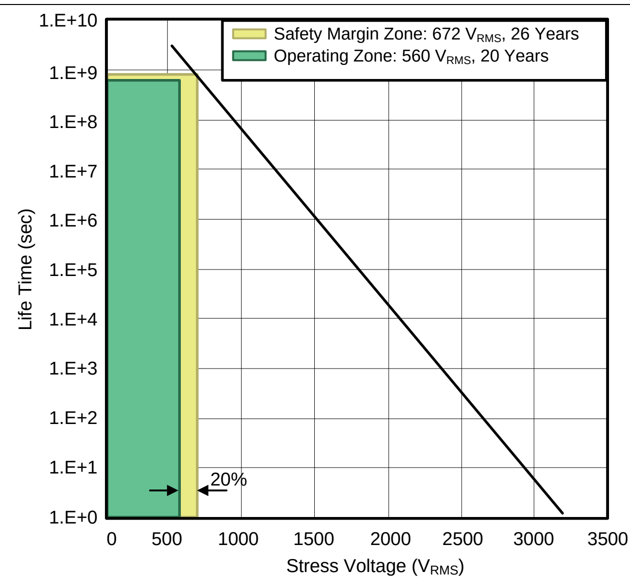


图 1. Isolation Capacitor Life Time Projection

Thermal Derating Curves (接下页)

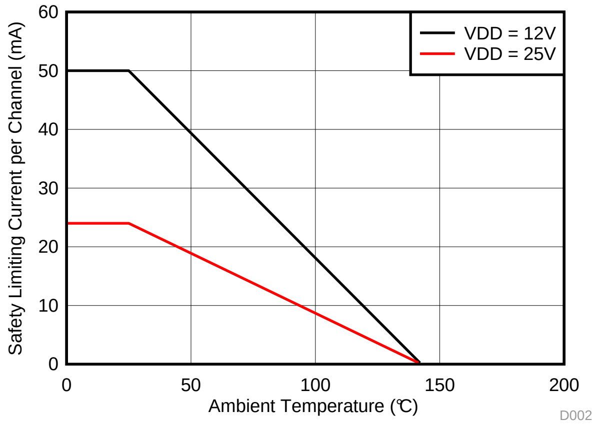


图 2. Thermal Derating Curve for Safety-Related Limiting Current
(Current in Each Channel with Both Channels Running Simultaneously)

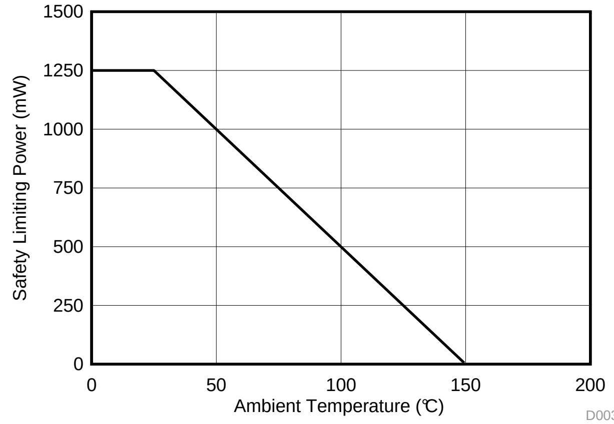


图 3. Thermal Derating Curve for Safety-Related Limiting Power

6.12 Typical Characteristics

VDDA = VDDB= 12 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

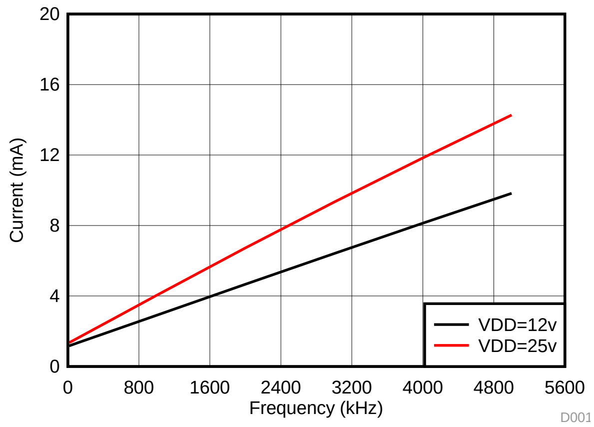


图 4. Per Channel Current Consumption vs. Frequency (No Load, VDD = 12 V or 25 V)

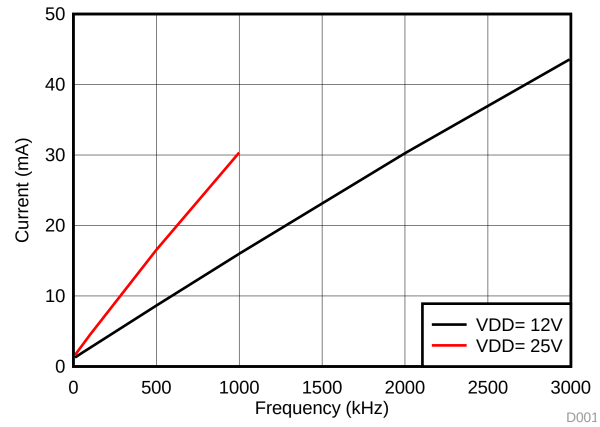


图 5. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (1-nF Load, VDD = 12 V or 25 V)

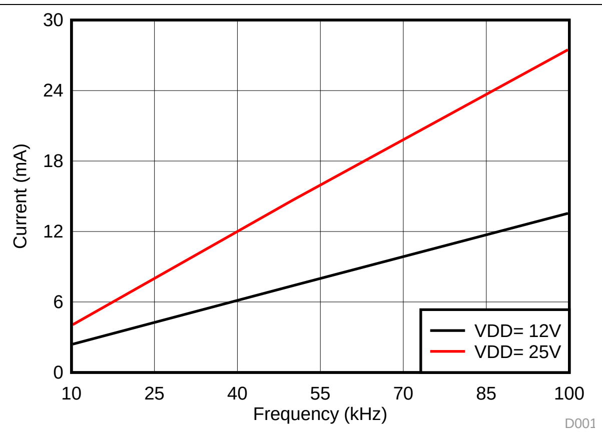


图 6. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (10-nF Load, VDD = 12 V or 25 V)

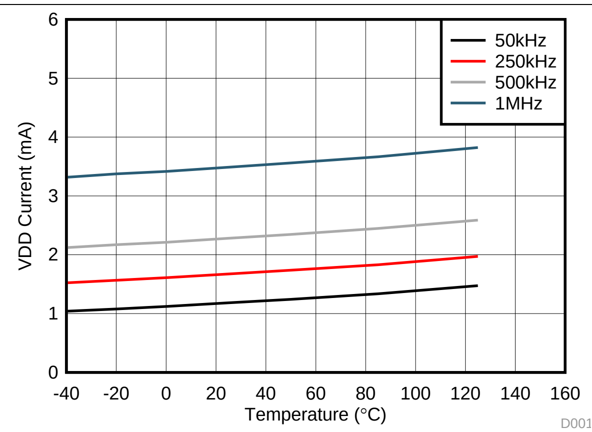


图 7. Per Channel ($I_{VDDA/B}$) Supply Current Vs. Temperature (No Load, Different Switching Frequencies)

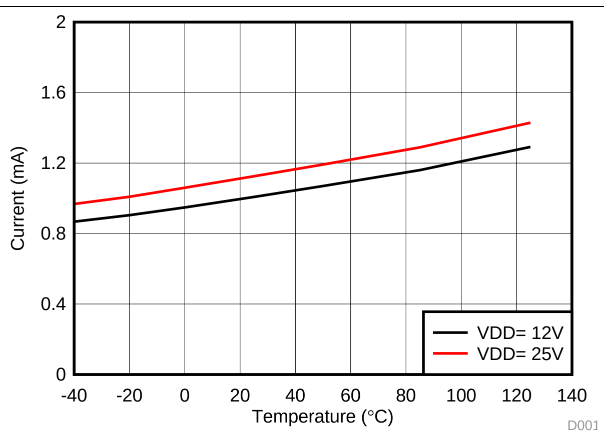


图 8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

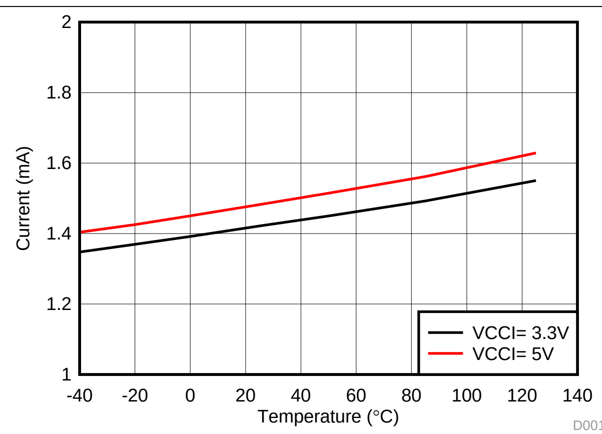


图 9. I_{VCCI} Quiescent Supply Current vs Temperature (No Load, DIS is High, No Switching)

Typical Characteristics (接下页)

VDDA = VDDB= 12 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

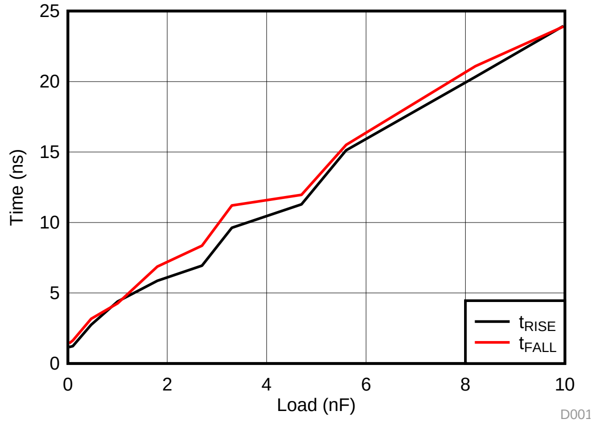


图 10. Rising and Falling Times vs. Load (VDD = 12 V)

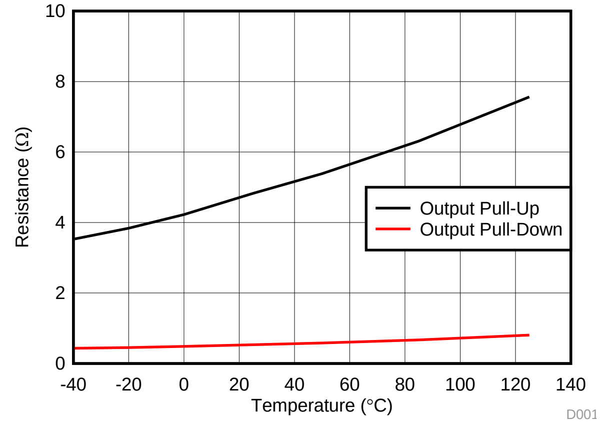


图 11. Output Resistance vs. Temperature

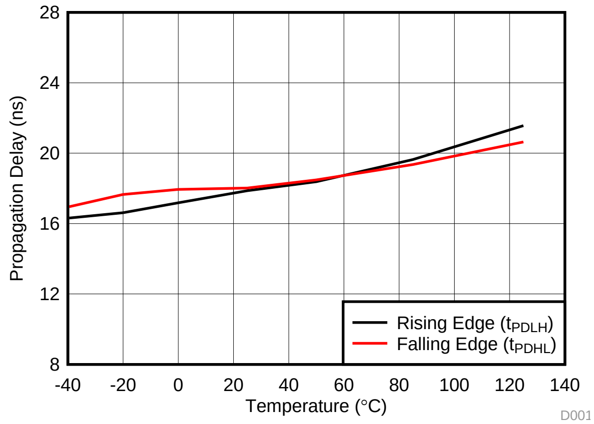


图 12. Propagation Delay vs. Temperature

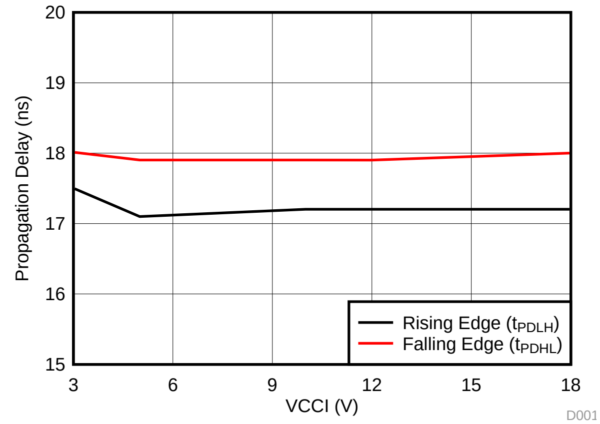


图 13. Propagation Delay vs. VCCI

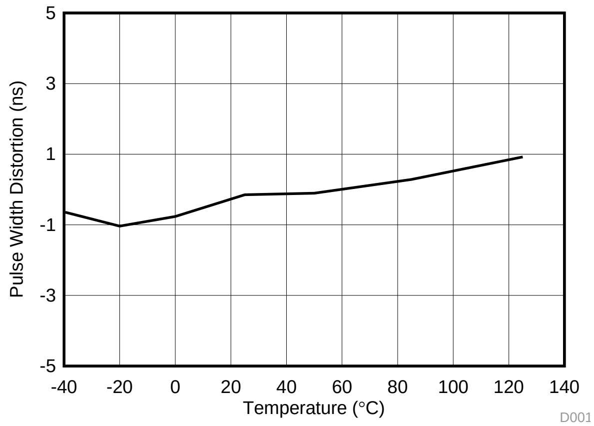


图 14. Pulse Width Distortion vs. Temperature

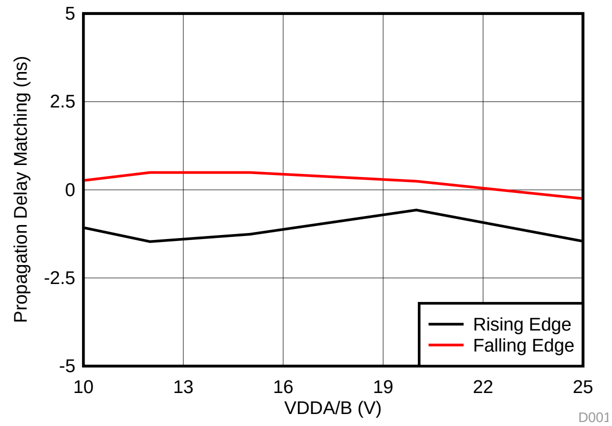


图 15. Propagation Delay Matching (t_{DM}) vs. VDD

Typical Characteristics (接下页)

VDDA = VDDB= 12 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

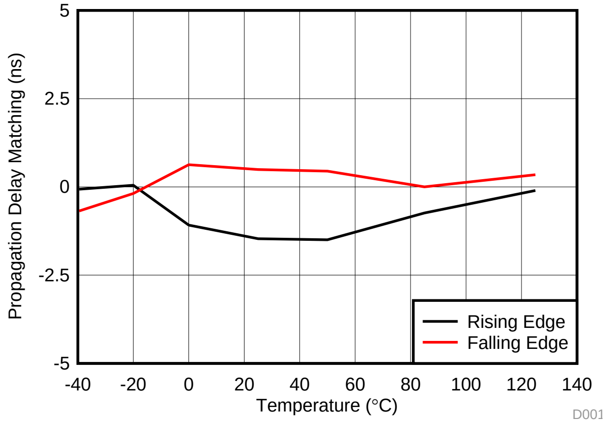


图 16. Propagation Delay Matching (t_{DM}) vs. Temperature

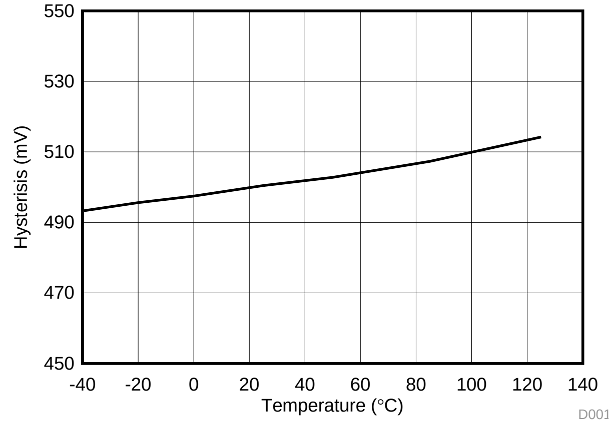


图 17. VDD UVLO Hysteresis vs. Temperature

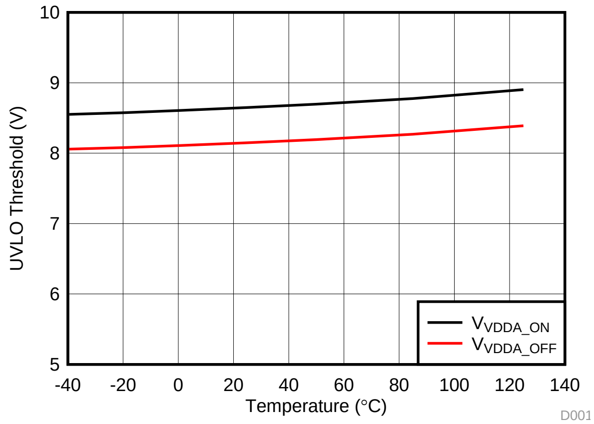


图 18. VDD UVLO Threshold vs. Temperature

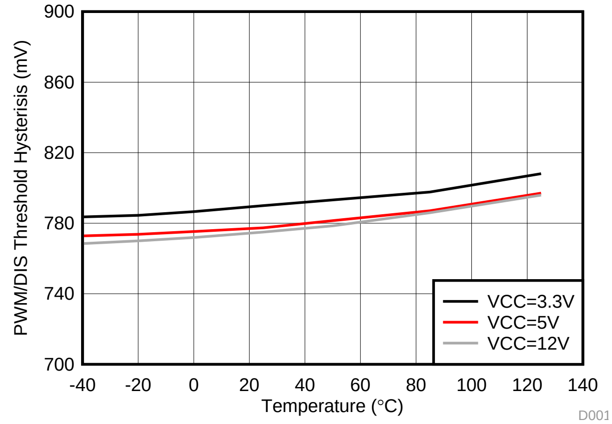


图 19. PWM/DIS Hysteresis vs. Temperature

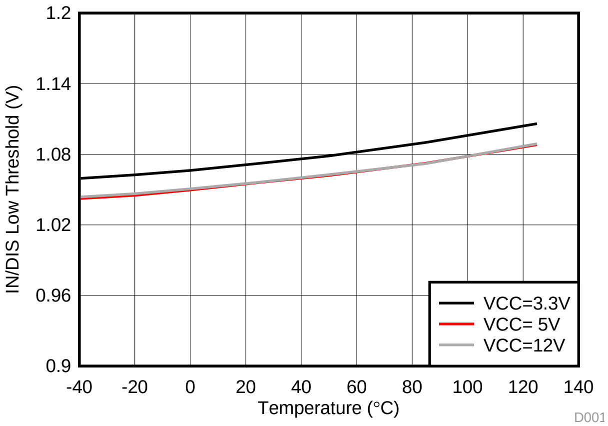


图 20. PWM/DIS Low Threshold

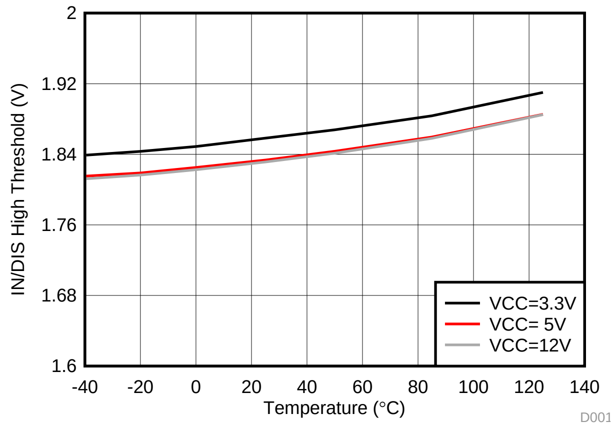


图 21. PWM/DIS High Threshold

Typical Characteristics (接下页)

VDDA = VDDB= 12 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

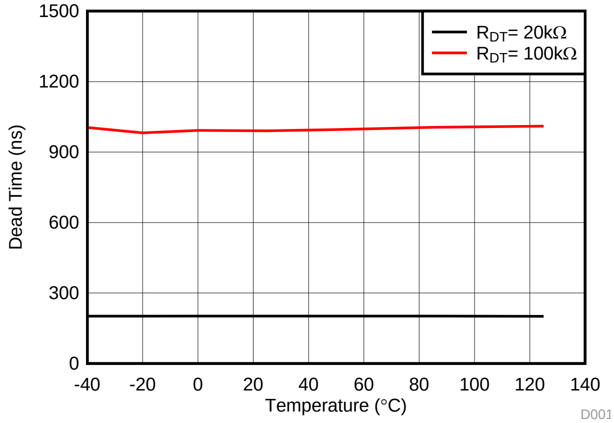


图 22. Dead Time vs. Temperature (with R_{DT} = 20 kΩ and 100 kΩ)

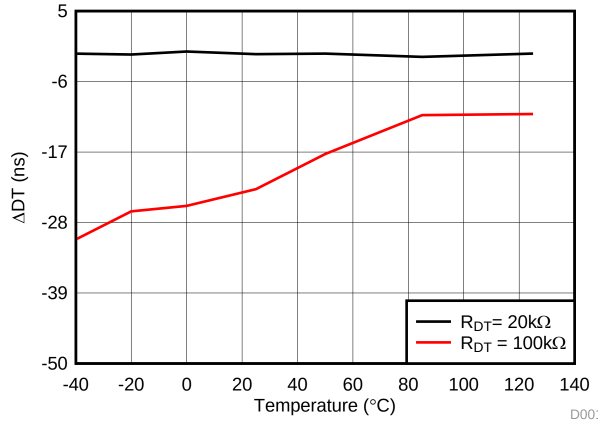


图 23. Dead Time Matching vs. Temperature (with R_{DT} = 20 kΩ and 100 kΩ)

7 Parameter Measurement Information

7.1 Propagation Delay and Pulse Width Distortion

图 24 shows how to calculate pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. These parameters can be measured by disabling the dead time function by shorting the DT Pin to VCC.

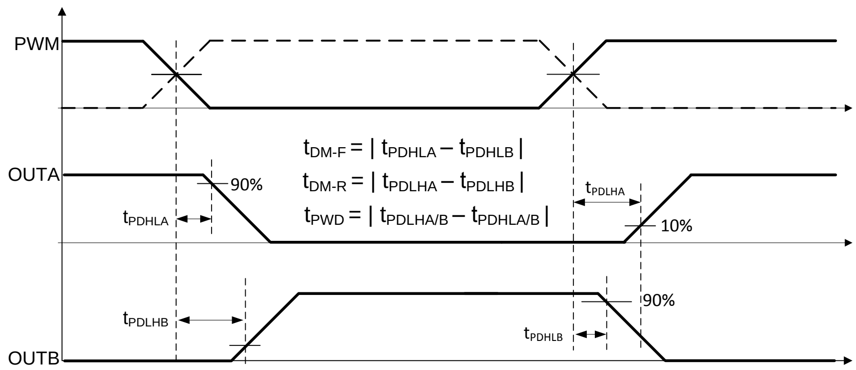


图 24. Propagation Delay Matching and Pulse Width Distortion

7.2 Rising and Falling Time

图 25 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see Output Stage.

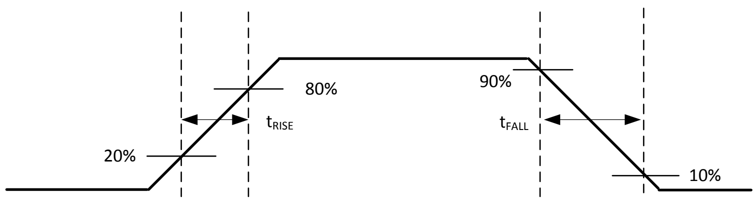


图 25. Rising and Falling Time Criteria

7.3 PWM Input and Disable Response Time

图 26 shows the response time of the disable function. For more information, see Disable Pin.

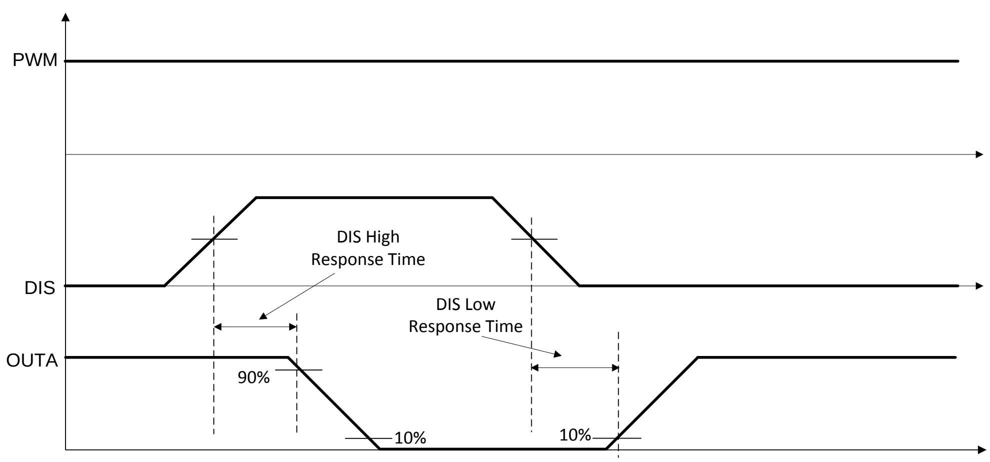


图 26. Disable Pin Timing

7.4 Programable Dead Time

Leaving the DT pin open or tying it to GND through an appropriate resistor (R_{DT}) sets a dead-time interval. For more details on dead time, refer to Programmable Dead Time (DT) Pin.

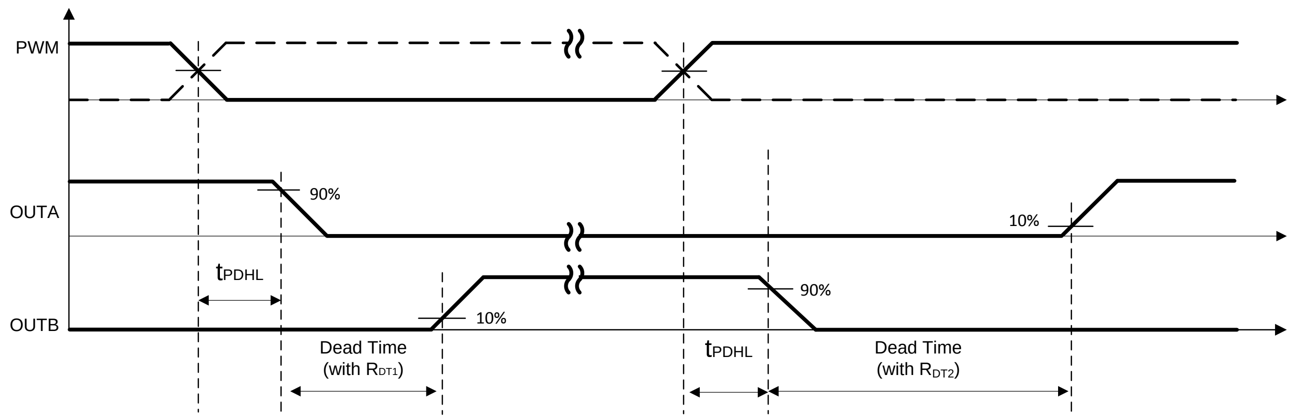


图 27. Dead-Time Switching Parameters

7.5 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+ \text{ to } OUT}$ for VCCI UVLO (typically 40-µs) and $t_{VDD+ \text{ to } OUT}$ for VDD UVLO (typically 50-µs). It is recommended to consider proper margin before launching PWM signal after the driver's VCCI and VDD bias supply is ready. 图 28 and 图 29 show the power-up UVLO delay timing diagram for VCCI and VDD.

If PWM are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+ \text{ to } OUT}$ or $t_{VDD+ \text{ to } OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <1µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

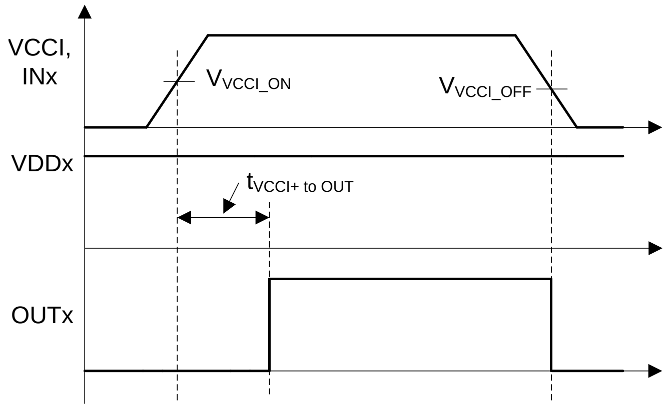


图 28. VCCI Power-up UVLO Delay

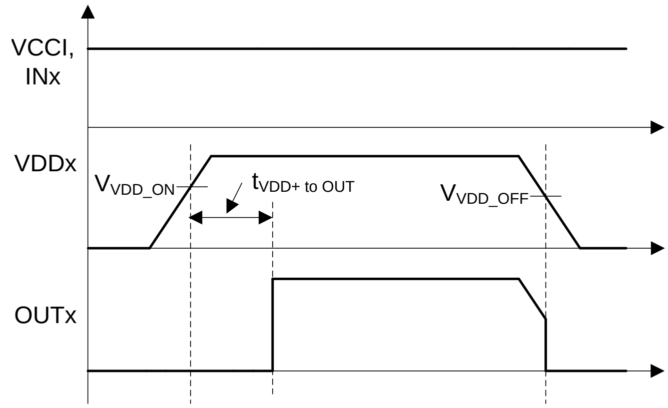


图 29. VDDA/B Power-up UVLO Delay

7.6 CMTI Testing

图 30 is a simplified diagram of the CMTI testing configuration.

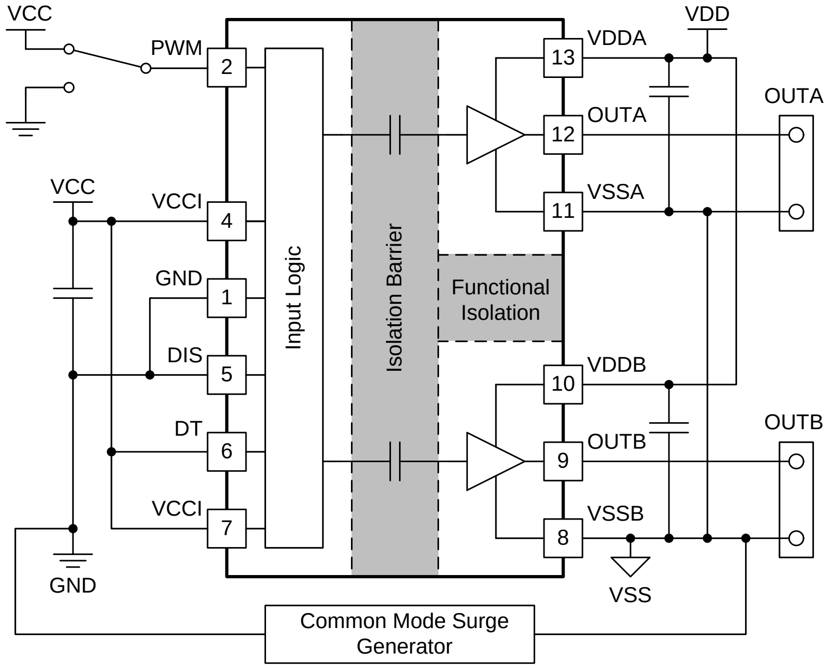


图 30. Simplified CMTI Testing Setup

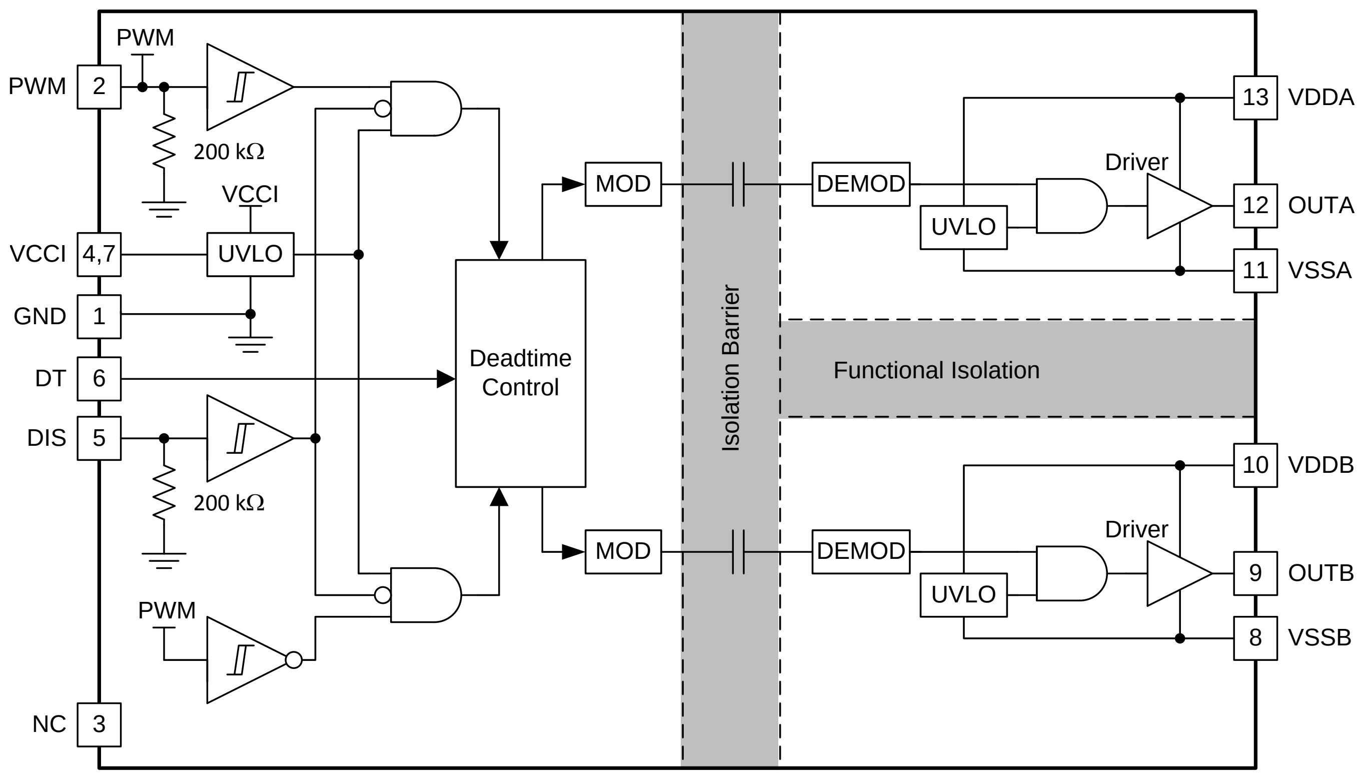
8 Detailed Description

8.1 Overview

There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA. In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors.

The UCC20225 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. UCC20225 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, a DISABLE pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC20225 also holds its OUTA low when the PWM is left open or when the PWM pulse is not wide enough. The driver input PWM is CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Importantly, Channel A is in phase with PWM input and Channel B is always complimentary with Channel A with programmed dead time.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC20225 has an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the effected outputs low, regardless of the status of the input pin (PWM).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (illustrated in 图 31). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5V, when no bias power is available. The clamp sinking current is limited only by the per-channel safety supply power, the ambient temperature, and the 6A peak sink current rating.

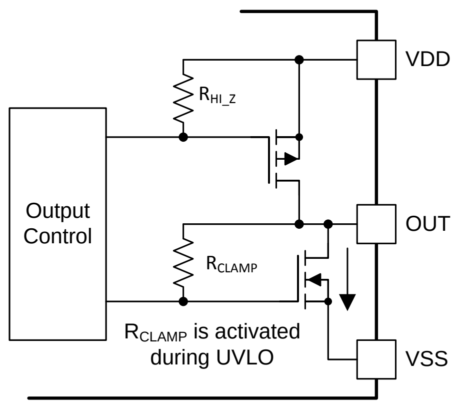


图 31. Simplified Representation of Active Pull Down Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. This also allows the device to accept small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC20225 also has an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the voltage at VCCI exceeds V_{VCCI_ON}. A signal will cease to be delivered when VCCI receives a voltage less than V_{VCCI_OFF}. As with the UVLO for VDD, there is hystersis (V_{VCCI_HYS}) to ensure stable operation.

If PWM is active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until 50µs (typical) after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective UVLO off thresholds, there is <1µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

Feature Description (接下页)

The UCC20225 can withstand an absolute maximum of 30 V for VDD, and 20 V for VCCI.

表 1. UCC20225 VCCI UVLO Feature Logic

CONDITION	INPUT	OUTPUTS	
	PWM	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L

表 2. UCC20225 VDD UVLO Feature Logic

CONDITION	INPUT	OUTPUTS	
	PWM	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L

8.3.2 Input and Output Logic Table

Assume VCCI, VDDA, VDDB are powered up. See VDD, VCCI, and Under Voltage Lock Out (UVLO) for more information on UVLO operation modes.

表 3. INPUT/OUTPUT Logic Table(1)

INPUT	DISABLE(2)	OUTPUTS		NOTE
PWM		OUTA	OUTB	
L or Left Open	L or Left Open	L	H	Output transitions occur after the dead time expires. See Programmable Dead Time (DT) Pin
H	L or Left Open	H	L	
X	H	L	L	-

(1) "X" means L, H or left open.
(2) DIS pin disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.

8.3.3 Input Stage

The input pins (PWM and DIS) of UCC20225 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V micro-controllers), since UCC20225 has a typical high threshold (V_{PWMH}) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see 图 20,图 21). A wide hysteresis (V_{PWM_HYS}) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ (See Functional Block Diagram). However, it is still recommended to ground an input if it is not being used for improved noise immunity.

Since the input side of UCC20225 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn’t exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for any gate. That said, the amplitude of any signal applied to PWM must *never* be at a voltage higher than VCCI.

8.3.4 Output Stage

The UCC20225's output stages features a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.47-Ω when activated.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC20225 pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter, yielding a faster turn-on. The turn-on phase output resistance is the parallel combination $R_{OH}||R_{NMOS}$.

The pull-down structure in UCC20225 is simply composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC20225 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

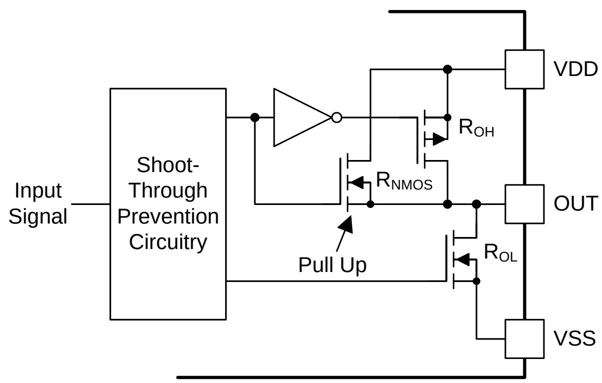


图 32. Output Stage

8.3.5 Diode Structure in UCC20225

图 33 illustrates the multiple diodes involved in the ESD protection components of the UCC20225. This provides a pictorial representation of the absolute maximum rating for the device.

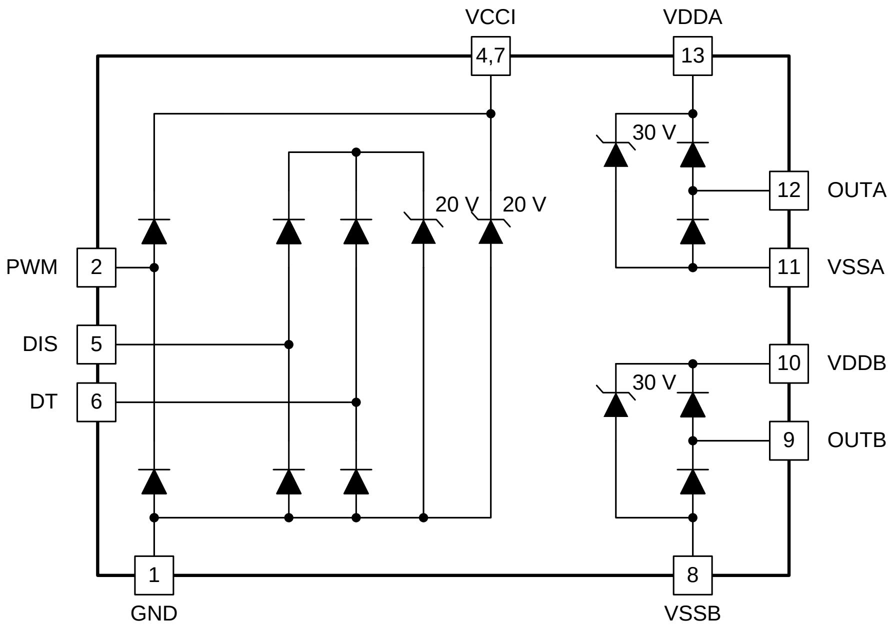


图 33. ESD Structure

8.4 Device Functional Modes

8.4.1 Disable Pin

Setting the DISABLE pin high shuts down both outputs simultaneously. Grounding (or left open) the DISABLE pin allows UCC20225 to operate normally. The DISABLE response time is in the range of 20ns and quite responsive, which is as fast as propagation delay. The DISABLE pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DISABLE pin is not used to achieve better noise immunity.

8.4.2 Programmable Dead Time (DT) Pin

UCC20225 allows the user to adjust dead time (DT) in the following ways:

8.4.2.1 Tying the DT Pin to VCC

If DT pin is tied to VCC, dead time function between OUTA and OUTB is disabled and the dead time between the two output channels is around 0ns.

Device Functional Modes (接下页)

8.4.2.2 DT Pin Left Open or Connected to a Programming Resistor between DT and GND Pins

If the DT pin is left open, the dead time duration (t_{DT}) is set to <15-ns. One can program t_{DT} by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined from 公式 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

The steady state voltage at DT pin is around 0.8V, and the DT pin current will be less than 10uA when R_{DT}=100-kΩ. Since the DT pin current is used internally to set the dead time, and this current decreases as R_{DT} increases, it is recommended to parallel a ceramic capacitor, 2.2-nF or above, close to DT pin to achieve better noise immunity and better dead time matching between two channels, especially when the dead time is larger than 300-ns.

The input signal's falling edge activates the programmed dead time for the output. An output signal's dead time is always set to the driver's programmed dead time. The driver dead time logic is illustrated in 图 34:

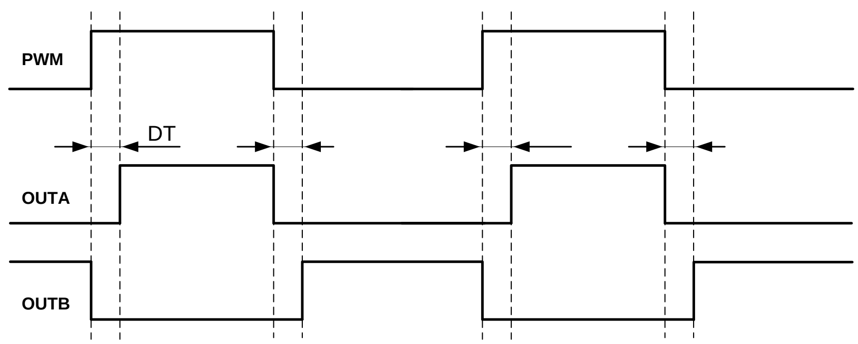


图 34. Input and Output Logic Relationship with Dead Time

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC20225 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC20225 (with up to 18-V VCCI and 25-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance, the UCC20225 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

9.2 Typical Application

The circuit in 图 35 shows a reference design with UCC20225 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

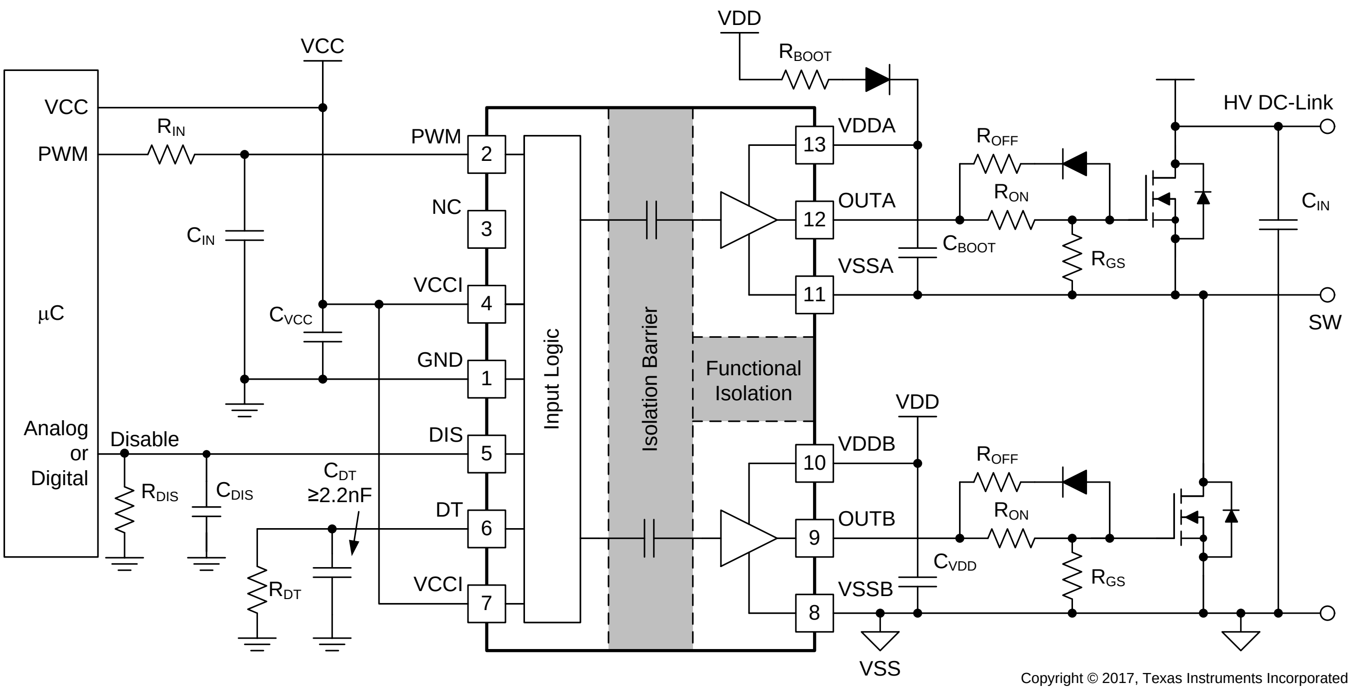


图 35. Typical Application Schematic

Typical Application (接下页)

9.2.1 Design Requirements

表 4 lists reference design parameters for the example application: UCC20225 driving 700-V MOSFETs in a high side-low side configuration.

表 4. UCC20225 Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	IPB65R150CFD	-
VCC	5.0	V
VDD	12	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	200	kHz
DC link voltage	400	V

9.2.2 Detailed Design Procedure

9.2.2.1 Designing PWM Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0-Ω to 100-Ω and a C_{IN} between 10-pF and 100-pF. In the example, an R_{IN} = 51-Ω and a C_{IN} = 33-pF are selected, with a corner frequency of approximately 100-MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

9.2.2.2 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 800 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 600-V ultrafast diode, MURA160T3G, is chosen in this example.

A bootstrap resistor, R_{BOOT}, is used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.7 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot\,(PK)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{12\ V - 1.5\ V}{2.7\ \Omega} \approx 4\ A$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop at 4 A. (2)

9.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in Output Stage, the UCC20225 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \parallel R_{OH} + R_{ON} + R_{GFET\_Int}}\right)$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \parallel R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \quad (3)$$

where

- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance. (4)

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \parallel R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12\ V - 1.3\ V}{1.47\ \Omega \parallel 5\ \Omega + 2.2\ \Omega + 1.5\ \Omega} \approx 2.2\ A \quad (5)$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \parallel R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12\ V}{1.47\ \Omega \parallel 5\ \Omega + 2.2\ \Omega + 1.5\ \Omega} \approx 2.5\ A \quad (6)$$

Therefore, the high-side and low-side peak source current is 2.2 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET\_Int}}\right)$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET\_Int}}\right) \quad (7)$$

where

- R_{OFF}: External turn-off resistance.
- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.
- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance. (8)

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET\_Int}} = \frac{12\ V - 0.8\ V - 0.75\ V}{0.55\ \Omega + 0\ \Omega + 1.5\ \Omega} \approx 5.1\ A \quad (9)$$

$$I_{OB-} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET\_Int}} = \frac{12\ V - 0.75\ V}{0.55\ \Omega + 0\ \Omega + 1.5\ \Omega} \approx 5.5\ A \quad (10)$$

Therefore, the high-side and low-side peak sink current is 5.1 A and 5.5 A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

9.2.2.4 Estimate Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC20225 (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC20225, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. 图 4 shows the per output channel current consumption vs. operating frequency with no load. In this example, V_{VCCI} = 5 V and V_{VDD} = 12 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 200 kHz is measured to be I_{VCCI} = 2 mA, and I_{VDDA} = I_{VDDB} = 1.5 mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{VDDA} + V_{VDDB} \times I_{VDDB} \approx 46\ mW \quad (11)$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW}$$

where

- Q_G is the gate charge of the power transistor. (12)

If a split rail is used to turn on and turn off, then VDD is the total difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 12\ V \times 100\ nC \times 200\ kHz = 480\ mW \quad (13)$$

Q_G represents the total gate charge of the power transistor switching 400 V at 14 A, and is subject to change with different testing conditions. The UCC20225 gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances and power transistor internal resistances are 0 Ω, and all the gate driver loss is dissipated inside the UCC20225. If there are external turn-on and turn-off resistance, the total loss will be distributed between the gate driver pull-up/down resistances, external gate resistances, and power transistor internal resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2}\left(\frac{R_{OH} \parallel R_{NMOS}}{R_{OH} \parallel R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET\_Int}}\right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC20225 gate driver loss can be estimated with:

$$P_{GDO} = \frac{480\text{ mW}}{2}\left(\frac{5\ \Omega \parallel 1.47\ \Omega}{5\ \Omega \parallel 1.47\ \Omega + 2.2\ \Omega + 1.5\ \Omega} + \frac{0.55\ \Omega}{0.55\ \Omega + 0\ \Omega + 1.5\ \Omega}\right) \approx 120\text{ mW} \tag{15}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4\text{ A} \times \int_0^{T_{R\_Sys}} \left(V_{DD} - V_{OUT_{A/B}}(t)\right)dt + 6\text{ A} \times \int_0^{T_{F\_Sys}} V_{OUT_{A/B}}(t)\,dt\right]$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off period. In cases where the output is saturated for some time, this can be simplified as a constant current source (4 A at turn-on and 6 A at turn-off) charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted. (16)

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion.

Total gate driver loss dissipated in the gate driver UCC20225, P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} = 46\text{ mW} + 120\text{ mW} = 166\text{ mW} \tag{17}$$

which is equal to 127 mW in the design example.

9.2.2.5 Estimating Junction Temperature

The junction temperature (T_J) of the UCC20225 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD}$$

where

- T_C is the UCC20225 case-top temperature measured with a thermocouple or some other instrument, and
- Ψ_{JT} is the Junction-to-top characterization parameter from the Thermal Information table. (18)

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the Semiconductor and IC Package Thermal Metrics application report.

9.2.2.6 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

9.2.2.6.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

9.2.2.6.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}\ @\ 200\ \text{kHz (No Load)}}{f_{SW}} = 100\ \text{nC} + \frac{1.5\ \text{mA}}{200\ \text{kHz}} = 107.5\ \text{nC}$$

where

- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 200kHz. (19)

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{DDA}} = \frac{107.5\ \text{nC}}{0.5\ \text{V}} \approx 0.22\ \mu\text{F}$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example. (20)

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\ \mu\text{F} \tag{21}$$

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor with a low capacitance value, in this example a 100 nF, in parallel with C_{Boot} to optimize the transient performance.

注

Too large C_{BOOT} can be detrimental. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET will not follow input signal commands for several cycles. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

9.2.2.6.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as C_{VDD} in 图 35) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 0.22-µF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10 µF, should be used in parallel with C_{VDD}.

9.2.2.7 Dead Time Setting Guidelines

For power converter topologies utilizing half-bridges, the dead time setting between the top and bottom transistor is important for preventing shoot-through during dynamic switching.

The UCC20225 dead time specification in the electrical table is defined as the time interval from 90% of one channel's falling edge to 10% of the other channel's rising edge (see 图 27). This definition ensures that the dead time setting is independent of the load condition, and guarantees linearity through manufacture testing. However, this dead time setting may not reflect the dead time in the power converter system, since the dead time setting is dependent on the external gate drive turn-on/off resistor, DC-Link switching voltage/current, as well as the input capacitance of the load transistor.

Here is a suggestion on how to select an appropriate dead time for UCC20225:

$$DT_{Setting} = DT_{Req} + T_{F\_Sys} + T_{R\_Sys} - T_{D(on)}$$

where

- $DT_{setting}$: UCC20225 dead time setting in ns, $DT_{Setting}$ = 10 × RDT(in kΩ).
- DT_{Req}: System required dead time between the real V_{GS} signal of the top and bottom switch with enough margin, or ZVS requirement.
- T_{F_Sys}: In-system gate turn-off falling time at worst case of load, voltage/current conditions.
- T_{R_Sys}: In-system gate turn-on rising time at worst case of load, voltage/current conditions.
- $T_{D(on)}$: Turn-on delay time, from 10% of the transistor gate signal to power transistor gate threshold. (22)

In the example, $DT_{Setting}$ is set to 250-ns.

It should be noted that the UCC20225 dead time setting is decided by the DT pin configuration (See Programmable Dead Time (DT) Pin), and it cannot automatically fine-tune the dead time based on system conditions. It is recommended to parallel a ceramic capacitor, 2.2-nF or above, close to DT pin to achieve better noise immunity and dead time matching.

9.2.2.8 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

图 36 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 25 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 25 V – 5.1 V ≈ 20 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

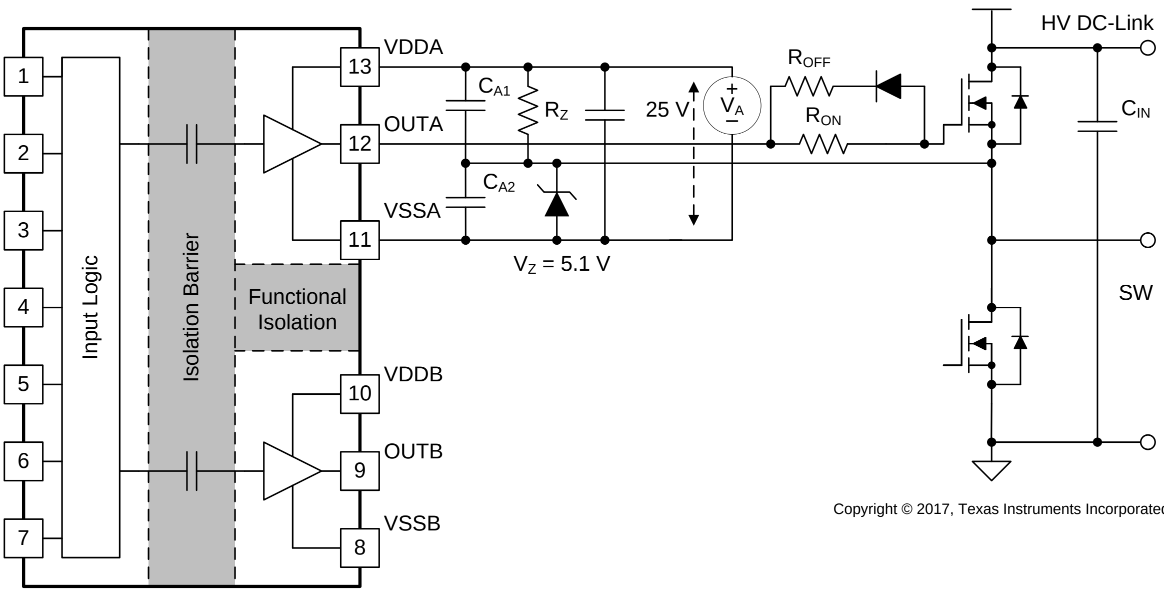


图 36. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

图 37 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and V_{A-} determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

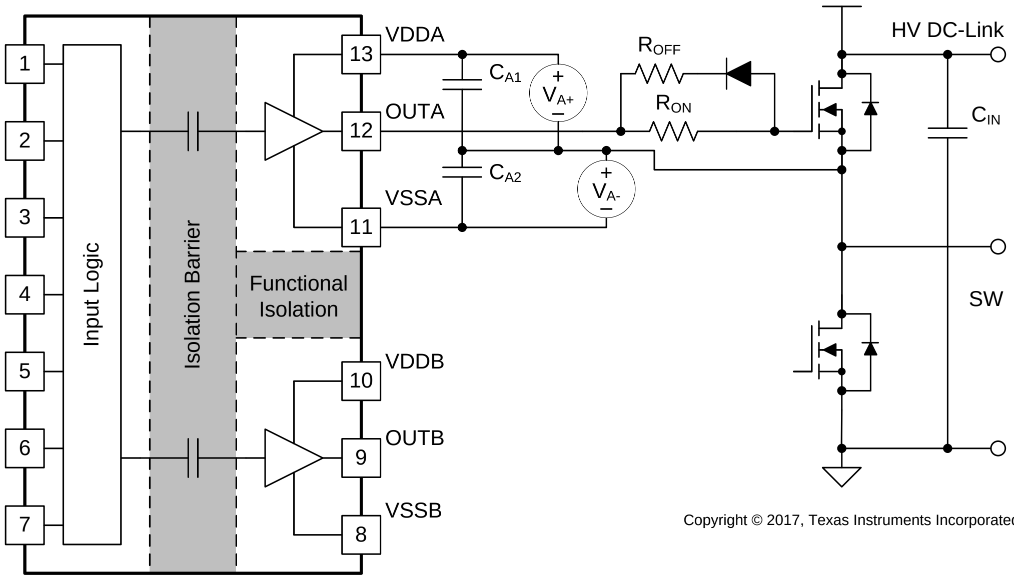


图 37. Negative Bias with Two Iso-Bias Power Supplies

The last example, shown in 图 38, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant converters or phase shift converters favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

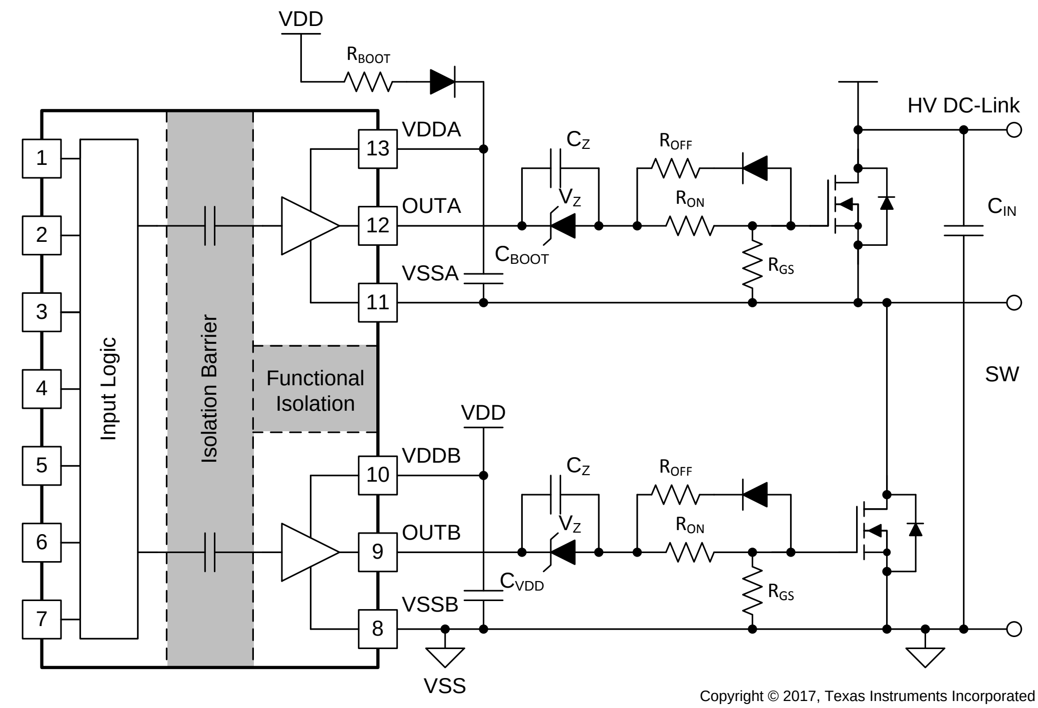


图 38. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

9.2.3 Application Curves

图 39 and 图 40 shows the bench test waveforms for the design example shown in 图 35 under these conditions: VCC = 5 V, VDD = 12 V, f_{SW} = 200 kHz, $V_{DC\text{-}Link}$ = 400 V.

Channel 1 (Indigo): UCC20225 PWM pin signal.

Channel 2 (Cyan): Gate-source signal on the high side power transistor.

Channel 3 (Magenta): Gate-source signal on the low side power transistor.

In 图 39, PWM is sent a 3.3 V, 20% duty-cycle signal. The gate drive signals on the power transistor have a 250-ns dead time, shown in the measurement section of 图 39. The dead time matching is 10-ns with the 250-ns dead time setting. Note that with high voltage present, lower bandwidth differential probes are required, which limits the achievable accuracy of the measurement.

图 40 shows a zoomed-in version of the waveform of 图 39, with measurements for propagation delay and rising/falling time. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver OUTA and OUTB pins. Due to the split on and off resistors (R_{ON}, R_{OFF}), different sink and source currents, and the Miller plateau, different rising (60, 120 ns) and falling time (25 ns) are observed in 图 40.

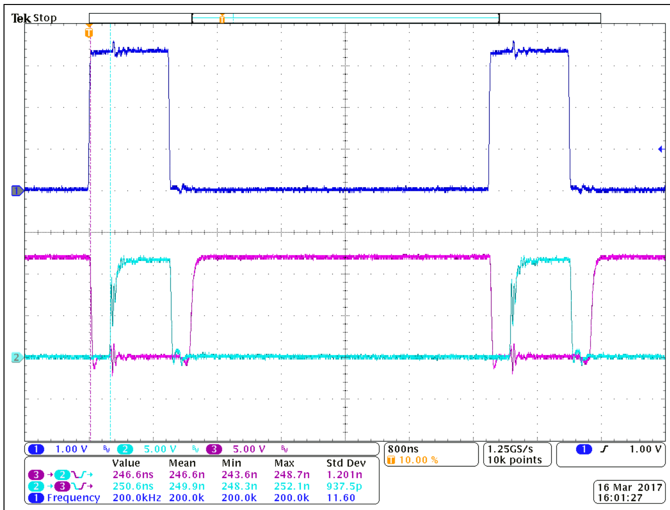


图 39. Bench Test Waveform for PWM and OUTA/B

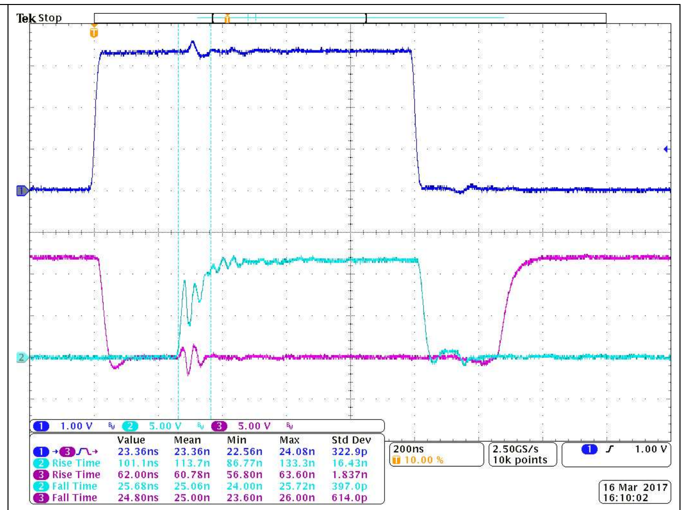


图 40. Zoomed-In bench-test waveform

10 Power Supply Recommendations

The recommended input supply voltage (VCCI) for UCC20225 is between 3-V and 18-V. The recommended output bias supply voltage (VDDA/VDDB) range is between 9.2-V to 25-V. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. VDD and VCCI should not fall below their respective UVLO thresholds for normal operation, or else gate driver outputs can become clamped low for >50µs by the UVLO protection feature (for more information on UVLO see VDD, VCCI, and Under Voltage Lock Out (UVLO)). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by UCC20225, and should not exceed the recommended maximum VDDA/VDDB of 25-V.

A local bypass capacitor should be placed between the VDD and VSS pins, with a value of between 220 nF and 10 µF for device biasing. It is further suggested that an additional 100-nF capacitor be placed in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low ESR, ceramic surface mount capacitors are recommended.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of UCC20225, this bypass capacitor has a minimum recommended value of 100 nF.

11 Layout

11.1 Layout Guidelines

One must pay close attention to PCB layout in order to achieve optimum performance for the UCC20225. Below are some key points.

Component Placement:

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to place the dead time setting resistor, R_{DT}, and its bypassing capacitor close to DT pin of UCC20225.
- It is recommended to bypass using a ≈1nF low ESR/ESL capacitor, C_{DIS}, close to DIS pin when connecting to a µC with distance.
- **Grounding Considerations:**
- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

High-Voltage Considerations:

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. PCB cutting or scoring beneath the IC are not recommended, since this can severely exacerbate board warping and twisting issues.
- For half-bridge, or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to 700 V_{DC}, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

Thermal Considerations:

- A large amount of power may be dissipated by the UCC20225 if the driving voltage is high, the load is heavy, or the switching frequency is high (Refer to Estimate Gate Driver Power Loss for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see 图 42 and 图 43). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that there shouldn't be any traces/coppers from different high voltage planes overlapping.

11.2 Layout Example

图 41 shows a 2-layer PCB layout example with the signals and key components labeled.

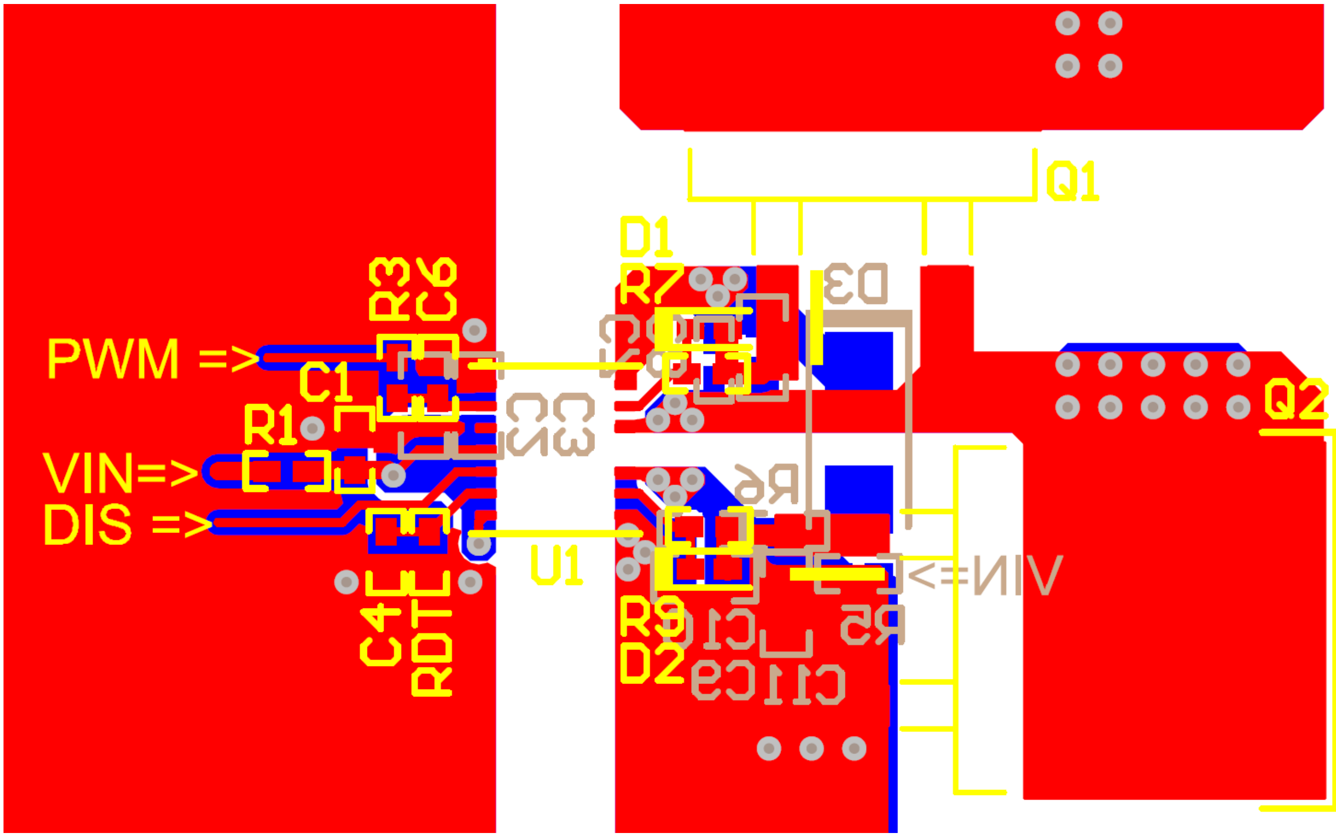


图 41. Layout Example

图 42 and 图 43 shows top and bottom layer traces and copper.

注

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

Layout Example (接下页)

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

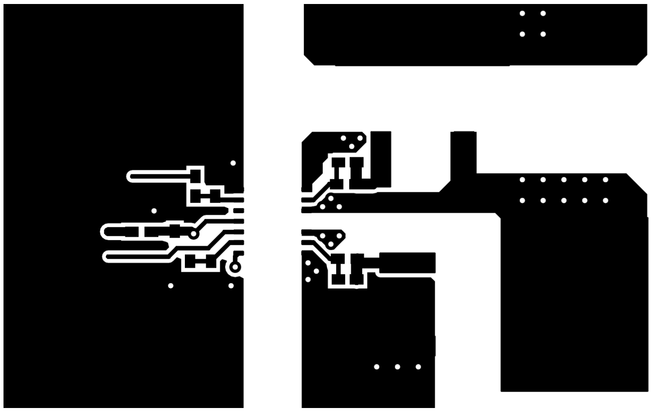


图 42. Top Layer Traces and Copper

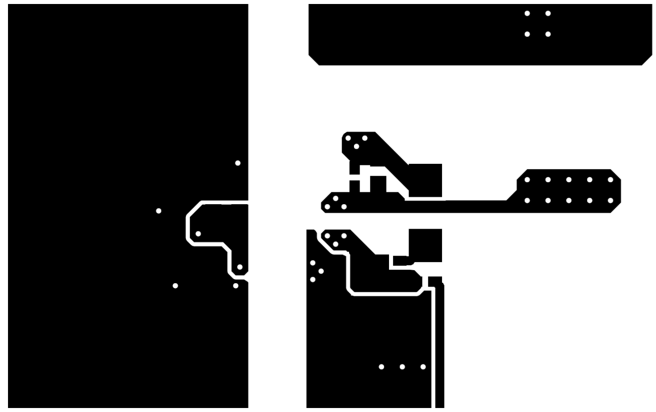


图 43. Bottom Layer Traces and Copper

图 44 and 图 45 are 3D layout pictures with top view and bottom views.

注

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

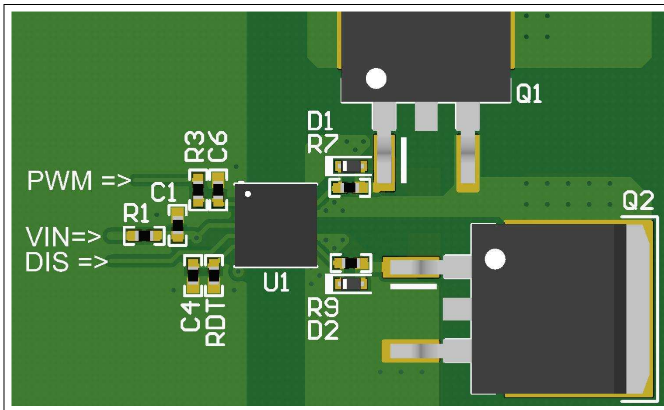


图 44. 3-D PCB Top View

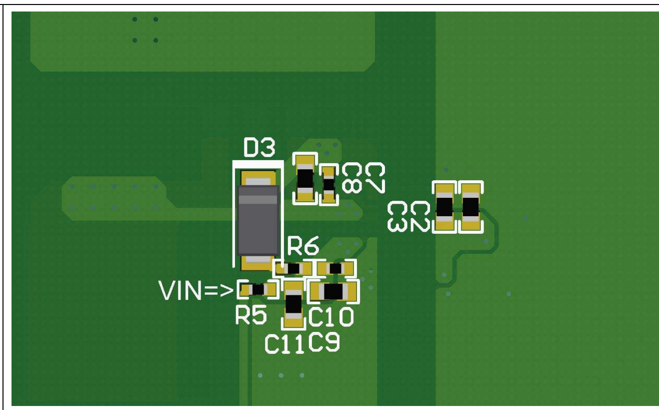


图 45. 3-D PCB Bottom View

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅：

- 隔离相关术语

12.2 认证

UL 在线认证目录，*“FPPT2.E181974 非光学隔离器件 - 组件”*，证书编号：20170718-E181974，

VDE Pruf- und Zertifizierungsinstitut 认证，工厂监督合格证书

CQC 在线认证目录，“GB4943.1-2011 数字隔离器证书”，证书编号：CQC18001186974

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区***。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGE OPTION ADDENDUM

6-Feb-2026

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC20225NPLR	Active	Production	VLGA (NPL) | 13	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	UCC20225
UCC20225NPLR.A	Active	Production	VLGA (NPL) | 13	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	UCC20225

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

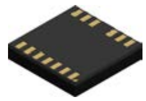
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

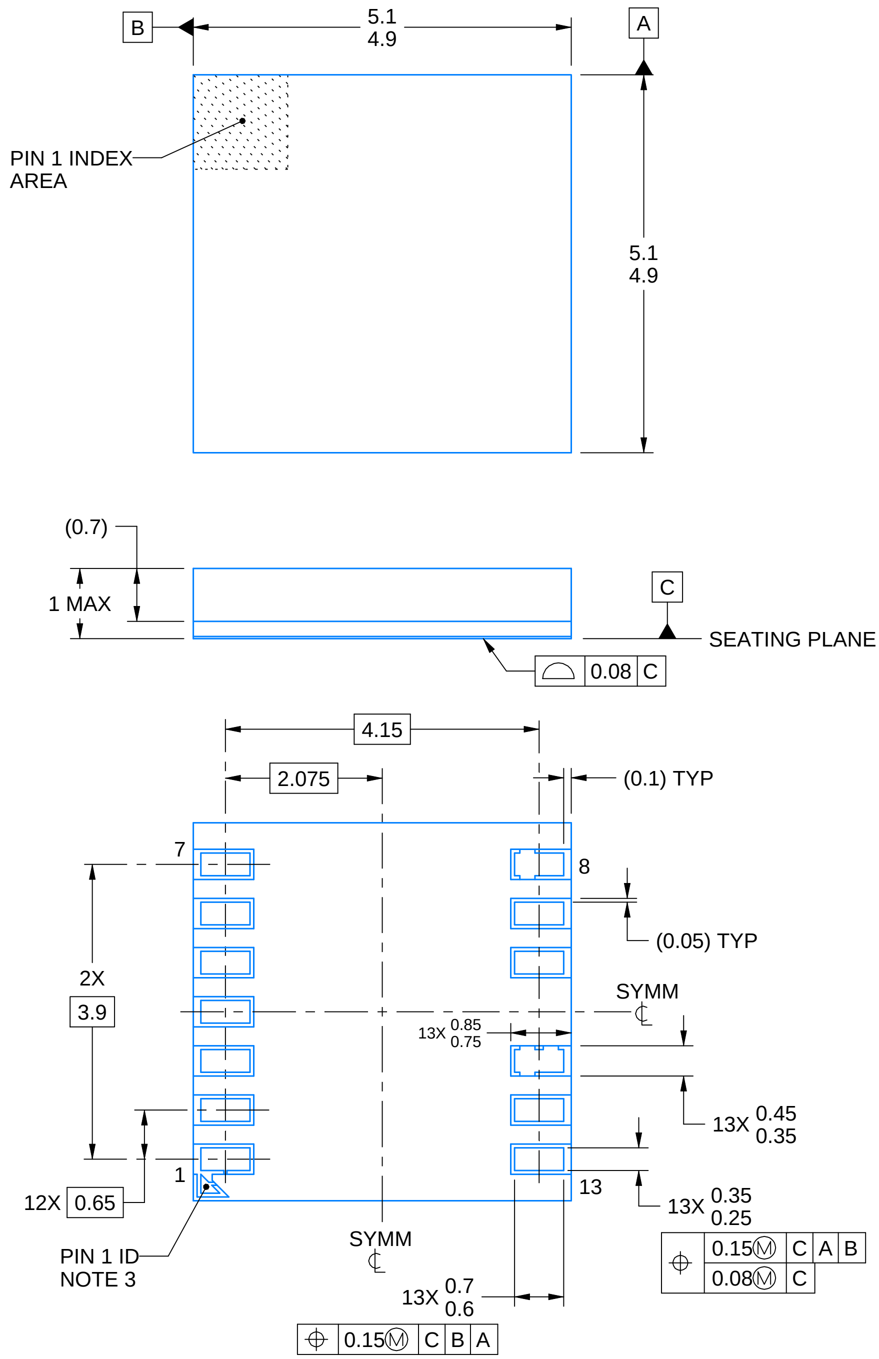
OTHER QUALIFIED VERSIONS OF UCC20225 :

- Automotive : UCC20225-Q1

NOTE: Qualified Version Definitions:

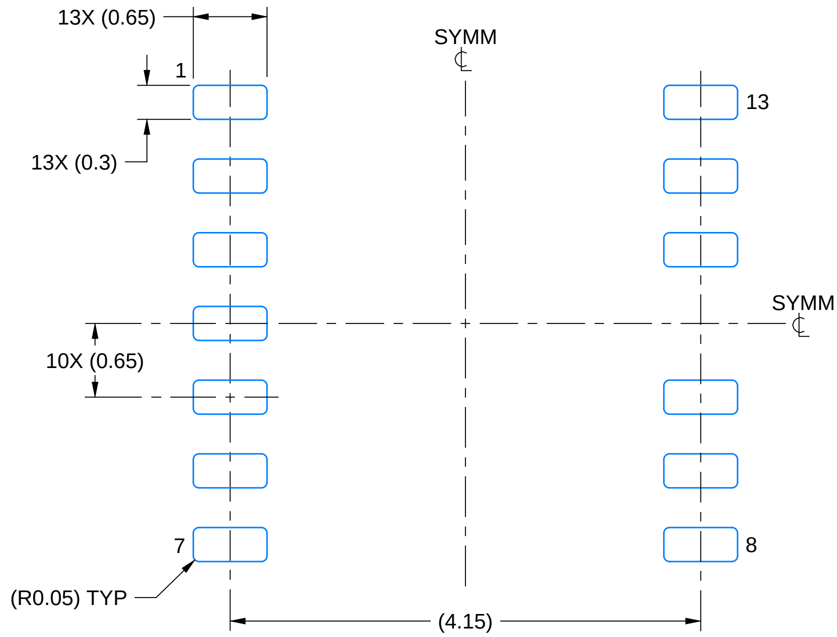
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



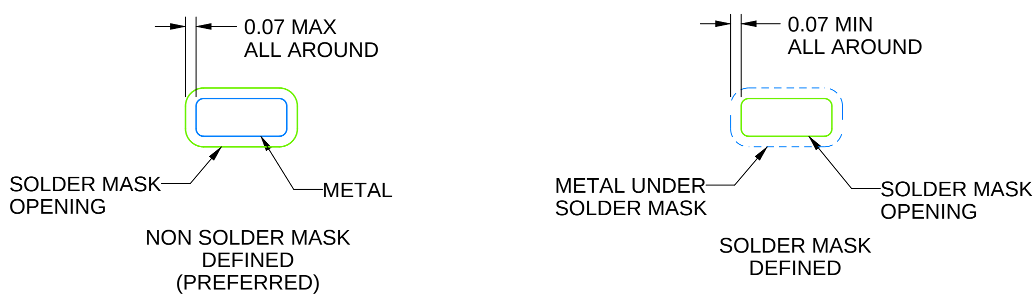


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin 1 indicator is electrically connected to pin 1.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:15X

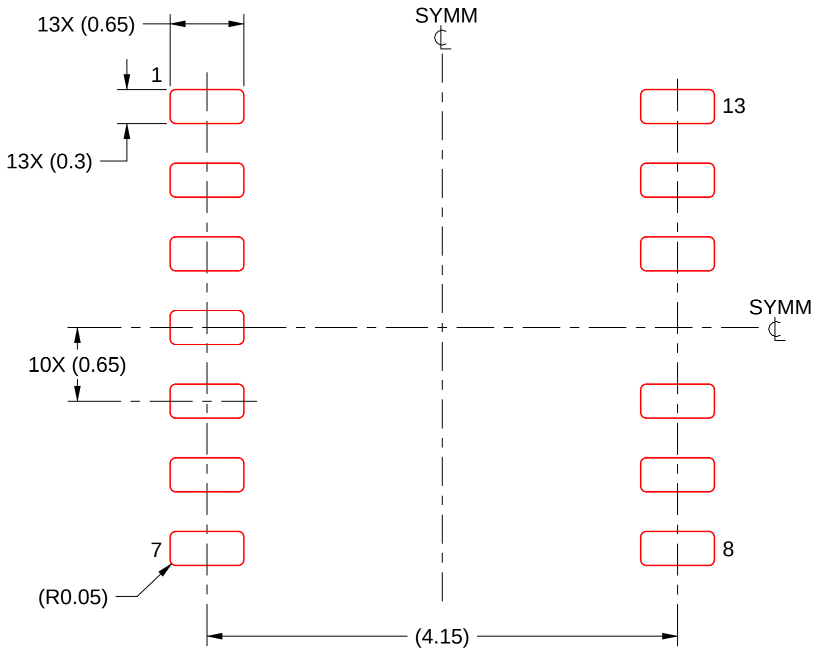


SOLDER MASK DETAILS
NOT TO SCALE

4222800/C 08/2024

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4222800/C 08/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.