SLUS621A − AUGUST 2004 − SEPTEMBER 2005

HIGH-EFFICIENCY SYNCHRONOUS BUCK PWM CONTROLLER

FEATURES

- **On-Chip Predictive Gate Drive™ for High-Efficiency Synchronous Buck Operation**
- **Dual ±3-A TrueDrive™ Outputs**
- **On-Board Programmable Oscillator with 1-MHz Frequency Operation**
- **TR Input for Sequencing Operation**
- **Overcurrent Protection using a Parallel Average Current Mode Control Loop**
- **3 Modes to Support 2.7-V to 35-V Input Bias**
- **Reverse Current Protection for Output Stage**
- **User Programmable Shutdown Using SS Pin**
- **±1.0% Initial Tolerance Bandgap Reference**
- **High Bandwidth Error Amplifiers**
- **Thermally Enhanced HTSSOP 20-Pin PowerPAD™ Package and QFN−32 Pin**
- **Synchronization Input**
- **Supports Pre-Bias Applications**

APPLICATIONS

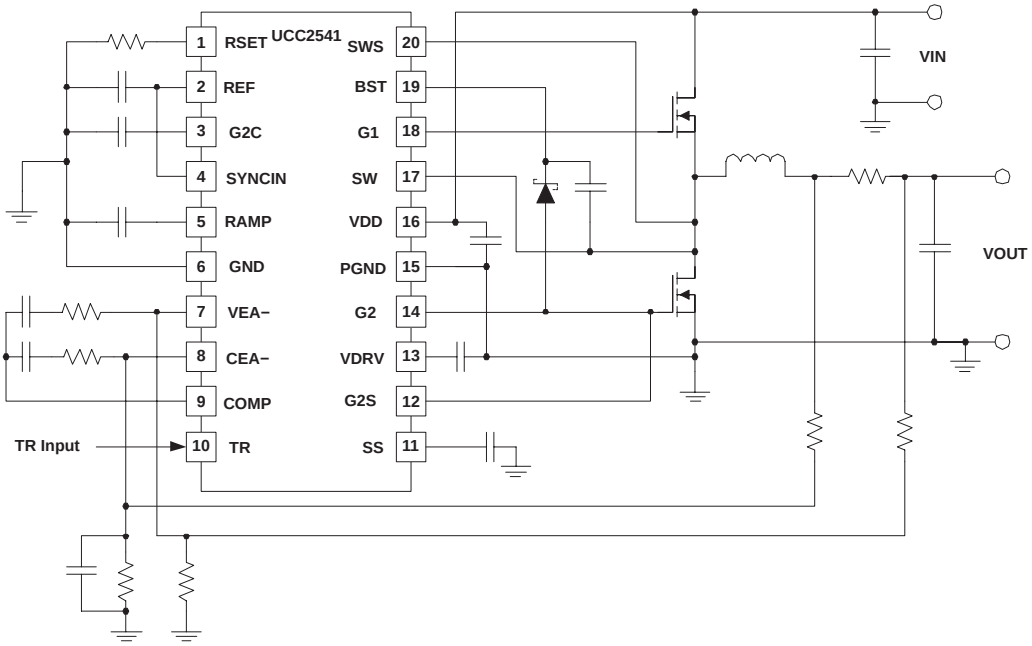
- **High Efficiency Non-Isolated Converters Requiring Advanced Features such as Pre-Bias Support and Tracking Capability**
- **Point-of-Load Modules for Servers, Telecom, and Data communication Equipments**
- **Good for Input Voltages of 3.3 V, 5.0 V, 12.0 V, or Intermediate Bus Voltages**

DESCRIPTION

The UCC2541 is a synchronous buck PWM controller for high current and low output voltage applications.

For higher efficiency, it incorporates the Predictive Gate Drive™ technology that virtually eliminates body diode conduction losses in synchronous rectifiers.

SIMPLIFIED APPLICATION DIAGRAM



Predictive Gate Drive™, TrueDrive™ and PowerPAD™ are trademarks of Texas Instruments Incorporated.

DESCRIPTION (CONT.)

The UCC2541 is available in the extended temperature range of –40°C to 105°C and is offered in thermally enhanced PowerPAD™ 20-pin HTSSOP (PWP) or 32-pin quad flatpack (RHB) package. This space saving package with standard 20-pin TSSOP footprint has a drastically lower thermal resistance of 1.4°C/W θ_{JC} to accommodate the dual high-current drivers on board.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		UCC2541	UNIT
Supply voltage range, VDD		36	V
Supply current, I_{VDD}	VDD	50	mA
Analog input voltages	CEA−, COMP, G2C, RAMP, SS, TR, VEA−	−0.3 to 3.6	V
	VDRV	−0.3 to 9	
	G1, BST	SW−0.3 to SW+9	
	SW, SWS	−1 to 36	
	G2, G2S	−1 to 9	
	SYNCIN	−0.3 to 8.0	
Sink current (peak), I_{OUT_SINK}	G1, G2	3.5	A
Source current (peak), I_{OUT_SOURCE}	G1, G2	−3.5	
Operating junction temperature range, T_J		−55 to 150	°C
Storage temperature, T_{stg}		−65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND. Currents are positive into, and negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, VDD	Mode 1	8.5		35	V
Supply voltage, VDRV	Mode 2	4.75		9.00	
Supply voltage, REF	Mode 3	3.0	3.3	3.6	
Supply voltage bypass, C_{VDD}		1.0	2.2		µF
Reference bypass capacitor, C_{REF}		0.1	1.0	2.2	
VDRV bypass capacitor, C_{VDRV}		0.2			
BST−SW bypass capacitor, C_{BST-SW}		0.1			
Timer current resistor range, R_{RSET}		10		50	kΩ
PWM ramp capacitor range, C_{RAMP}		100		680	pF
Turn-off capacitor range, C_{G2C}		120		1000	
COMP pin load range, R_{LOAD}		6.5			kΩ
Junction operating temperature, T_J		−40		105	°C

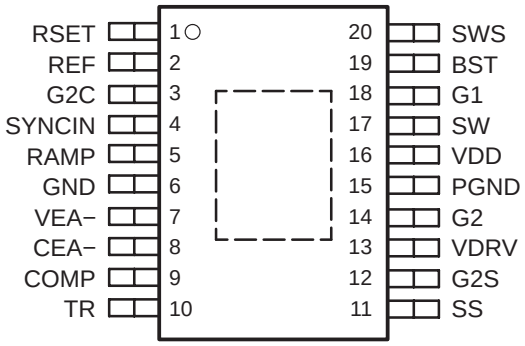
ORDERING INFORMATION

$T_A = T_J$	HTSSOP−20 (PWP)(1)	QFN−32 (RHB)(1)
	Bulk	Bulk
−40°C to +105°C	UCC2541PWP	UCC2541RHB

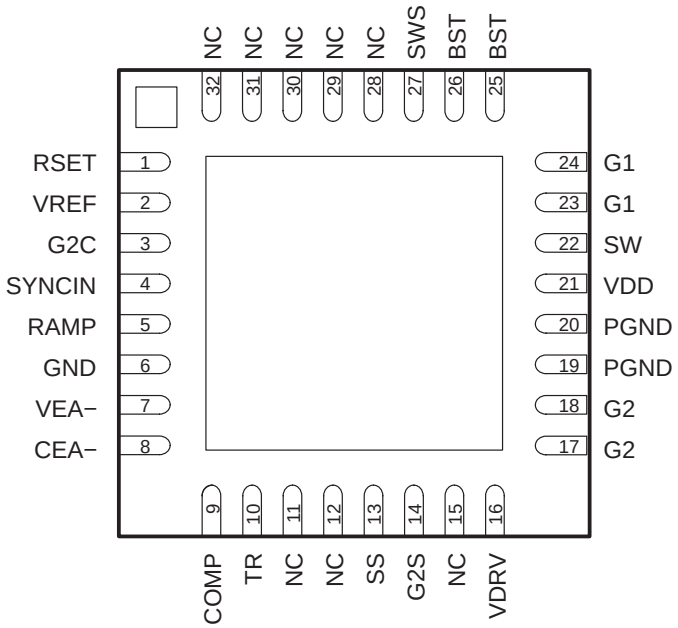
(1) The PWP and RHB packages are also available at 73 devices per tube and taped and reeled at 3,000 devices per reel. Add an R suffix to the device type (i.e., UCC2541PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

CONNECTION DIAGRAM

PWP PACKAGE
(TOP VIEW)



RHB PACKAGE
(TOP VIEW)



NC − No internal connection

NOTE: The PowerPAD™ is not directly connected to any lead of the package, but is thermally connected to the substrate of the device. The exposed dimension is 1.3 mm x 1.7 mm for the PWP package and 3.25 mm x 3.25 mm for the RHB package. However, the tolerances can be +1.05 mm / −0.05 mm (+41 mils / −2 mils) due to position and mold flow variation.

THERMAL INFORMATION

PACKAGE FAMILY	PACKAGE DESIGNATOR	θ_{JA} (°C/W) (with PowerPAD)	θ_{JC} (°C/W) (without PowerPAD)	θ_{JC} (°C/W) (with PowerPAD)	MAXIMUM DIE TEMPERATURE
PowerPAD™ HTSSOP−20	PWP	22.3 to 32.6 (500 to 0 LFM)	19.9	1.4	125°C
Quad Flatpack QFN−32	RHB	22.3 to 32.6 (500 to 0 LFM)	19.9	1.4	125°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from BST to SW, 1-µF capacitor from REF to GND, 0.1-µF and 2.2-µF capacitors from VDRV to PGND, C_{RAMP} = 517 pF, R_{SET} = 10 kΩ, $T_A = T_J$ = −40°C to 105°C, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
I_{VDD}	Operating current	DC, after G2 timeout	5	8	10	mA
		C_{LOAD} = 2.2 nF	9	18	30	
UNDERVOLTAGE LOCKOUT						
V_{VDD}	Start threshold voltage	MODE 1	8.0	8.5	9.0	V
V_{VDD}	Stop threshold voltage	MODE 1	7.5	8.0	8.5	
V_{VDD}	Hysteresis	MODE 1	0.3	0.5	0.8	
V_{VDRV}	Start threshold voltage	MODE 2	4.30	4.65	4.85	
V_{VDRV}	Stop threshold voltage	MODE 2	4.0	4.3	4.6	
V_{VDRV}	Hysteresis	MODE 2	0.15	0.35	0.55	
V_{REF}	Start threshold voltage	MODE 3 V_{VDD}= V_{VDRV}	2.5	2.8	3.2	
V_{REF}	Stop threshold voltage	MODE 3	2.2	2.5	2.8	
V_{REF}	Hysteresis	MODE 3	0.15	0.35	0.55	
VOLTAGE REFERENCE (REF)						
V_{REF}	Reference output voltage	T_A = 25°C	3.28	3.30	3.35	V
		Total variation	3.2	3.3	3.4	
I_{SC}	Short circuit current	V_{REF} = 0 V, T_A = 25°C	10	13	20	mA
	Line regulation	5.25 V ≤ V_{DRV} ≤ 7.2 V	0	1.5	15	mV
	Load regulation	0 mA ≤ I_{REF} ≤ 5 mA	0	30	70	
OscillatorPWM (RAMP)						
f_{SW}	Oscillator frequency		270	300	330	kHz
D_{MIN}	Minimum duty cycle				0%	
V_{RAMP}	Offset voltage		0.10	0.25	0.50	V
	Oscillator peak voltage		1.7	2.0	2.3	
t_{DEAD}	G1 deadtime at maximum duty cycle ratio		150	175	200	ns
I_{RAMP}	Ramp charge current	R_{RSET} = 10 kΩ	−325	−300	−275	µA
CURRENT ERROR AMPLIFIER						
V_{CEA+}	Offset voltage	Total variation	45	50	55	mV
GBW	Gain bandwidth(3)		3	4		MHz
V_{OL}	Low-level output voltage	I_{COMP} = 0 A, $V_{CEA−}$ = 3.3 V, $V_{VEA−}$ = 2.0 V			0.1	V
		I_{COMP} = 100 µA, $V_{CEA−}$ = 1.5 V $V_{VEA−}$ = 1 V	0	0.60	0.90	
V_{OH}	High-level output voltage	I_{COMP} = 0 A, $V_{CEA−}$ = 0 V, $V_{VEA−}$ = 1 V	2.2	2.5	3.0	V
A_{VOL}	Open loop		60	100	160	dB
I_{BIAS}	Bias current		−200	−80	−10	nA
I_{SINK}	Sink current	V_{COMP} = 1.0 V, $V_{CEA−}$ = 1.5 V, $V_{VEA−}$ = 1 V	0.30	0.80	1.70	mA
CMR	Common mode input range(3)		0		2	V

(3) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from BST to SW, 1-µF capacitor from REF to GND, 0.1-µF and 2.2-µF capacitors from VDRV to PGND, C_{RAMP} = 517 pF, R_{SET} = 10 kΩ, $T_A = T_J$ = −40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE ERROR AMPLIFIER						
V_{SS_OFF}	Offset voltage from soft-start input	$V_{COMP} = V_{VEA-}$, V_{SS-} = 1.5 V	0.40	0.75	1.00	V
V_{TR_OFF}	Offset voltage from tracking input	V_{TR} = 1.0 V	−10		10	mV
V_{VEA+}	Threshold voltage (from VEA− to COMP)	0°C ≤ T_A ≤ 105°C	1.485	1.500	1.515	V
		Total variation	1.47	1.50	1.53	
GBW	Gain bandwidth(3)		3	4		MHz
V_{OL}	Low-level output voltage	I_{COMP} = 0 A, V_{CEA-} = 3.3 V, V_{VEA-} = 2.0 V,			0.1	V
		I_{COMP} = 100 µA, V_{CEA-} = 0 V, V_{VEA-} = 1 V, V_{TR} = 0 V	0	0.60	0.9	
V_{OH}	High-level output voltage	I_{COMP} = 0 A, V_{CEA-} = 0 V V_{VEA-} = 1 V	2.2	2.5	3.0	
A_{VOL}	Open loop		60	100	140	dB
I_{BIAS}	Bias current		−500	−250	−50	nA
I_{SINK}	Sink current	V_{COMP} = 1.0 V, V_{CEA-} = 0 V, V_{VEA-} = 1.0 V, V_{TR} = 0 V	0.30	0.80	1.70	mA
CURRENT SET						
I_{OUT}	Output current	R_{RSET} = 10 kΩ	−158	−150	−142	µA
V_{RSET}	R_{SET} voltage	R_{RSET} = 10 kΩ	1.42	1.50	1.58	V
SYNCHRONIZATION AND SHUTDOWN TIMER (SYNCIN, G2C)						
	Timer threshold		2.3	2.5	2.7	V
	SYNCIN threshold		1.50	1.65	1.80	
$I_{CHG(G2C)}$	Shutdown timer charge current	R_{RSET} = 10 kΩ	−325	−300	−275	µA
SOFT-START (SS)						
$I_{CH(SS)}$	Charge current	R_{RSET} = 10 kΩ	−230	−200	−170	µA
$I_{DSCH(SS)}$	Discharge current	R_{RSET} = 10 kΩ	45	70	100	
	Discharge/shutdown threshold		0.35	0.45	0.55	V
DRIVE REGULATOR (VDRV)						
V_{VDRV}	Output voltage		6.87	7.20	7.53	V
	Line regulation	9 V ≤ V_{VDD} ≤ 35 V	0	50	100	mV
	Load regulation	−5 mA ≤ I_{VDRV} ≤ 0 mA	0	50	100	
I_{SC}	Short-circuit current		15	30	50	mA
G2S GATE DRIVE SENSE						
	G2S rising threshold voltage	V_{SWS} = 0 V	1.90	2.25	3.10	V
	G2S falling threshold voltage	V_{SWS} = 0 V	1.00	1.25	1.30	
I_{G2S}	Current	V_{G2S} = 0 V	−0.70	−0.50	−0.37	mA
SWS SWITCH NODE SENSE						
	SWS rising threshold voltage	V_{G2S} = 0 V	1.90	2.25	2.90	V
	SWS falling threshold voltage	V_{G2S} = 0 V	1.0	1.2	1.3	
I_{SWS}	Current	V_{SWS} = 0 V	−1.8	−1.3	−0.9	mA
		Outputs disabled	−1.0		1.0	µA
	Negative threshold voltage		−0.5	−0.3	−0.1	V

(3) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from BST to SW, 1-µF capacitor from REF to GND, 0.1-µF and 2.2-µF capacitors from VDRV to PGND, C_{RAMP} = 517 pF, R_{SET} = 10 kΩ, $T_A = T_J$ = −40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
G1 MAIN OUTPUT								
R_{SINK}	Sink resistance	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 0.3 V	0.3	0.7	1.3	Ω
R_{SRC}	Source resistance	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 5.7 V	10	25	45	Ω
I_{SINK}	Sink current(3)	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 3.0 V		3		A
I_{SRCE}	Source current(3)	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 3.0 V		−3		A
t_{RISE}	Rise time	C_{LOAD} = 2.2 nF, from G1 to SW				12	25	ns
t_{FALL}	Fall time	C_{LOAD} = 2.2 nF, from G1 to SW				12	25	ns
G2 SYNCHRONOUS RECTIFIER OUTPUT								
R_{SINK}	Sink resistance	V_{G2} = 0.3 V			5	15	30	Ω
I_{SINK}	Sink current(3)	V_{G2} = 3.25 V				3		A
I_{SRC}	Source current(3)	V_{G2} = 3.25 V				−3		A
t_{RISE}	Rise time	C_{LOAD} = 2.2 nF, from G2 to PGND				12	25	ns
t_{FALL}	Fall time	C_{LOAD} = 2.2 nF, from G2 to PGND				12	25	ns
V_{OH}	High-level output voltage, G2	V_{SW} = GND			6.2	6.7	7.5	V
DEADTIME DELAY (see Figure 1)								
$t_{ON(G1)}$	RAMP rising to G1 rising				90	115	130	ns
$t_{OFF(G1)}$	SYNCIN falling to G1 falling				50	70	90	ns
$t_{ON(G2)}$ $t_{OFF(G2)}$	Delay control resolution				3.5	5.0	6.5	ns
$t_{ON(G2)}$	G2 on-time minimum	wrt G1 falling				−24		ns
$t_{ON(G2)}$	G2 on-time maximum	wrt G1 falling				62		ns
$t_{OFF(G2)}$	G2 off-time minimum	wrt G1 rising				−68		ns
$t_{OFF(G2)}$	G2 off-time maximum	wrt G1 rising				10		ns

(3) Ensured by design. Not production tested.

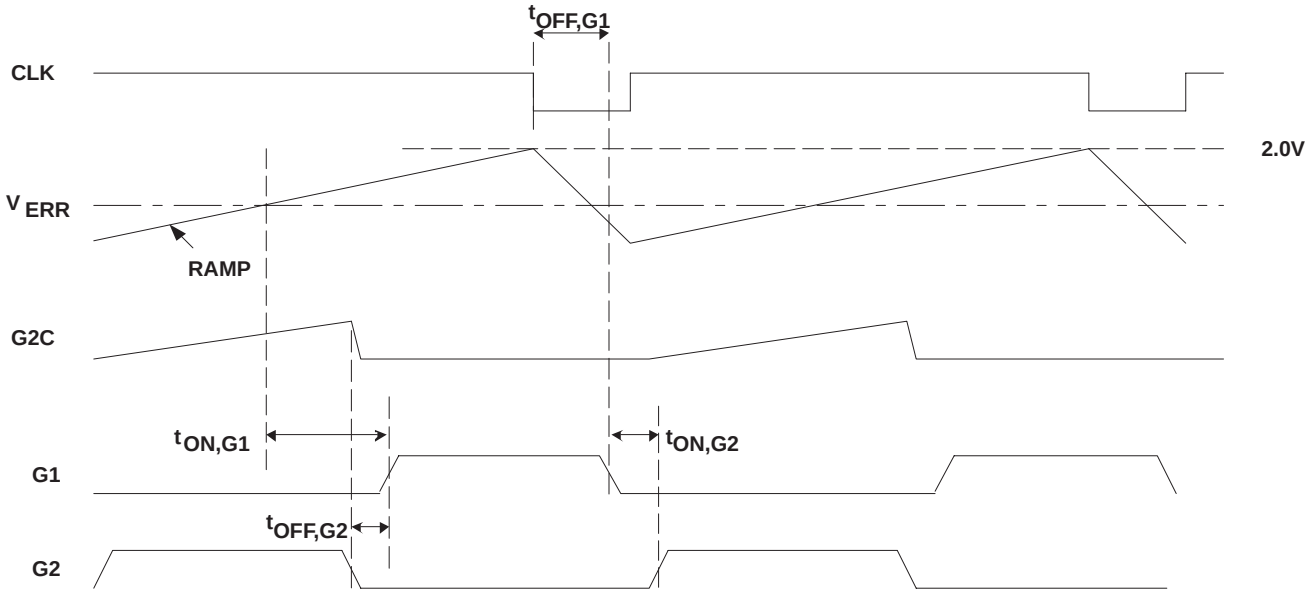
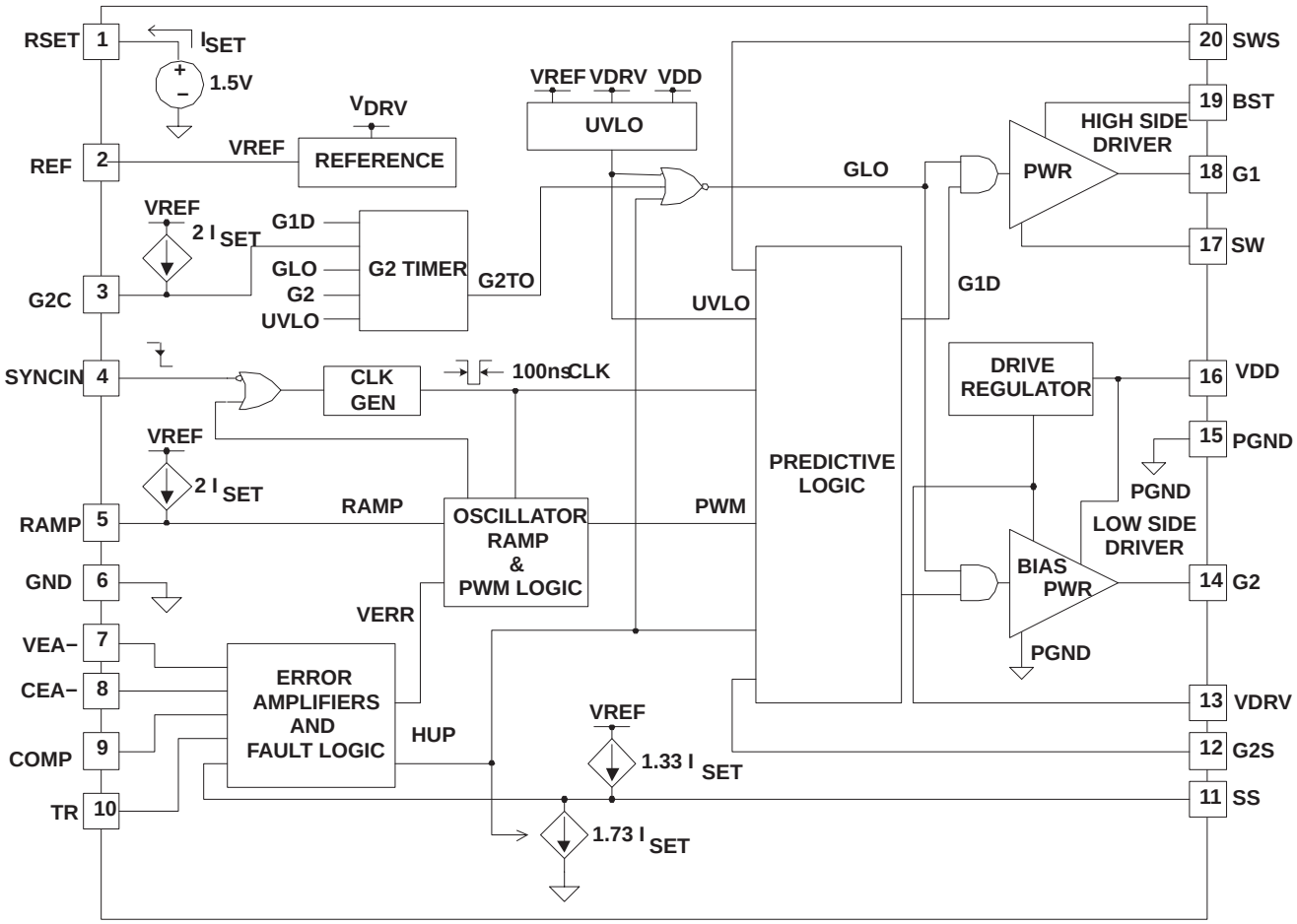


Figure 1. Predictive Gate Drive Timing Diagram

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BST	19	I	Floating G1 driver supply pin. VHI is fed by an external Schottky diode during the SR MOSFET on time. Bypass BST to SW with an external capacitor.
CEA−	8	I	Inverting input of the current error amplifier used for output current regulation.
COMP	9	I	Output of the voltage and current error amplifiers for compensation.
G1	18	O	High-side gate driver output that swings between SW and BST.
G2	14	O	Low-side gate driver output that swings between PGND and VDRV.
G2C	3	I	Timer pin to turn off synchronous rectifier. The capacitor connected to this pin programs the maximum duration that G2 is allowed to stay HIGH.
G2S	12	I	Used by the predictive deadtime controller for sensing the SR MOSFET gate voltage to set the appropriate dead-time.
GND	6	−	Ground for internal circuitry. GND and PGND should be tied together under the device. See layout guidelines for further details.
PGND	15	−	Ground return for the G2 driver. Connect PGND to the pc-board ground plane with several vias.
RAMP	5	I	Input pin to connect timing capacitor to GND to generate the oscillator PWM ramp.
REF(1)	2	I/O	3.3-V reference pin. All analog control circuits are powered from this 3.3-V rail. Bypass this pin with at least 0.1 μF of capacitance for REF loads that are 0 mA to −1 mA. Bypass this pin with at least 1 μF of capacitance if it is used as an input (Mode 3) or if it has large or pulsating loads.
RSET	1	I	Pin to program timer currents for G2C, RAMP, SS charge and SS discharge. This pin generates a current proportional to the value of the external resistor connected from RSET pin to GND. RSET range is 10 kΩ to 50 kΩ (giving a programmable nominal ISET range of 30 μA to 150 μA, respectively).
SS	11	I	Soft start and shutdown pin. Connect a capacitor to GND to set the soft-start time. Add switch to GND for immediate shutdown functionality.
SYNCIN	4	I	Input pin for timing signal. Tie to logic high (V_{REF}) when not used.
SW	17	−	G1 driver return connection.
SWS	20	I	Used by the predictive controller to sense SR body-diode conduction. Connect to SR MOSFET drain close to the MOSFET package.
TR	10	I	Tracking input to the voltage error amplifier. Connect to REF when not used.
VDD	16	I	Power supply pin to the device and input to the internal VDRV drive regulator. Normal V_{DD} range is from 4.5 V to 36 V. Bypass the pin with at least 1 μF of capacitance.
VDRV	13	I	Output of the drive regulator and power supply pin for the G2 driver. VDRV is also the supply voltage for the internal logic and control circuitry.
VEA−	7	I	Inverting input of the voltage error amplifier used for output voltage regulation.

(1) REF is an input in Mode 3 only.

APPLICATION INFORMATION

The UCC2541 is a high-efficiency synchronous buck controller that can be used in many point-of-load applications.

CEA− and VEA− pins: Current Limit and Hiccup Mode

Typical power supply load voltage versus load current is shown in Figure 2. This figure shows steady state operation for no-load to overcurrent shutdown (soft-start retry is not depicted in the diagram). During the voltage regulation conditions, the voltage error amplifier output is lower than the current error amplifier, allowing the voltage error amplifier to control operation. During the current limit conditions, the current error amplifier output is lower than the voltage error amplifier, allowing the current error amplifier to control operation. The boundary between voltage and current control occurs when the difference between CEA− and VEA− tries to exceed 50 mV.

Current limiting begins to occur when the difference between CEA− and VEA− exceeds 50 mV. For currents that exceed this operating condition, the UCC2541 controls the converter to operate as a pure current source until the output voltage falls to half of its rated steady state level. Then the UCC2541 sets both G1 and G2 outputs to LOW and it latches a fault that discharges the soft-start voltage at 30% of its charging rate. The UCC2541 inhibits a retry until the soft-start voltage falls below 0.5 V. A functional diagram of the voltage and current error amplifiers is shown in Figure 3.

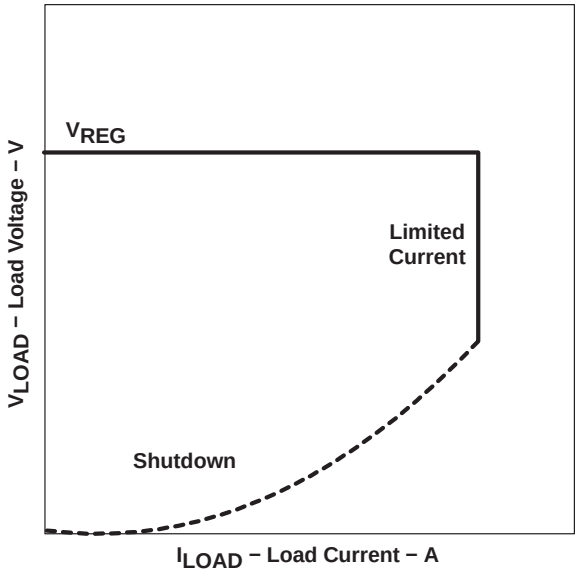


Figure 2. Typical Power Supply Load Voltage vs Current

APPLICATION INFORMATION

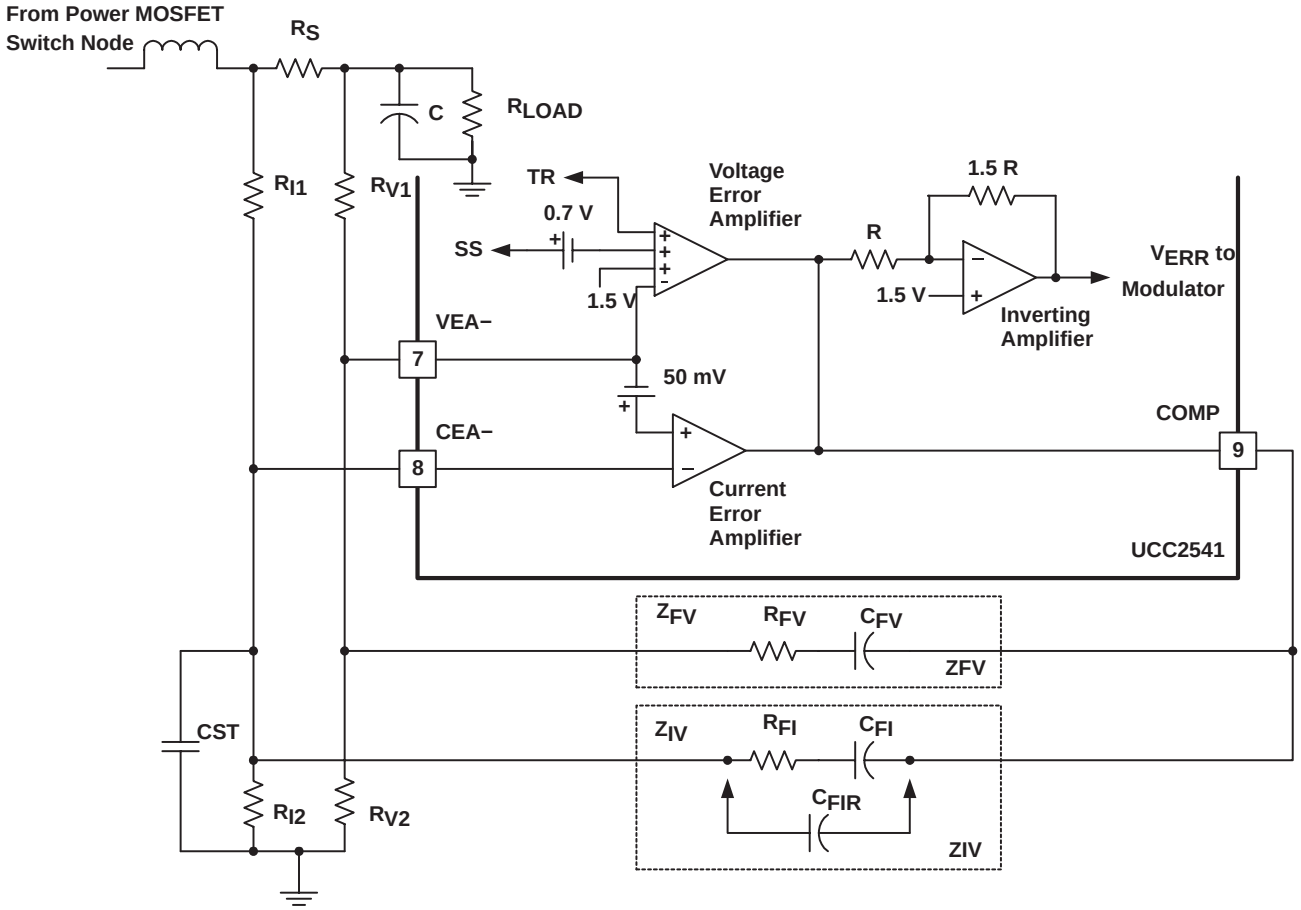


Figure 3. Error Amplifier Configuration

Component selection includes setting the voltage regulation threshold, then the current limit threshold, as described below.

Voltage vs. Current Programming (refer to Figure 3):

1. Determine the ratio $\frac{R_{V1}}{R_{V2}} = \frac{V_{LOAD(reg)}}{V_{VEA-} + \text{Threshold Voltage}} - 1\ V = \frac{V_{LOAD(reg)}}{1.5\ V\ (typ)} - 1\ V$
2. Sense resistor $R_S = \left(1 + \frac{R_{V1}}{R_{V2}}\right) \times \frac{V_{CEA+}\text{offset voltage}}{I_{S(max)}}$, where $I_{S(max)}$ is the current limit level, V_{CEA+}offset = 50 mV (typ).
3. Arbitrarily select either R_{V1} or R_{V2} so that the smallest of the two resistors is between 6.5 kΩ and 20 kΩ. Then calculate the value of the other resistor using the equation in the first step.

If the converter is in a current-limit condition and the output voltage falls below half of the regulated output voltage, the UCC2541 enters into a hiccup (restart-retry) mode. Figure 4 shows typical signals during hiccup mode.

APPLICATION INFORMATION

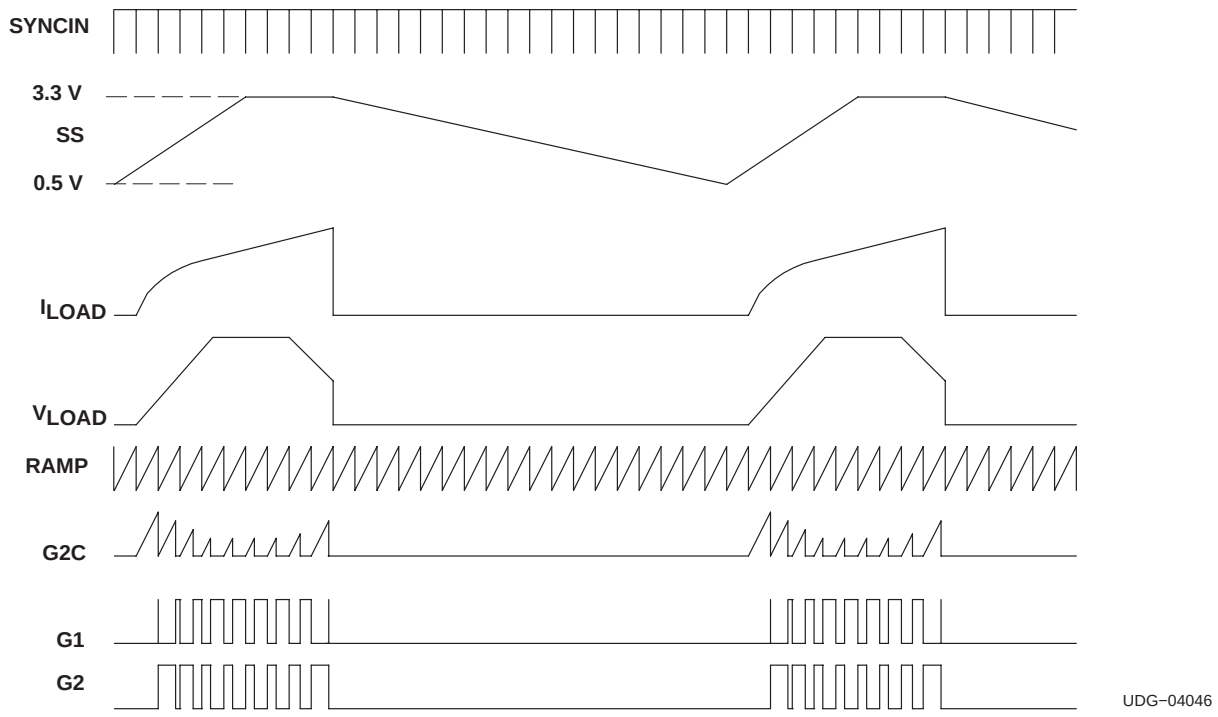


Figure 4. Typical Hiccup Mode waveforms

COMP, VEA− and CEA− pins: Voltage and Current Error Amplifiers

From no-load to full rated load operating conditions, the UCC2541 operates as a voltage mode controller. Above the programmed rated current, there are two levels of over current protection; constant current limit and overcurrent reset/retry. This section gives suggestions on how to design the voltage controller and current controller so that they interact with one another in a stable fashion. Refer to the functional diagram of the voltage and current error amplifiers in Figure 3. The voltage error amplifier in the figure shows three non-inverting inputs. The lowest of the three non-inverting inputs (1.5 V, SS and TR) is summed with the inverting input to achieve the voltage error signal. The lowest of the two outputs drives the inverting stage which in turn, drives the modulator.

During steady state voltage control operation, the feedback elements in the current loop have no effect on the loop stability. When current limit occurs, the voltage error amplifier effectively shuts OFF and the current error amplifier takes control. During steady state current limit operation, the negative feedback elements in the voltage error amplifier loop become positive feedback elements in the current error amplifier loop. In order for the current error amplifier to be stable, the impedances in the feedback path of the current error amplifier must be lower than the impedances in the feedback path of the voltage error amplifier. This means that resistors in the current error amplifier negative feedback path must be less than the resistors in the voltage error amplifier negative feedback path. Also capacitors in the current error amplifier negative feedback path must be larger than capacitors in the negative feedback path of the voltage error amplifier negative feedback path. (Capacitance is really an admittance value rather than an impedance value). This concept is illustrated in Figure 3.

In order for the current loop to be stable in Figure 3, $||Z_{IV}||$ must be less than $||Z_{FV}||$ over all frequencies. This can be achieved if $R_{FI} < R_{FV}$ and $C_{FI} > C_{FV}$.

APPLICATION INFORMATION

Another issue that can occur during current limit operation is modulator stability. In order for the modulator to be stable, the rising slope of the current ripple measured at the COMP pin must be smaller than the rising slope that is measured at the RAMP pin. This can be met either in the selection of the ratio of $||Z_{IV}||$ to $||Z_{FV}||$, or by the addition of a capacitor in parallel to R_{FI} and C_{FI}, such as C_{FIR}, in Figure 3.

In some applications, this current and voltage error amplifier configuration may lead to difficulties with startup at turn on and with restarting after current limit hiccup operation. A small capacitor from CEA− to ground can filter this node to alleviate this issue. This capacitor is shown as C_{ST} in Figure 3.

Stable Dynamic Current Loop Design (refer to Figure 3):

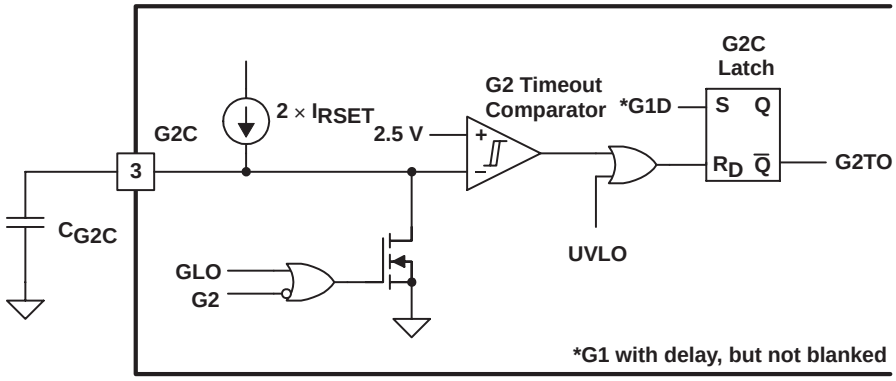
1. Using any favorite approach, design the voltage error amplifier for stable voltage mode design. Use at least 15 kΩ for any resistors in the negative feedback path of the voltage error amplifier (between pins 9 and 7). This does not apply to resistance values between the power supply output voltage and pin 7; it also does not apply to resistance values between ground and pin 7.
2. The goal is to design the current limit control loop so that it drives the converter to maintain 50 mV between the VEA− pin and the CEA− pin during current-limit conditions. Select the current sense element and the voltage divider ratios for the VEA− pin to ground and the CEA− pin to ground to provide the desired current limit level.
3. Place the same configuration of components in the negative feedback path of the current error amplifier (between pins 9 and 8), that are in the negative feedback path of the voltage error amplifier (between pins 9 and 7). However, use resistors with values that are 67% of the corresponding resistors that are between pins 9 and 7 and use capacitors that are 150% of the corresponding capacitors that are between pin 9 and pin 7.
4. Check the COMP signal. If it is unstable, place a capacitor (or increase the capacitance) between pins 9 and 8 in order to attenuate the current ripple. Raise the value of the capacitor until the COMP pin voltage becomes stable. Compare the COMP voltage with the RAMP voltage. With stable operation, the rising slope of the COMP voltage ripple is less than the rising slope of the RAMP pin.

APPLICATION INFORMATION

RSET, RAMP, G2C, SS pins: Programming the Timer Currents

Set the base current to the timers with a resistor between RSET and GND. The block diagram of the UCC2541 shows the interaction of the RSET pin and the dependent current sources for the RAMP, G2C and SS features. The RSET pin is a voltage source; the current of the RSET pin is reflected and multiplied by a gain and distributed to the RAMP (gain = 2), G2C (gain = 2) and SS (charge gain = 1.33, net discharge gain = 0.4). The resistance applied to the RSET pin and GND should be in the range of 10 kΩ < R_{RSET} < 50 kΩ. RAMP, G2C and SS timers are programmed by the selection of capacitors tied between each of their respective pins and GND.

G2C pin: G2 Timer for Output Stage Reverse Current Protection



UDG−04047

Figure 5. Functional diagram of the G2 Timer

The G2C pin programs the maximum duration of the synchronous rectifier to facilitate low or zero duty ratio operation. Figure 5 shows the functional diagram. This function is programmed by connecting a capacitor between the G2C pin and GND. The capacitor on G2C should be slightly larger than the capacitor on the RAMP pin. For best results, program the typical G2 time limit to be between 1.5 and 3 times the switching period (T). Notice that when the G2 timer reaches its limit, both G1 and G2 are forced to a LOW output. This feature prevents the current in the output inductor from excessive negative excursions during zero-duty ratio conditions. Program the G2 time-out (G2TO) duration using equation (1):

$$C_{G2C} = \frac{2 \times V_{RSET}}{R_{RSET}} \times \frac{\text{G2 Timeout Duration}}{\text{G2C Timer Threshold}}, \text{ Farads} \quad (1)$$

where

- V_{RSET} = 1.5 V(typ)
- 1.5 T < G2 Timeout Duration < $3T_S$
- G2C Timer Threshold = 2.5 V (typ)

APPLICATION INFORMATION

RAMP pin: Oscillator and PWM Ramp

The RAMP pin serves two purposes: (1) a capacitor on this pin sets the oscillator charging time to program the frequency of operation for the converter and (2) the peak voltage on RAMP defines the gain of the PWM modulator. The UCC2541 has a leading edge modulator that compares the error output with the RAMP voltage. A diagram of the oscillator and PWM modulator is shown in Figure 6.

The current charging the capacitor from RAMP to ground is equal to 2 x I_{RSET}. In the UCC2541, with leading edge modulation, a switching cycle can be considered to begin when the oscillator ramp reaches 2.0 V. This voltage level triggers the negative-going clock signal which enables the RAMP discharge transistor and simultaneously sends a G1 turn-off command to the PWM control. The internal clock signal is held low for approximately 100 ns, and this sets the maximum desired value for the capacitor on the RAMP pin. Note that the RAMP discharge transistor must also sink 2 x I_{RSET} while it is discharging the external RAMP capacitor.

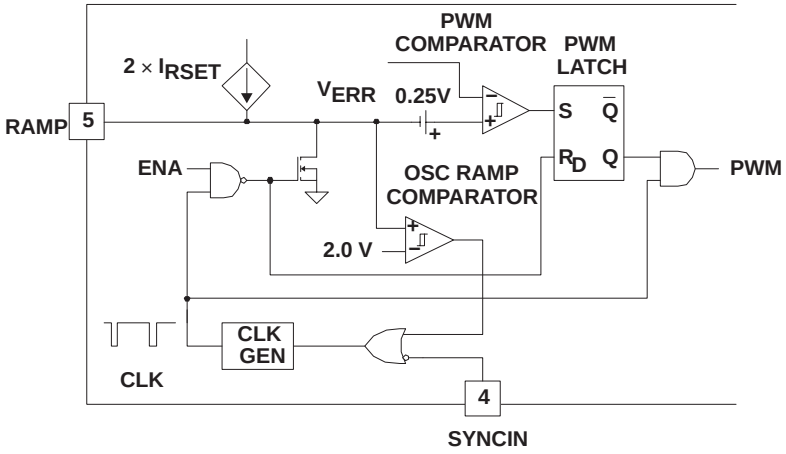


Figure 6. Oscillator and PWM Modulator

The oscillator frequency is programmed by proper selection of the resistor connected to RSET (pin 1) and the capacitor connected to RAMP (pin 5). With RSET selected within the preferred range of 10 kΩ to 50 kΩ the RAMP capacitor C_{RAMP} can be selected from:

$$C_{RAMP} = \frac{1.5\left(\frac{1}{f_{SW}} - 100\ ns\right)}{R_{SET}} \quad (2)$$

where fsw is the desired switching frequency, and R_{SET} is the resistor connected to pin 1. This expression is derived by summing the time required for a linear current source to change the RAMP capaitor with the internal delay of approximately 100 ns. The constant term 1.5 is equal to:

$$\left(\frac{I_{RAMP}}{I_{RSET}}\right)\left(\frac{V_{RSET}}{V_{RAMP(pk)}}\right) \quad (3)$$

APPLICATION INFORMATION

The UCC2541 can be synchronized to an external source if an external SYNCIN signal (falling edge) is applied to pin 4 before the oscillator reaches 2.0 V. The internal circuitry uses the falling edge on SYNCIN to generate the 100-ns internal clock signal and turn off G1. The free-running frequency programmed by the internal oscillator/RAMP capacitor should be approximately 20% lower than an intended external sync frequency. The SYNCIN pin should be tied to V_{REF} if not used.

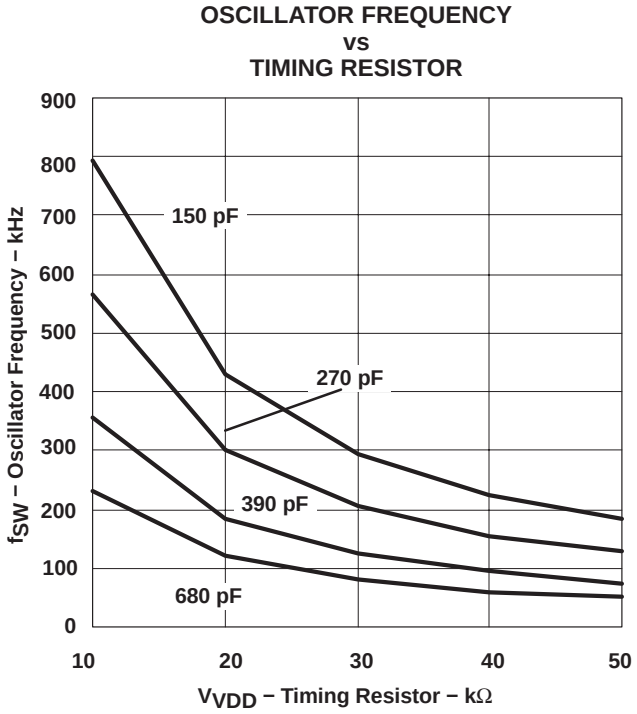


Figure 7

VDD, VDRV, VREF and BST pins: Modes of Operation

Depending on the available bias voltage for the UCC2541, the startup, shutdown, and restart conditions are different. There are three distinct configurations or modes of biasing the UCC2541. The mode is detected and latched into an internal register during power-up when VREF crosses 2 V. The register is cleared when VDD, VDRV and VREF are simultaneously less than 1 V. A summary of the modes and their programming requirements are listed in Table 1.

Table 1. Modes and Programming Requirements

Mode	V_{BIAS} Range (V)	Bias Pin	UVLO ON (V)	UVLO OFF (V)	Mode Requirement at Power-Up and V_{VREF} = 2 V	Remarks
1	8.5 to 36	VDD [16]	V_{VDD} = 8.5	V_{VDD} = 8.0	$V_{VDD} > (V_{VDRV}$ and $V_{REF})$	Widest line operation
2	4.75 to 8.5	VDRV [13]	V_{VDRV} = 4.65	V_{VDRV} = 4.3	$V_{VDRV} > (V_{VDD}$ and $V_{REF})$	
3	3.0 to 3.6	VREF [2]	V_{REF} = 2.8	V_{REF}= 2.5	$V_{REF} > (V_{VDD}$ and $V_{VDRV})$	Needs regulated bias and low V_{TH} power MOSFETs

APPLICATION INFORMATION

VDD, VDRV, VREF and BST pins: Modes of Operation (cont.)

- Mode 1, or normal operation requires the availability of a bias of 8.5 V or higher for the device. Here, the bias drives the VDD pin. The low-side drive bias, V_{VDRV} = 7 V, is generated from an internal linear regulator and it directly draws current from the VDD pin. The high-side driver bias is a flying capacitor that is charged from the VDRV pin through the G2 pin, when G2 is HI, via a diode between G2 and BST. The UCC2541 operates in Mode 1 if V_{VDD} > (V_{VDRV} and V_{VREF}) when V_{VREF} rises above 2 V. Mode 1 permits the widest range of bias voltages, operational from 8.5 V < V_{VDD} < 35 V. This mode is compatible with systems that have a 12 V_{DC} bias supply already available.
- Mode 2 is suitable for applications where the bias is typically 5 V (between 4.5 V and 8.0 V). The bias voltage is applied to the VDRV terminal of the UCC2541. The high-side driver bias is a flying capacitor that is charged from the VDRV pin through the G2 pin, when G2 is HI. Bias voltage to the VDD pin is obtained through an external voltage-doubler charge pump. If the system uses low threshold voltage power MOSFETs, VDD can be directly tied to the VDRV pin. The bias voltage could be either a bus converter output or an auxiliary supply.
- Mode 3 is for synchronous buck converter applications where the bias voltage is a regulated 3.3-V source. This is a common main output voltage in multiple output power converters. The bias voltage is applied to the VREF pin of the UCC2541. The UCC2541 operates in Mode 3 if it detects (V_{VREF} > V_{VDRV} and VDD) when V_{VREF} rises above 2 V.

Assorted combinations of modes and biasing schemes are shown in Figure 7 through Figure 12. In Mode 1 and Mode 2, the bias voltage can either be an independent auxiliary supply or it can be supplied by the power stage voltage, as shown in Figure 7 through Figure 11. A regulated auxiliary supply must be used with Mode 3 because the tolerance of the VREF voltage is the control tolerance of the UCC2541. In Mode 3, the regulated auxiliary supply can be independent of the power supply input voltage (as shown in Figure 12), or the regulated auxiliary supply can be the same source as the power supply input voltage.

APPLICATION INFORMATION

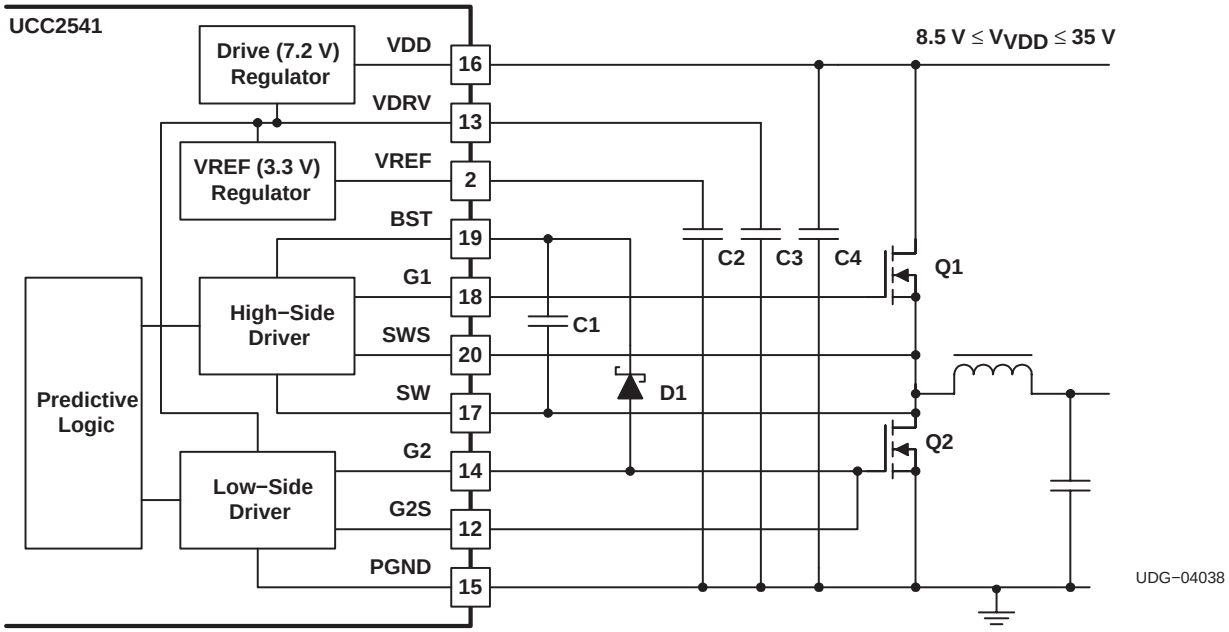


Figure 8. Mode 1 With Combined Power/Bias for Input Voltages Between 8.5 V and 35 V

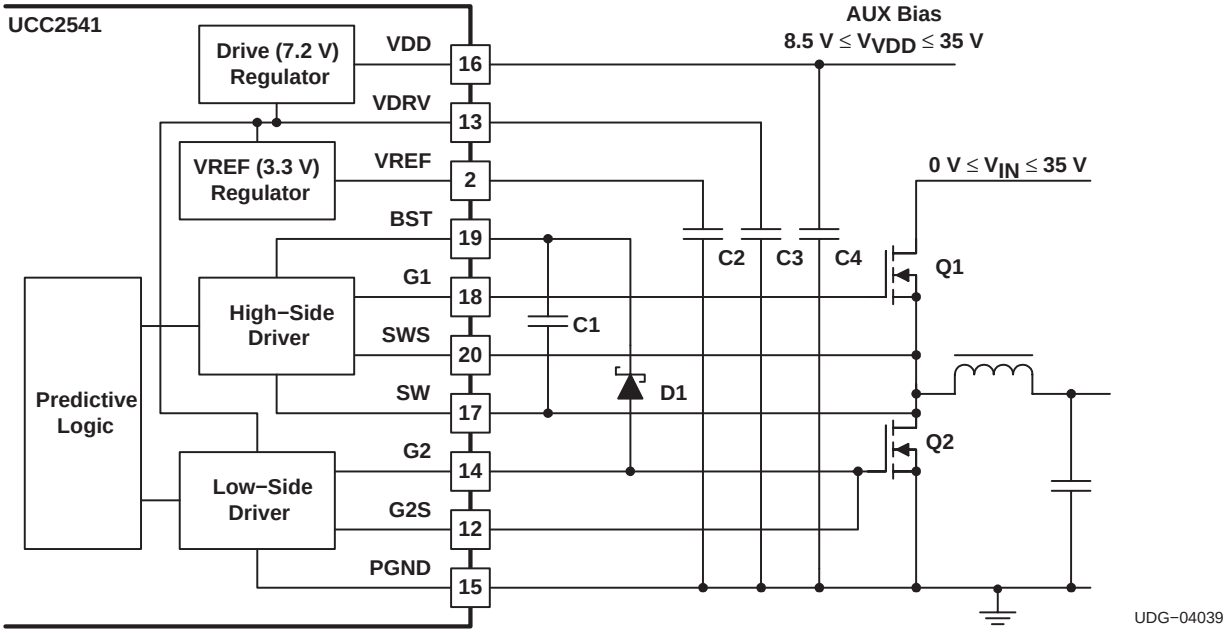


Figure 9. Mode 1 With Separate Power/ Bias Voltages Between 8.5 V and 35 V

APPLICATION INFORMATION

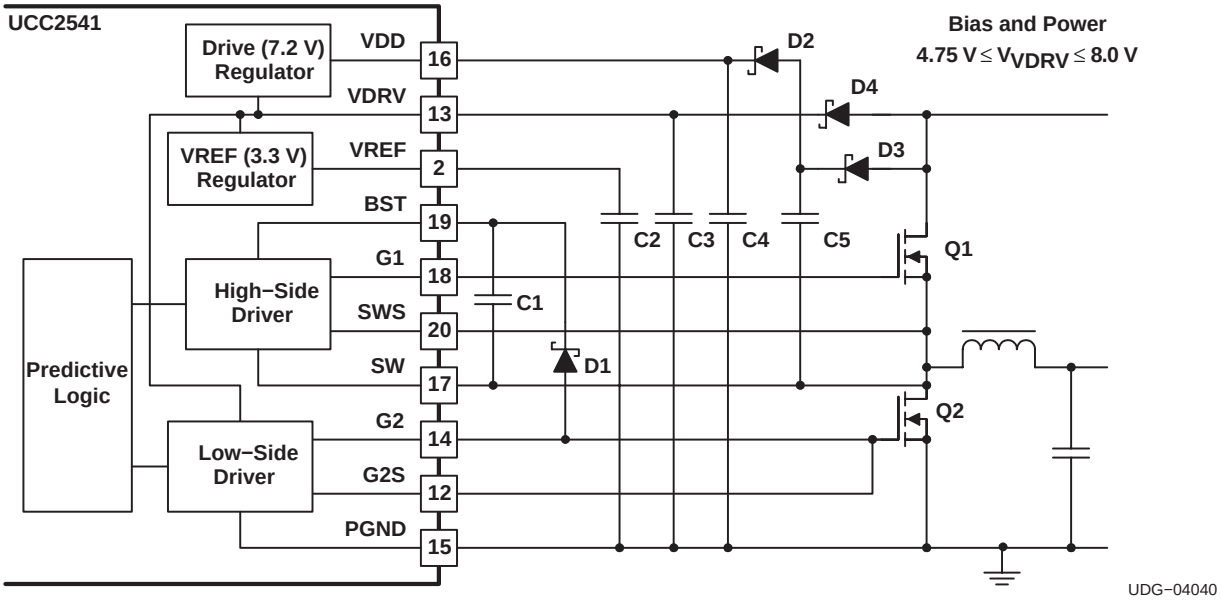


Figure 10. Mode 2 With Common Bias and Power Input Voltages Between 4.75 V and 8.0 V

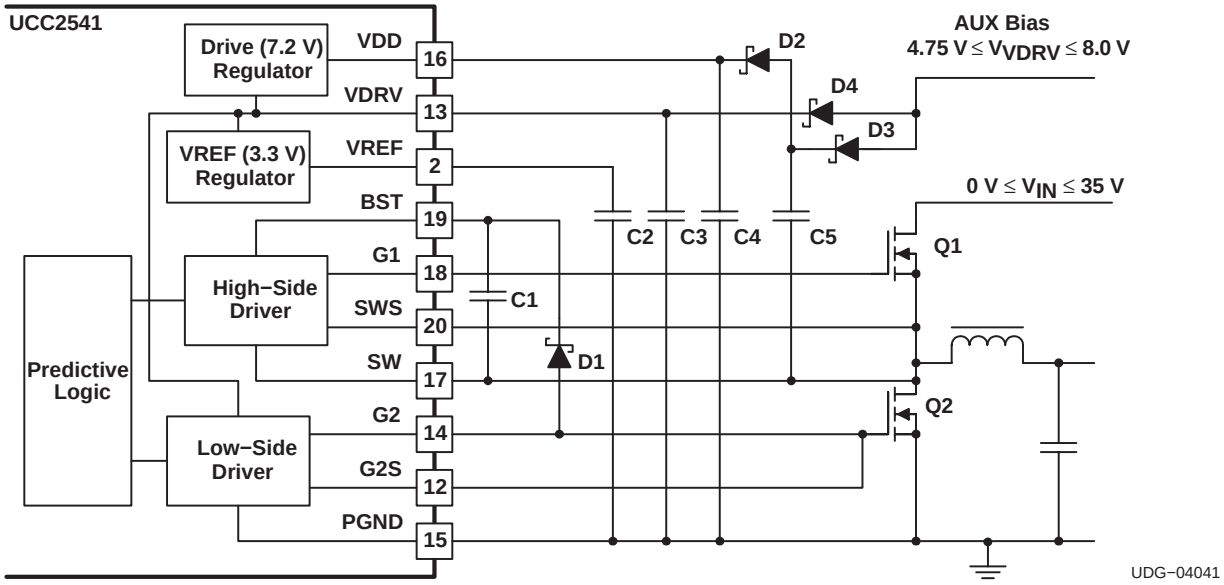


Figure 11. Mode 2 With Separate Power/ Bias (4.75 V and 8.0 V)

APPLICATION INFORMATION

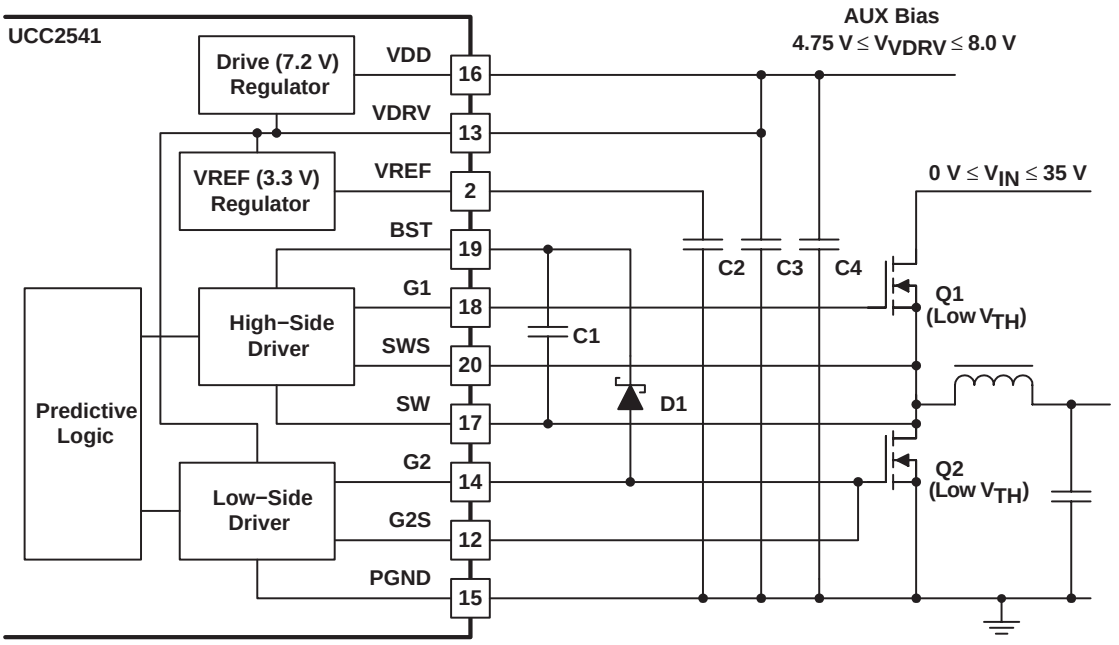


Figure 12. Mode 2 With Auxiliary Biasing for Bias Voltages Between 4.75 V and 8.0 V and Logic Level or Low Threshold Power MOSFET Transistors

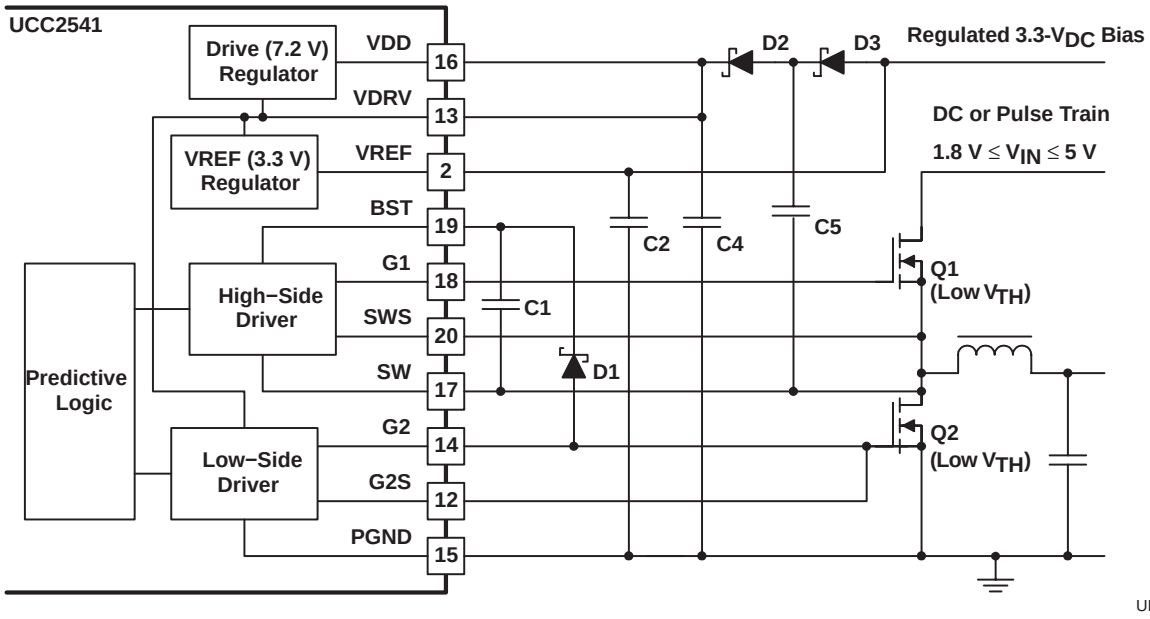


Figure 13. Mode 3 With Regulated 3.3-V_{DC} Bias, Low Threshold Power MOSFETs

APPLICATION INFORMATION

Figure 14 illustrates a combined operational mode (referred to as Mode 4) which allows a converter operating from intermediate bus voltages ranging from 6 V to >14 V to safely cross the boundary between Mode 1 and Mode 2 operation. A simple circuit utilizing an NPN transistor, zener diode, and resistor allows the circuit to start under the control of Mode 2 UVLO thresholds. Once the power stage is operational VDD is pumped up by D2 and D3 and the internal VDRV regulator raises VDRV to 7.2 V, shutting off the NPN transitor. The zener clamp on the NPN base prevents VDRV voltage rating from being exceeded during 12-V startup. It should be noted the circuit will run down to input voltages below 3.5 V, shutting off when VDRV has fallen to its turn-off threshold of 4.3 V.

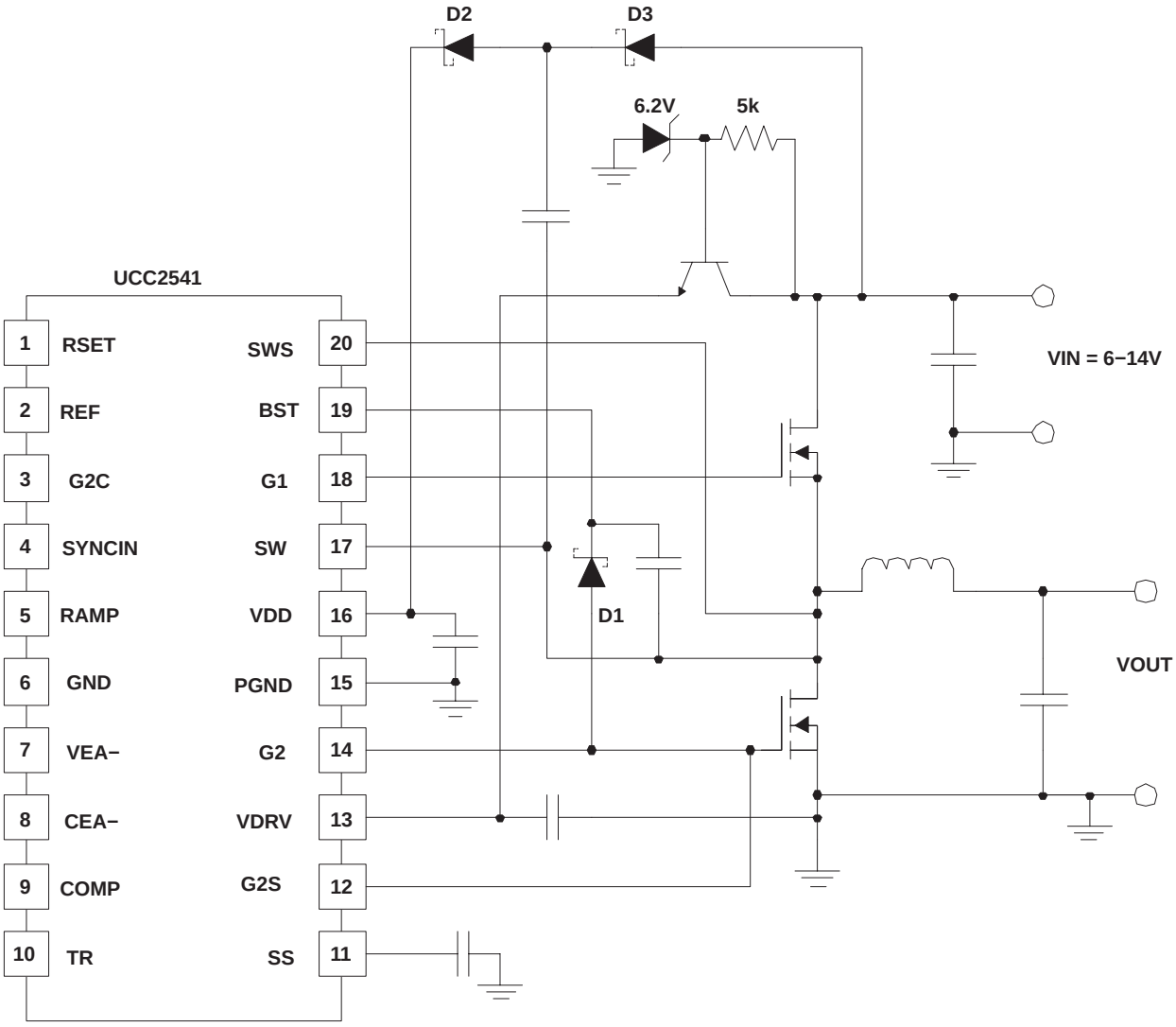


Figure 14. Mode 4 Operation

APPLICATION INFORMATION

Charge Pump Capacitor Selection

Capacitors C1 through C5 are all part of a charge distribution network that allows the UCC2541 to pass charge to the MOSFET gates of Q1 and Q2 (all reference designators in this section refer to the schematics in Figure 8 through Figure 13). This section gives guidelines on selecting the values of C1 through C5 so that the converter functions properly. Specific capacitor values may need to be larger than the recommended value due to MOSFET characteristics, diode D1 – D4 characteristics and closed-loop converter performance. All three modes of operation require a charge pump capacitor and diode, C1 and D1, in order to drive the high-side power MOSFET. Modes 2 and 3 require additional charge pump capacitors and diodes in order to supply voltage to VDD. In general, all charge pump diodes should be Schottky diodes in order to have low forward voltage and high speed. The charge pump capacitors should be ceramic capacitors with low effective series resistance (ESR), such as X5R or X7R capacitors.

The value of the charge pump capacitor C1 depends on the power MOSFET gate charge and capacitance, the voltage level of the Miller plateau threshold, the forward drop of D1 and the closed-loop response time. The unloaded high-side gate driver typically draws 2 nC of charge per rising edge plus 30 μA of direct current from C1. Usually, the unloaded high−side gate driver load is miniscule compared to the gate charge requirements of the high-side power MOSFET, Q1. Typical values for C1 are approximately 50 to 100 times the input capacitance (C_{ISS}) of MOSFET Q1. This usually allows for transient operation at extremely large duty ratio, where C1 does not have sufficient time to fully recharge. If C1 is excessively large, its ESR and ESL prevents it from recharging during transients, including the start-up transient.

Capacitors C2 through C5 are then selected based on the direction of charge transfer and the requirements of the UCC2541. Selection guidelines are shown in Table 2. Keep in mind that each converter design may require adjustments for larger capacitor ratios than those that are suggested in Table 2. The selection process begins at the left side of Table 2 and progresses towards the right side of the table, which is the reverse order of the charge flow during the first few cycles of start-up. If iteration is required in the design process, review the progression of the capacitors in the order from left to right that is shown in the table.

Table 2. Charge Pump and Bias Capacitor Selection Guidelines

Mode	High-Side Drive Capacitor (≥ 0.1 μF)	VDRV Filter Capacitor	VREF Filter Capacitor	VDD Filter Capacitor	VDD Charging Capacitor
1	C1 ≥ 50 C_{ISS}	C3 ≥ 2 × C1	C2 ≥ 0.1 μF	C4 ≥ 1 μF	n/a
2	C1 ≥ 50 C_{ISS}	C3 ≥ 2 × C1	C2 ≥ 0.1 μF	C4 ≥ 1 μF, 2 × C3	C5 ≥ 2 × C4
3	C1 ≥ 50 C_{ISS}	C4 ≥ 1 μF 2 × C1	C2 ≥ 1.0 μF	C4 ≥ 1 μF, 2 × C1	C5 ≥ 2 × C4

For Modes 2 and 3, the VDD filter capacitor, C4, in Table 2 must supply the I_{VDD} idle current to the UCC2541 (approximately 11 mA) plus the charge to drive the gates G1 and G2. Capacitor C4 must be large enough to sustain adequate operating voltages during start-ups and other transients under the full operational I_{VDD} current. Knowing the operating frequency and the MOSFET gate charges (Q_G), the average I_{VDD} current can be estimated as:

$$I_{VDD} = I_{VDD(idle)} + \left(Q_{G1} + Q_{G2}\right) \times f_S \quad (4)$$

- where f_S is switching frequency

In order to prevent noise problems, C4 must be at least 1 μF. Furthermore, it needs to be large enough to pass charge along to the power MOSFET gates. Thus C4 often needs to have at least twice the capacitance of the VDRV filter capacitor, as shown in Table 2.

APPLICATION INFORMATION

Output Stage

The UCC2541 includes dual gate drive outputs and each is capable of ±3-A peak current. The pull-up/ pull-down circuits of the driver are bipolar and MOSFET transistors in parallel. High-side and low-side dual drivers provide a true 3-A high-current capability at the MOSFET's Miller Plateau switching region where it is most needed. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

The output drivers can switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external-schottky-clamp diodes are not required. The outputs are also designed to withstand 500-mA reverse current without either damage to the device or logic upset.

For additional information on drive current requirements at MOSFET's Miller plateau region, refer to the Power Supply Seminar SEM−1400 [3].

Predictive Gate Drive™ Technology

The Predictive Gate Drive™ technology maximizes efficiency by minimizing body diode conduction. It utilizes a digital feedback system to detect body diode conduction, and adjusts the deadtime delays to minimize the conduction time interval. This closed loop system virtually eliminates body diode conduction while adjusting for different MOSFETs, temperature, and load dependent delays. Since the power dissipation is minimized, a higher switching frequency can be utilized, allowing for a smaller component size. Precise gate timing at the nanosecond level reduces the reverse recovery time of the synchronous rectifier MOSFET body diode, which reduces reverse recovery losses seen in the main (high-side) MOSFET. Finally, the lower power dissipation results in increased reliability.

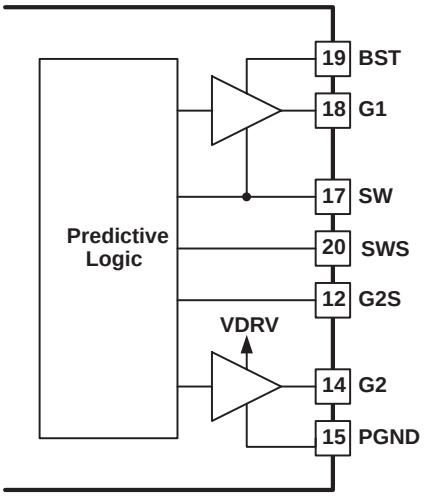


Figure 15.

For additional information on Predictive Gate Drive™ control and efficiency comparisons to earlier adaptive delay and adaptive control techniques, refer to the Application Note SLUA285 [1].

APPLICATION INFORMATION

VDD and IDD

Although quiescent VDD current is low, total supply current is higher, depending on output gate drive requirements and the programmed oscillator frequency. Total VDD current (I_{VDD}) is the sum of quiescent VDD current and the average output currents of G1 and G2, as described in equation (5). Knowing the operating frequency and the MOSFET gate charge (Q_G), average driver output current, per gate, can be calculated from:

$$I_G = Q_G \times f_S \quad (5)$$

where

- f_S is switching frequency

To prevent noise problems, connect a 1-µF ceramic capacitor between the VDD and GND pins. Place the 1-µF ceramic capacitor as close to the UCC2541 as possible. This capacitor is in addition to any electrolytic energy storage capacitors that may be used in the bias supply design.

Soft-Start and Tracking Features

Separate pins are provided for the soft-start feature and the tracking feature. Soft-start or tracking (sequencing) can be easily implemented with this configuration using a minimum number of external components. During a power-up transient, the converter output tracks the lower of the SS voltage, the TR voltage or a 1.5-V internal reference, provided the system is not in current limit. In other words, the voltage control loop is closed during power-up, provided the system is not current limited. Figure 16 shows the UCC2541 configured for soft-start operation. For applications that do not use the tracking feature, connect the TR pin to either SS or REF, as shown in the figure. Remote shutdown and sequential power-up can be easily implemented as a transistor switch across C_{SS}.

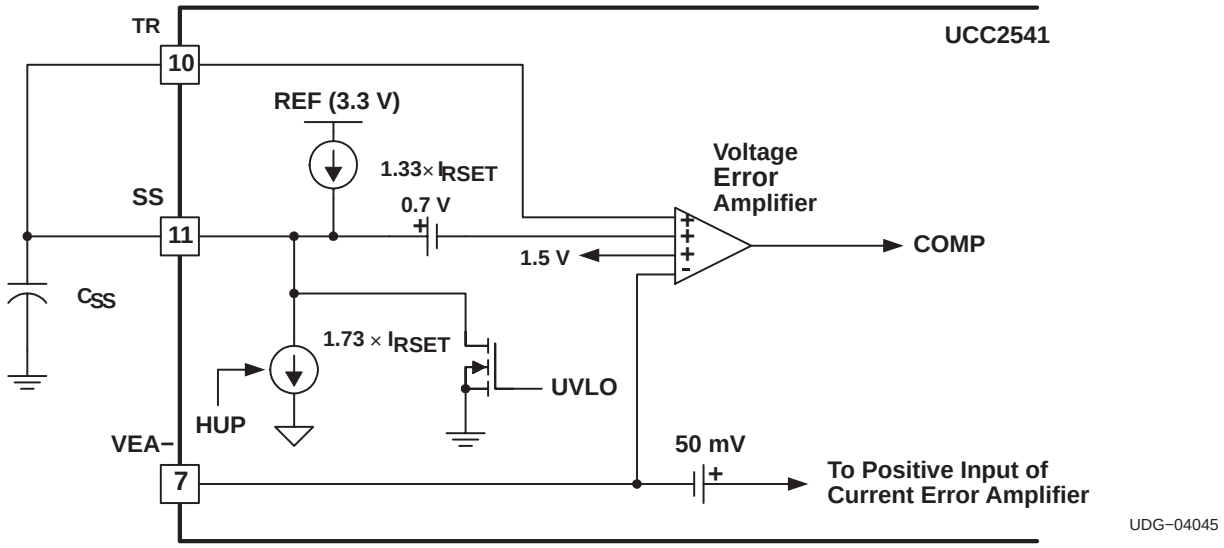


Figure 16. Using the Soft-Start Feature

APPLICATION INFORMATION

The soft-start interval begins when the UCC2541 recognizes that the appropriate voltage (see Mode 1, 2 or 3) is above the UVLO level. The voltage of C_{SS} then linearly increases until it is clamped at the REF voltage of 3.3V. Regulation should be reached when the soft-start voltage reaches about 2.2 V (1.5 V plus a diode drop). Select a C_{SS} capacitor value using equation (5) to program a desired soft-start duration, Δt_{SS}.

$$C_{SS} = 1.33 \times \frac{V_{RSET}}{R_{SET}} \times \frac{\Delta t_{SS}}{\Delta V_{SS}} = 1.33 \times \frac{1.5\ V}{R_{SET}} \times \frac{\Delta t_{SS}}{2.2\ V}\ \text{Farads} \quad (6)$$

If a UVLO fault is encountered, both outputs of the UCC2541 are disabled and the soft-start pin (SS) is discharged to GND. The UCC2541 does not retry until the UVLO fault is cleared.

Using the TR pin, the UCC2541 can be programmed to track another converter output voltage. If the voltage to be tracked is between 0 V and 3.3 V, simply connect the TR pin to the voltage to be tracked with a resistor that is approximately equal to the DC impedance that is connected to the VEA− terminal ($R_{V1} \parallel R_{V2}$, in Figure 3). If the voltage is above that range, use a voltage divider, again with an equivalent resistance that approximately equals the DC impedance that is connected to the VEA− terminal. Other strategies can be used to achieve sequential, ratiometric or simultaneous power supply tracking[4].

An implementation of sequential sequencing using TPS3103K33[2] in a multiple output power supply[4] is shown in Figure 17. Applications where the loads include a processor with a core voltage of 1.5 V and I/O ports that require 3.3 V can require sequential sequencing in order to resolve system level bus contention problems during start-up. In this circumstance the core must power-up first, then after an initialization period of 130 ms, the ports are allowed to power-up. This is illustrated in Figure 18.

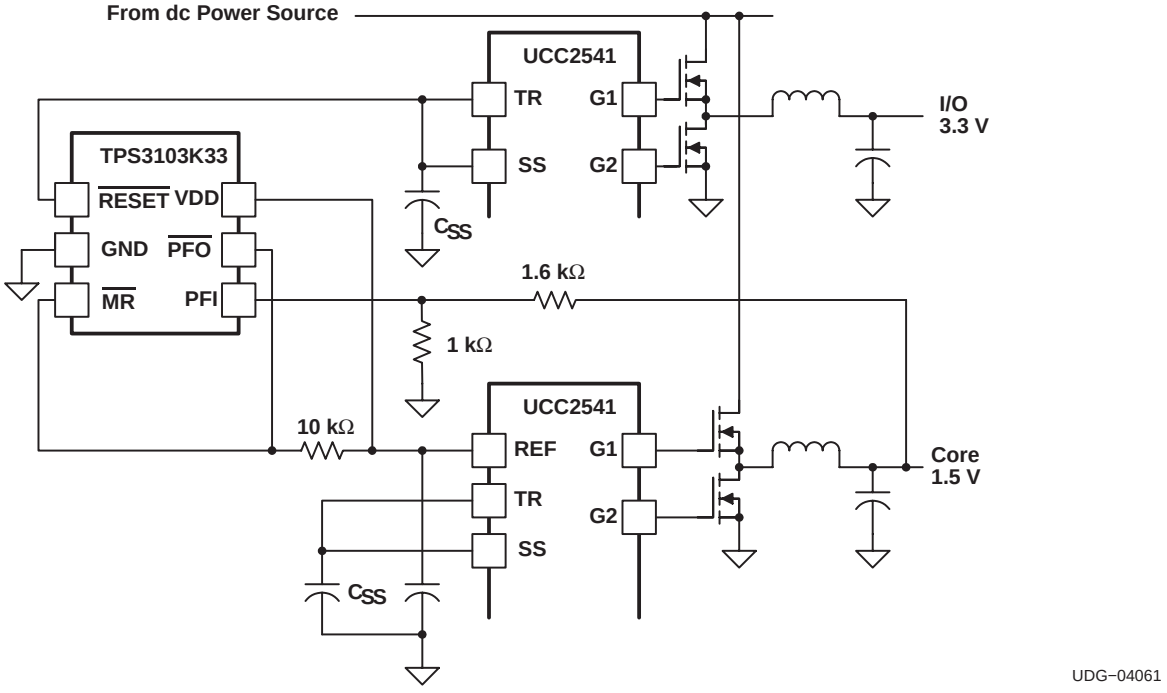


Figure 17. Sequencing a Multiple Output Post Regulated Power Supply

APPLICATION INFORMATION

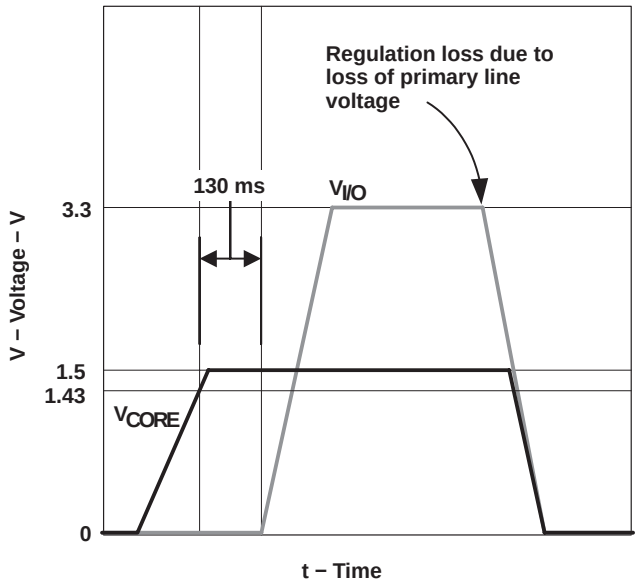


Figure 18.

Using the TR pin, the UCC2541 can be programmed to ratio-metrically track another converter output voltage[4]. Ratio-metric tracking is when the ratio of the output voltages is constant from zero volts to the point where one or more of the outputs lock into regulation. The TR pin is easier to use for tracking than the SS pin because the external currents that would be applied to the SS pin may interfere with SS discharge currents and fault recovery. It should be understood that the voltage that is being tracked must lag the bias voltages (VDD, VDRV and REF) on start-up and lead the bias voltages during shutdown. Furthermore, the output that is being tracked must not reach its steady state DC level before the output that is tracking reaches its steady state DC level. Figure 18 illustrates the concept of programming an output voltage V_C, to ratio-metrically track another output, V_M.

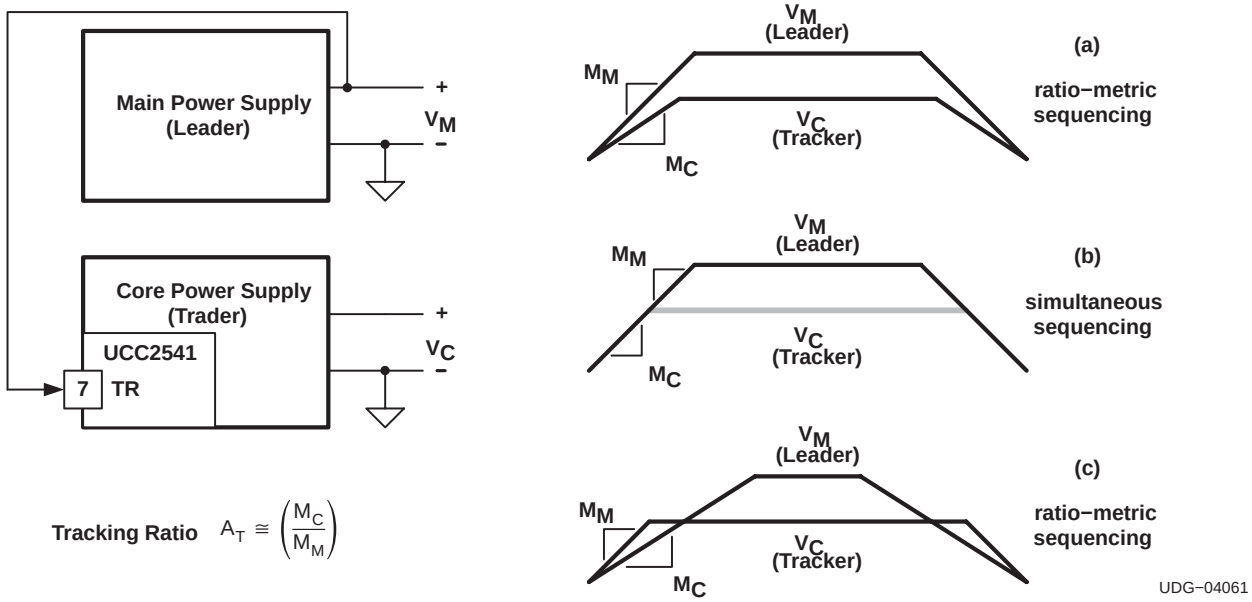


Figure 19. Ratio−Metric Tracking

APPLICATION INFORMATION

The general circuit to program the UCC2541 to track the leader supply voltage by the tracking ratio A_T is shown in Figure 20. To program the tracking profile gains G_{T1} and G_{T2}, follow the ratio-metric tracking design procedure that is listed below. The special case of simultaneous sequencing for $V_M > 1.5V$ is the simplest to design; set $R_{T1} = R_{V1}$ and $R_{T2} = R_{V2}$, G_{T2} is not needed. In many other cases, the circuit can be simplified with the removal of the operational amplifier for G_{T2} and the Zener clamping diode. If an operational amplifier is necessary, it should be capable of rail to rail operation and usually low voltage bias; the TLV271 is an inexpensive solution for both of those requirements. Notice that the tracking circuit in Figure 20 also has a soft-start capacitor, C_{SS}. The soft-start capacitor is useful for limiting the time between short-circuit retry attempts and it can prevent overshoot when recovering from a fault that is experienced in only the tracking supply but not the main supply.

Ratio-Metric Tracking Design Procedure (see Figures 22 and 23)

1. Determine the tracking ratio, A_T.

$$A_T = \frac{M_C}{M_M} \tag{7}$$

where M_C and M_M are the soft-start slopes of V_C and V_M, respectively.

2. Determine G_V.

$$G_V = \frac{R_{V2}}{R_{V1} + R_{V2}} \tag{8}$$

where R_{V2} and R_{V1} are selected when designing the voltage control loop.

3. Test G_{T2} if necessary when $V_M \leq 1.5$ V or $A_T G_V > 1$.

   a. If G_{T2} is needed, set GT2 so that both equations (8) and (9) apply.

$$G_{T2} = 1 + \frac{R_{F1}}{R_{F2}} \tag{9}$$

   so that both of the following apply:

$$G_{T2} = \left(\frac{1.5\ V}{V_M \times G_{T1}}\right) \quad \text{and} \quad G_{T2} > \left(A_T \times G_V\right) \tag{10}$$

   b. If G_{T2} is not needed, set $G_{T2} = 1$.

4. Set G_{T1} .

$$G_{T1} = \frac{A_T \times G_V}{G_{T2}} = \frac{R_{T2}}{R_{T1} + R_{T2}} \tag{11}$$

5. Select R_{T1} and R_{T2} so that $R_{T1} \parallel R_{T2} \approx R_{V1} \parallel R_{V2}$ to minimize offset differences.

APPLICATION INFORMATION

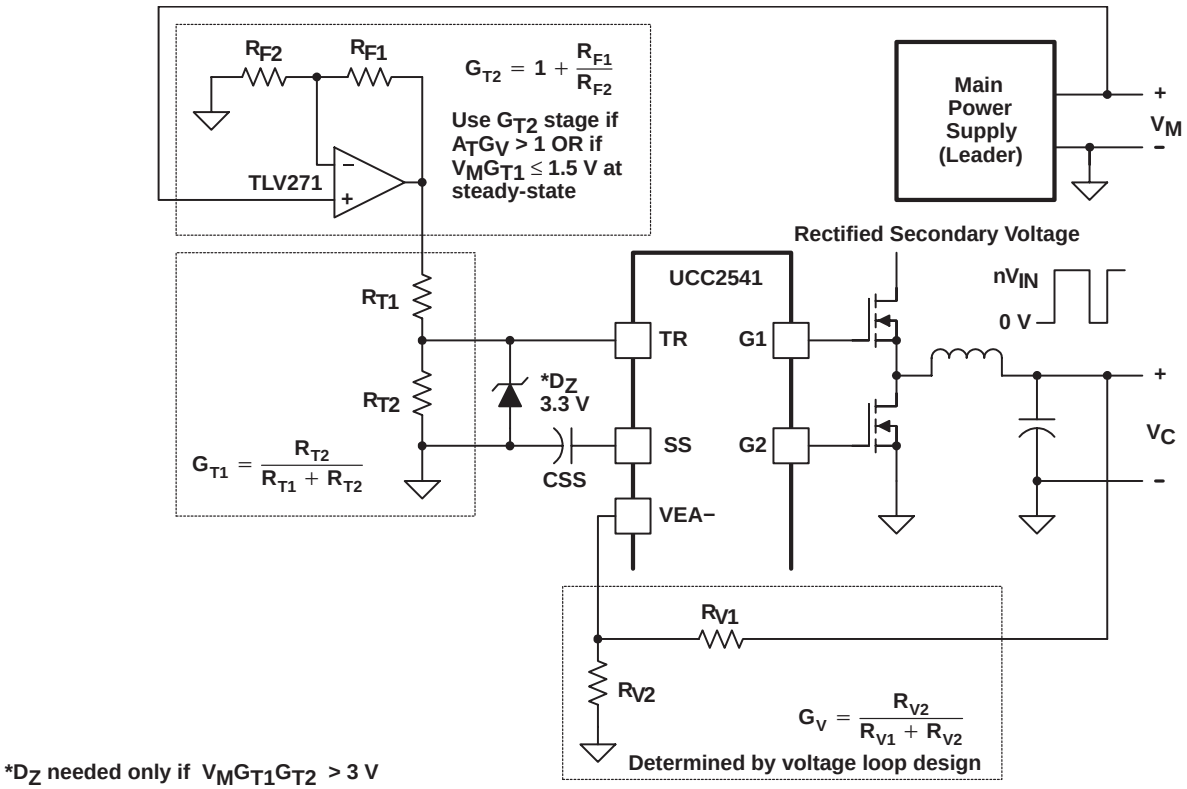


Figure 20. Programming the UCC2541 to Track Another Output

More elaborate power supply sequencing and tracking can easily be implemented by extending the above techniques. Consult Reference [4] for further information.

The following schematic shows an example POL (point of load) converter capable of delivering 20 A at 2.5 V from an unregulated IBC (intermediate bus converter) providing 9 V to14 V. In this application, the UCC2541 is configured to operate in Mode 1, and the converter turns ON when the UCC2541 UVLO threshold of 8.5 V is exceeded. The upper input voltage rating is limited by the MOSFET and capacitor voltage ratings, not the UCC2541. For lower current requirements from 10 A to15 A a single lower MOSFET would suffice.

APPLICATION INFORMATION

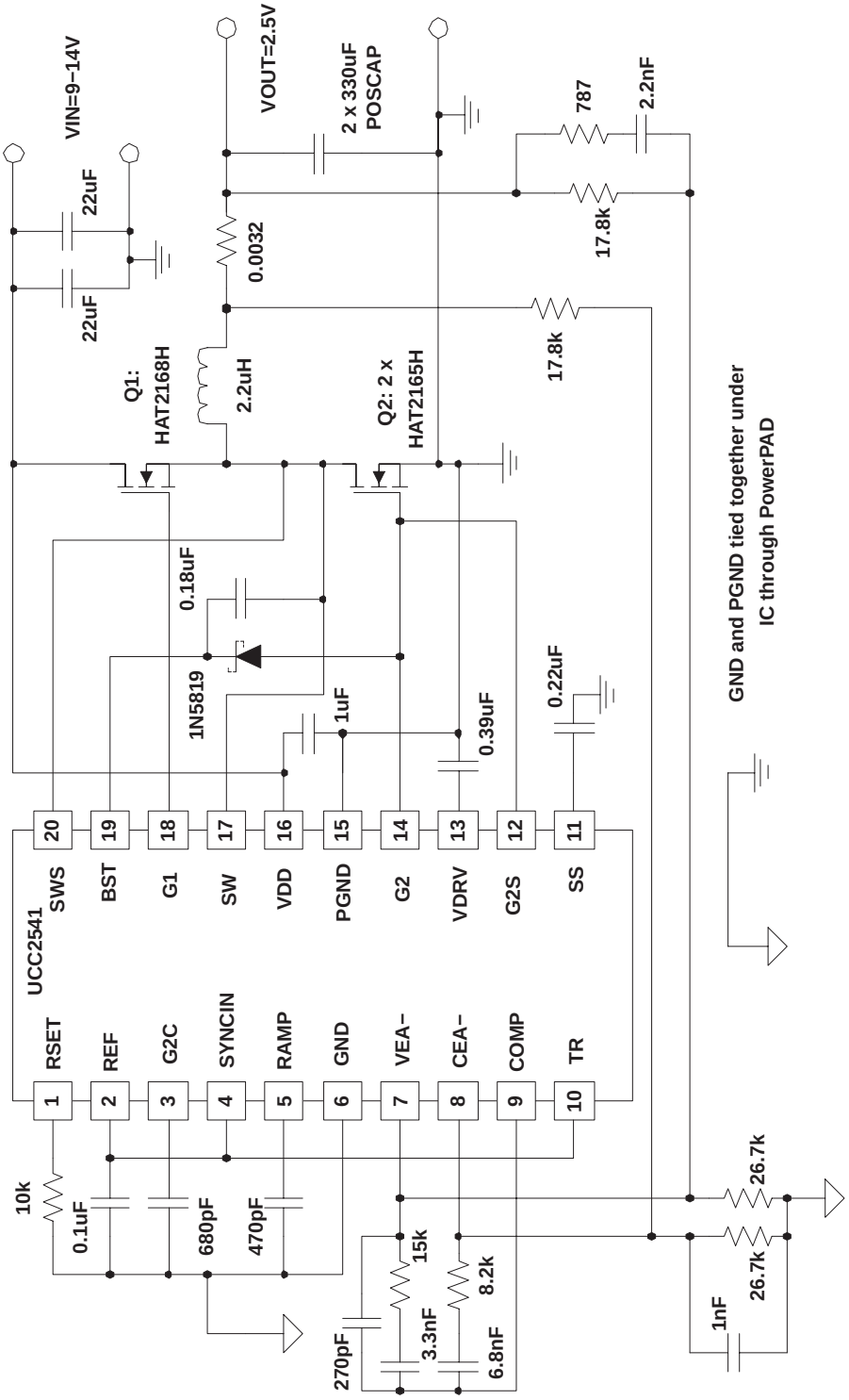


Figure 21. 20-A POL (Point of Load) Converter

APPLICATION INFORMATION

In the 20-A converter the output current is sensed by R4. The UCC2541 limits output current when the C_{EA}− (pin 8) exceeds the V_{EA}− (pin 7) by 50 mV. To select the current sense resistor the 50-mV signal must be gained up by the reciprocal of the output feedback divider ratio given by:

$$\frac{R8}{R8 + R9} = \frac{R12}{R12 + R10} \tag{12}$$

For this 2.5-V output, the divider ratio is 0.6, and the following calculation can determine the typical voltage across the sense resistor to begin current limit operation:

$$V_{RSNS} = V_{R4} = \frac{1}{0.6} \times 50\ mV = 83.3\ mV \tag{13}$$

The peak inductor ripple current should also be considered in R_{SNS} selection, and is 1/2 the peak-to-peak inductor current calculated during the OFF-time of the converter:

$$dI_{PP}\left(\frac{1}{f_S} - \frac{V_O}{V_{IN} \times f_S}\right) \times \frac{V_O}{L} = 3\ A_{PP} \tag{14}$$

with V_O=2.5 V, V_{IN}=12 V, f_S=300 kHz, and L1=2.2 µH. In this design IL1, peak =21.5 A.

For a 20-A converter with current limiting at 20% overload the sense resistor can be calculated as:

$$R_{SNS} = \frac{V_{RSNS}}{1.2 \times IL_{PEAK}} = \frac{83.3\ mV}{1.2 \times 21.5\ A} = 3.2\ m\Omega \tag{15}$$

With this value of sense resistor the average power dissipation can be calculated to be:

$$P_{RSNS} = I_{OUT}{}^2 \times R_{SNS} = 20\ A^2 \times 3.2\ m\Omega = 1.28\ W \tag{16}$$

Low value current sense resistors are commonly available in 1-W surface mount packages, so two packages should be paralleled to meet the power dissipation requirements in high current designs, and the final value used will be a compromise of available components. In surface mount applications a Kelvin connection to the sense resistor is not easily attainable, so the connection resistance from the sense resistors to the PCB must be included in the effective sense resistance.

The voltage and current feedback component magnitudes were ratioed according to the discussion in section, COMP, VEA− AND CEA− pin: Voltage and Current Error Amplifiers. In this application, the optional component CFIR was not needed. However, a 1-nF capacitor (CST in Figure 3) was needed to filter the C_{EA}− signal to allow the converter to start at turn on and to restart after current limit hiccup operation.

THERMAL INFORMATION

The useful temperature range of a controller that contains high-current output drivers is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2541 is available in the 20-pin HTSSOP PowerPAD™ package and also the 32-pin QFN PowerPAD™ package.

The PowerPAD™ offers the most effective means of removing the heat from the semiconductor junction and therefore long term reliability improvement. As illustrated in [5], the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the device package, reducing the θjc down to 2°C/W. Data is presented in [5] to show that the power dissipation can be quadrupled in the PowerPAD™ configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in [6] to realize a significant improvement in heat−sinking over standard non-PowerPAD™ surface mount packages.

TYPICAL CHARACTERISTICS

OUTPUT REFERENCE VOLTAGE vs TEMPERATURE

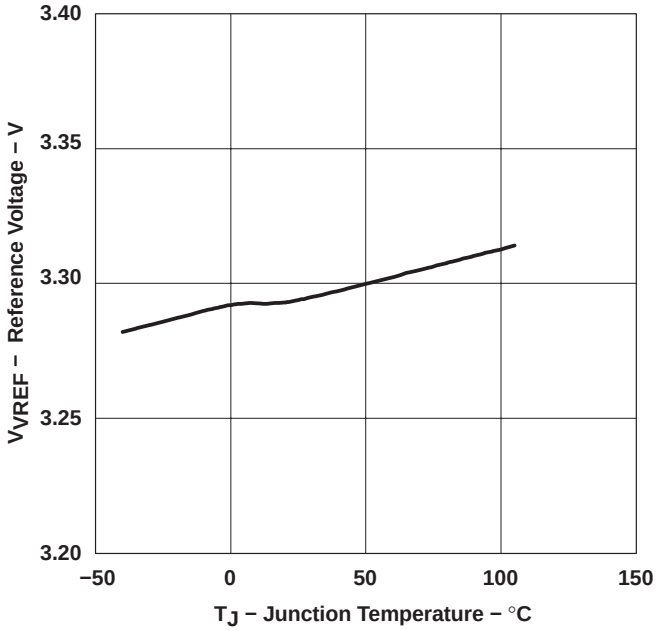


Figure 22

RAMP CURRENT vs TEMPERATURE

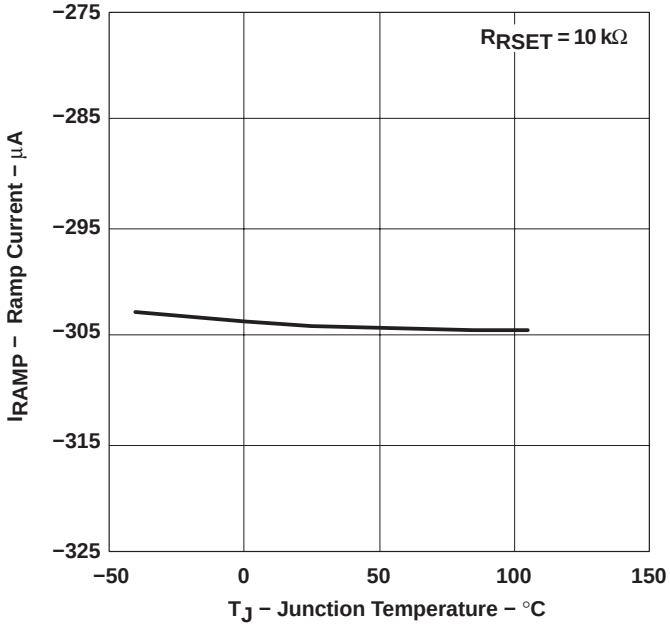


Figure 23

TYPICAL CHARACTERISTICS

I_{G2C}/I_{RAMP} AND I_{SS}/I_{RAMP} vs TEMPERATURE

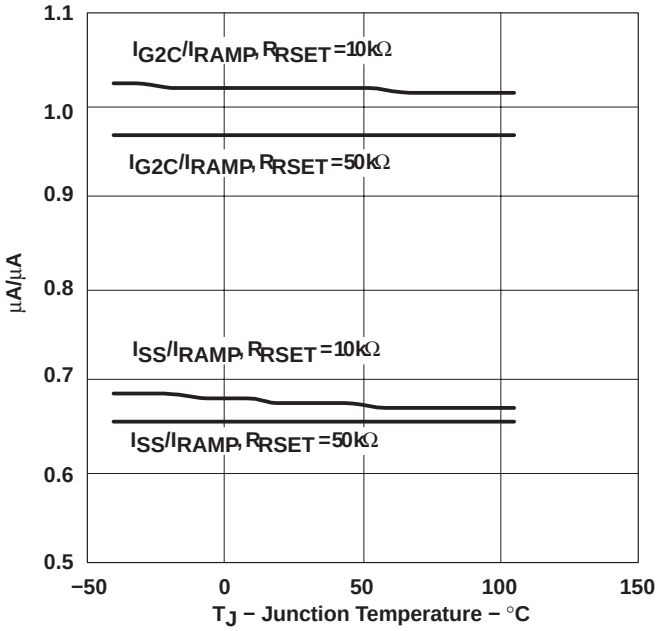


Figure 24

REGULATOR OUTPUT VOLTAGE vs TEMPERATURE

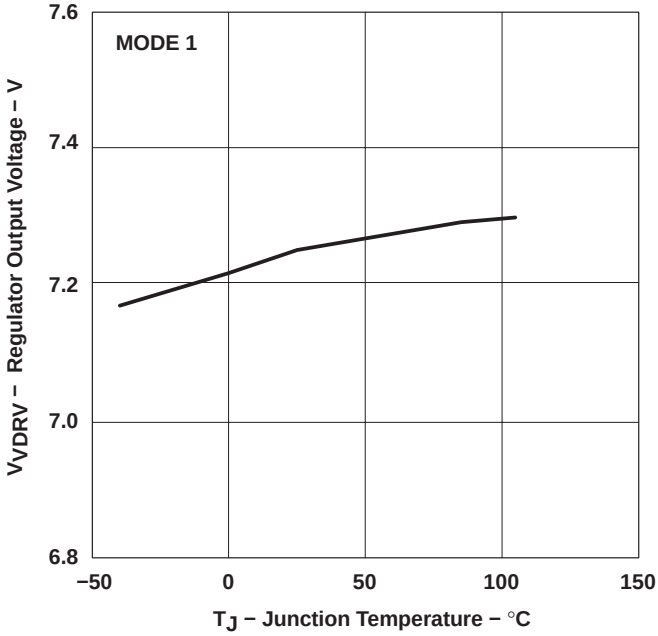


Figure 25

OSCILLATOR FREQUENCY vs TEMPERATURE

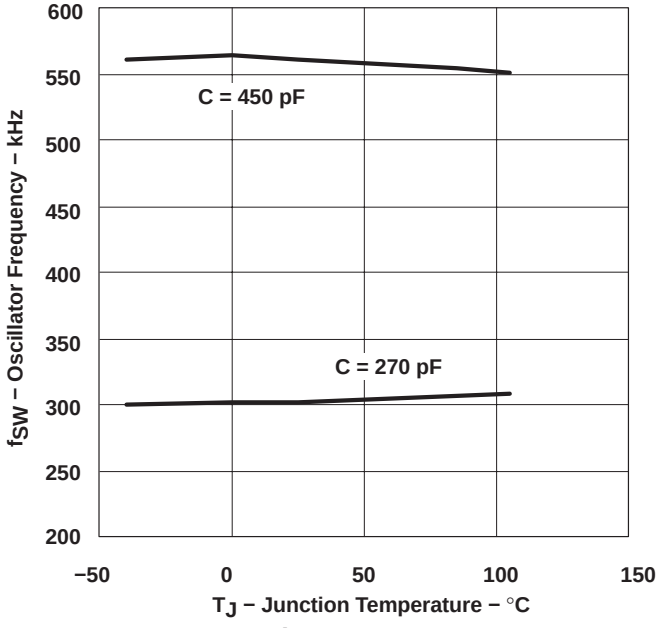


Figure 26

CURRENT ERROR AMPLIFIER OFFSET vs TEMPERATURE

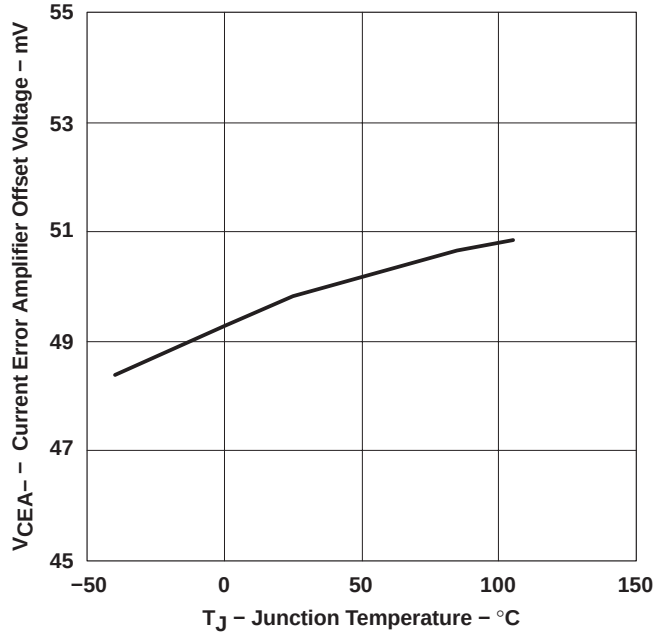


Figure 27

TYPICAL CHARACTERISTICS

SYNCIN THRESHOLD VOLTAGE
vs
TEMPERATURE

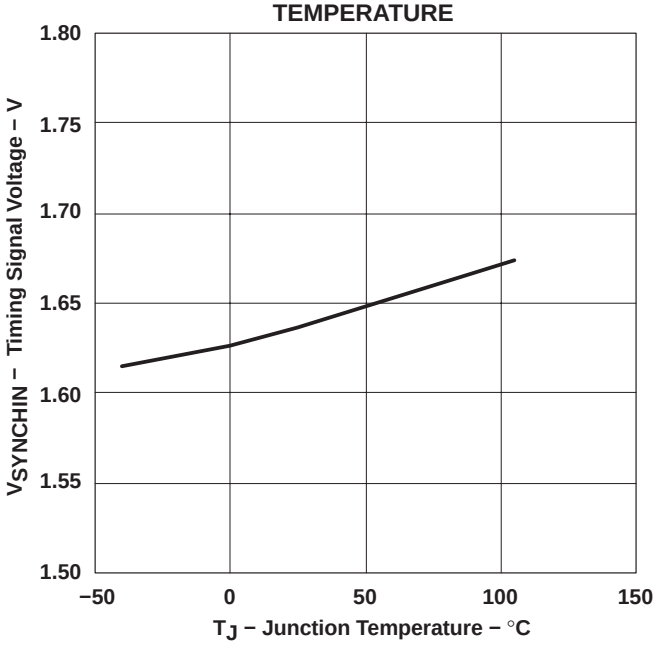


Figure 28

INVERTING AMPLIFIER GAIN AND PHASE
vs
FREQUENCY

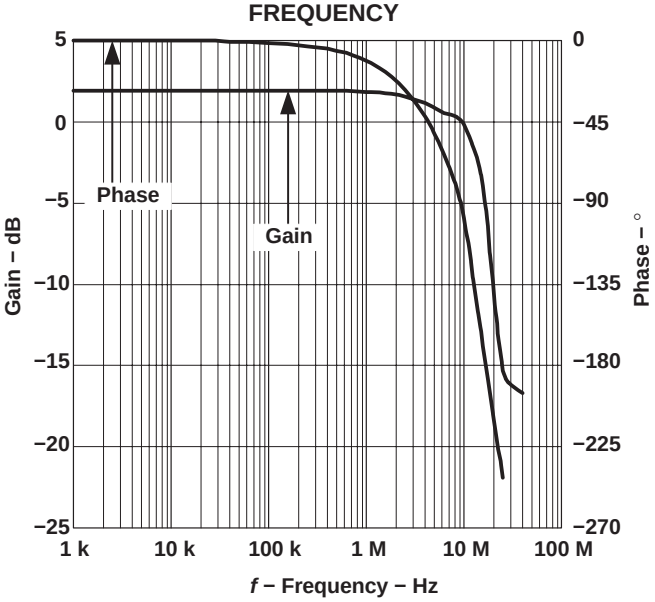


Figure 29

CURRENT ERROR AMPLIFIER GAIN AND PHASE
vs
FREQUENCY

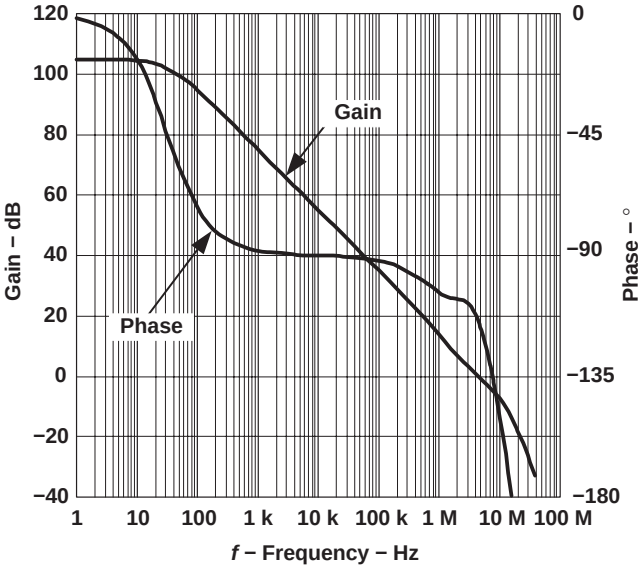


Figure 30

VOLTAGE ERROR AMPLIFIER GAIN AND PHASE
vs
FREQUENCY

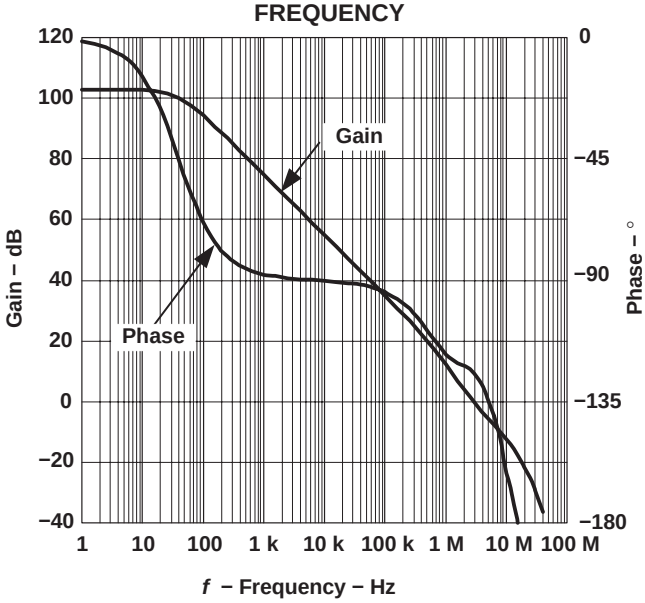


Figure 31

TYPICAL CHARACTERISTICS

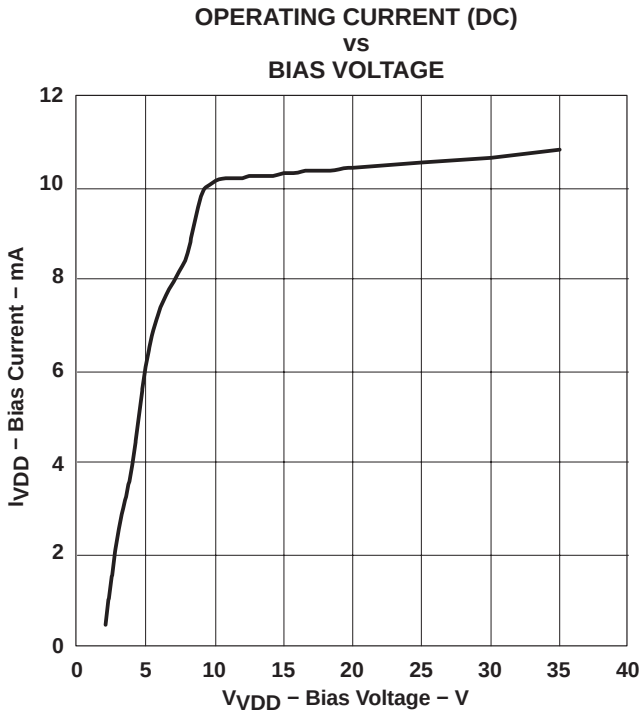


Figure 32

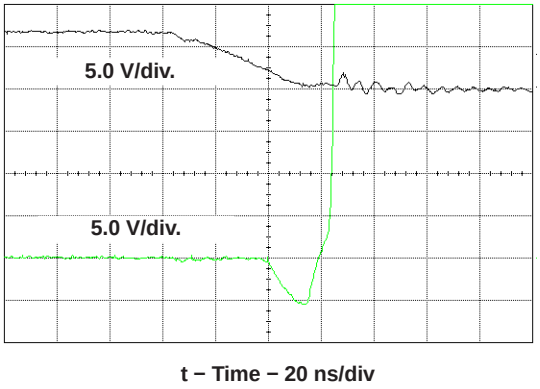


Figure 33. Predictive Gate Drive − G2 Falling

RELATED PRODUCTS

- UCC27223 High Efficiency Predictive Synchronous Buck Driver with Enable
- UCC2540 High-Efficiency Secondary-Side Synchronous Buck PWM Converter
- TPS40070/1 High-Efficiency Midrange Input Synchronous Buck Controller With Voltage Feed-Forward

REFERENCES

1. Application Note, *Predictive Gate Drive™ FAQ*, by Steve Mappus (SLUA285)
2. Datasheet, *TPS3103K33 Ultra-Low Supply Current/Supply Voltage Supervisory Circuits*, (SLVS363)
3. Power Supply Seminar SEM−1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by L. Balogh, (SLUP133)
4. Power Supply Seminar SEM1600 Topic 2: Sequencing Power Supplies in Multiple Voltage Rail Environments, by D. Daniels, D. Gehrke, and M. Segal, (SLUP224)
5. Technical Brief, *PowerPAD Thermally Enhanced Package*, (SLMA002)
6. Application Brief, *PowerPAD Made Easy*, (SLMA004)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2541PWPR	NRND	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCC2541
UCC2541PWPR.A	NRND	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCC2541

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

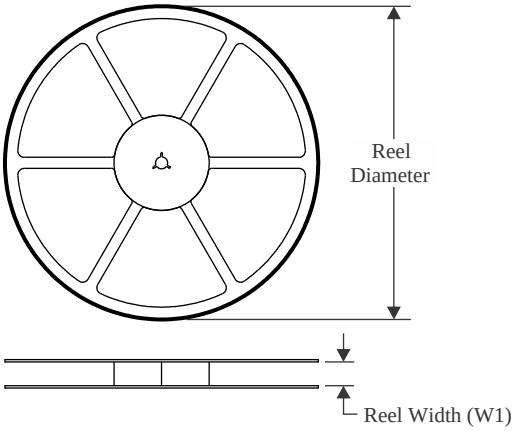
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

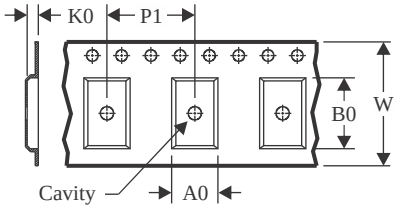
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

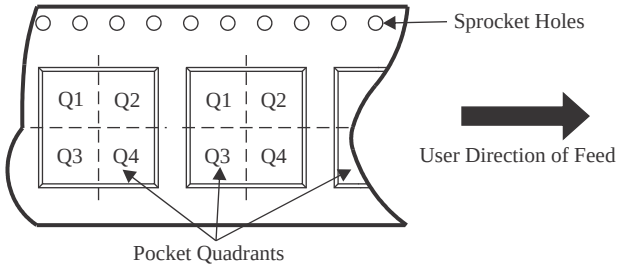


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

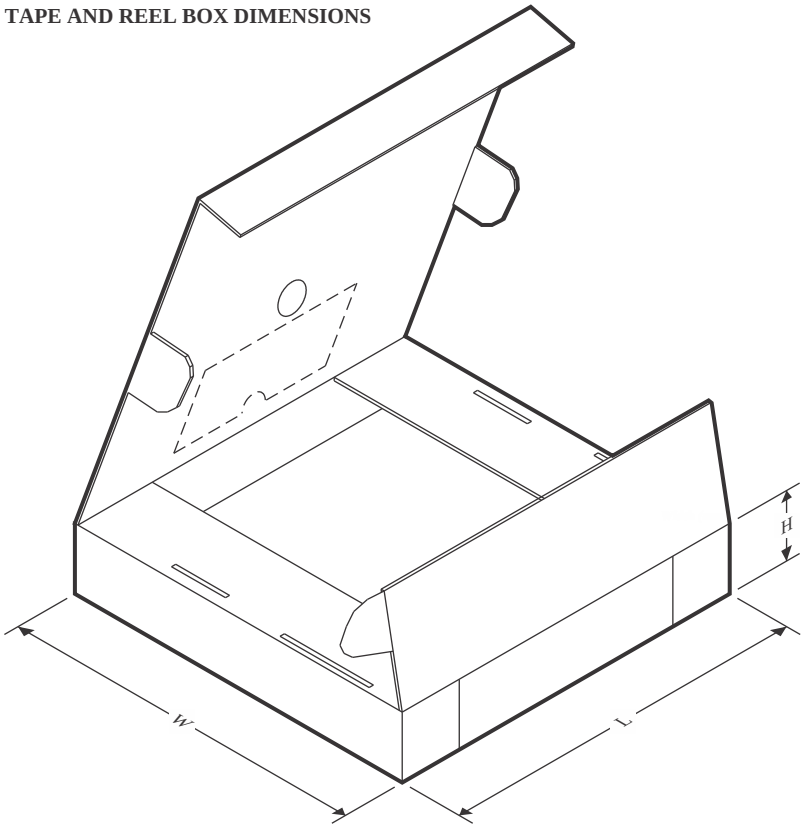
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2541PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2541PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

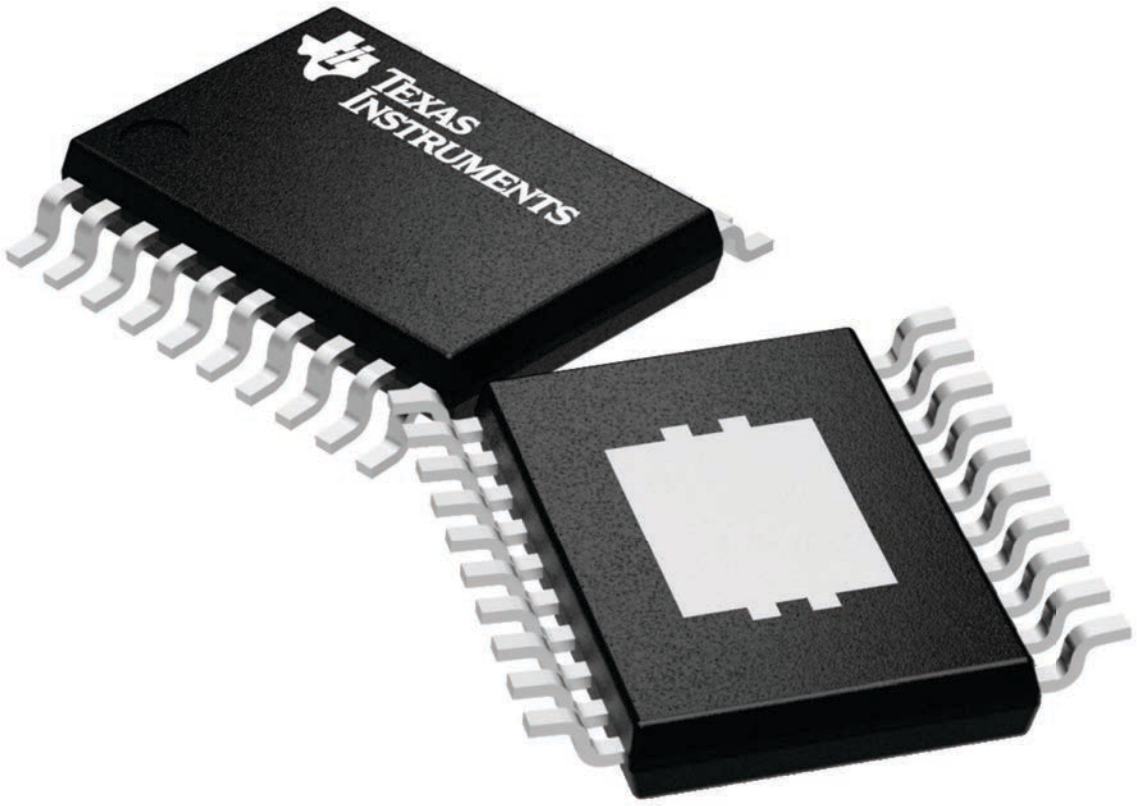
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

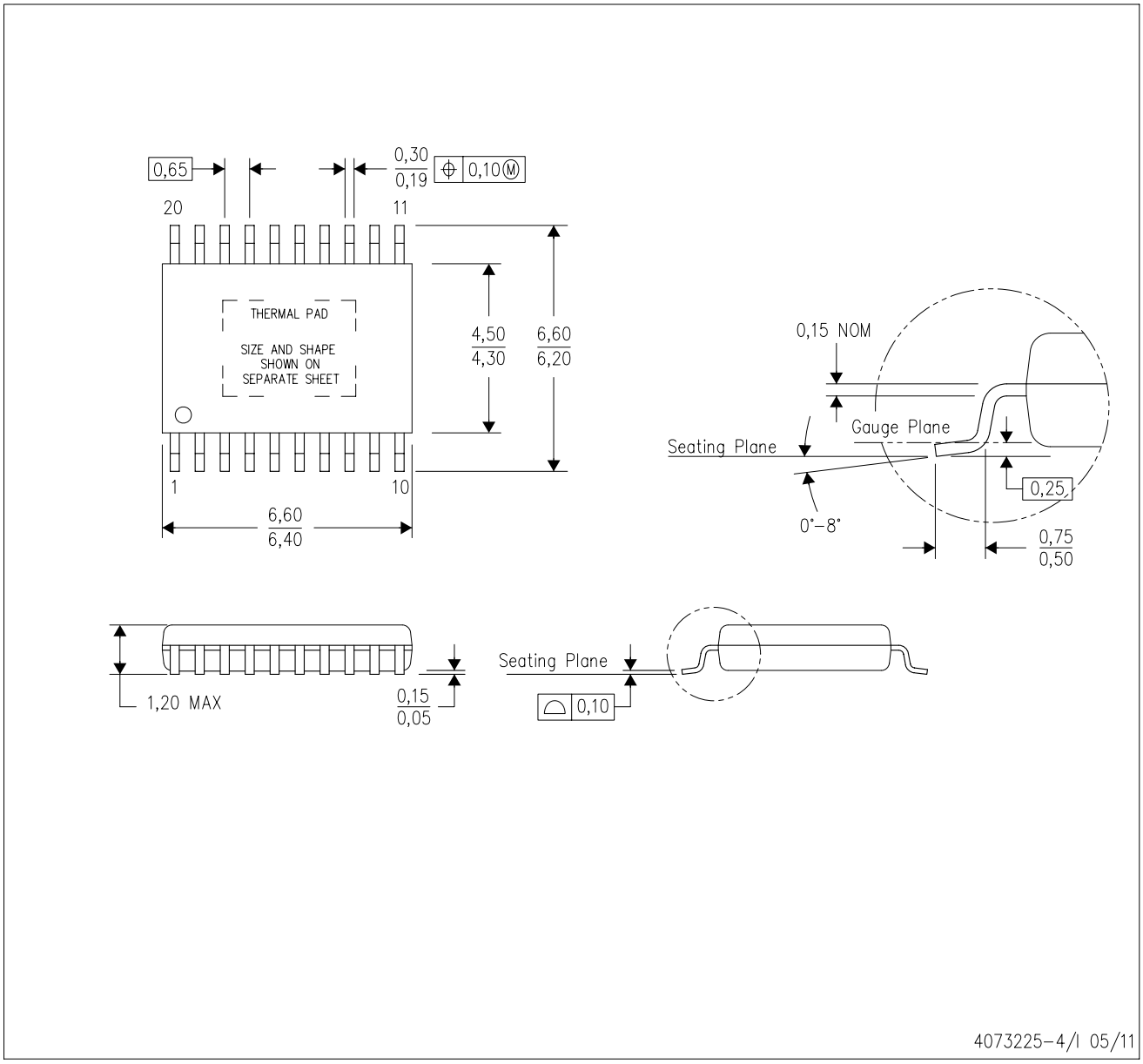
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

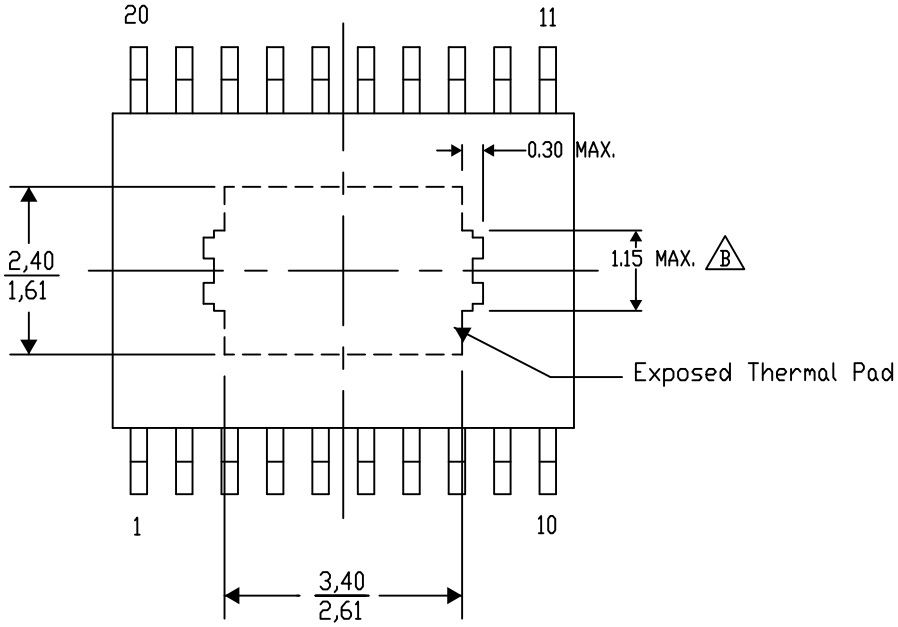
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

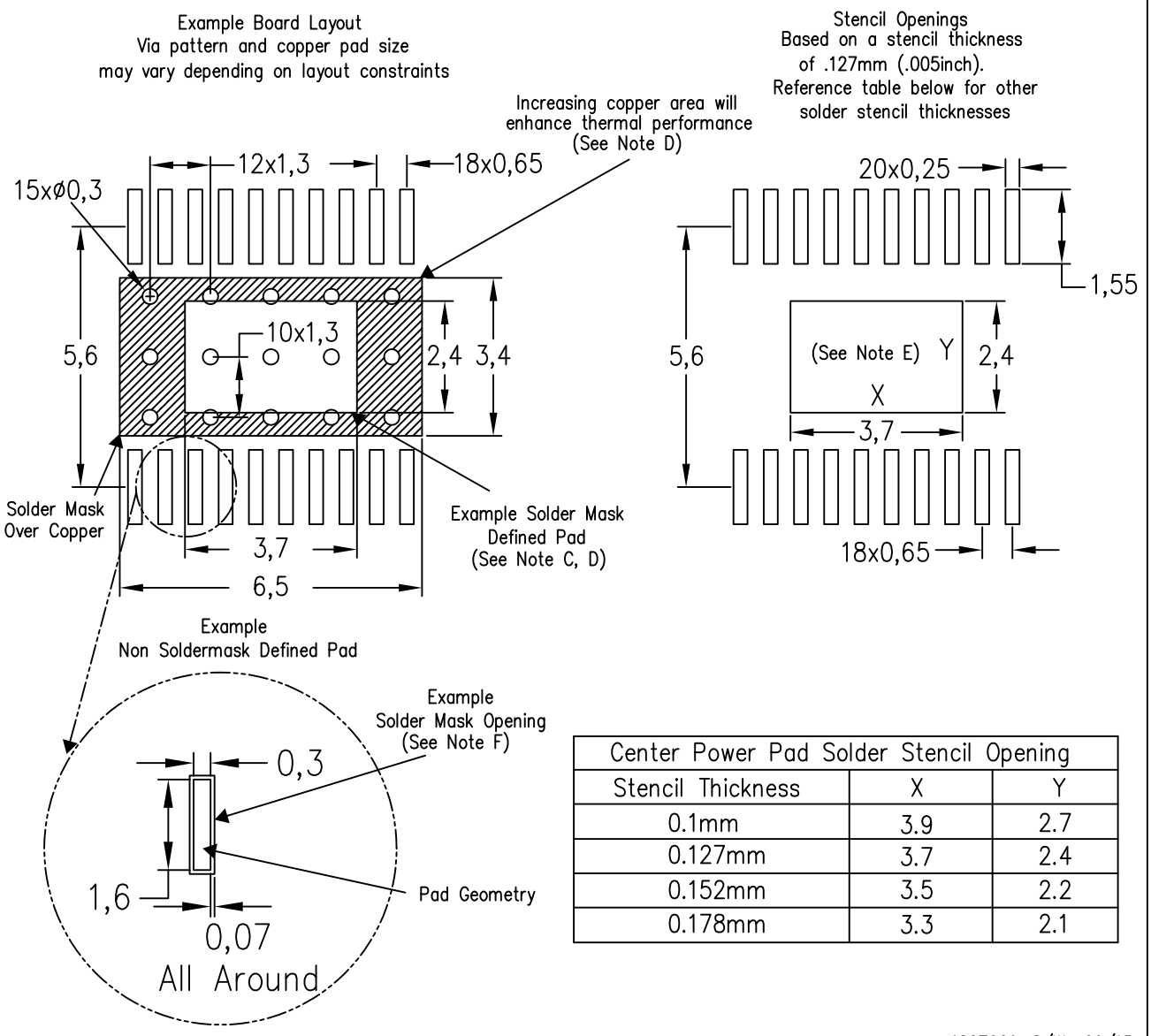
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025