

# **Simple Power Solution Using LDOs For TMS320C2834x Microcontrollers**

Ambreesh Tripathi

PMP - DC/DC Low-Power Converters

## **ABSTRACT**

This reference design is intended for users designing with the TMS320C2834x Microcontrollers. This design, employing sequenced power supplies, describes a system with an input voltage of 5V, and uses LDOs for a simple, small design.

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## **1 Introduction**

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and obtain reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power up and power down operations.

Sequencing refers to the order, timing, and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first failure represents a threat to the long term reliability of the dual voltage device, while the second failure poses the possibility of immediate damage to interface circuits in the processor or system devices such as memory, logic or data converter ICs.

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up, which may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

The power-on sequencing for TMS320C2834x Microcontrollers are shown in the Power Requirements table below. As mentioned in the table all voltage rails should be powered up within 5ms.

## **2 Power Requirements**

The power requirements are as specified in [Table 1](#).

**Table 1. TMS320C2834x Power Specs**

	PIN NAME(s)	VOLTAGE (V)	I <sub>max</sub> (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
Core	VDD	1.1 / 1.2 <sup>(1)</sup>	1000 <sup>(2)</sup>	±5%	1	All voltage rails should be powered up within 5ms
I/O	VDD18	1.8	80	±5%	2	
I/O	VDDIO	3.3	200	±5%	2	

<sup>(1)</sup> CVDD = 1.2V for 300MHz devices; CVDD = 1.1V for 200MHz.

<sup>(2)</sup> Max current on VDD at 300MHz is 1000mA; max current on VDD at 200MHz is 600mA.

## 2.1 Features

The design uses the following LDOs

<b>Devices:</b>	<b>TPS74801 (for 1.2V), TPS74701 (for 3.3V), TPS71718(1.8)</b>
Power supply specs:	
V <sub>in</sub>	5 V ± 10%
V <sub>out1</sub>	1.1 V/1.2 V ± 5% at 1000 mA
V <sub>out2</sub>	1.8 V ± 5% at 80 mA
V <sub>out3</sub>	3.3 V ± 5% at 200 mA
Sequencing	1) V <sub>out1</sub> 2) V <sub>out2</sub> and V <sub>out3</sub>

### TPS74801 and TPS74701

- V<sub>OUT</sub> Range: 0.8V to 3.6V
- 2% Accuracy Over Line/Load/Temperature
- Programmable Soft-Start Provides Linear Voltage Startup
- Stable with Any Output Capacitor ≥ 2.2μF
- Available in a Small 3mm × 3mm × 1mm SON-10 and 5 × 5 QFN-20 Packages

### TPS71718

- 150mA Low-Dropout Regulator with Enable
- Low Noise: 30μV typical (100Hz to 100kHz)
- Excellent Load/Line Transient Response
- Small SC70-5, 2mm × 2mm SON-6, and 1.5mm × 1.5mm SON-6 Packages

More information on the Devices can be found from the datasheets.

TPS74801 –[SBVS074F](#)

TPS74701 –[SBVS099D](#)

TPS71718 –[SBVS068G](#)

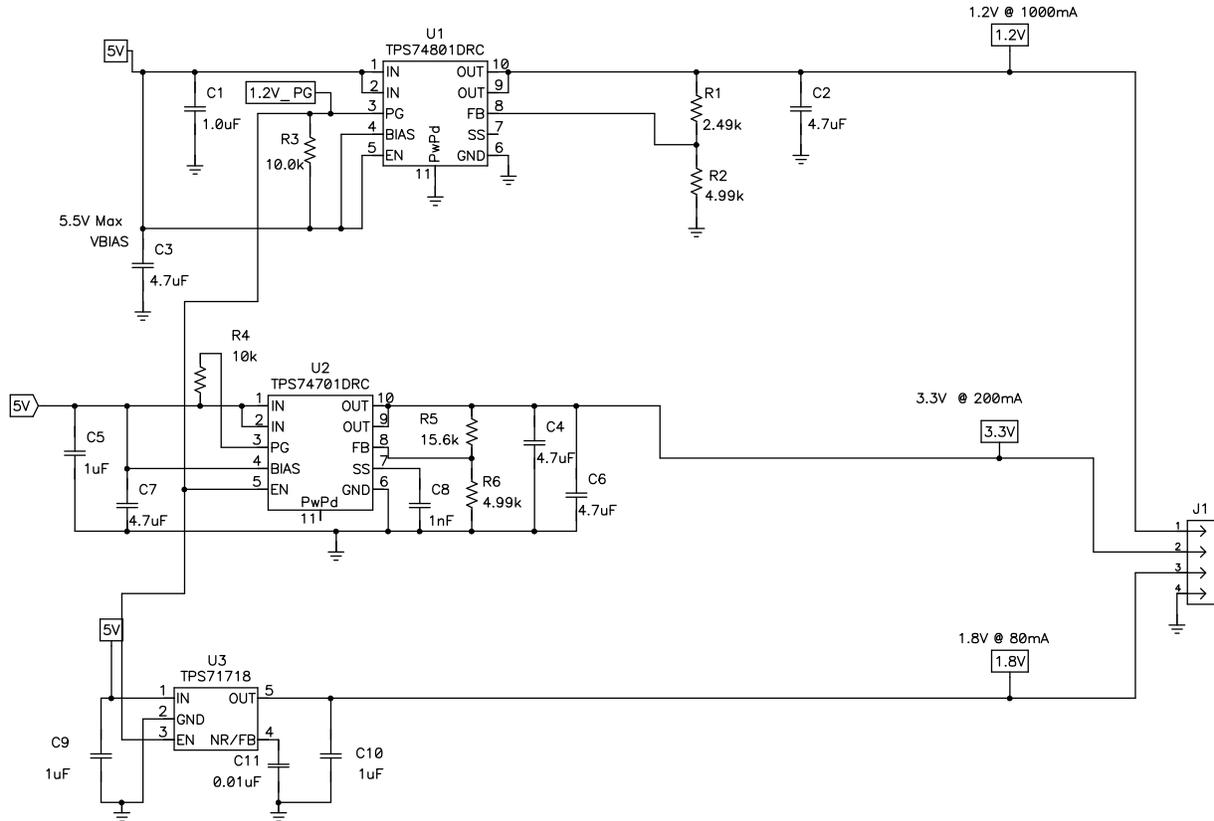


Figure 1. PMP4999 Reference Design Schematic

Proper sequencing is achieved in the design with the use of enable pins. The Core 1.2V at 1000mA (TPS74801) comes first, the PG output then enables the TPS74701 and TPS71718 devices, thus following the required sequence.

### 3 List of Material

Table 2. PMP4999 List of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	C1	1.0 $\mu$ F	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK	5650
1	C2	4.7 $\mu$ F	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J106M	TDK	5650
1	C3	4.7 $\mu$ F	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J475K	TDK	5650
3	C4	4.7 $\mu$ F	Capacitor, Ceramic, 4.7 $\mu$ F, 6.3V, X5R	0603	C1608X5R0J475M	TDK	5650
1	C5	1 $\mu$ F	Capacitor, Ceramic, 1 $\mu$ F, 16V, X5R	0603	C1608X5R1C105K	TDK	5650
	C6	4.7 $\mu$ F	Capacitor, Ceramic, 4.7 $\mu$ F, 6.3V, X5R	0603	C1608X5R0J475M	TDK	5650
	C7	4.7 $\mu$ F	Capacitor, Ceramic, 4.7 $\mu$ F, 6.3V, X5R	0603	C1608X5R0J475M	TDK	5650
1	C8	1 nF	Capacitor, Ceramic, 1000 pF, 50V, X7R, 10%	0603	C1608X7R1H102K	TDK	5650
2	C9	1 $\mu$ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	C1608X5R1E105M	TDK	5650
	C10	1 $\mu$ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	C1608X5R1E105M	TDK	5650
1	C11	0.01 $\mu$ F	Capacitor, Ceramic, 50V, COG, 10%	0402	Std	Std	2800
1	J1	PEC36SAAN	Header, Male 4-pin, 100mil spacing, (36-pin strip)	0.100 inch x 4	PEC36SAAN	Sullins	50000
1	R1	2.49k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R2	4.99k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R3	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R4	10k	Resistor, Chip, 10k $\Omega$ 1/16W, 5%	0603	Std	Std	5,650

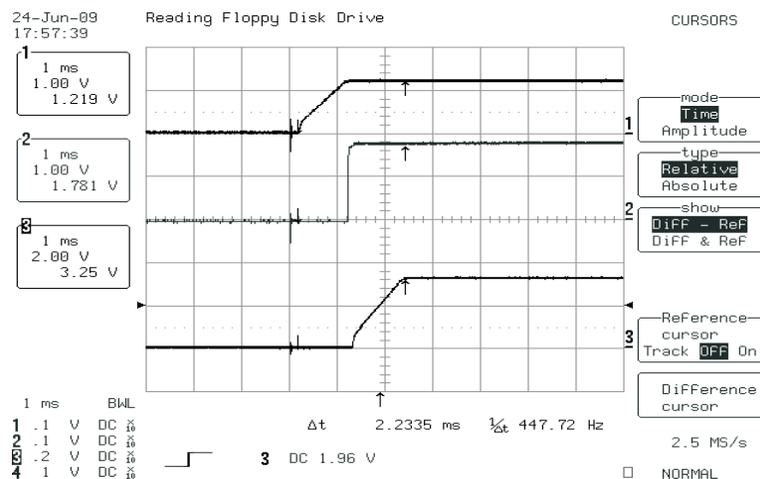
**Table 2. PMP4999 List of Materials (continued)**

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	R5	15.6k	Resistor, Chip, 2k49 Ω, 1/16W, 5%	0603	Std	Std	5,650
1	R6	4.99k	Resistor, Chip, 4k99 Ω, 1/16W, 5%	0603	Std	Std	5,650
1	U1	TPS74801DRC	IC, 1.5A LDO Regulator with Soft-Start	SON-10	TPS74801DRC	TI	30400
1	U2	TPS74701DRC	IC, 1.5A LDO Regulator with Soft-Start	SON-10	TPS74701DRC	TI	30400
1	U3	TPS71718	IC, 150mA, Low Iq, Wide Bandwidth, LDO Linear Regulators	SC70	TPS71718	TI	18600

- Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
  2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
  3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
  4. Ref designators marked with an asterisk (\*\*\*) cannot be substituted. All other components can be substituted with equivalent MFG's components.

## 4 Test Result

The startup waveform, shown in [Figure 2](#), demonstrates that the required sequencing order is followed.



**Figure 2. Shows Sequencing in Start up Waveform**

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