User's Guide

TPS54625 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS54625 as well as support documentation for the TPS54625EVM-608 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS54625EVM-608.

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1 Introduction

The TPS54625 is a single, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a very low external component count. The D-CAP2™ control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 650 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS54625 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54625 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS54625 dc/dc synchronous converter is designed to provide up to a 6.5-A output from an input voltage source of 4.5 V to 18 V. The output voltage range is from 0.76 V to 5.5 V. Rated input voltage and output current ranges for the evaluation module are given in Table 1-1.

The TPS54625EVM-608 evaluation module is a single, synchronous buck converter providing 1.05 V at 6.5 A from 4.5-V to 18-V input. This user's guide describes the TPS54625EVM-608 performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54625EVM-538	V_{IN} = 4.5 V to 18 V	0 A to 6.5 A

2 Performance Specification Summary

A summary of the TPS54625EVM-608 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.05 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS54625EVM-608 Performance Specifications Summary

Specifications		Test Conditions	Min	Typ	Max	Unit
	Input voltage range (V_{IN})		4.5	12	18	V
CH1	Output voltage			1.05		V
	Operating frequency	V_{IN} = 9 V, I_O = 1 A		650		kHz
	Output current range		0		6.5	A
	Over current limit	V_{IN} = 12 V, L_O = 1.5 µH		8.2		A
	Output ripple voltage	V_{IN} = 12 V, I_O = 6.5 A		7		mV_{PP}

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54625. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.765 V. The value of R1 for a specific output voltage can be calculated using Equation 1.

$$VO = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Table 3-1 lists the R1 values for some common output voltages. For higher output voltages of 1.8 V or above, a feedforward capacitor (C2) may be required to improve phase margin. Pads for this component (C2) are provided on the printed-circuit board. Note that the values given in Table 3-1 are standard values and not the exact value calculated using Table 3-1.

Table 3-1. Output Voltages

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C2 (pF)	L1 (µH)			C9 + C10 + C11 (µF)
				Min	Typ	Max	
1.0	6.81	22.1	5 - 220	1.0	1.5	4.7	22 - 68
1.05	8.25	22.1	5 - 220	1.0	1.5	4.7	22 - 68
1.2	12.7	22.1	5 - 100	1.0	1.5	4.7	22 - 68
1.5	21.5	22.1	5 - 68	1.0	1.5	4.7	22 - 68
1.8	30.1	22.1	5 - 22	1.2	1.5	4.7	22 - 68
2.5	49.9	22.1	5 - 22	1.5	2.2	4.7	22 - 68
3.3	73.2	22.1	5 - 22	1.8	2.2	4.7	22 - 68
5.0	124	22.1	5 - 22	2.5	3.3	4.7	22 - 68

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54625EVM-608. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

The TPS54625EVM-608 is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP7 is used to monitor the output voltage with TP8 as the ground reference.

Table 4-1. Connection and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 1.05 V at 6.5-A maximum
JP1	EN control. Connect EN to OFF to disable, connect EN to ON to enable.
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	EN test point
TP4	Analog ground test point
TP5	Switch node test point
TP6	Power good test point
TP7	Output voltage test point
TP8	Ground test point at output connector

4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) is set from EN to OFF.
2. Apply appropriate V_{IN} voltage to VIN and PGND terminals at J1.
3. Move the jumper at JP1 (Enable control) to cover EN and ON. The EVM enables the output voltage.

4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS54625EVM-608 at an ambient temperature of 25°C.

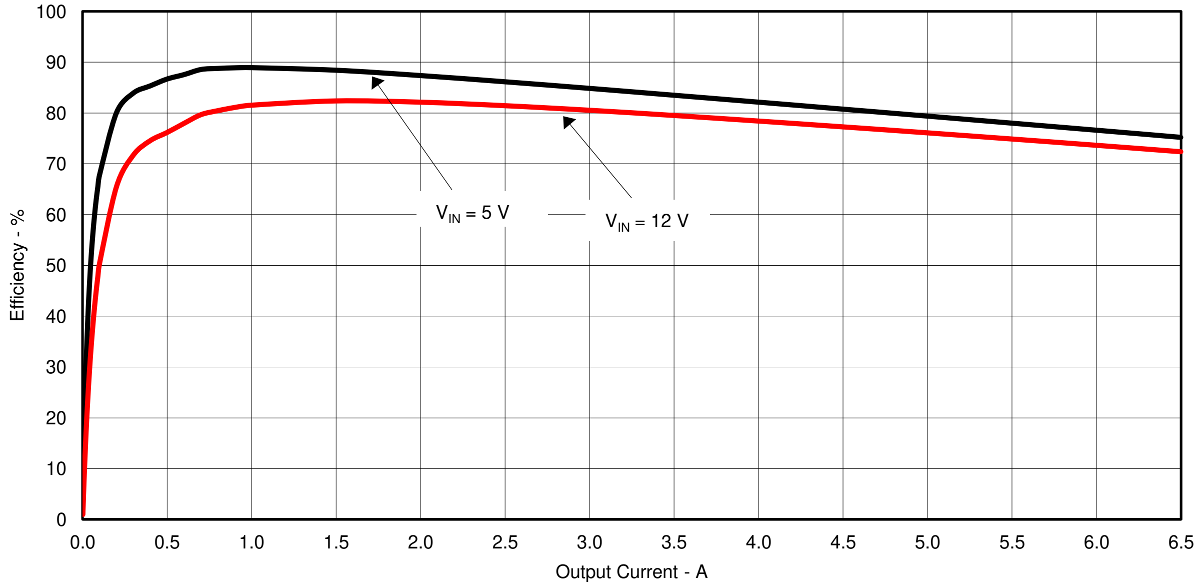

Figure 4-1. TPS54625EVM-608 Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS54625EVM-608 at an ambient temperature of 25°C.

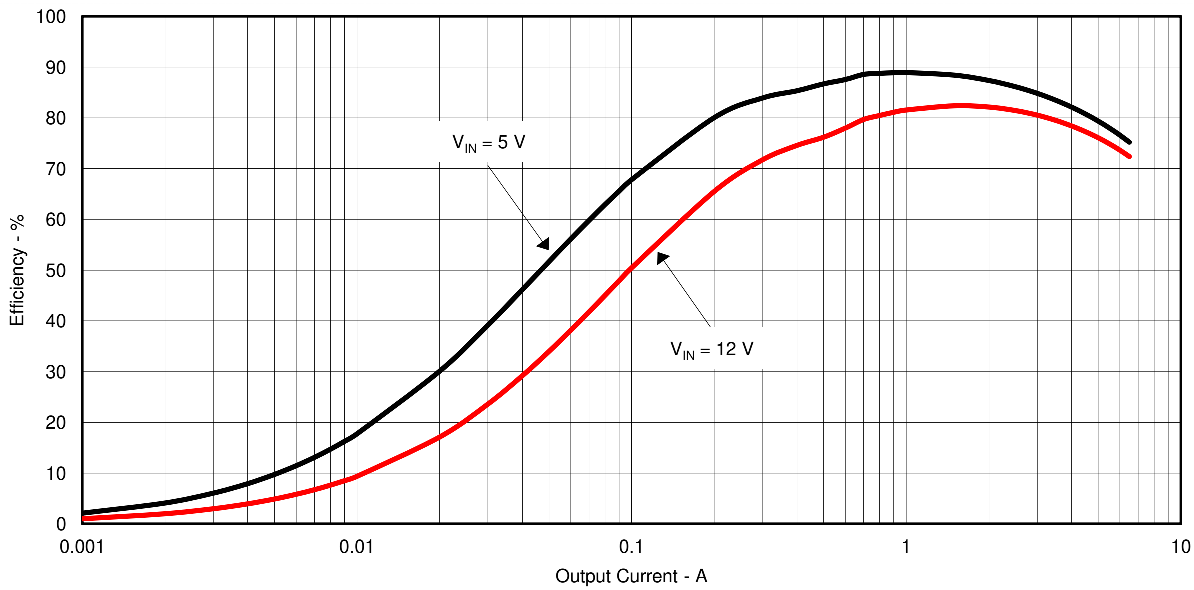

Figure 4-2. TPS54625EVM-608 Light Load Efficiency

4.4 Load Regulation

The load regulation for the TPS54625EVM-608 is shown in Figure 4-3.

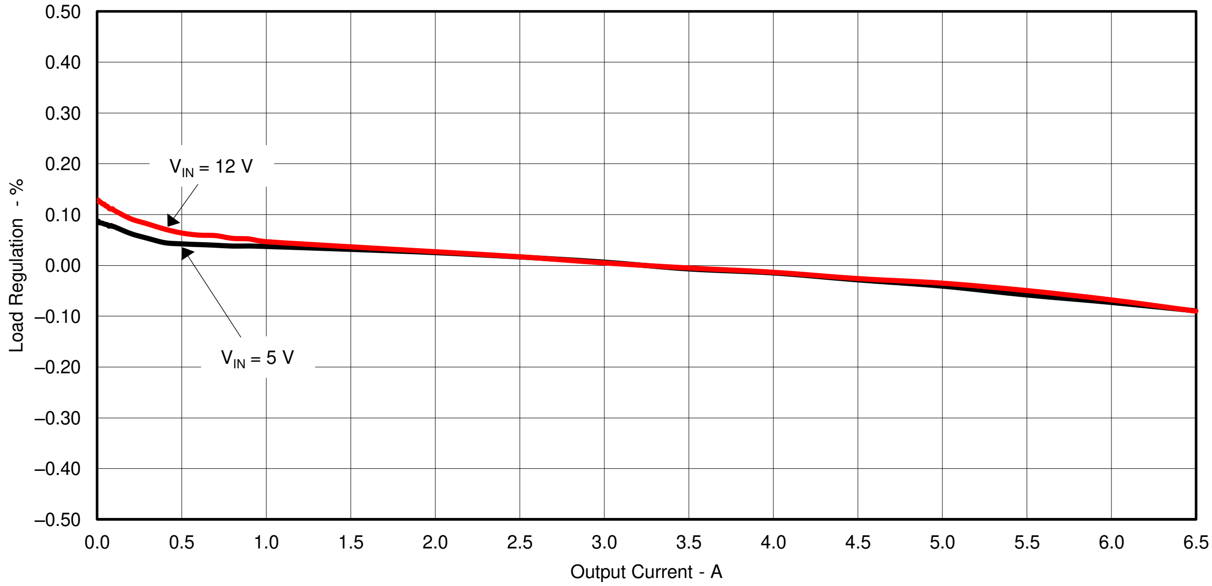

Figure 4-3. TPS54625EVM-608 Load Regulation

4.5 Line Regulation

The line regulation for the TPS54625EVM-608 is shown in Figure 4-4.

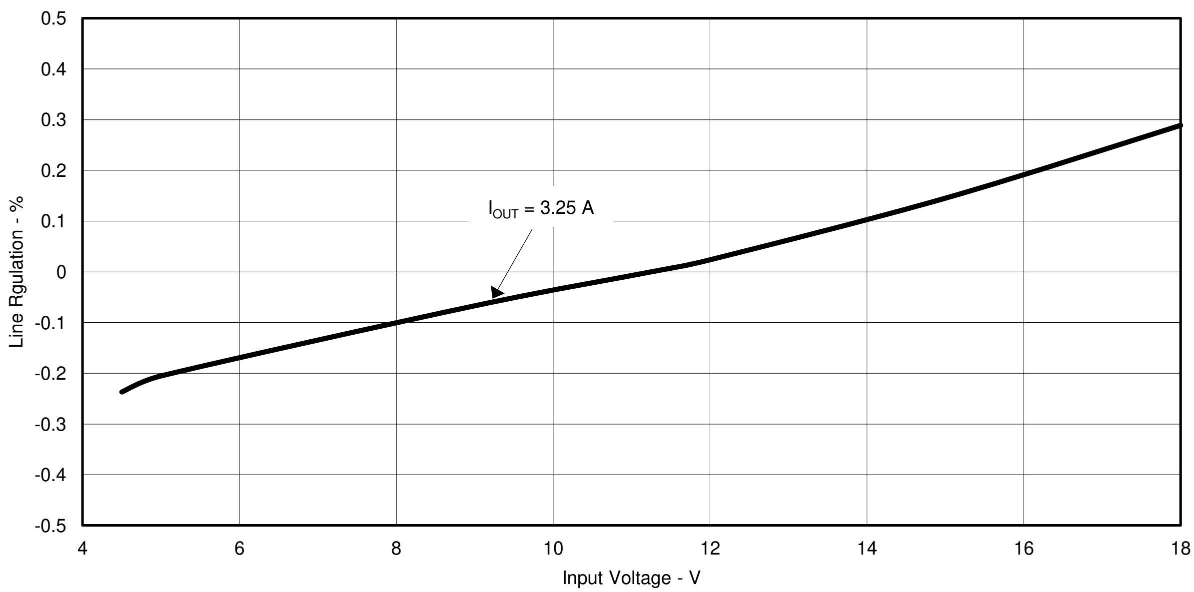

Figure 4-4. TPS54625EVM-608 Line Regulation

4.6 Load Transient Response

The TPS54625EVM-608 response to load transient is shown in Figure 4-5 and Figure 4-6. The current steps and slew rates are indicated in the figures. Total peak-to-peak voltage variation is as shown.

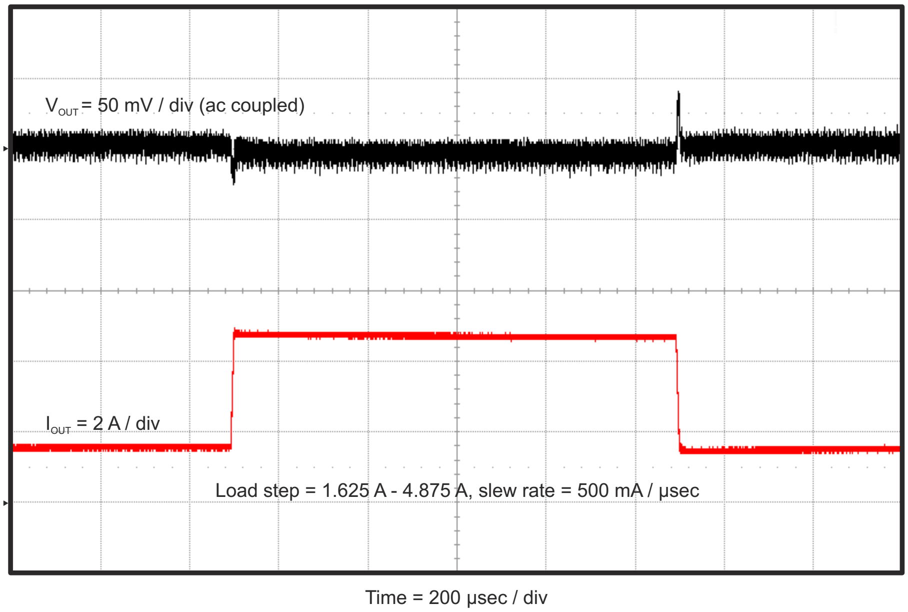

Figure 4-5. TPS54625EVM-608 Load Transient Response, 25% to 75% Load Step

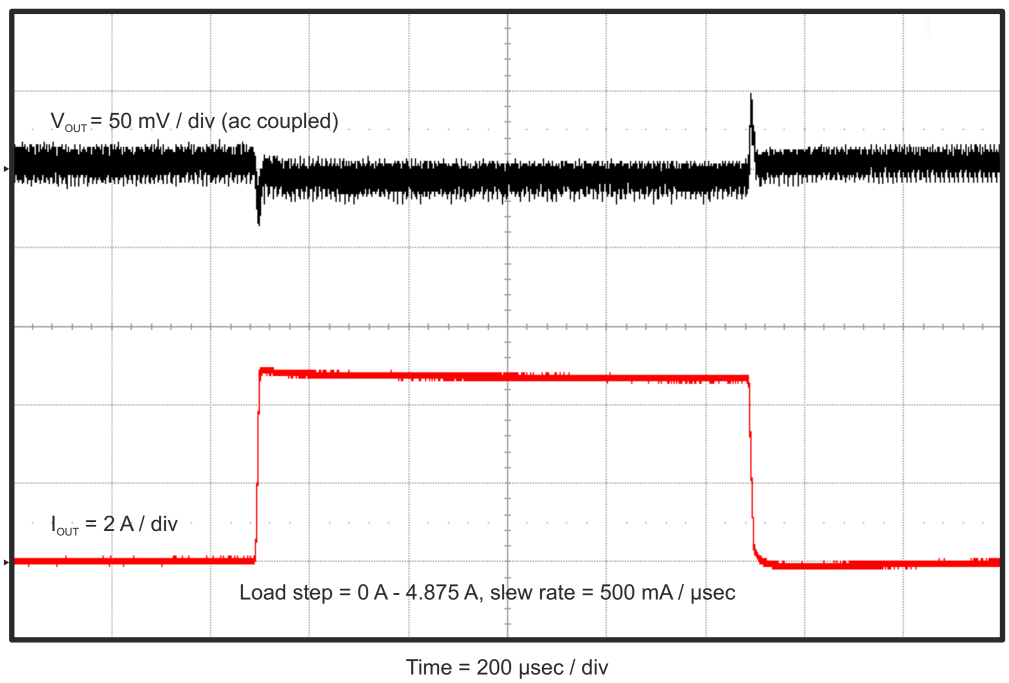

Figure 4-6. TPS54625EVM-608 Load Transient Response, No Load to 75% Load Step

4.7 Output Voltage Ripple

The TPS54625EVM-608 output voltage ripple is shown in Figure 4-7, Figure 4-8, and Figure 4-9. The output currents are as indicated.

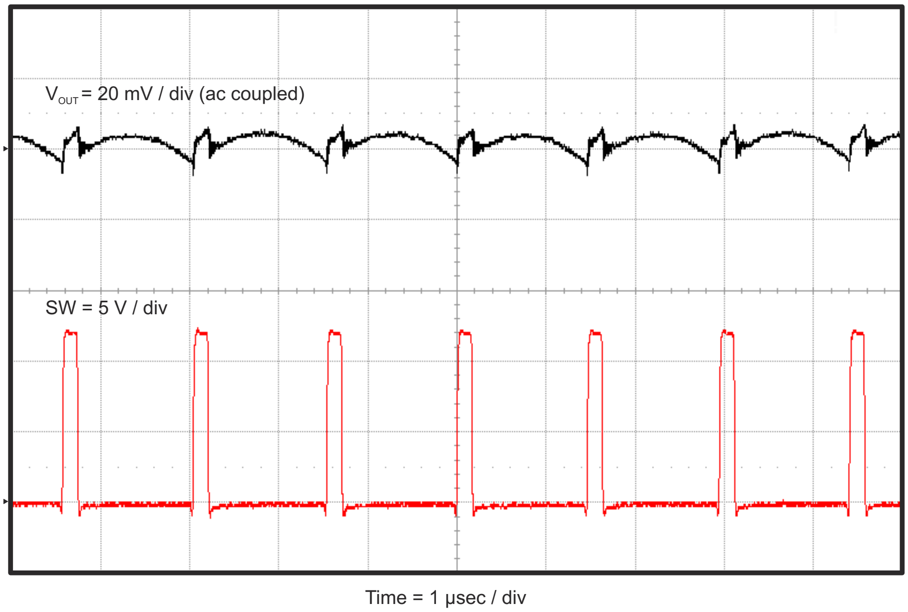

Figure 4-7. TPS54625EVM-608 Output Voltage Ripple, I_{OUT} = 6.5 A

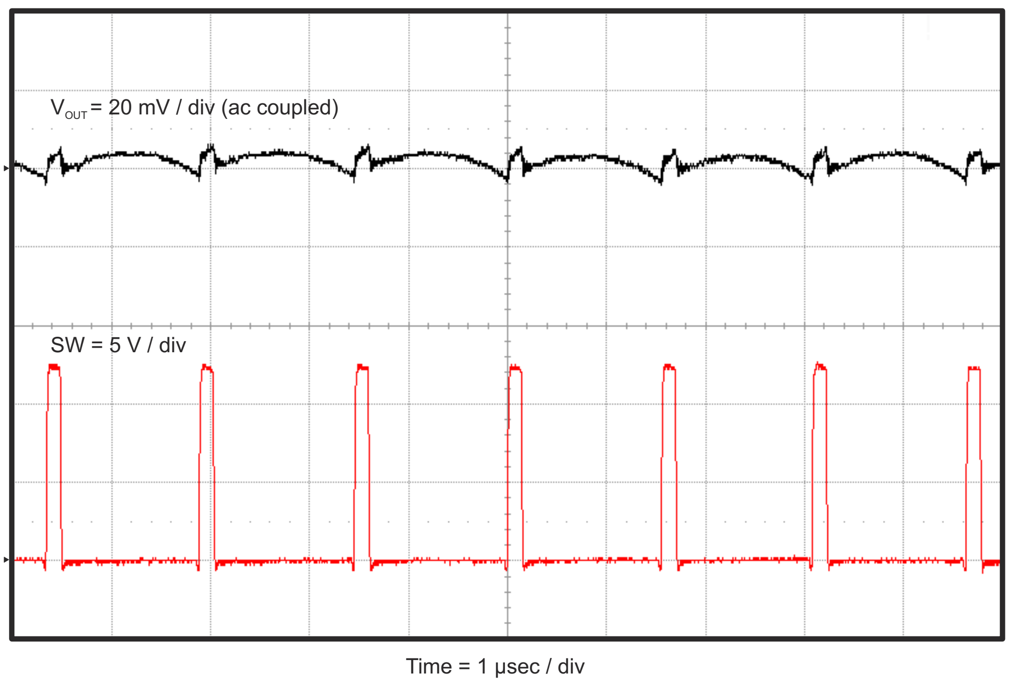

Figure 4-8. TPS54625EVM-608 Output Voltage Ripple, I_{OUT} = 1 A

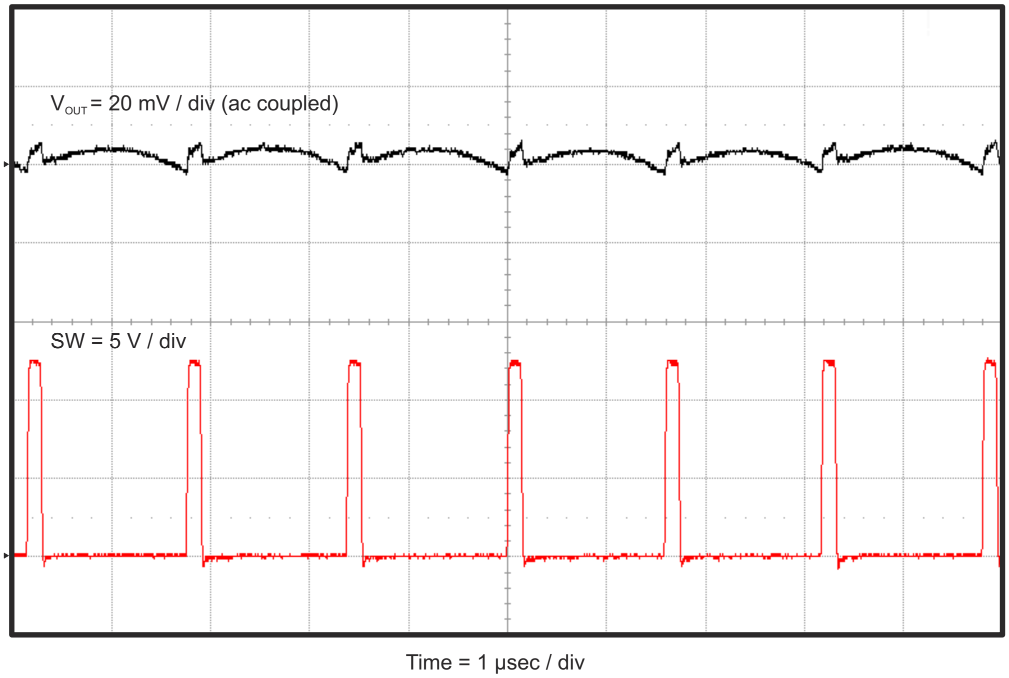

Figure 4-9. TPS54625EVM-608 Output Voltage Ripple, I_{OUT} = 0 A

4.8 Input Voltage Ripple

The TPS54625EVM-608 input voltage ripple is shown in Figure 4-10. The output current is as indicated.

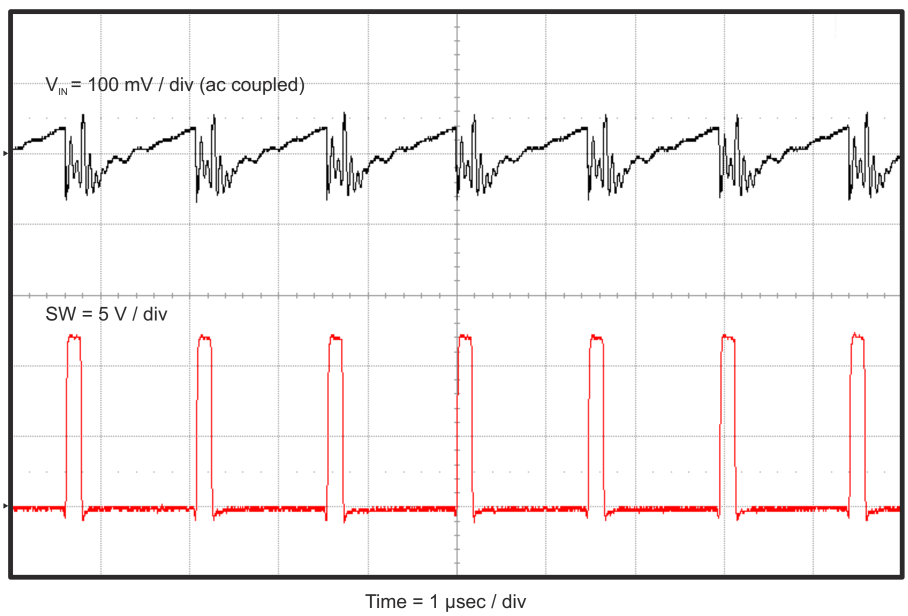

Figure 4-10. TPS54625EVM-608 Input Voltage Ripple, I_{OUT} = 6.5 A

4.9 Start-Up

The TPS54625EVM-608 start-up waveform relative to V_{IN} is shown in Figure 4-11. Load = 1 Ω resistive.

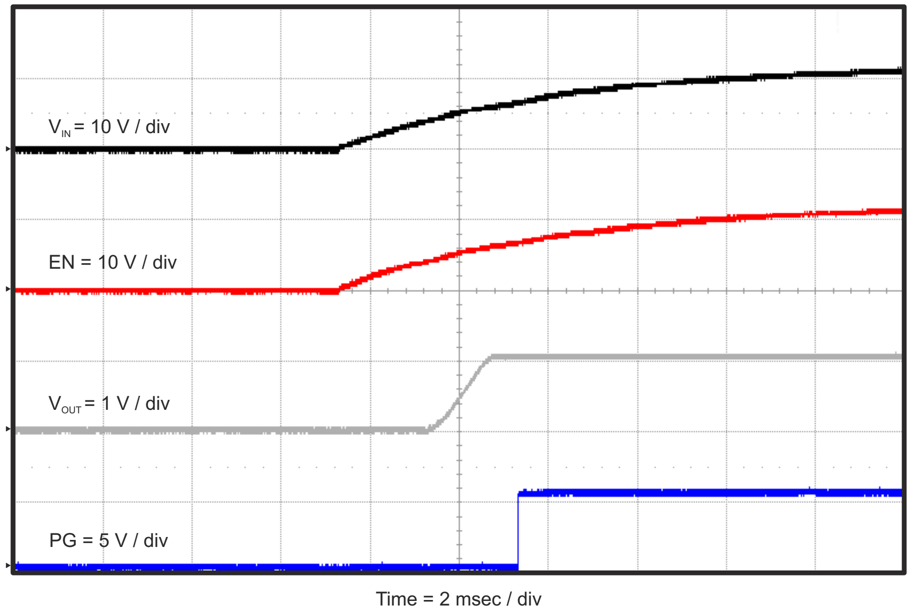

Figure 4-11. TPS54625EVM-608 Start-Up Relative to V_{IN}

The TPS54625EVM-608 start-up waveform relative to enable (EN) is shown in Figure 4-12. Load = 1 Ω resistive.

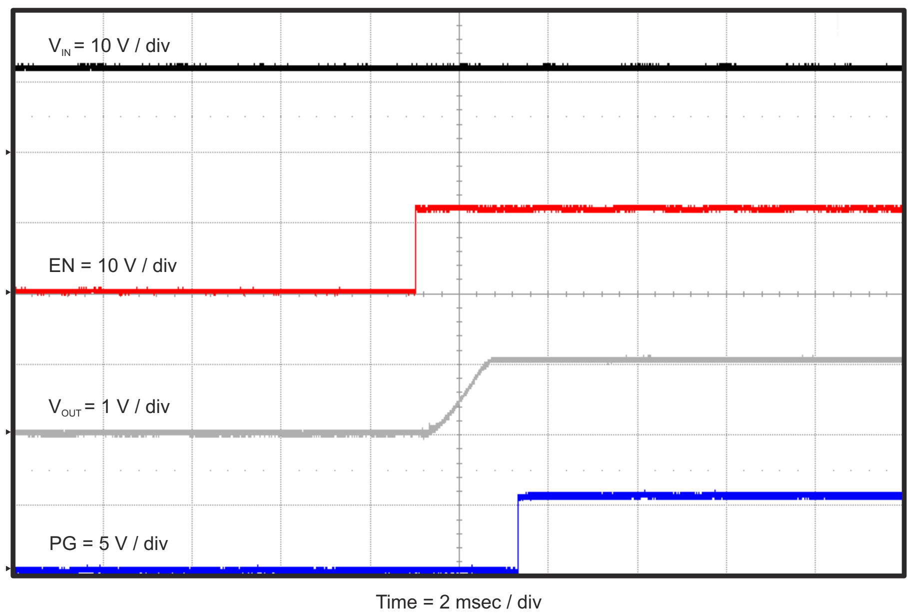

Figure 4-12. TPS54625EVM-608 Start-Up Relative to EN

4.10 Shut-Down

The TPS54625EVM-608 shut-down waveform relative to V_{IN} is shown in Figure 4-13. Load = 1 Ω resistive.

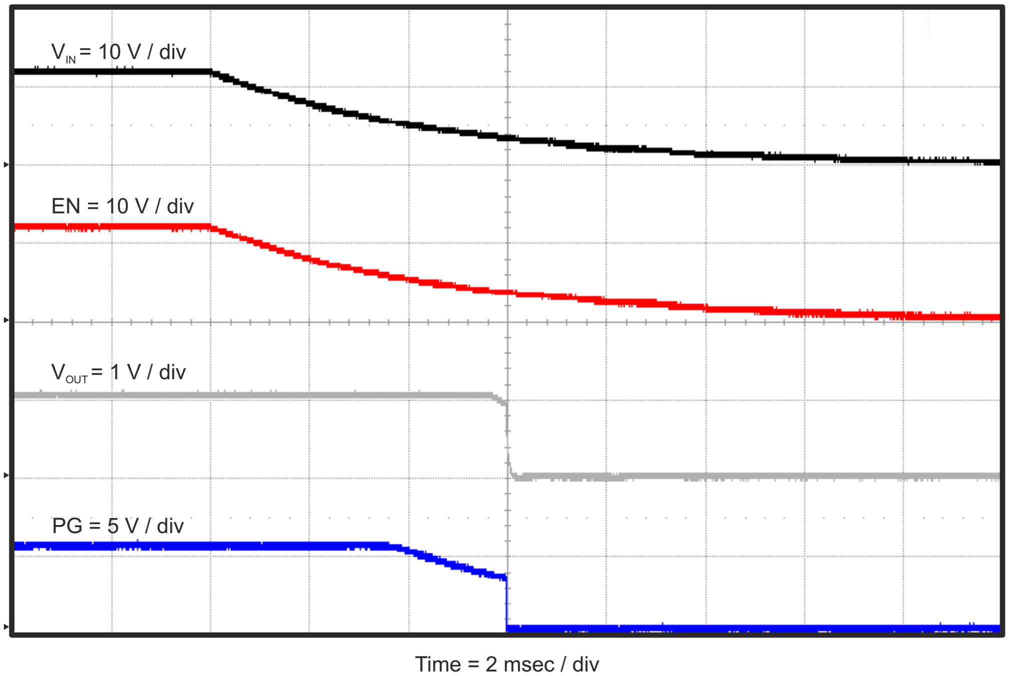

Figure 4-13. TPS54625EVM-608 Shut-Down Relative to V_{IN}

The TPS54625EVM-608 shut-down waveform relative to EN is shown in Figure 4-14. Load = 1 Ω resistive.

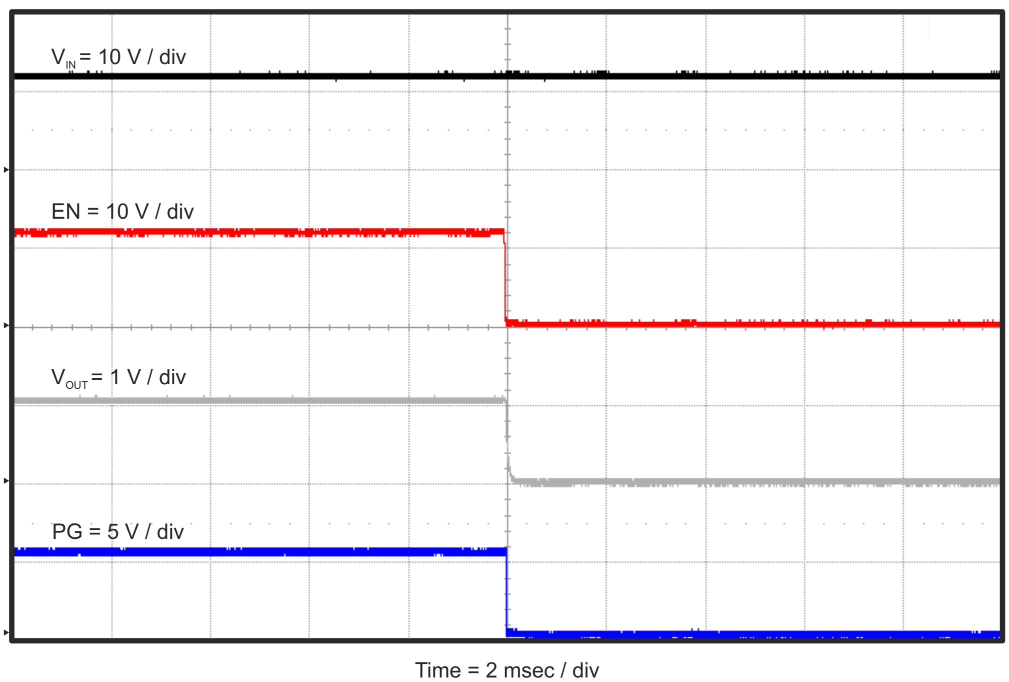

Figure 4-14. TPS54625EVM-608 Shut-Down Relative to EN

5 Board Layout

This section provides a description of the TPS54625EVM-608, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS54625EVM-608 is shown in Figure 5-1 through Figure 5-6. The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS54625 and a large area filled with ground. Many of the signal traces also are located on the top side. The input decoupling capacitors are located as close to the IC as possible. The input and output connectors, test points, and most of the components are located on the top side. R3, the 0-Ω resistor that connects VIN to VCC and R4, the power good pull up, are located on the back side. Analog ground and power ground are connected at a single point on the top layer near pin 5 of the TPS54625. The internal layer 1 is a split plane containing analog and power grounds. The internal layer 2 is primarily power ground but also has a fill area of VIN and a trace routing VCC to the enable control jumper JP1. The bottom layer is primarily analog ground but also has traces to connect VIN to VCC through R3, traces for the power good signal, and the feedback trace from VOUT to the voltage setpoint divider network.

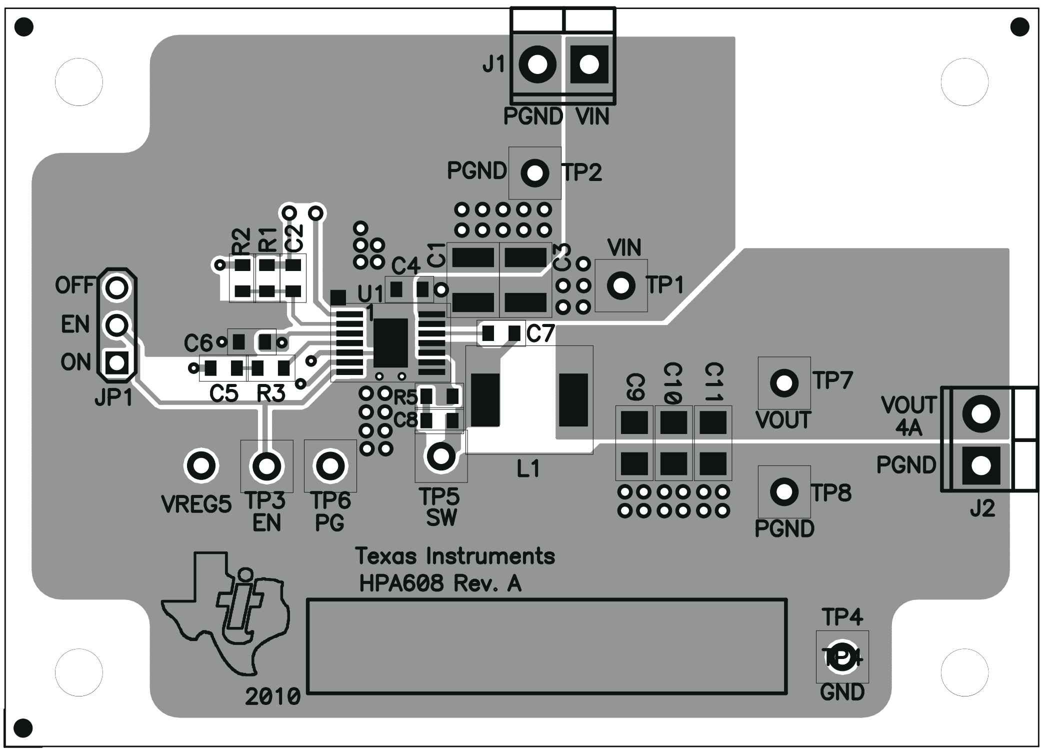

Figure 5-1. Top Assembly

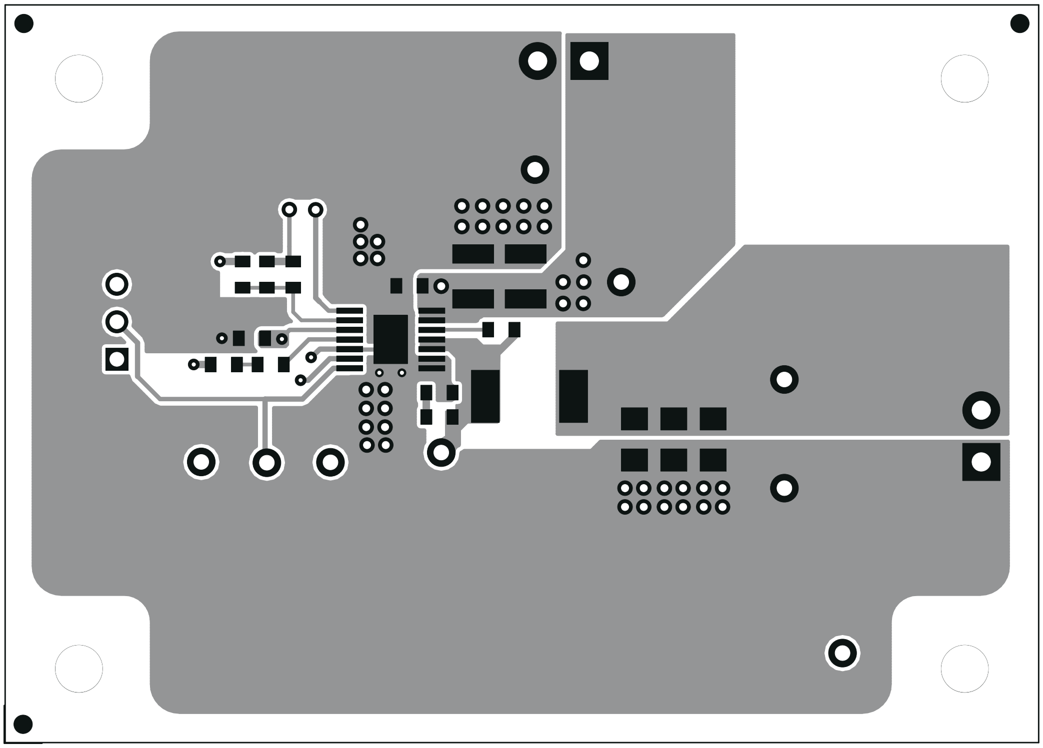

Figure 5-2. Top Layer

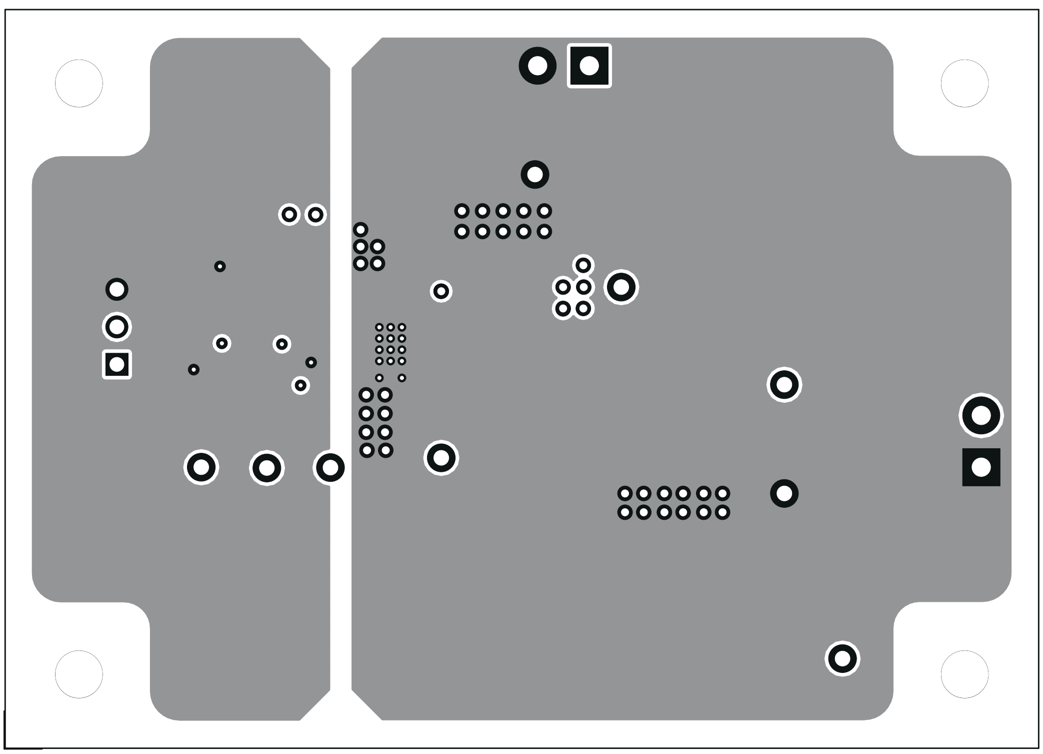

Figure 5-3. Internal Layer 1

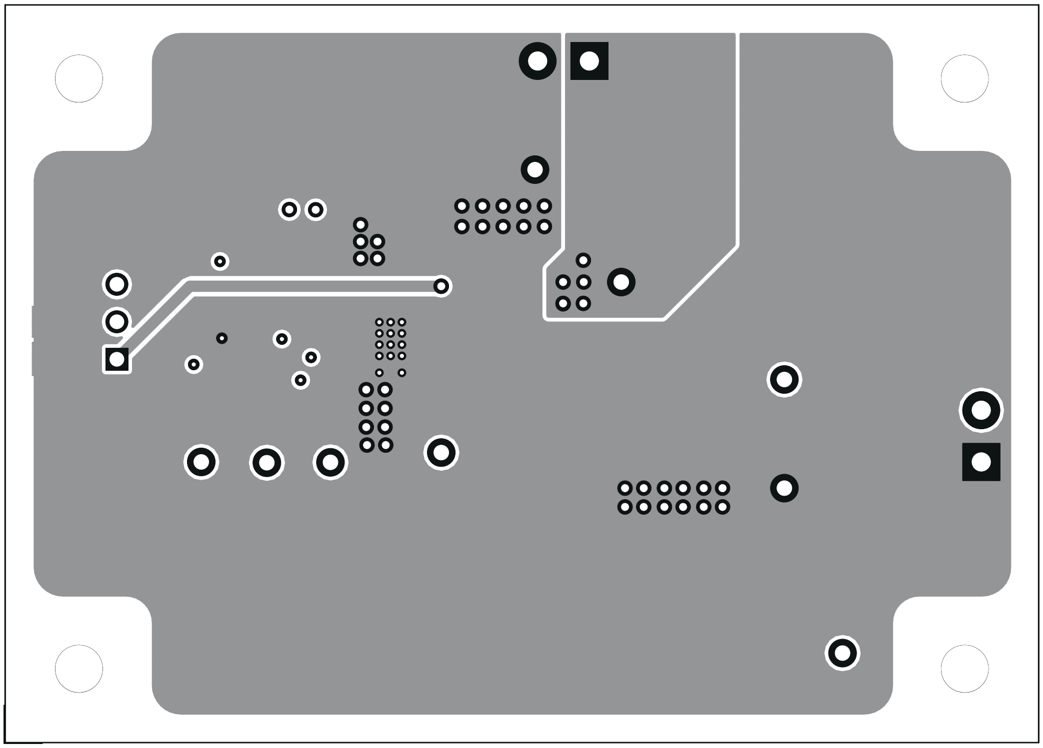

Figure 5-4. Internal Layer 2

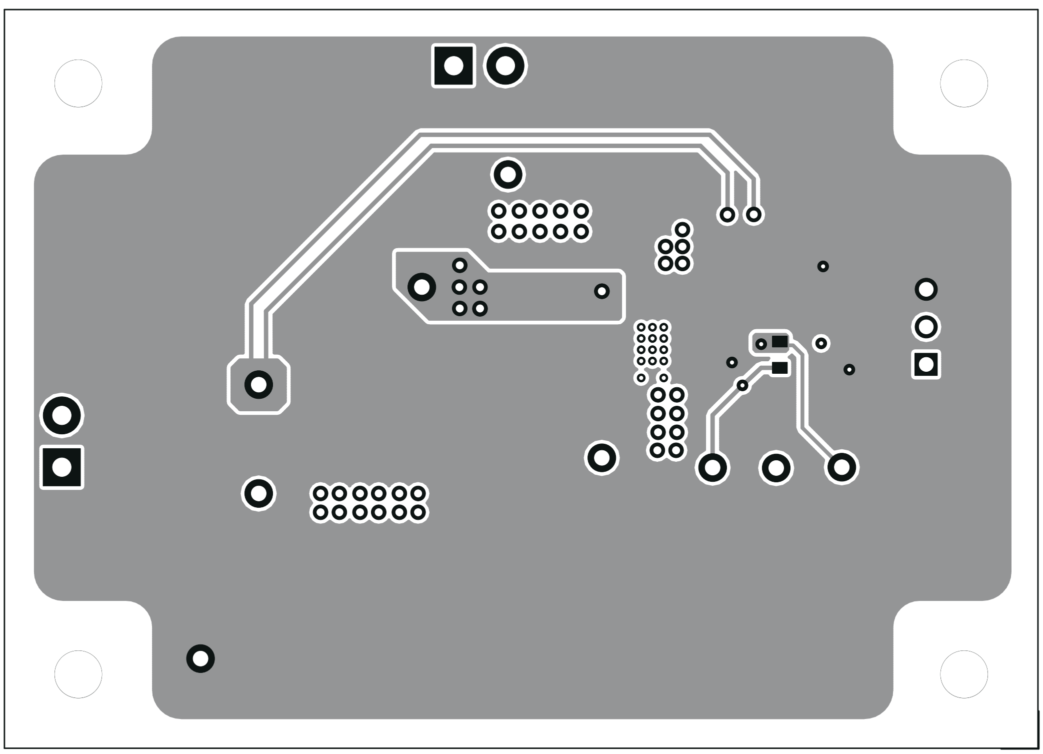

Figure 5-5. Bottom Layer

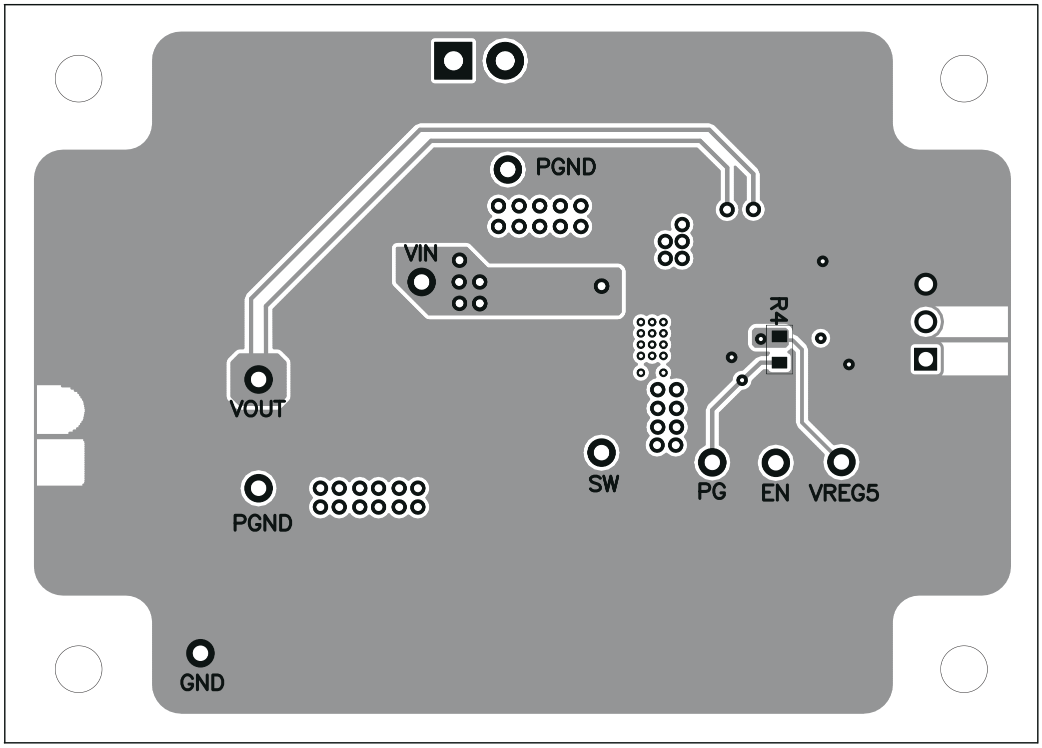

Figure 5-6. Bottom Assembly

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS54625EVM-538.

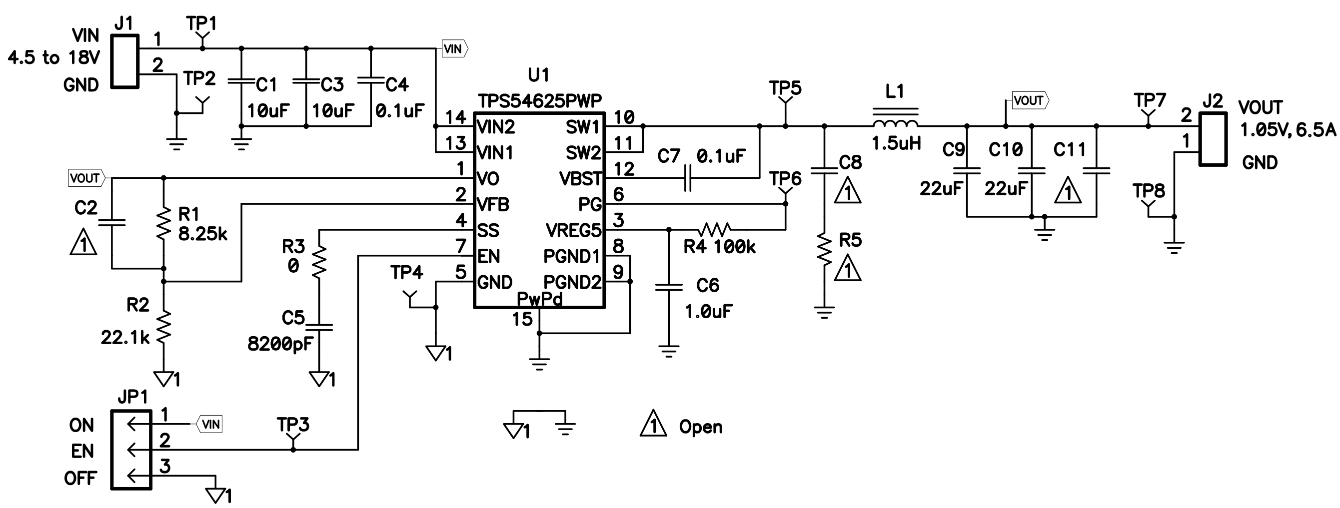

Figure 6-1. TPS54625EVM-608 Schematic Diagram

6.2 Bill of Materials

Table 6-1. Bill of Materials

RefDes	QTY	Value	Description	Size	Part Number	MFR
C1, C3	2	10 µF	Capacitor, ceramic, 25 V, X5R, 20%	1210	C3225X5R1E106M	TDK
C11	0	Open	Capacitor, ceramic	1206	Std	Std
C2, C8	0	Open	Capacitor, ceramic	0603	Std	Std
C5	1	8200 pF	Capacitor, ceramic, 25 V, X7R , 10%	0603	Std	Std
C6	1	1.0 µF	Capacitor, ceramic, 16 V, X7R, 10%	0603	Std	Std
C4, C7	1	0.1 µF	Capacitor, ceramic, 50 V, X7R, 10%	0603	Std	Std
C9, C10	2	22 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	1206	C3216X5R0J226M	TDK
J1, J2	2	ED555/2DS	Terminal block, 2-pin, 6 A, 3.5 mm	0.27 × 0.25 in	ED555/2DS	Sullins
JP1	1	PEC03SAAN	Header, male 3-pin, 100 mil spacing	0.100 in × 3	PEC03SAAN	Sullins
L1	1	1.5 µH	Inductor, SMT, 11 A, 9.7 mΩ	0.256 × 0.280 in	SPM6530T-1R5M100	TDK
R1	1	8.25 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
R2	1	22.1 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
R3	1	0 Ω	Resistor, chip, 1/16W, 1%	0603	Std	Std
R4	1	100 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
R5	0	Open	Resistor, chip, 1/16W, 1%	0603	Std	Std
TP1, TP3, TP4, TP6, TP7, TP8, TP9	3	5000	Test point, red, thru hole color keyed	0.100 × 0.100 in	5000	Keystone
TP2, TP5, TP9	3	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 in	5001	Keystone
U1	1	TPS54625PWP	IC, 6.5-A output single sync. step-down converter		TPS54625PWP	TI
–	1		Shunt, 100 mil, black	0.100	929950-00	3M
–	1		PCB, 2.76 in × 1.97 in × 0.062 in		HPA608	Any

6.3 Reference

Texas Instruments, *TPS54625, 4.5V to 18V Input, 6.5-A Synchronous Step-Down Converter Data Sheet*

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2013) to Revision A (August 2021) **Page**

- Updated user's guide title... 3
- Updated the numbering format for tables, figures, and cross-references throughout the document. 3

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