

# Use of Flash Test Pins on TMSx70 F035 Devices

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## ABSTRACT

Texas Instruments TMSx70 microcontrollers built using TI's F035 Flash process have one or two test pins used for advanced testing of the Flash memory. This application report discusses how to utilize these pins when designing circuit boards for one of these processors.

## Contents

1	Introduction .....	1
2	Flash Test Pins .....	1

## 1 Introduction

TI's F035 microcontrollers have two test pads used for testing the Flash memory: FLTP1 and FLTP2. FLTP1 is also available as a pin on the device. FLTP2 may be available as a pin, but may only exist as a pad on the die. In the device-specific data sheet, these pins will be listed as:

*For proper operation this pin must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event.*

Or, on older data sheets the note will be:

*For proper operation, this pin must not be connected [no connect (NC)].*

## 2 Flash Test Pins

When designing a circuit board, the simplest implementation is to not connect these two pins, to leave them as no-connects. While this is acceptable, it might make it difficult to properly verify custom Flash programming tools.

The Flash test points are analog pins connected through a pass-gate transistor to the Flash pump or bank. In non-test modes, the pass-gates are off and the pins are electrically isolated. In some test modes the pins are outputs, allowing TI to measure internal voltages or currents used to program or erase the Flash. In other test modes the pins are inputs and can be used to measure the voltage threshold level of a programmed or erased Flash cell.

When a customer creates their own tool to program or erase Flash using TI's Flash API, TI validates that tool by measuring the levels on the Flash cells and comparing it to the levels created by using a known tool such as TI's FLASH470 or nowFlash™. Because moving the device from one board to another can slightly affect the levels achieved during program and erase, it is best to do this comparison using both tools on the same circuit board. Access to the IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) pins and FLTP1 is required to perform these measurements. Access to FLTP1 can be achieved with a *bed-of-nails* fixture, or by creating a test pad to which a wire can be soldered. No other components should be connected to this test pad. Having access to the JTAG pins and FLTP1 can be very useful in performing initial debug of returns suspected of having Flash failures.

Because the Flash test pins are required to handle voltages up to 10 V, they can not have the same electro-static discharge (ESD) structures as the device I/O pins. This makes these pins more sensitive to damage from an ESD event. To minimize this risk, the Flash test points should not be routed to any connector that is exposed in the final product. A test point on the circuit board that can only be accessed after removing the product's cover is a good solution. Routing the Flash test point to a connector that attaches to a wiring harness is not a good solution.

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