

These assemblies are ESD sensitive, ESD precautions shall be observed. Use of no clean flux is not acceptable. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable. These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Layer 1 - Top Layer	Copper	1.40mil		
4	Dielectric 1	370HR	5.20mil	4.2	
5	Layer 2 - GND	Copper	1.42mil		
6	Dielectric 2	370HR	43.00mil	4.2	
7	Layer 3 - PWR	Copper	1.42mil		
8	Dielectric 3	370HR	5.20mil	4.2	
9	Layer 4 - Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 20 MIL
 MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-408 FR-4 High Tg OTHER
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:

REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:

SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 100% TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL:

CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

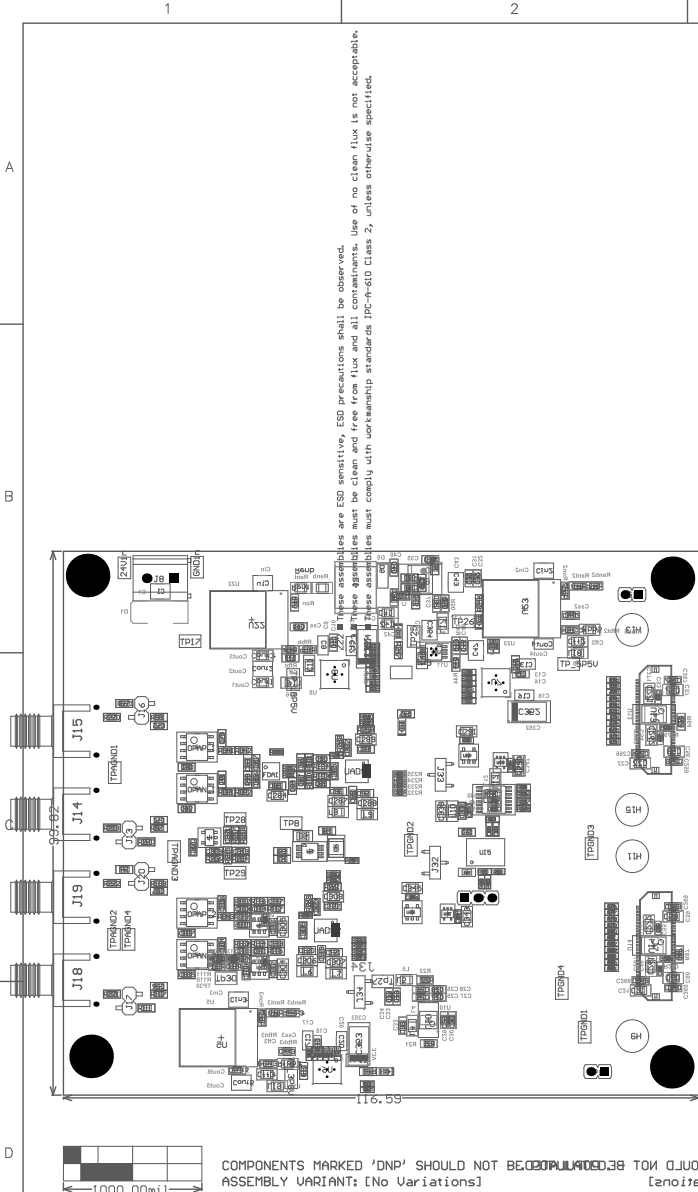
ADDITIONAL REQUIREMENTS:

MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER



PROJECT TITLE:
 OPA625 ADC Driver
 DESIGNED FOR:
 Public Release
 FILE NAME:
 OPA625 ADC Driver.PcbDoc

PCB NAME: TIDA-01050-01 LAYER NAME: Top Layer PLOT NAME: TIDA-01050-01_Top Layer	BOARD #: TID #: DATE:	PART #: QTY:	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: Taras Dudar SCALE: 1.00	ALTIM DESIGNER VERSION: 16.1.12.290
--	-----------------------------	-----------------	--	---	--



These assemblies are ESD sensitive, ESD precautions shall be observed. Use of no clean flux is not acceptable. Use of no clean flux must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable. These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ADDITIONAL COMMENTS:	13	BOARD #0201A0105GH	DATE:	EI	SUN 30 2010 10:30:00 AM
LAYER NAME =	13	TID #:	01068010	#	D1T
PLotted in File: Layer 2 - GND Assembly	13	GENERATED: 11:22:13 11/23/10	13	13	13

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Layer 1 - Top Layer	Copper	1.40mil		
4	Dielectric 1	370HR	5.20mil	4.2	
5	Layer 2 - GND	Copper	1.42mil		
6	Dielectric 2	370HR	43.00mil	4.2	
7	Layer 3 - PWR	Copper	1.42mil		
8	Dielectric 3	370HR	5.20mil	4.2	
9	Layer 4 - Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 20 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-408 FR-4 High Tg OTHER
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:

REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:

SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 100% TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

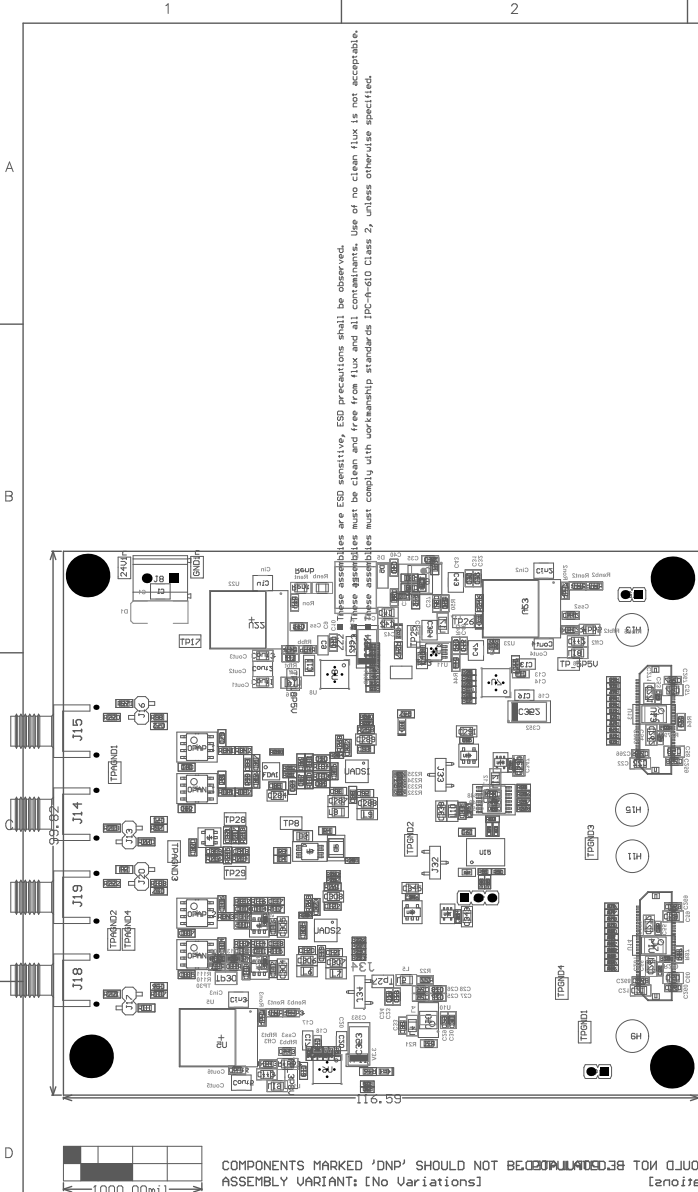
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94-V0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER



TEXAS INSTRUMENTS	
PROJECT TITLE: OPA625 ADC Driver	
DESIGNED FOR: Public Release	
FILE NAME: OPA625 ADC Driver.PcbDoc	
ENGINEER: Taras Dudar	ALTIUM DESIGNER VERSION: 16.1.12.230
SCALE: 1.00	



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Layer 1 - Top Layer	Copper	1.40mil		
4	Dielectric 1	370HR	5.20mil	4.2	
5	Layer 2 - GND	Copper	1.42mil		
6	Dielectric 2	370HR	43.00mil	4.2	
7	Layer 3 - PWR	Copper	1.42mil		
8	Dielectric 3	370HR	5.20mil	4.2	
9	Layer 4 - Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 20 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL:
 CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94-V0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER



PROJECT TITLE:
OPA625 ADC Driver

DESIGNED FOR:
Public Release

FILE NAME:
OPA625 ADC Driver.PcbDoc

ADDITIONAL INFORMATION: BOARD #0201A0105GH DATE: E1 SUN 3/28/10 10:08:31 AM

LAYER NAME = FRONT TID #: 01068010 :# 011

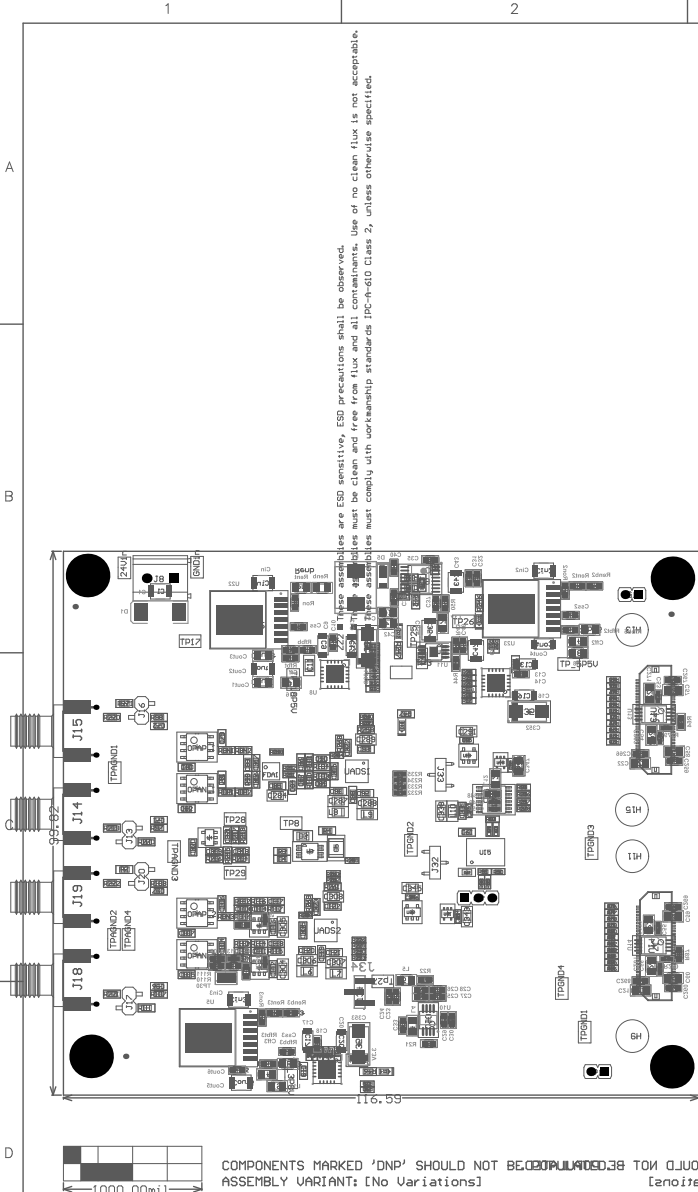
PLOTTED IN LAYER 3 - PARASITIC CAPACITORS GENERATED !! : 11/27/10 13:07:30 AM : TEXAS INSTRUMENTS LLP

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:
Taras Dudar

SCALE: 1.00

ALTIUM DESIGNER VERSION:
16.1.12.230



These assemblies are ESD sensitive, ESD precautions shall be observed. Use of no clean flux is not acceptable. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable. These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. TO ORDER, CONTACT THE MANUFACTURER.
 ASSEMBLY VARIANT: [No Variations]

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Layer 1 - Top Layer	Copper	1.40mil		
4	Dielectric 1	370HR	5.20mil	4.2	
5	Layer 2 - GND	Copper	1.42mil		
6	Dielectric 2	370HR	43.00mil	4.2	
7	Layer 3 - PWR	Copper	1.42mil		
8	Dielectric 3	370HR	5.20mil	4.2	
9	Layer 4 - Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 20 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL:
 CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER



PROJECT TITLE:
 OPA625 ADC Driver
 DESIGNED FOR:
 Public Release
 FILE NAME:
 OPA625 ADC Driver.PcbDoc

PCB LAYER NAME = Bottom Layer PLOT NAME = Bottom Layer	BOARD # 010501 TID #: 0106010 DATE: 11/20/11	ENGINEER: EI DESIGNED BY: Taras Dudar	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: Taras Dudar	SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.1.12.290
---	--	--	--	--------------------------	-------------	---

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated