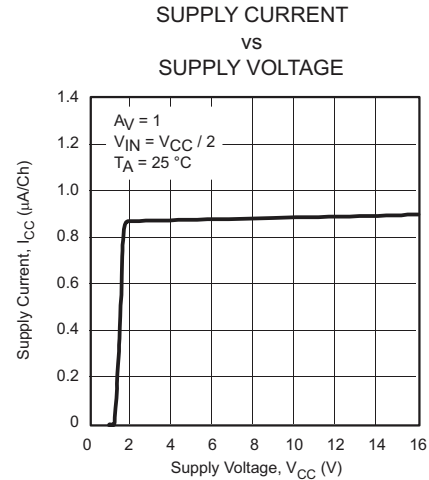


具有反向电池保护功能的每通道 **880 nA** 轨至轨输入/输出运算放大器产品系列

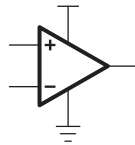
 查询样品: [TLV2401-Q1](#), [TLV2402-Q1](#), [TLV2404-Q1](#)

特性

- 符合汽车应用要求
- 低功耗工作...每通道不足 **1 μ A**
- 输入共模范围超过电轨... **-0.1 V** 至 **$V_{CC} + 5 V$**
- 反向电池保护高达 **18 V**
- 轨至轨输入/输出
- 增益带宽产品... **5.5 kHz**
- 电源电压范围... **2.5 V** 至 **16 V**
- 特定温度范围: **-40°C** 至 **125°C**
- 超小型封装
 - **5 引脚 SOT-23 (TLV2401-Q1)**
 - **8 引脚 MSOP (TLV2402-Q1)**
- 通用运算放大器 **EVM** (指 **EVM 选择指南 SLOU060**)



Operational Amplifier



说明 / 订购信息

TLV240x 系列单电源运算放大器支持当前最低的电源电流, 单位通道仅为 **880 nA**。逆向电池保护可在电池安装不当产生过大电流时保护放大器。在恶劣环境下, 输入电压可超过正电源轨 **5 V**, 不会损坏器件。

低电源电流与极低输入偏置电流相结合, 使其可用于 **mega-W** 电阻器, 是长时间工作便携式应用的理想选择。典型失调电压低至 **390 μ V**, **CMRR** 为 **120 dB**, **2.7 V** 时最小开环增益为 **130 V/mV**, 可确保 DC 准确度。

最大推荐电源电压高达 **16 V**, 低至 **2.5 V** 的电压也可确保工作, 电气特性电压指定为 **2.7 V**、**5 V** 及 **15 V**。**2.5 V** 电压工作使其兼容于锂离子电池供电系统以及当前提供的众多微功率微处理器, 其中包括德州仪器 (TI) 的 **MSP430**。

该系列旗下的所有产品均采用 **PDIP** 与 **SOIC** 封装, 单通道器件采用小型 **SOT-23** 封装, 双通道器件采用 **MSOP** 封装, 四通道产品采用 **TSSOP** 封装。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



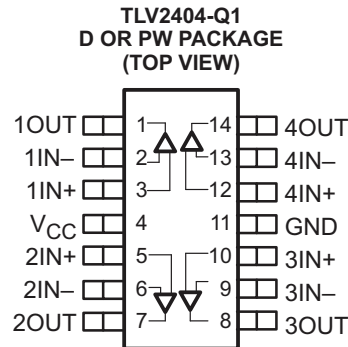
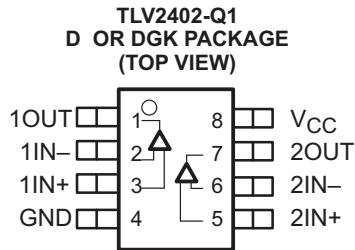
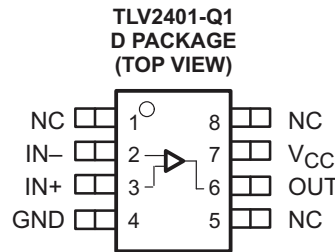
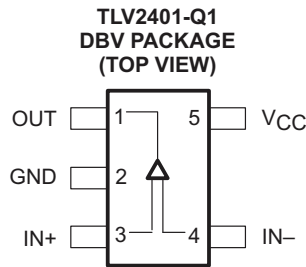
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS⁽¹⁾⁽²⁾

DEVICE	V _{CC} (V)	V _{IO} (mV)	BW (MHz)	SLEW RATE (V/μs)	I _{CC/ch} (μA)	RAIL-TO-RAIL
TLV240x-Q1 ⁽²⁾	2.5–16	0.390	0.005	0.002	0.880	I/O

- (1) All specifications are typical values measured at 5 V.
- (2) This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.

DEVICE INFORMATION



NC – No internal connection

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	MSOP – DGK	Reel of 2500	TLV2402QDQGRQ1	QWX
	SOIC – D	Reel of 2500	TLV2401QDRQ1	Product Preview
			TLV2402QDRQ1	
			TLV2404QDRQ1	
SOT – DBV	Reel of 3000	TLV2401QDBVRQ1	Product Preview	
TSSOP – PW	Reel of 2000	TLV2404QPWRQ1	Product Preview	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		17	V
V _{ID}	Differential input voltage range		±20	V
I _I	Input current range (any input)		±10	mA
I _O	Output current range		±10	mA
Continuous total power dissipation		See Dissipation Ratings Table		
T _A	Operating free-air temperature range	–40	125	°C
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	–60	125	°C
ESD	Electrostatic discharge ⁽³⁾	Human-Body Model (HBM)		500
		Machine Model (MM)		200
		Field-Induced-Charged Device Model (CDM)		1000
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.
- (3) Tested in accordance with AEC-Q100.

DISSIPATION RATINGS

PACKAGE	Q _{JC} (°C/W)	Q _{JA} (°C/W)	T _A ≤ 25°C POWER RATING	T _A = 125°C POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
PW (14)	29.3	173.6	720 mW	144 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Single supply	2.5	16
		Split supply	±1.25	±8
V _{ICR}	Common-mode input voltage range	–0.1	V _{CC} +5	V
T _A	Operating free-air temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS
DC Performance

V_{CC} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT	
DC Performance									
V _{IO}	Input offset voltage	V _O = V _{CC} /2 V, V _{IC} = V _{CC} /2 V, R _S = 50 Ω		25°C	390	1900		μV	
				Full range		2800			
αV _{IO}	Offset voltage draft			25°C		3		μV/°C	
CMRR	Common mode rejection ratio	V _{IC} = 0 to V _{CC} , R _S = 50 Ω		V _{CC} = 2.7 V		25°C	60	120	dB
				Full range			56		
				V _{CC} = 5 V		25°C	65	120	
				Full range			58		
				V _{CC} = 15 V		25°C	73	120	
				Full range			73		
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 2.7 V, V _{O(pp)} = 1 V, R _L = 500 kΩ		25°C	130	400		V/mV	
				Full range		12			
		V _{CC} = 5 V, V _{O(pp)} = 3 V, R _L = 500 kΩ		25°C	300	1000			
				Full range		37			
		V _{CC} = 15 V, V _{O(pp)} = 6 V, R _L = 500 kΩ		25°C	1000	1800			
				Full range		66			
Input Characteristics									
I _{IO}	Input offset current	V _O = V _{CC} /2 V, V _{IC} = V _{CC} /2 V, R _S = 50 Ω		25°C	25	250		pA	
				Full range		400			
I _{IB}	Input bias current	V _O = V _{CC} /2 V, V _{IC} = V _{CC} /2 V, R _S = 50 Ω		25°C	100	300		pA	
				Full range		900			
r _{i(d)}	Differential input resistance			25°C	300			MΩ	
C _{i(c)}	Common-mode input capacitance	f = 100 kHz		25°C	3			pF	

**ELECTRICAL CHARACTERISTICS
DC Performance (continued)**
 $V_{CC} = 2.7\text{ V}, 5\text{ V}, \text{ and } 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
Output Characteristics								
V_{OH}	High-level output voltage	$V_{IC} = V_{CC}/2,$ $I_{OH} = -2\ \mu\text{A}$	$V_{CC} = 2.7\text{ V}$	25°C	2.65	2.68	V	
				Full range	2.63			
			$V_{CC} = 5\text{ V}$	25°C	4.95	4.98		
				Full range	4.93			
			$V_{CC} = 15\text{ V}$	25°C	14.95	14.98		
				Full range	14.93			
		$V_{IC} = V_{CC}/2,$ $I_{OH} = -50\ \mu\text{A}$	$V_{CC} = 2.7\text{ V}$	25°C	2.62	2.65		
				Full range	2.6			
			$V_{CC} = 5\text{ V}$	25°C	4.92	4.95		
				Full range	4.9			
			$V_{CC} = 15\text{ V}$	25°C	14.92	14.95		
				Full range	14.9			
V_{OL}	Low-level output voltage	$V_{IC} = V_{CC}/2, I_{OL} = 2\ \mu\text{A}$	25°C	90	150	mV		
			Full range	180				
		$V_{IC} = V_{CC}/2, I_{OL} = 50\ \mu\text{A}$	25°C	180	230			
			Full range	260				
I_O	Output current	$V_O = 0.5\text{ V}$ from rail		25°C	±200		μA	
Power Supply								
I_{CC}	Supply current (per channel)	$V_O = V_{CC}/2$	$V_{CC} = 2.7\text{ V}$ or 5 V	25°C	880	990	nA	
				Full range	1300			
			$V_{CC} = 15\text{ V}$	25°C	900	1050		
				Full range	1400			
Reverse supply current		$V_{CC} = -18\text{ V}, V_{IN} = 0\text{ V}, V_O = \text{Open circuit}$		25°C	50		nA	
PSRR	Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		$V_{CC} = 2.7\text{ V}$ or $5\text{ V}, V_{IC} = V_{CC}/2, \text{ No load}$	25°C	100	120	dB	
				Full range	83			
			$V_{CC} = 5$ to $15\text{ V}, V_{IC} = V_{CC}/2, \text{ No load}$	25°C	100	120	dB	
				Full range	97			
Dynamic Performance								
UGBW	Unity gain bandwidth	$R_L = 500\text{ k}\Omega, C_L = 100\text{ pF}$		25°C	5.5		kHz	
SR	Slew rate at unity gain			25°C	2.5		V/ms	
ϕ_M	Phase margin	$R_L = 500\text{ k}\Omega, C_L = 100\text{ pF}$		25°C	60°		dB	
	Gain margin				15			
t_S	Settling time	$V_{CC} = 2.7\text{ V}$ or $5\text{ V},$ $V_{(\text{STEP})\text{PP}} = 1\text{ V},$ $A_V = -1,$	$C_L = 100\text{ pF}$ $R_L = 100\text{ k}\Omega$	0.1%	25°C	1.84		ms
			$V_{CC} = 15\text{ V},$ $V_{(\text{STEP})\text{PP}} = 1\text{ V},$ $A_V = -1,$	$C_L = 100\text{ pF}$ $R_L = 100\text{ k}\Omega$		0.1%	6.1	
				0.01%		32		

ELECTRICAL CHARACTERISTICS
DC Performance (continued)

V_{CC} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
Noise/Distortion Performance							
V _n	Equivalent input noise voltage	f = 10 Hz	25°C	800			nV/√Hz
		f = 100 Hz		500			
I _n	Equivalent input noise current	f = 100 Hz		8			fA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input Offset Voltage	vs Common-mode input voltage	Figure 1 , Figure 2 , Figure 3
I_{IB}	Input Bias Current	vs Free-air temperature	Figure 4 , Figure 6 , Figure 8
		vs Common-mode input voltage	Figure 5 , Figure 7 , Figure 9
I_{IO}	Input Offset Current	vs Free-air temperature	Figure 4 , Figure 6 , Figure 8
		vs Common-mode input voltage	Figure 5 , Figure 7 , Figure 9
CMRR	Common-mode rejection ratio	vs Frequency	Figure 10
V_{OH}	High-level output voltage	vs High-level output current	Figure 11 , Figure 13 , Figure 15
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 12 , Figure 14 , Figure 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	Figure 17
Z_o	Output impedance	vs Frequency	Figure 18
I_{CC}	Supply current	vs Supply voltage	Figure 19
PSRR	Power supply rejection ratio	vs Frequency	Figure 20
A_{VD}	Differential voltage gain	vs Frequency	Figure 21
	Phase	vs Frequency	Figure 21
	Gain-bandwidth product	vs Supply voltage	Figure 22
	SR Slew rate	vs Free-air temperature	Figure 23
ϕ_m	Phase margin	vs Capacitive load	Figure 24
	Gain margin	vs Capacitive load	Figure 25
	Supply current	vs Reverse voltage	Figure 26
	Voltage noise over a 10 Second Period		Figure 27
	Large signal follower pulse response		Figure 28 , Figure 29 , Figure 30
	Small signal follower pulse response		Figure 31
	Large signal inverting pulse response		Figure 32 , Figure 33 , Figure 34
	Small signal inverting pulse response		Figure 35
	Crosstalk	vs Frequency	Figure 36

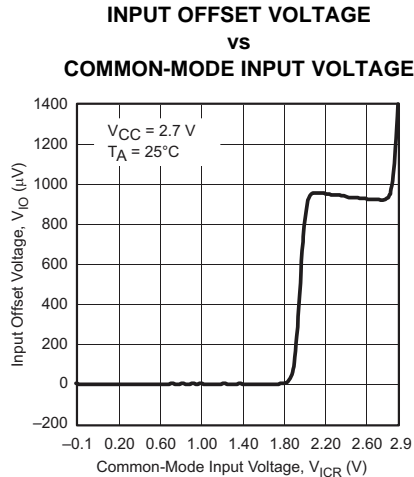


Figure 1.

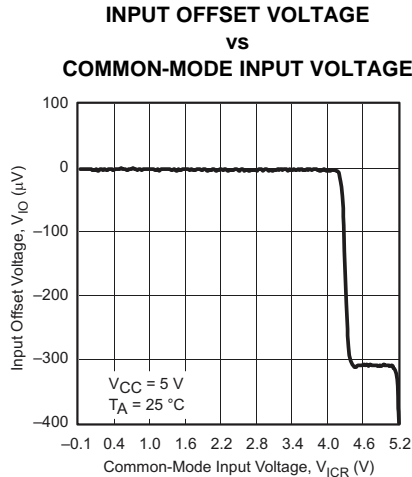


Figure 2.

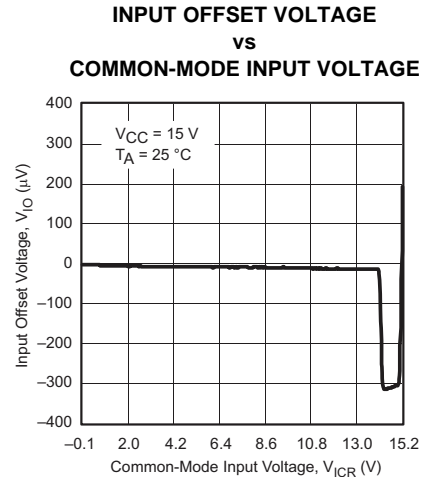


Figure 3.

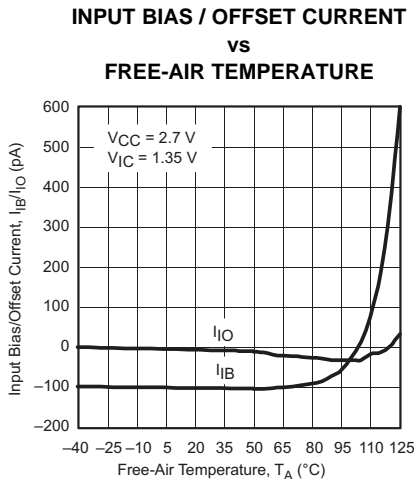


Figure 4.

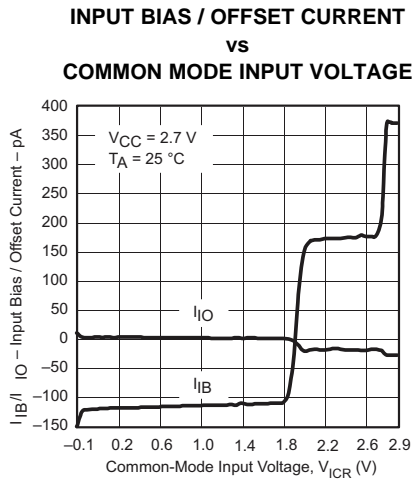


Figure 5.

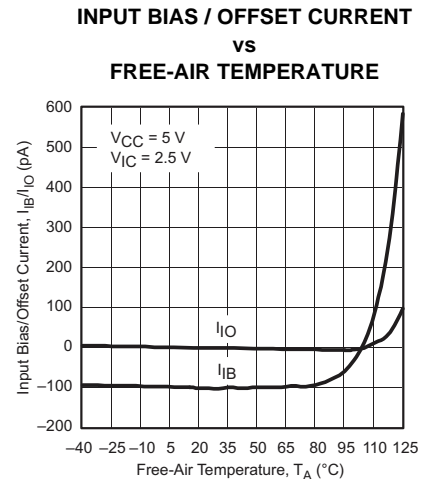


Figure 6.

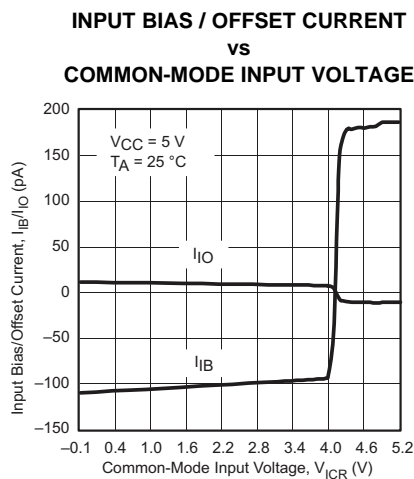


Figure 7.

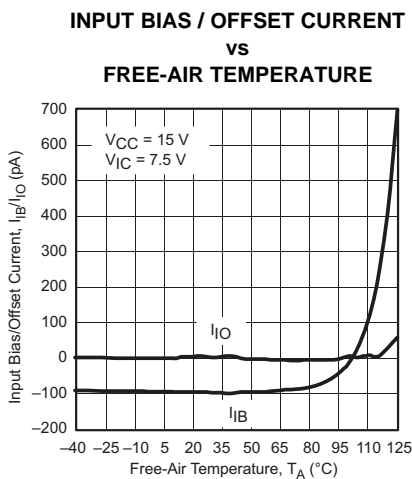


Figure 8.

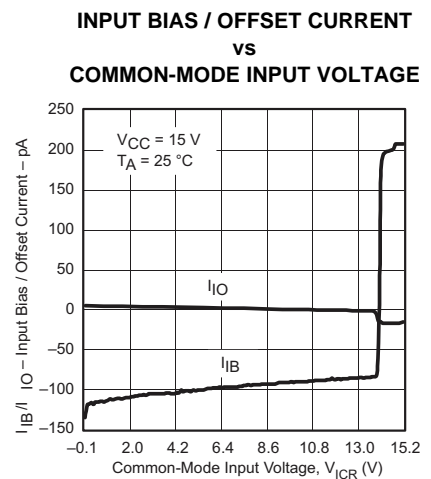


Figure 9.

**COMMON-MODE REJECTION RATIO
vs
FREQUENCY**

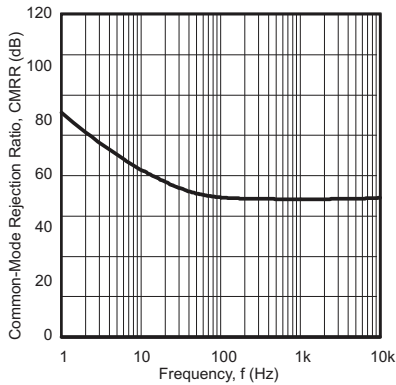


Figure 10.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

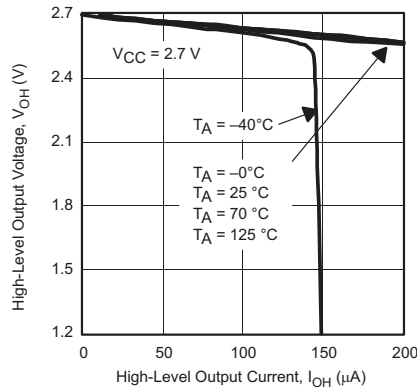


Figure 11.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

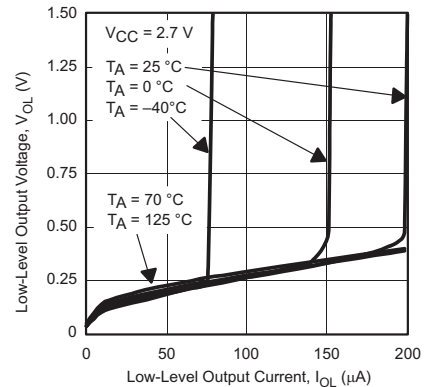


Figure 12.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

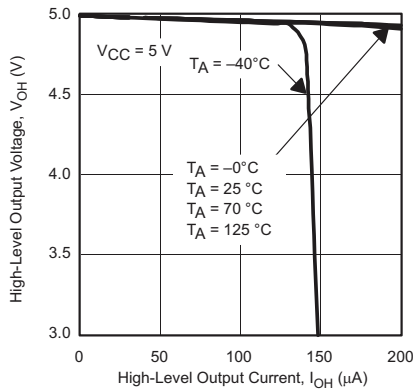


Figure 13.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

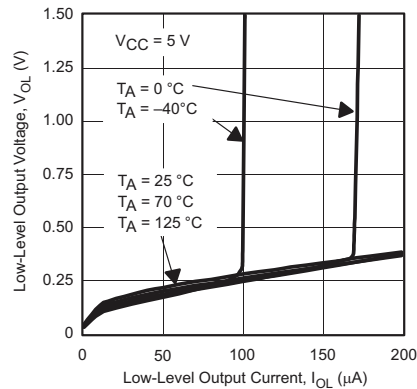


Figure 14.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

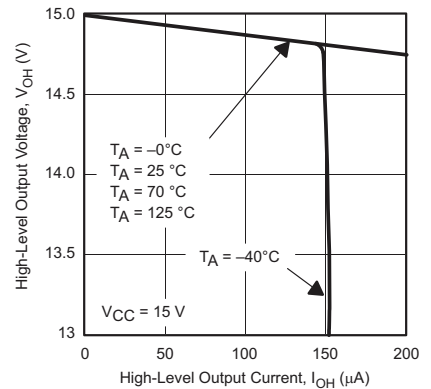


Figure 15.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

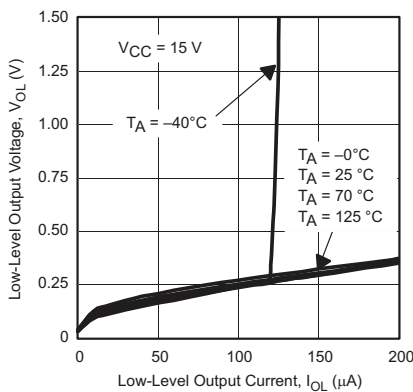


Figure 16.

**OUTPUT VOLTAGE PEAK-TO-PEAK
vs
FREQUENCY**

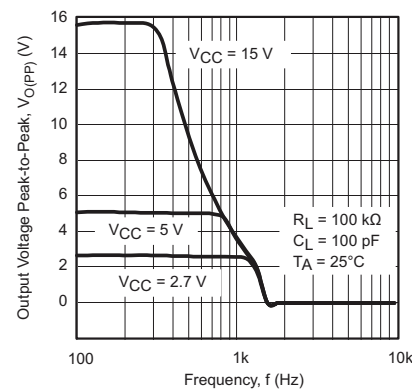


Figure 17.

**OUTPUT IMPEDANCE
vs
FREQUENCY**

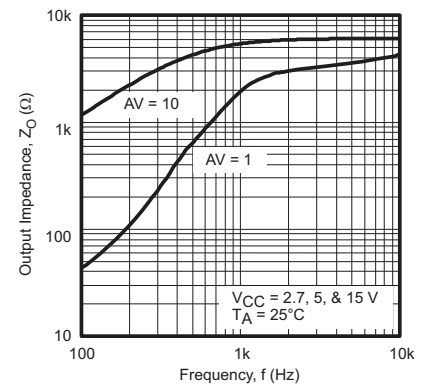


Figure 18.

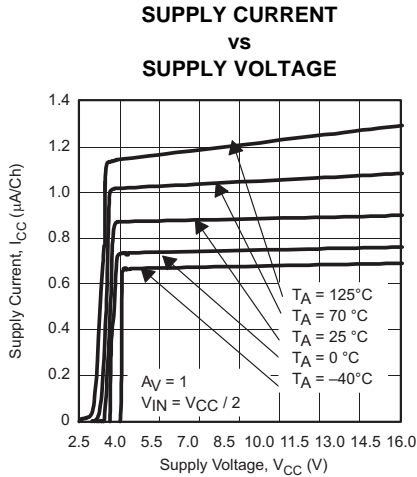


Figure 19.

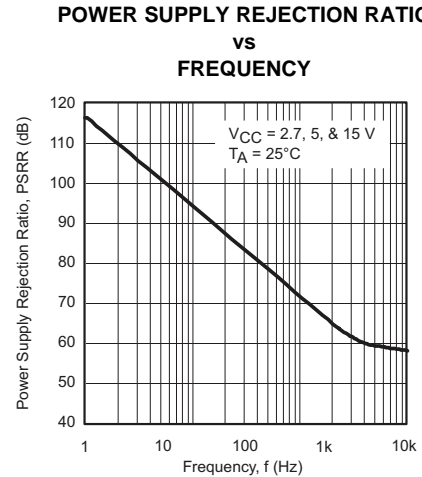


Figure 20.

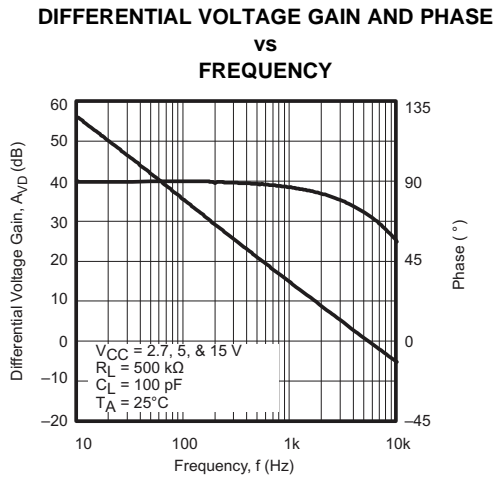


Figure 21.

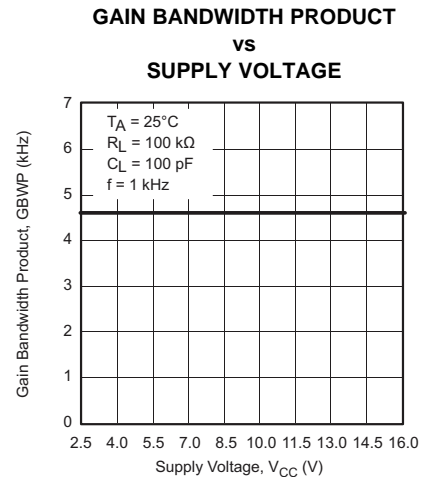


Figure 22.

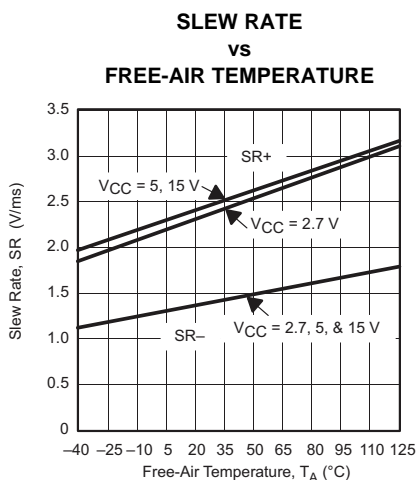


Figure 23.

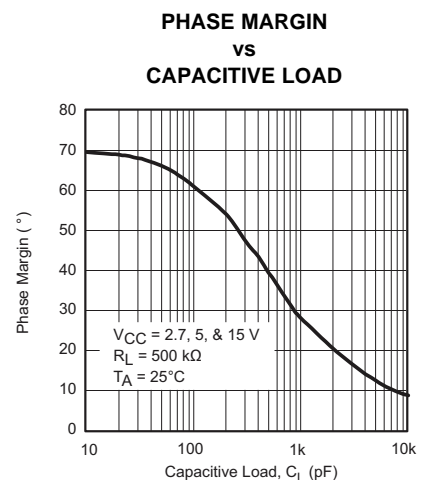


Figure 24.

**GAIN MARGIN
vs
CAPACITIVE LOAD**

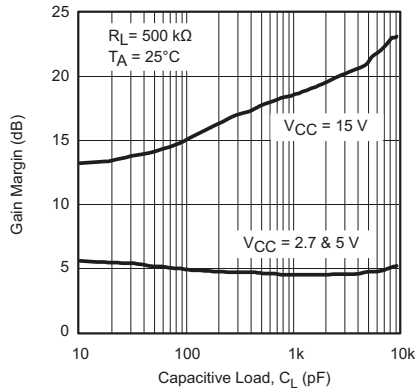


Figure 25.

**SUPPLY CURRENT
vs
REVERSE VOLTAGE**

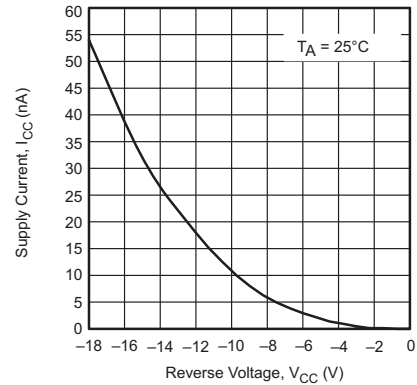


Figure 26.

**VOLTAGE NOISE
OVER A 10 SECOND PERIOD**

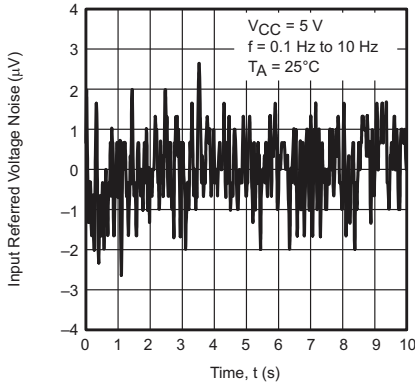


Figure 27.

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE**

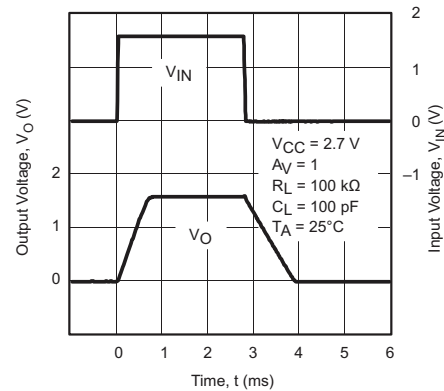


Figure 28.

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE**

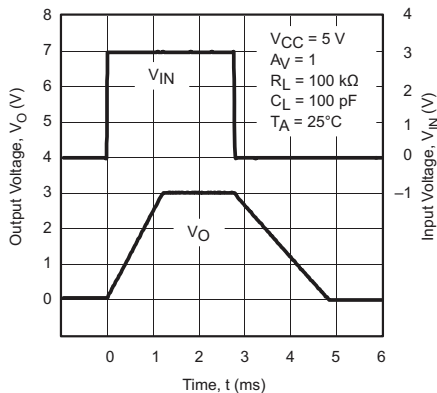


Figure 29.

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE**

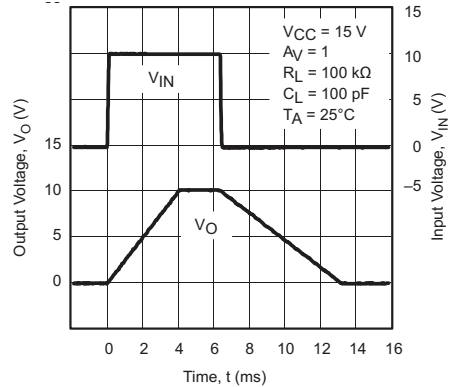


Figure 30.

**SMALL SIGNAL FOLLOWER
PULSE RESPONSE**

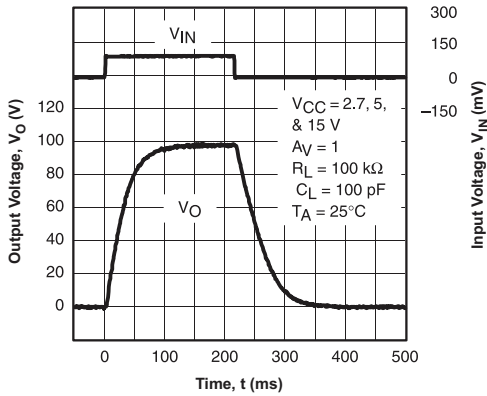


Figure 31.

**LARGE SIGNAL INVERTING
PULSE RESPONSE**

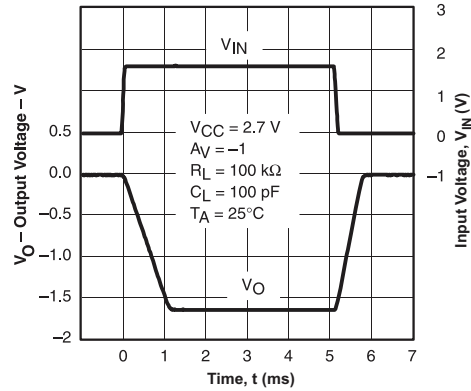


Figure 32.

**LARGE SIGNAL INVERTING
PULSE RESPONSE**

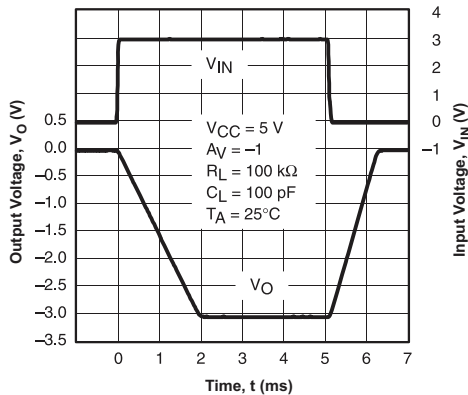


Figure 33.

**LARGE SIGNAL INVERTING
PULSE RESPONSE**

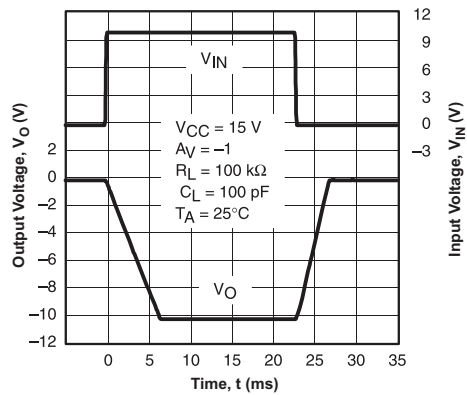


Figure 34.

**SMALL SIGNAL INVERTING
PULSE RESPONSE**

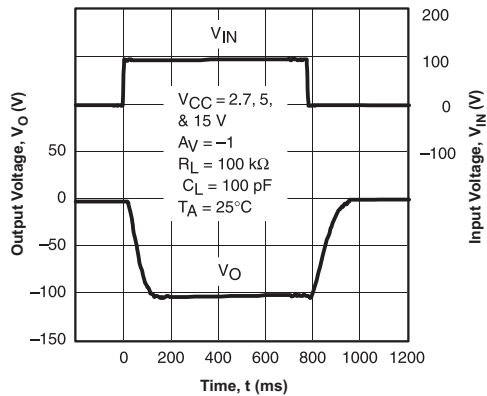


Figure 35.

**CROSSTALK
vs
FREQUENCY**

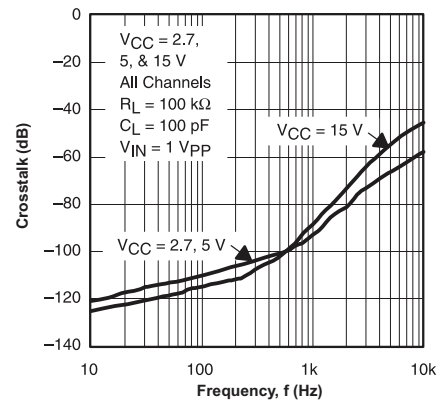


Figure 36.

APPLICATION INFORMATION

Reverse Battery Protection

The TLV240x-Q1 are protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of 6 Schottky diodes and will therefore increase as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure will turn on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

Common-Mode Input Range

The TLV240x-Q1 has rail-to-rail input and outputs. For common-mode inputs from -0.1 V to $V_{CC} - 0.8\text{ V}$ a PNP differential pair will provide the gain.

For inputs between $V_{CC} - 0.8\text{ V}$ and V_{CC} , two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails, because as the inputs go above V_{CC} , the NPNs switch from functioning as transistors to functioning as diodes. This will lead to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC} .

The TLV240x-Q1 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain will be observed with the ultimate possibility of phase inversion.

Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

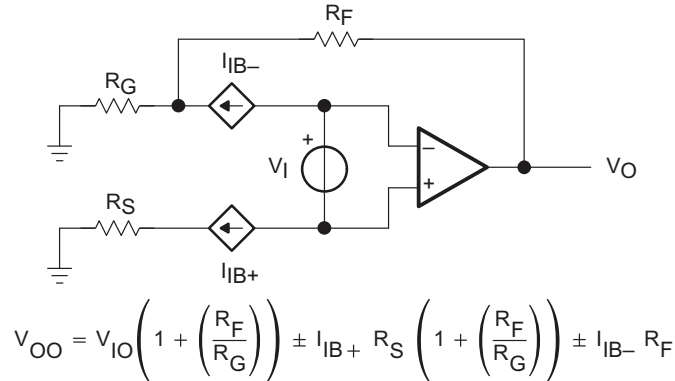


Figure 37. Output Offset Voltage Model

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 38).

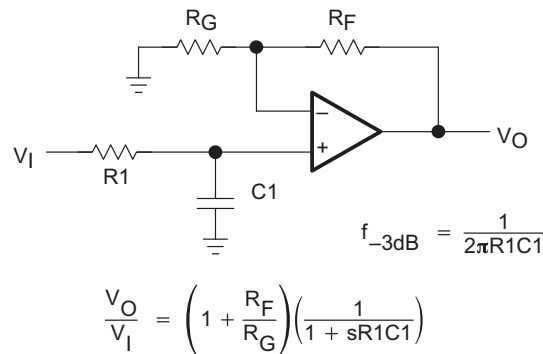


Figure 38. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

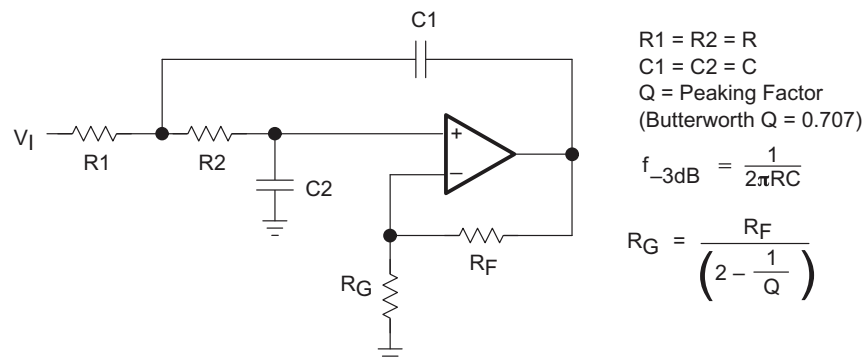


Figure 39. 2-Pole Low-Pass Sallen-Key Filter

Circuit Layout Considerations

To achieve the levels of high performance of the TLV240x-Q1, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-mF tantalum capacitor in parallel with a 0.1-mF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-mF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-mF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

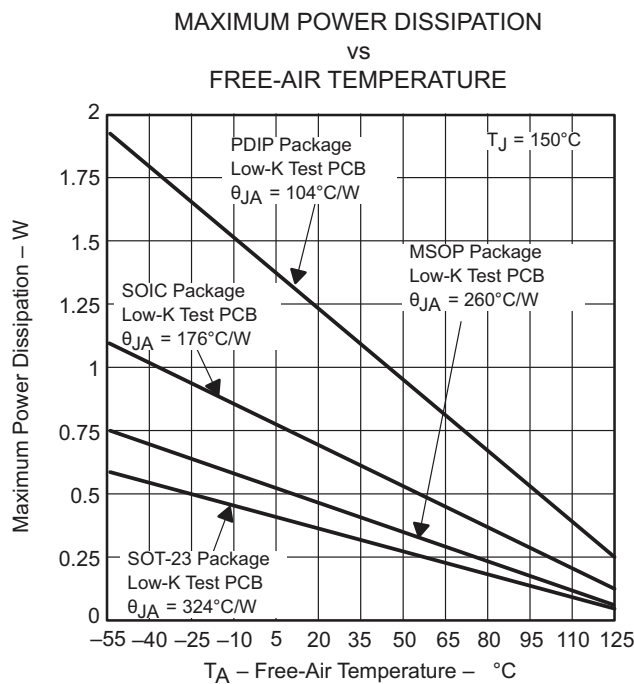
General Power Dissipation Considerations

For a given θ_{JA} , the maximum power dissipation is shown in [Figure 40](#) and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- PD = Maximum power dissipation of THS240x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



(1) Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 40. Maximum Power Dissipation vs Free-Air Temperature

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2401QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1WU9
TLV2401QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WU9
TLV2402QDQGRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWX
TLV2402QDQGRQ1.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWX

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV2401-Q1, TLV2402-Q1 :

- Catalog : [TLV2401](#), [TLV2402](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

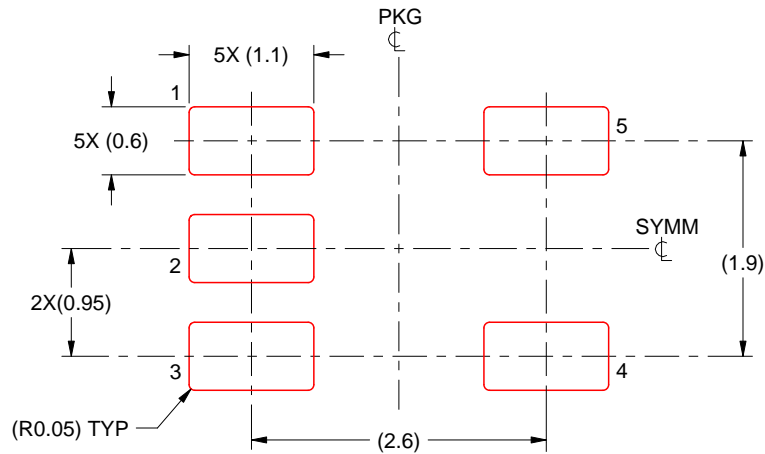
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

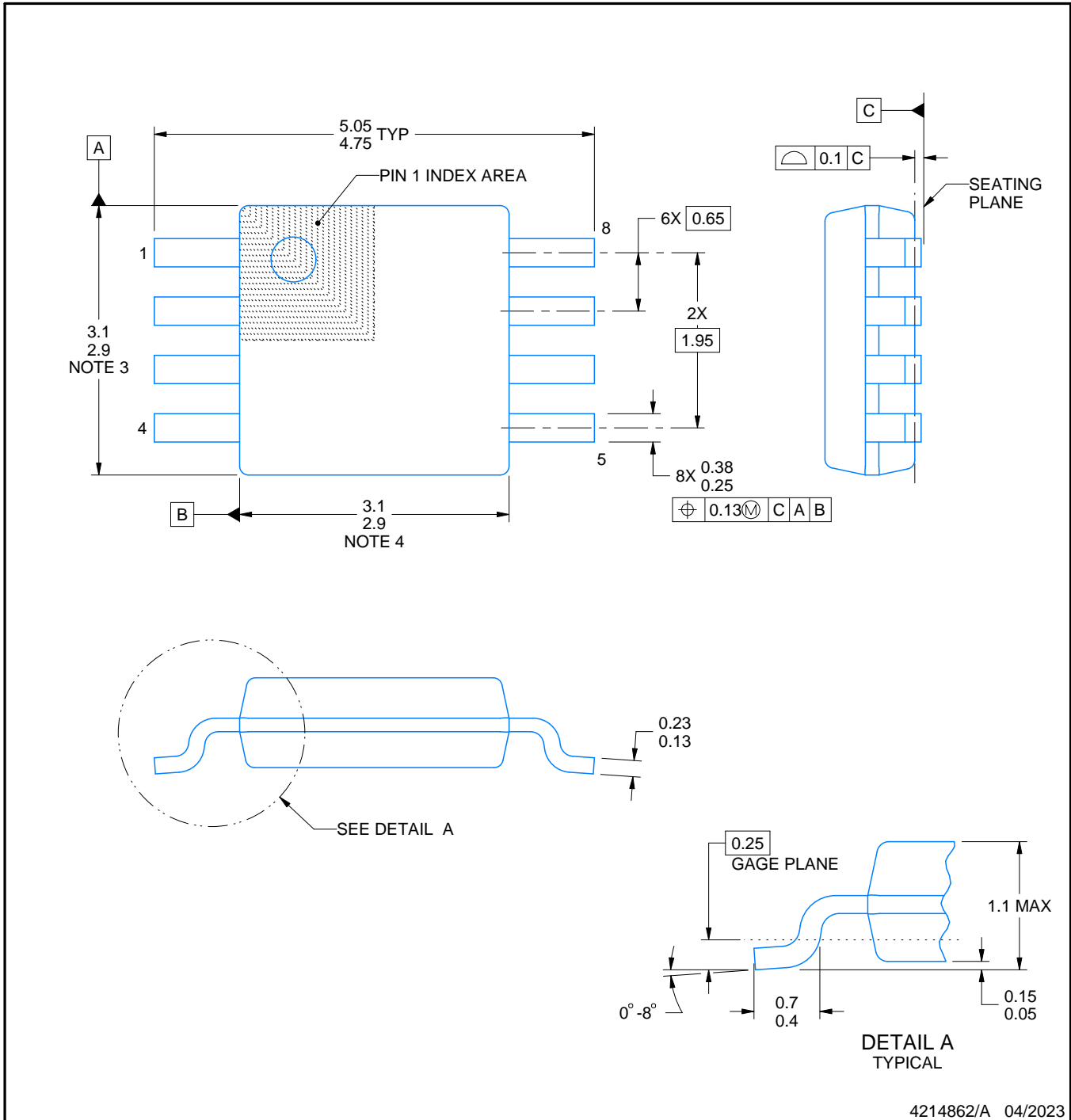
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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