

2V_{RMS} DirectPath™, 具有 32 位, 384kHz 脉冲编码调制 (PCM) 接口的 112/106/100dB 音频立体声数模转换器 (DAC)

查询样品: [PCM5100-Q1 \(Preliminary\)](#), [PCM5101-Q1 \(Preliminary\)](#), [PCM5102-Q1](#)

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果:
 - 器件温度 2 级: -40°C 至 105°C 的环境运行温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 **H2**
 - 器件充电器件模型 (CDM) ESD 分类等级 **C3B**
- 市场领先的低带外噪声
- 可选数字滤波器延迟与性能
- 无需隔离直流电流的电容器
- 集成的负电荷泵
- 用于采样率变化或者时钟暂停的内部无爆音控制
- 智能静噪系统: 针对带有无爆音操作 **120dB** 静噪信噪比 (SNR) 的上升/下降斜坡和模拟静噪。
- 具有对于内部生成 **SCK** 的 **BCK** 基准的集成高性能音频锁相环路 (PLL)
- 小型**20-pin** TSSOP封装

典型性能 (电源为 3.3V 时)

参数	PCM5102-Q1/PCM5101-Q1/PCM5100-Q1
SNR	112/106/100dB
动态范围	112/106/100dB
-1dBFS 上的总谐波失真 (THD)+D	-93/-92/-90dB
满量程输出	2.1V _{RMS} (中心接地 (GND))
正常 8x 过采样数字滤波器延迟:	22 / f _S
低延迟 8x 过采样数字滤波器延迟:	3.5 / f _S
采样频率	8kHz 至 384kHz
系统时钟倍乘器 (f _{SCK}):	64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; 高达 50MHz

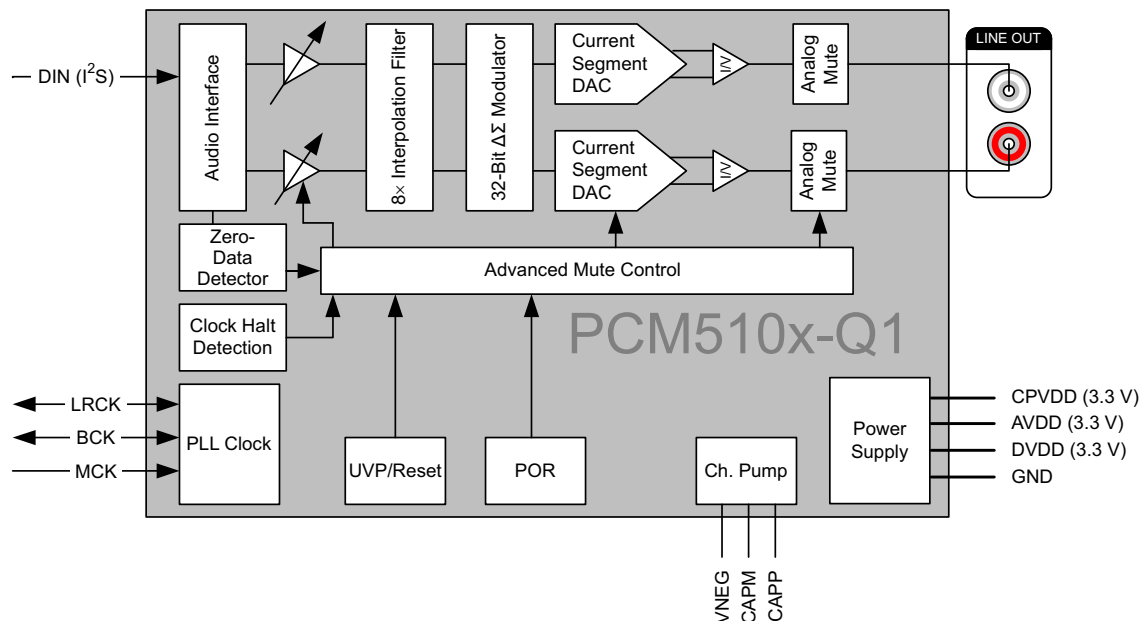


图 1. PCM510x-Q1功能方框图

其它关键特性



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Products conform to specifications per the terms of the Texas
Instruments standard warranty. Production processing does not
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English Data Sheet: [SLAS832](#)

- 接受 16, 24, 和 32 位音频数据
- **PCM** 数据样式: **I²S**, 左对齐
- 当 **LRCK** 和 **BCK** 被置为无效时, 自动进入省电模式
- **3.3V** 故障安全 **LVCOMS** 数字输入
- 硬件配置
- 单电源运行:
 - **3.3V** 模拟, **3.3V** 数字
- 集成型加电复位

应用范围

- **A/V** 接收器
- **DVD, BD** 播放器
- **HDTV** 接收器
- 需要 **2V_{RMS}** 音频输出的应用

说明

此PCM510x-Q1系列器件是单片 CMOS 集成电路, 此产品包括一个立体声数模转换器和采用小型薄型小外形尺寸 (TSSOP) 封装的附加支持电路。PCM510x-Q1 使用 TI 的高级分段 DAC 架构的最新一代产品来实现出色的动态性能并提升了对于时钟抖动的耐受度。

PCM510x-Q1提供了 2.1 V_{RMS}接地中心输出, 这使得设计人员不但能够去除输出上的隔直电容器, 而且能够免除对于传统上与单电源线路驱动器相关的外部静噪电路的需要。

集成的线路驱动器通过支持低至 1kΩ 的负载从而在性能上超过所有其它基于电荷泵的线路驱动器。通过支持低至 1kΩ 的负载, PCM510x-Q1实际能够驱动多达 10 个并联产品 (液晶电视, DVDR, AV 接收器等)。

器件上集成的 PLL 免除了对于系统时钟的需要 (通常称为主时钟)。这样可实现一个三线制 I²S 连接, 同时减少系统电磁干扰 (EMI)。

为了实现无爆音性能, 智能时钟误差和电源感测 (PowerSense) 欠压保护使用一个两级静噪系统。发生时钟误差或者系统电源故障时, 器件减弱数字数据 (或者已知最后的正确数据), 然后将模拟电路静噪

PCM510x-Q1提供比现有 DAC 技术最多低 20dB 的带外 (OBN) 噪声, 从而减少了下行放大器/模数转换器 (ADC) 中的 EMI 和失真。(从传统的 100kHz 噪声倍频带 (OBN) 测量一直到 3MHz 测量)

PCM510x-Q1接受具有 16 至 32 位数据的行业标准音频数据格式, 并且支持高达 384kHz 的采样率。

表 1. 订购信息

部件号	T _A	顶部符号
PCM5100TPWRQ1 (预览)	-40°C 至 105°C	PCM5100Q
PCM5101TPWRQ1 (预览)	-40°C 至 105°C	PCM5101Q
PCM5102TPWRQ1	-40°C 至 105°C	PCM5102Q

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage	AVDD, CPVDD, DVDD	-0.3 to 3.9	V
Digital input voltage		-0.3 to 3.9	
Analog input voltage		-0.3 to 3.9	
Operating temperature range		-40 to 105	°C
Storage temperature range		-65 to 150	
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B	750	V

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Theta JA	High K		91.2		°C/W
Ψ_{JT}	Psi JT			1		
Ψ_{JB}	Psi JB			41.5		
θ_{JC}	Theta JC	Top		25.3		
θ_{JB}	Theta JB			42		

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Power-Supply Requirements						
DV_{DD}	Digital supply voltage	Target $DV_{DD} = 3.3\text{ V}$	3	3.3	3.6	VDC
AV_{DD}	Analog supply voltage		3	3.3	3.6	VDC
CPV_{DD}	Charge-pump supply voltage		3	3.3	3.6	VDC
I_{DD}	DV_{DD} supply current at 3.3 V ⁽¹⁾	$f_S = 48\text{ kHz}$		7	12	mA
		$f_S = 96\text{ kHz}$		8		
		$f_S = 192\text{ kHz}$		9		
I_{DD}	DV_{DD} supply current at 3.3 V ⁽²⁾	$f_S = 48\text{ kHz}$		8	13	mA
		$f_S = 96\text{ kHz}$		9		
		$f_S = 192\text{ kHz}$		10		
I_{DD}	DV_{DD} supply current at 3.3 V ⁽³⁾			0.5	0.8	mA
I_{CC}	AV_{DD} / CPV_{DD} supply current ⁽¹⁾	$f_S = 48\text{ kHz}$		11	16	mA
		$f_S = 96\text{ kHz}$		11		
		$f_S = 192\text{ kHz}$		11		
I_{CC}	AV_{DD} / CPV_{DD} supply current ⁽²⁾	$f_S = 48\text{ kHz}$		22	32	mA
		$f_S = 96\text{ kHz}$		22		
		$f_S = 192\text{ kHz}$		22		
I_{CC}	AV_{DD} / CPV_{DD} supply current ⁽³⁾	$f_S = \text{N/A}$		0.2	0.4	mA
	Power dissipation, $DV_{DD} = 3.3\text{ V}$ ⁽¹⁾	$f_S = 48\text{ kHz}$		59.4	92.4	mW
		$f_S = 96\text{ kHz}$		62.7		
		$f_S = 192\text{ kHz}$		66		
	Power dissipation, $DV_{DD} = 3.3\text{ V}$ ⁽²⁾	$f_S = 48\text{ kHz}$		99	148.5	mW
		$f_S = 96\text{ kHz}$		102.3		
		$f_S = 192\text{ kHz}$		105.6		
	Power dissipation, $DV_{DD} = 3.3\text{ V}$ ⁽³⁾	$f_S = \text{N/A}$ (power-down mode)		2.3	4	mW

(1) Input is bipolar-zero data.

(2) Input is 1-kHz, –1-dBFS data.

(3) Power-down mode

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
	Resolution		16	24	32	Bits		
Data Format (PCM Mode)								
	Audio data interface format		I ² S, left justified					
	Audio data bit length		16, 24, 32-bit acceptable					
	Audio data format		MSB-first, 2s complement					
f _S	Sampling frequency		8		384	kHz		
	System clock frequency		64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 f _{SCK} , up to 50 Mhz					
Digital Input/Output								
Logic family: 3.3-V LVCMOS compatible								
V _{IH}	Input logic level		0.7 × DV _{DD}			V		
V _{IL}			0.3 × DV _{DD}					
I _{IH}	Input logic current	V _{IN} = V _{DD}	10			μA		
I _{IL}		V _{IN} = 0 V	–10					
V _{OH}	Output logic level	I _{OH} = –4 mA	0.8 × DV _{DD}			V		
V _{OL}		I _{OL} = 4 mA	0.22 × DV _{DD}					
Dynamic Performance (PCM Mode) ⁽¹⁾⁽²⁾ (Values shown for three devices PCM5102-Q1/PCM5101-Q1/PCM5100-Q1)								
	THD+N at –1 dBFS ⁽²⁾	f _S = 48 kHz	–93/–92/–90	–83/–82/–80	dB			
		f _S = 96 kHz	–93/–92/–90					
		f _S = 192 kHz	–93/–92/–90					
	Dynamic range ⁽²⁾	EIAJ, A-weighted, f _S = 48 kHz	106/100/95	112/106/100				
		EIAJ, A-weighted, f _S = 96 kHz		112/106/100				
		EIAJ, A-weighted, f _S = 192 kHz		112/106/100				
	Signal-to-noise ratio ⁽²⁾	EIAJ, A-weighted, f _S = 48 kHz		112/106/100				
		EIAJ, A-weighted, f _S = 96 kHz		112/106/100				
		EIAJ, A-weighted, f _S = 192 kHz		112/106/100				
	Signal-to-noise ratio with analog mute ⁽²⁾⁽³⁾	EIAJ, A-weighted, f _S = 48 kHz	113	123				
		EIAJ, A-weighted, f _S = 96 kHz		123				
		EIAJ, A-weighted, f _S = 192 kHz		123				
	Channel separation	f _S = 48 kHz	100/95/90	109/103/97				
		f _S = 96 kHz		109/103/97				
		f _S = 192 kHz		109/103/97				
Analog Output								
	Output voltage			2.1		V _{RMS}		
	Gain error		–6	±2	6	% of FSR		
	Gain mismatch, channel-to-channel		–6	±2	6	% of FSR		
	Bipolar-zero error	At bipolar zero	–5	±1	5	mV		
	Load impedance		1			kΩ		
Filter Characteristics–1: Normal								

- (1) Filter condition: THD+N: 20-Hz HPF, 20-kHz AES17 LPF; dynamic range: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted channel separation: 20-Hz HPF, 20-kHz AES17 LPF; using the System Two Cascade™ audio measurement system by Audio Precision™ in the rms mode to measure analog performance specifications.
- (2) Output load is 10 k Ω , with 470- Ω output resistor and a 2.2-nF shunt capacitor (see recommended output filter).
- (3) Both L-ch and R-ch are BPZ with XSMT de-asserted

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, and 24-bit data unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass band				$0.45 f_S$	
Stop band		$0.55 f_S$			
Stop-band attenuation		-60			dB
Pass-band ripple				± 0.02	
Delay time			$22 / f_S$		s
Filter Characteristics–2: Low Latency					
Pass band				$0.47 f_S$	
Stop band		$0.55 f_S$			
Stop-band attenuation		-52			dB
Pass-band ripple				± 0.0001	
Delay time			$3.5 / f_S$		s

DEVICE INFORMATION

TERMINAL FUNCTIONS, PCM510x-Q1

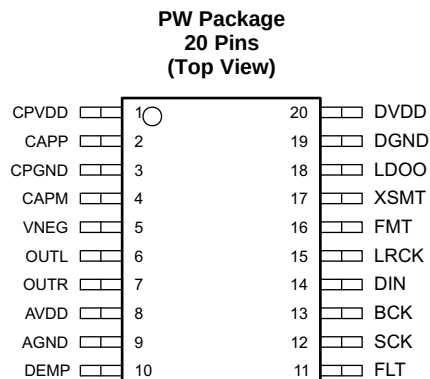


Table 2. PIN FUNCTIONS, PCM510x-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9	—	Analog ground
AVDD	8	—	Analog power supply, 3.3 V
BCK	13	I	Audio-data bit-clock input ⁽¹⁾
CAPM	4	O	Charge-pump flying-capacitor terminal for negative rail
CAPP	2	O	Charge-pump flying-capacitor terminal for positive rail
CPGND	3	—	Charge-pump ground
CPVDD	1	—	Charge-pump power supply, 3.3 V
DEMP	10	I	De-emphasis control for 44.1-kHz sampling rate ⁽¹⁾ : Off (Low), On (High)
DGND	19	—	Digital ground
DIN	14	I	Audio-data input ⁽¹⁾
DVDD	20	—	Digital power supply, 3.3 V
FLT	11	I	Filter select : Normal latency (Low) or Low latency (High)
FMT	16	I	Audio format selection : I ² S (Low) or Left-justified (High)

(1) Failsafe LVCMOS Schmitt-trigger input

Table 2. PIN FUNCTIONS, PCM510x-Q1 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
LDOO	18	—	Internal-logic supply-rail terminal for decoupling
LRCK	15	I	Audio-data word-clock input ⁽¹⁾
OUTL	6	O	Analog output from DAC left channel
OUTR	7	O	Analog output from DAC right channel
SCK	12	I	System clock input ⁽¹⁾
VNEG	5	O	Negative charge-pump rail terminal for decoupling, –3.3 V
XSMT	17	I	Soft-mute control ⁽¹⁾ : Soft mute (Low), Soft un-mute (High)

TYPICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_s = 48\text{ kHz}$, system clock = $512 f_s$, and 24-bit data unless otherwise noted.

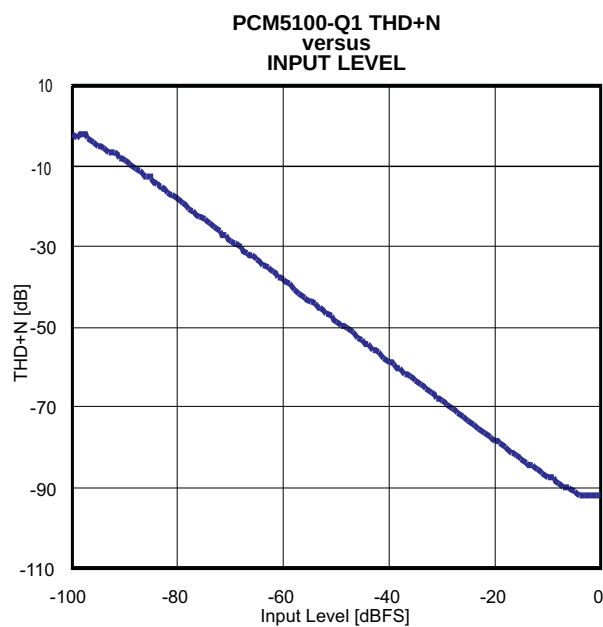


Figure 2.

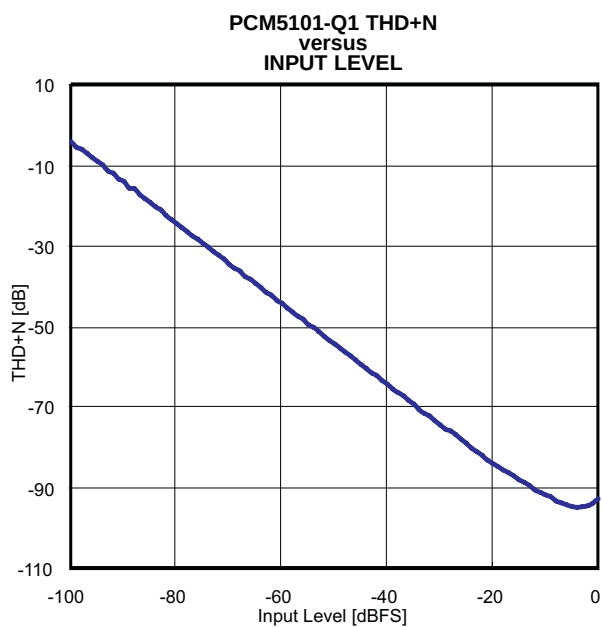


Figure 3.

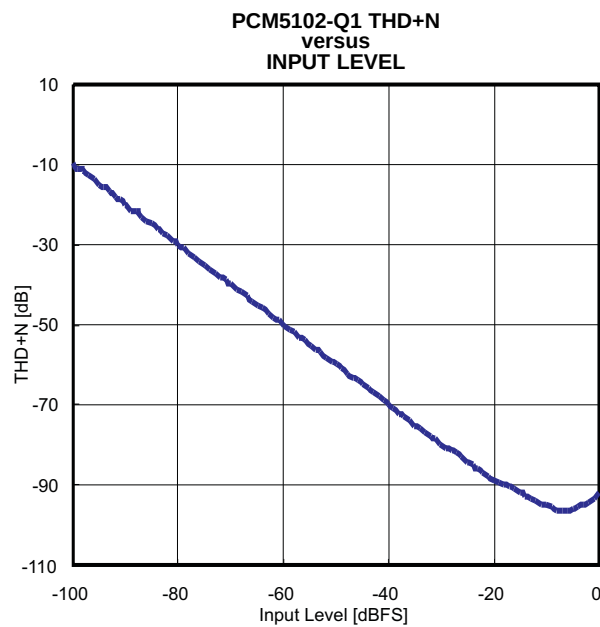


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, and 24-bit data unless otherwise noted.

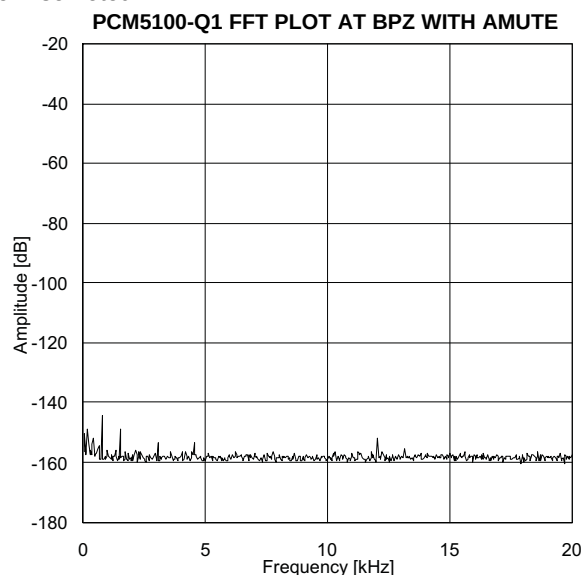


Figure 5.

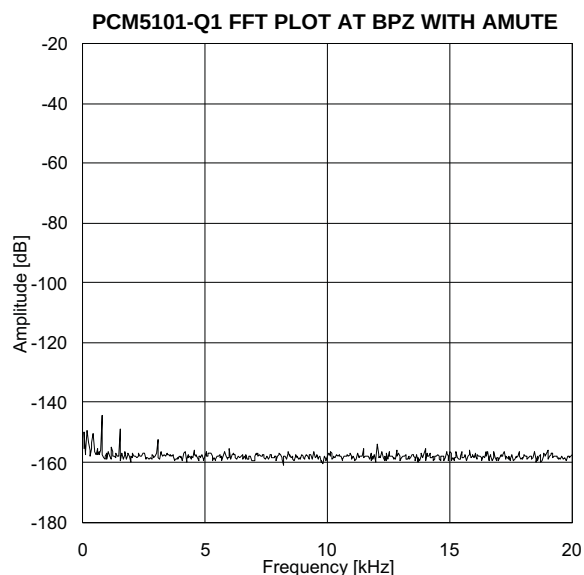


Figure 6.

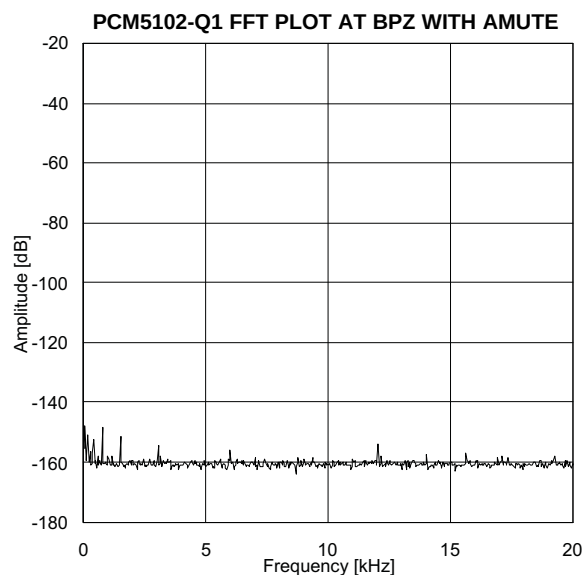


Figure 7.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, and 24-bit data unless otherwise noted.

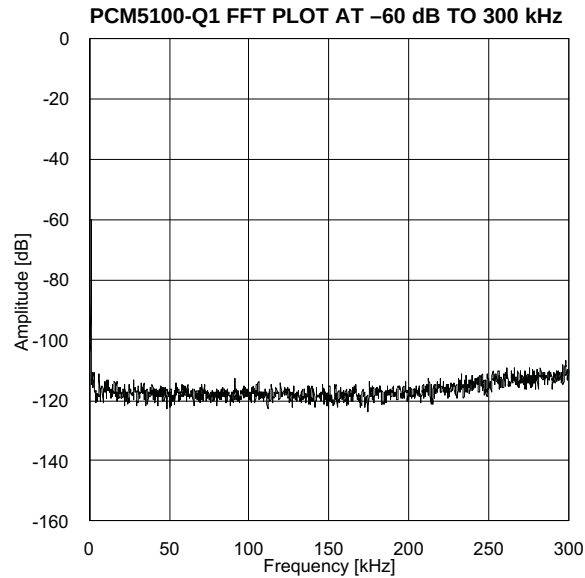


Figure 8.

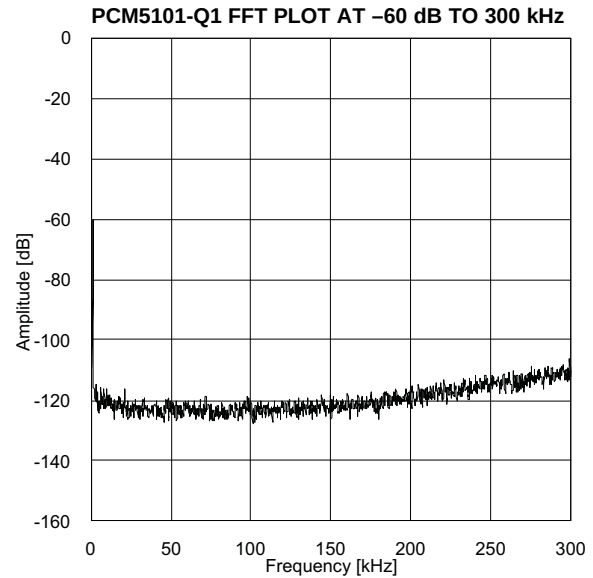


Figure 9.

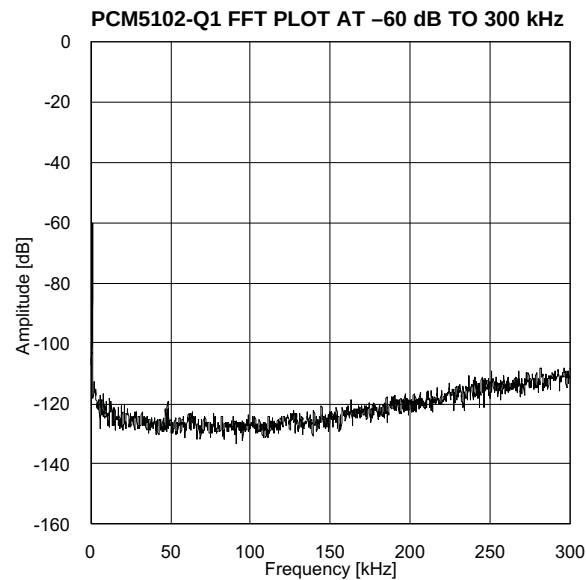


Figure 10.

APPLICATION INFORMATION

Reset and System Clock Functions

Power-On Reset Function

The PCM510x-Q1 includes a power-on-reset function shown in [Figure 11](#). Having $V_{DD} > 2.8$ V enables the power-on reset function. After the initialization period, the PCM510x-Q1 enters its default reset state.

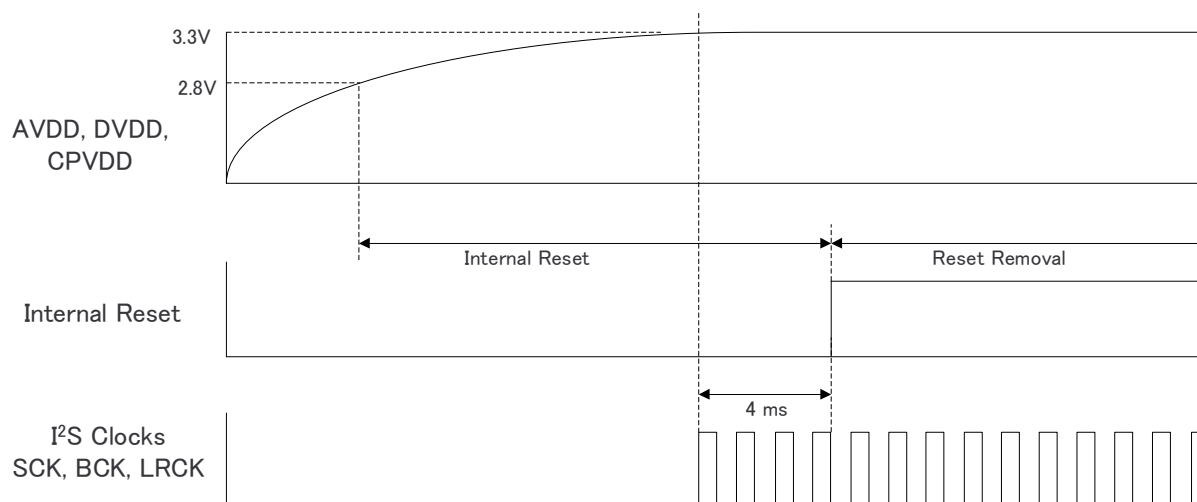


Figure 11. Power-On Reset Timing, DVDD = 3.3 V

System-Clock Input

The PCM510x-Q1 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock, applied at the SCK input (pin 12), supports up to 50 MHz. The PCM510x-Q1 has a system-clock detection circuit that automatically senses the system-clock frequency. The device supports common audio sampling frequencies of 8 kHz, 16 kHz, 32 kHz–44.1 kHz and 48 kHz, 88.2 kHz–96 kHz, 176.4 kHz–192 kHz, and 384 kHz with $\pm 4\%$ tolerance. The sampling-frequency detector sets the clock for the digital filter, delta-sigma modulator (DSM), and the negative charge pump (NCP) automatically. Table 3 shows examples of system clock frequencies for common audio sampling rates.

NOTE

The sampling frequency detector only detects six sampling-frequency options. Any sampling frequency between the range of 32 kHz–44.1 kHz (or if it is 48 kHz) is one option. The same case applies for the ranges from 88.2 kHz–96 kHz and 176.4 kHz–192 kHz.

The device supports SCK rates between 1 MHz and 50 MHz that are not common to standard audio clocks by configuring various PLL and clock-divider registers. This allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example, using 12 MHz to generate 44.1 kHz (LRCK) and 2.8224 MHz (BCK)).

Figure 12 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

Table 3. System Master Clock Inputs for Audio-Related Clocks

Sampling Frequency	System Clock Frequency (f_{SCK}) (MHz)											
	64 f_s	128 f_s	192 f_s	256 f_s	384 f_s	512 f_s	768 f_s	1024 f_s	1152 f_s	1536 f_s	2048 f_s	3072 f_s
8 kHz	— ⁽¹⁾	1.0240 ⁽²⁾	1.5360 ⁽²⁾	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	— ⁽¹⁾	2.0480 ⁽²⁾	3.0720 ⁽²⁾	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	— ⁽¹⁾	4.0960 ⁽²⁾	6.1440 ⁽²⁾	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	— ⁽¹⁾	— ⁽¹⁾
44.1 kHz	— ⁽¹⁾	5.6488 ⁽²⁾	8.4672 ⁽²⁾	11.2896	16.9344	22.5792	33.8688	45.1584	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾
48 kHz	— ⁽¹⁾	6.1440 ⁽²⁾	9.2160 ⁽²⁾	12.2880	18.4320	24.5760	36.8640	49.1520	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾
88.2 kHz	— ⁽¹⁾	11.2896 ⁽²⁾	16.9344	22.5792	33.8688	45.1584	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾
96 kHz	— ⁽¹⁾	12.2880 ⁽²⁾	18.4320	24.5760	36.8640	49.1520	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾
176.4 kHz	— ⁽¹⁾	22.5792	33.8688	45.1584	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾
192 kHz	— ⁽¹⁾	24.5760	36.8640	49.1520	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾
384 kHz	24.5760	49.1520	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾

(1) The device does not support this system clock rate for the given sampling frequency.

(2) PLL mode supports this system clock rate.

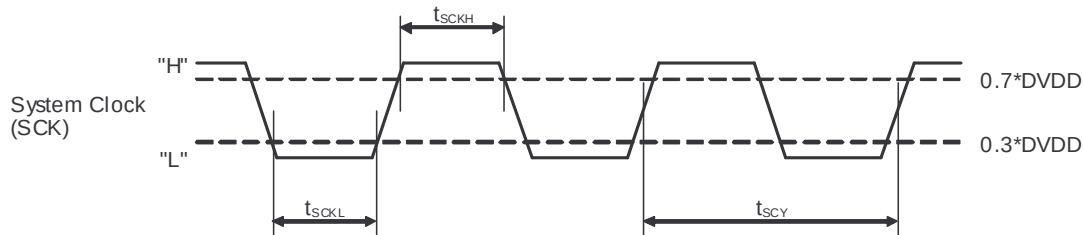


Figure 12. Timing Requirements for SCK Input

Table 4. Timing Requirements for SCK Input

	Parameters	Min	Max	Unit
t_{SCY}	System clock-pulse cycle time	20	1000	ns
t_{SCKH}	System clock-pulse duration, High	9		ns
t_{SCKL}	System clock-pulse duration, Low	9		ns

System Clock PLL Mode

The system clock PLL mode allows designers to use a simple three-wire I²S audio source when driving the DAC, thereby reducing the need for a high-frequency SCK, making PCB layout easier, and reducing high-frequency electromagnetic interference.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. In the PCM510x-Q1, supplying an external SCK disables the internal PLL; the device requires specific BCK rates to generate an appropriate master clock. [Table 5](#) describes the minimum and maximum BCK per LRCK for the integrated PLL to generate an internal SCK automatically.

Table 5. BCK Rates (MHz) by LRCK Sample Rate for PCM510x-Q1 PLL Operation

Sample f (kHz)	BCK (f _s)	
	32	64
8	–	–
16	–	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

Audio Data Interface

Audio Serial Interface

The audio interface port is a three-wire serial port. It includes LRCK (pin 15), BCK (pin 13), and DIN (pin 14). BCK is the serial audio bit clock, and it clocks the serial data present on DIN into the serial shift register of the audio interface. Clocking of serial data into the PCM510x-Q1 occurs on the rising edge of BCK. LRCK is the serial audio left/right word clock.

Table 6. PCM510x-Q1 Audio Data Formats, Bit Depths and Clock Rates

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f _s]	SCK RATE [× f _s]	BCK RATE [× f _s]
Hardware control	I ² S or LJ	32, 24, 20, 16	Up to 192 kHz	128–3072 (≤50 MHz)	64, 48, 32
			384 kHz	64, 128	64, 48, 32

The PCM510x-Q1 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, the device initializes internal operation within one sample period and forces analog outputs to the bipolar-zero level until the completion of resynchronization between LRCK and the system clock.

If the relationship between LRCK and BCK is invalid for more than 4 LRCK periods, the device initializes internal operation within one sample period and forces analog outputs to the bipolar-zero level until the completion of resynchronization between LRCK and BCK.

PCM Audio Data Formats and Timing

The PCM510x-Q1 supports industry-standard audio data formats, including standard I²S and left-justified. Data formats are selected using the FMT (pin 16), Low for I²S, and High for left-justified.

All formats require binary 2s-complement, MSB-first audio data. Figure 13 shows a detailed timing diagram for the serial audio interface.

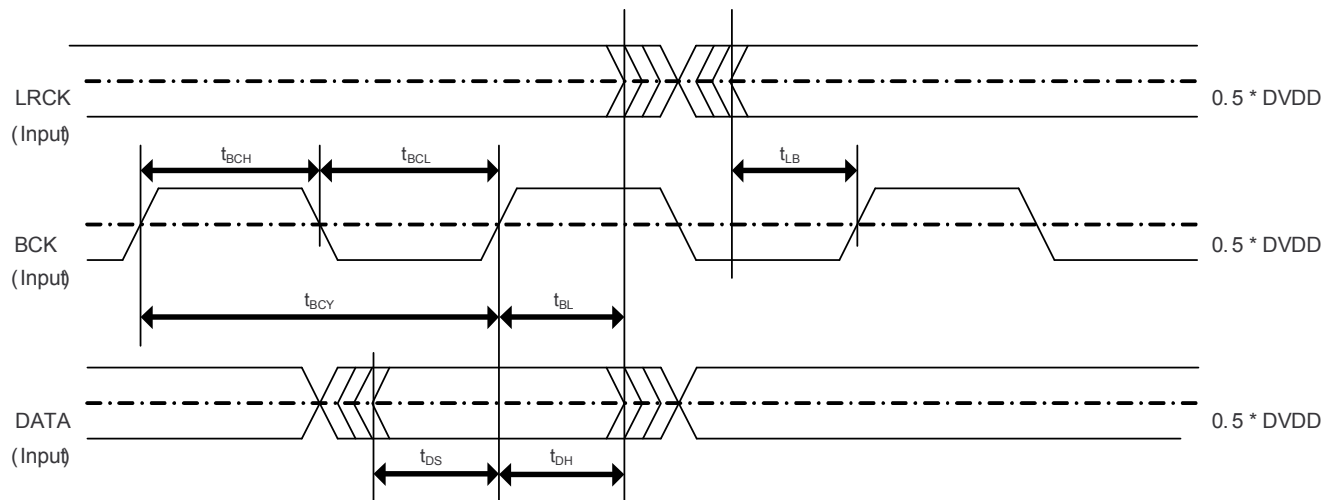


Figure 13. PCM510x-Q1 Serial Audio Timing - Slave

Table 7. Audio Interface Slave Timing

	Parameters	Min	Max	Unit
t_{BCY}	BCK pulse cycle time	40		ns
t_{BCL}	BCK pulse duration, LOW	16		ns
t_{BCH}	BCK pulse duration, HIGH	16		ns
t_{BL}	BCK rising edge to LRCK edge	8		ns
t_{LB}	LRCK edge to BCK rising edge	8		ns
t_{DS}	DATA setup time	8		ns
t_{DH}	DATA hold time	8		ns
f_{BCK}	BCK frequency at DVDD = 3.3 V		24.576	MHz

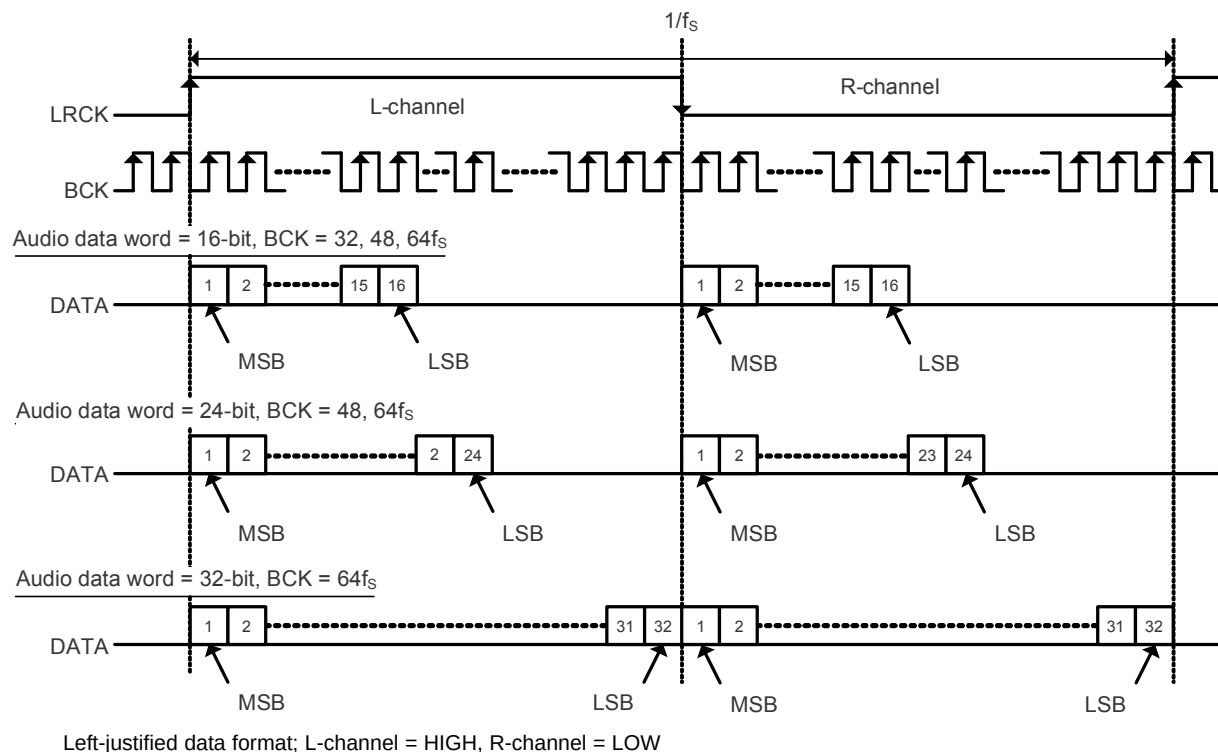


Figure 14. Left-Justified Audio Data Format

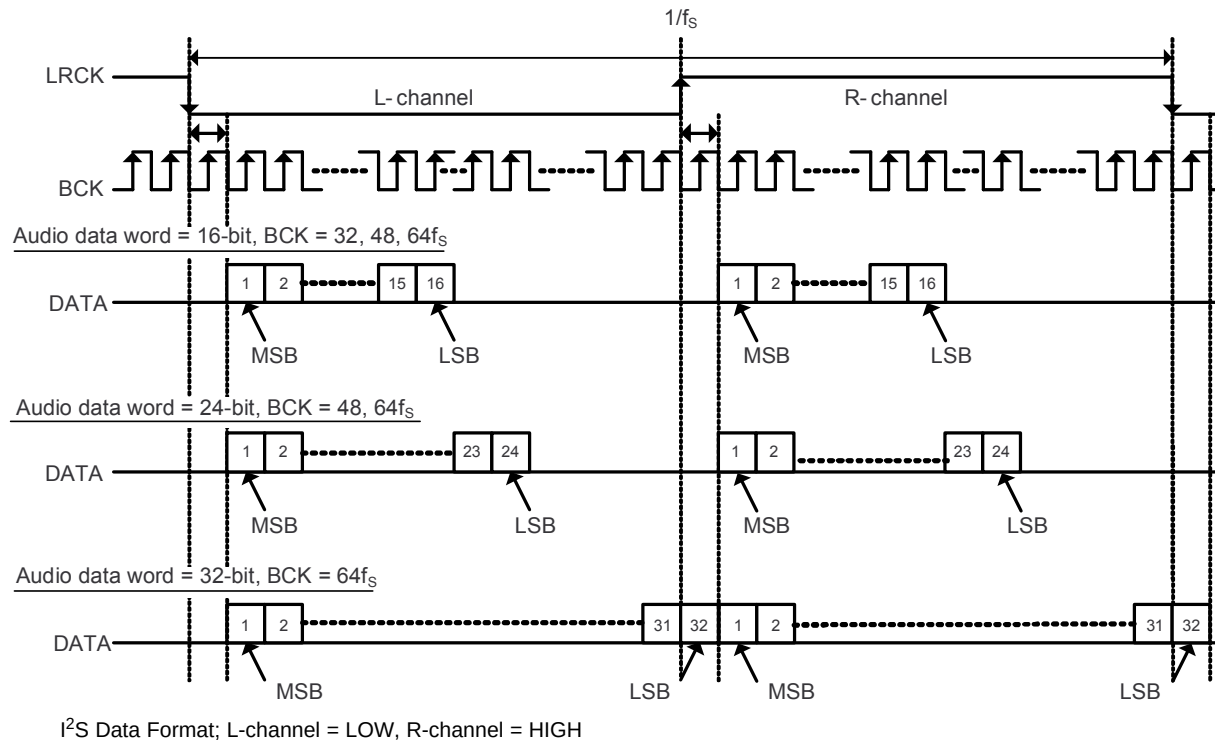


Figure 15. I²S Audio Data Format

Function Descriptions

Interpolation Filter

The PCM510x-Q1 provides two types of interpolation filter. Users can select which filter to use by using the FLT pin (pin11).

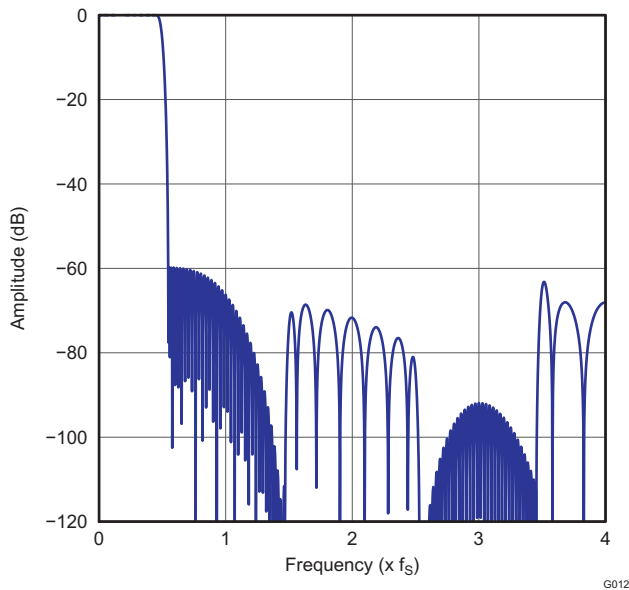
Table 8. Digital Interpolation Filter Options

FLT Pin	Description
0	FIR normal ×8, ×4, ×2, and ×1 interpolation filters
1	IIR low-latency ×8, ×4, ×2, and ×1 interpolation filters

The normal ×8, ×4, ×2, or ×1 (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_s) for from 8 kHz to 384 kHz.

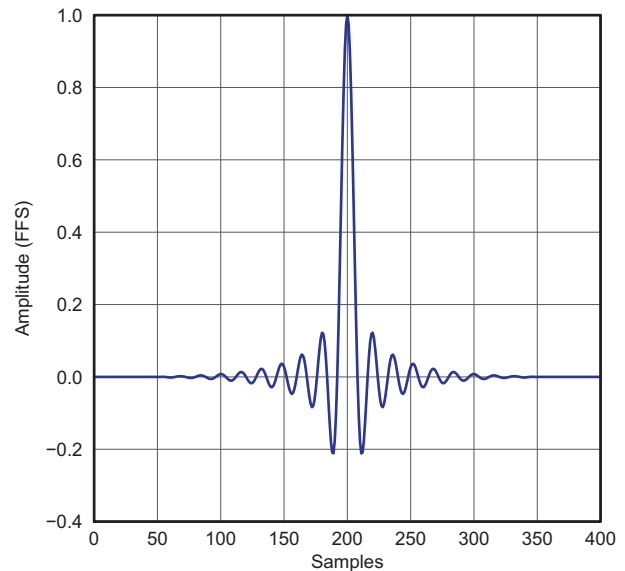
Table 9. Normal ×8 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	$0-0.45 f_s$		± 0.02	dB
Filter-gain stop band	$0.55 f_s-7.455 f_s$	-60		dB
Filter-group delay		$22 / f_s$		s



G012

Figure 16. Normal ×8 Interpolation-Filter Frequency Response



G023

Figure 17. Normal ×8 Interpolation-Filter Impulse Response

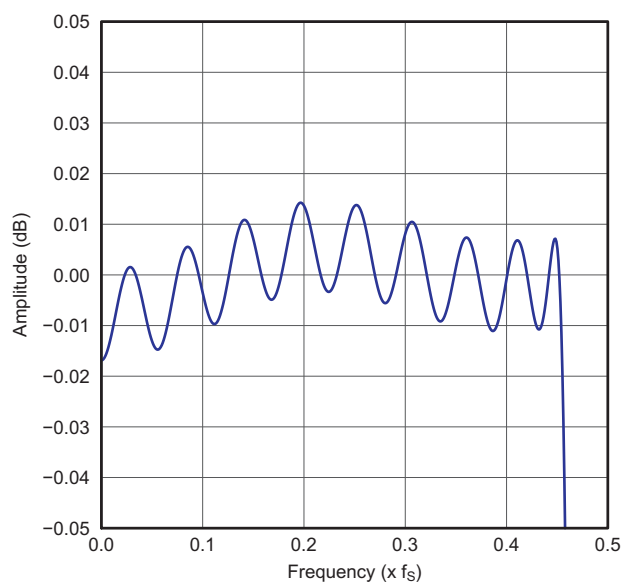


Figure 18. Normal x8 Interpolation-Filter Pass-Band Ripple

The normal $\times 4$, $\times 2$, or $\times 1$ (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_s) from 8 kHz to 384 kHz.

Table 10. Normal $\times 4$ Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	$0-0.45 f_s$		± 0.02	dB
Filter-gain stop band	$0.55 f_s-7.455 f_s$	-60		dB
Filter-group delay		$22 / f_s$		s

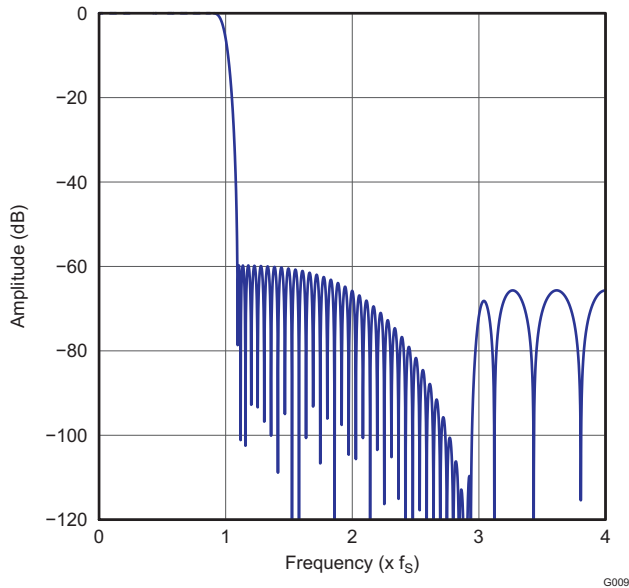


Figure 19. Normal $\times 4$ Interpolation-Filter Frequency Response

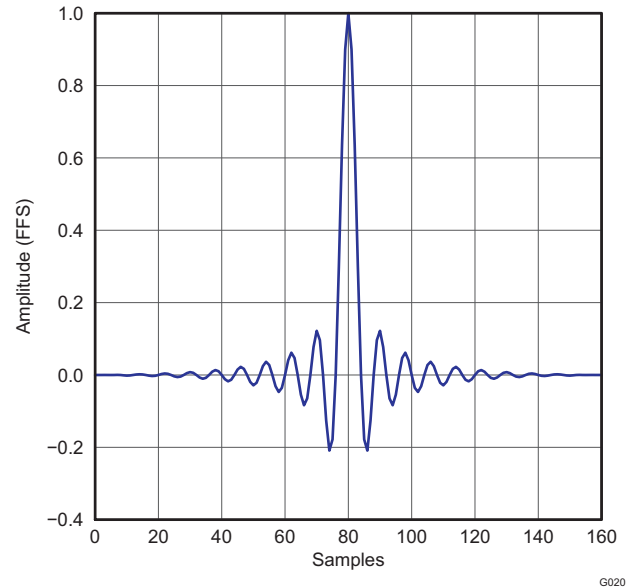


Figure 20. Normal $\times 4$ Interpolation-Filter Impulse Response

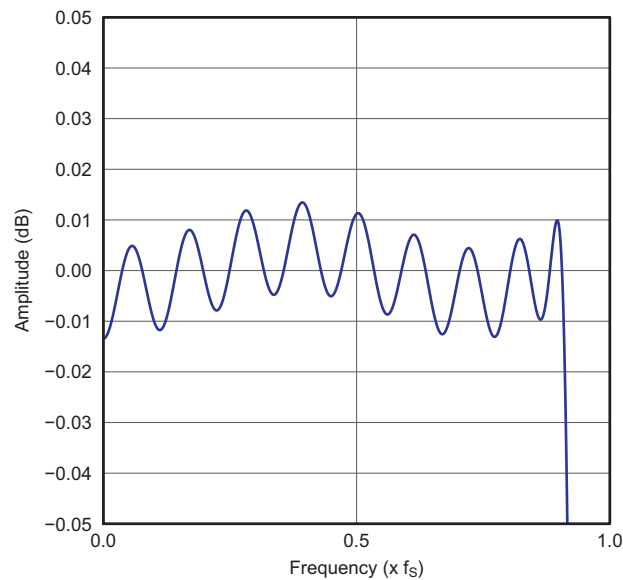


Figure 21. Normal $\times 4$ Interpolation-Filter Pass-Band Ripple

Normal $\times 2$ or $\times 1$ (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_s) from 8 kHz to 384 kHz.

Table 11. Normal $\times 2$ Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	$0-0.45 f_s$		± 0.02	dB
Filter-gain stop band	$0.55 f_s-7.455 f_s$	-60		dB
Filter-group delay		$22 / f_s$		s

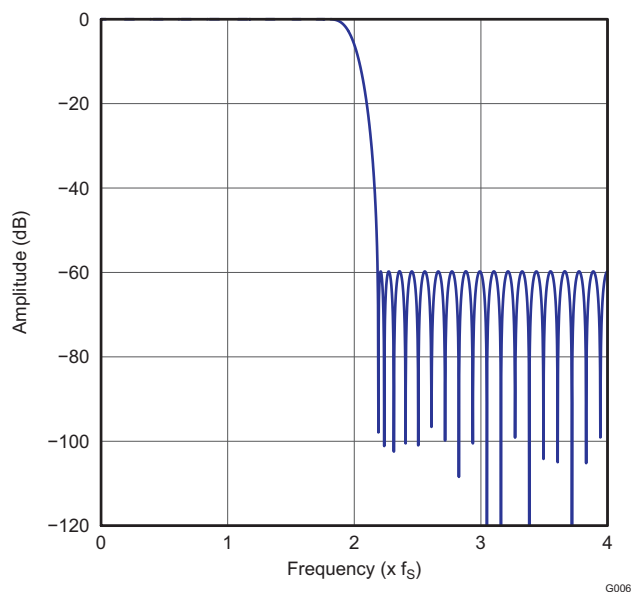


Figure 22. Normal $\times 2$ Interpolation-Filter Frequency Response

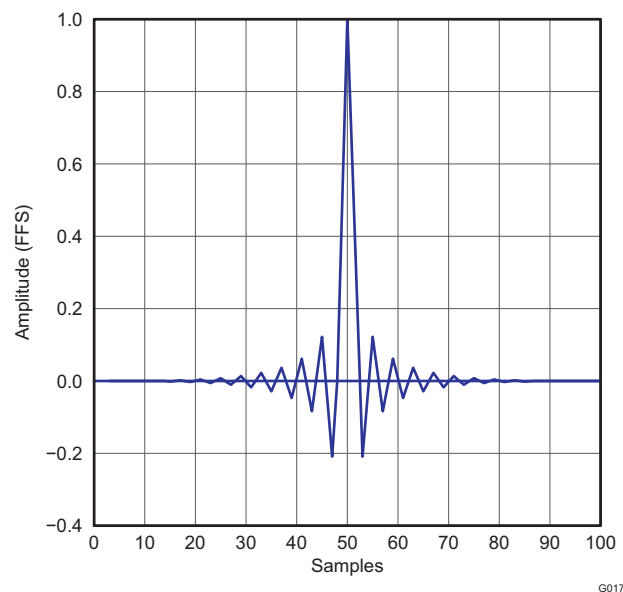


Figure 23. Normal $\times 2$ Interpolation-Filter Impulse Response

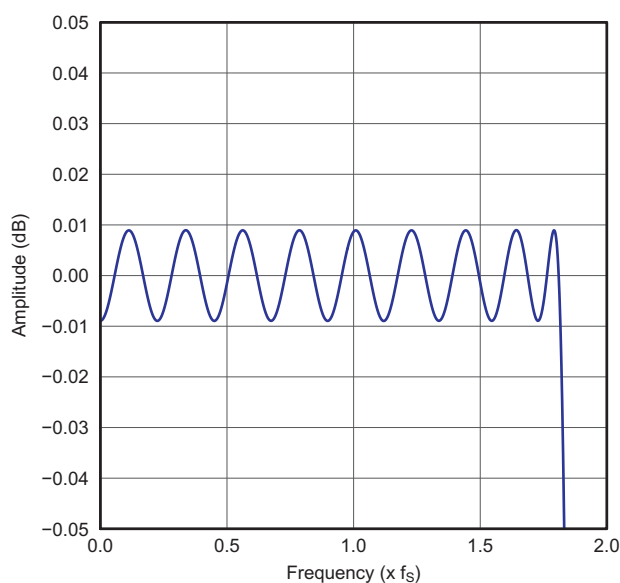


Figure 24. Normal $\times 2$ Interpolation-Filter Pass-Band Ripple

The low-latency $\times 8$, $\times 4$, $\times 2$, or $\times 1$ (bypass) interpolation filter is programmed in 256 cycles in $1 f_s$ from 8 kHz to 384 kHz.

Table 12. Low-Latency $\times 8$ Interpolation Filter

Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	$0-0.45 f_s$	± 0.0001	dB
Filter-gain stop band	$0.55 f_s-7.455 f_s$	-52	dB
Filter-group delay		$3.5 / f_s$	s

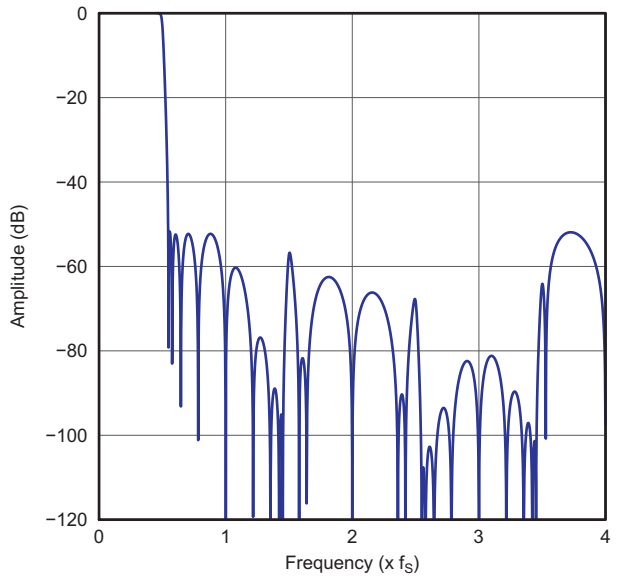


Figure 25. $\times 8$ Interpolation-Filter Frequency Response

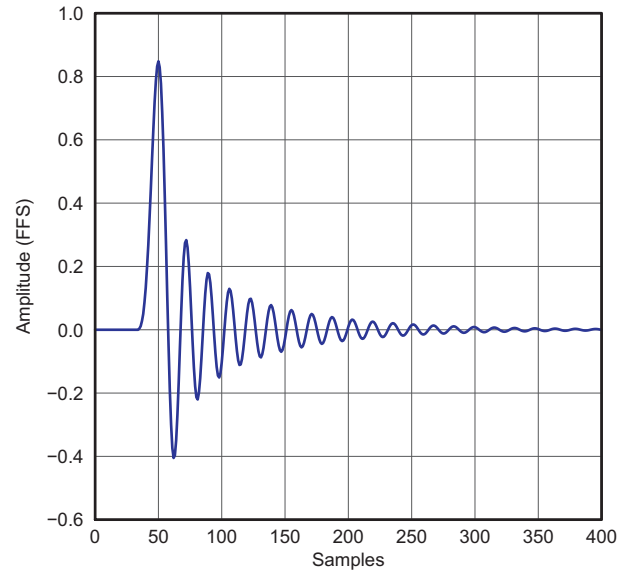


Figure 26. Low-Latency $\times 8$ Interpolation-Filter Impulse Response

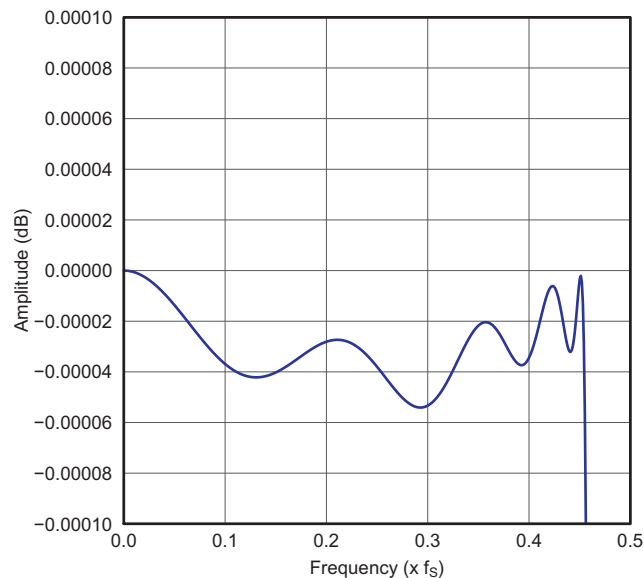


Figure 27. Low-Latency $\times 8$ Interpolation-Filter Pass-Band Ripple

Table 13. Low-Latency ×4 Interpolation Filter

Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	$0-0.45 f_s$	± 0.0001	dB
Filter-gain stop band	$0.55 f_s-3.455 f_s$	-52	dB
Filter-group delay		$3.5 / f_s$	s

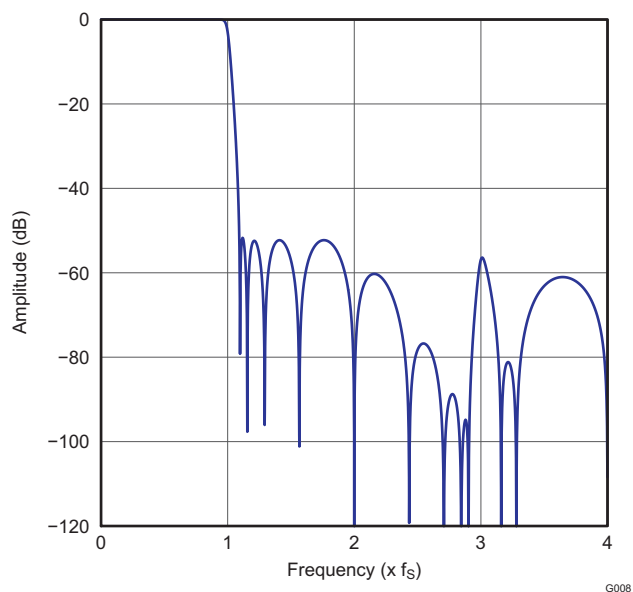


Figure 28. Low-Latency ×4 Interpolation-Filter Frequency Response

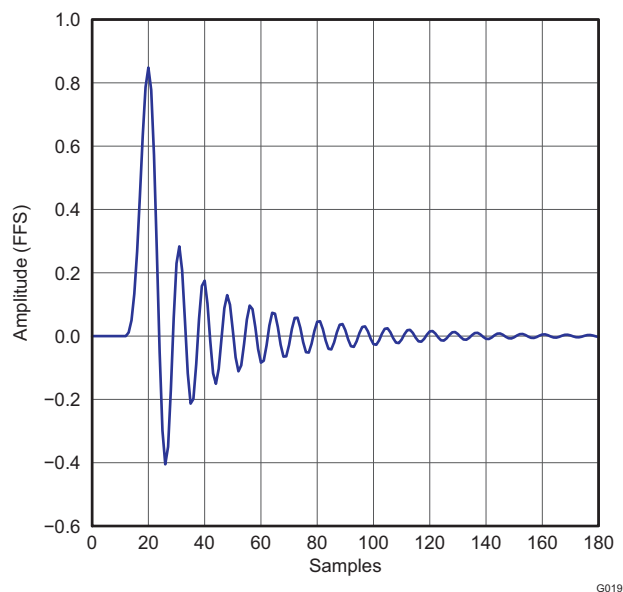


Figure 29. Low-Latency ×4 Interpolation-Filter Impulse Response

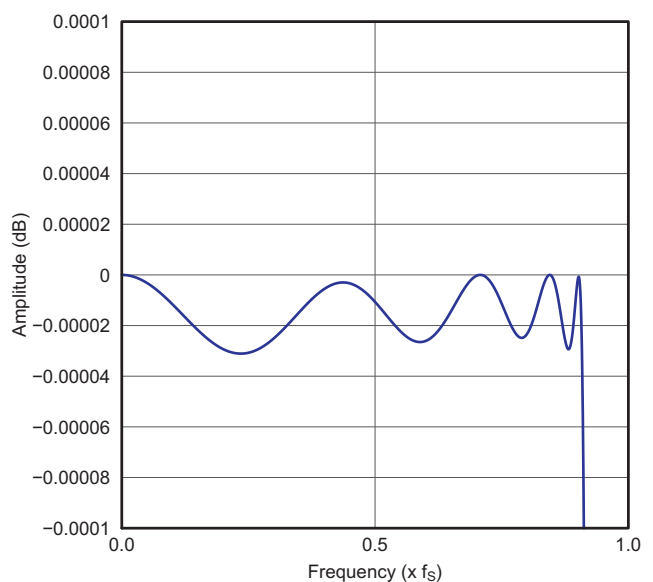


Figure 30. Low latency ×4 Interpolation-Filter Pass-Band Ripple

Table 14. Low-Latency ×2 Interpolation Filter

Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	0–0.45 f_s	± 0.0001	dB
Filter-gain stop band	0.55 f_s –1.455 f_s	–52	dB
Filter-group delay		$3.5 / f_s$	s

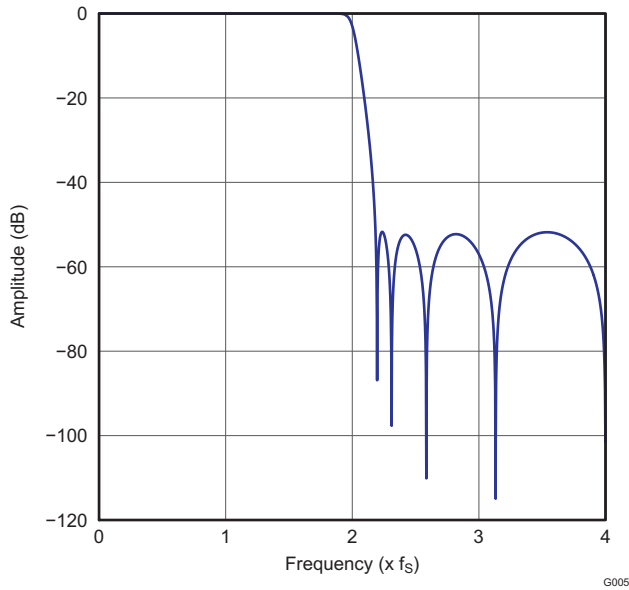


Figure 31. Low-Latency ×2 Interpolation-Filter Frequency Response

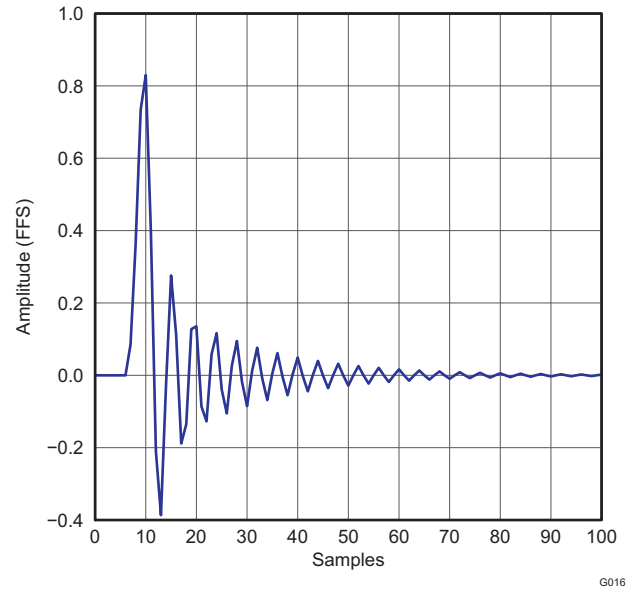


Figure 32. Low-Latency ×2 Interpolation-Filter Impulse Response

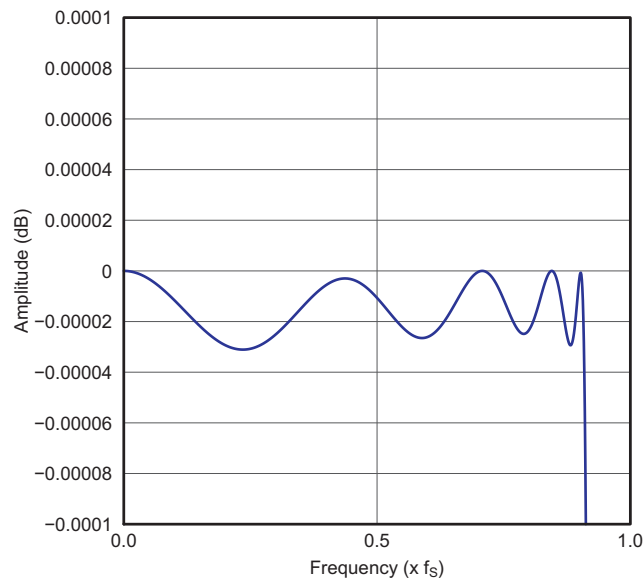


Figure 33. Low-Latency ×2 Interpolation-Filter Pass-Band Ripple

Zero-Data Detect

The PCM510x-Q1 has a zero-data detect function. When the device detects continuous zero data, it enters a full analog-mute condition.

The PCM510x-Q1 counts zero data over 1024 LRCKs (21 ms at 48 kHz) before setting analog mute.

Power-Save Mode

On detection of any kind of clock error (SCK, BCK, and LRCK) or clock halt, the PCM510x-Q1 enters standby mode automatically and powers down the current-segment DAC and line driver.

When BCK and LRCK halt to a low level for more than 1 second, the PCM510x-Q1 enters the power-down mode automatically. Power-down mode includes the negative charge pump and reference circuit power-down in addition to standby.

On application of expected audio clocks (SCK, BCK, LRCK) to the PCM510x-Q1, the device starts its power-up sequence automatically.

XSMT Pin (Soft Mute and Soft Un-Mute)

For external digital control of the PCM510x-Q1, an external digital host must drive the XSMT pin with a specific minimum rise time (t_r) and fall time (t_f) for soft mute and soft un-mute. The PCM510x-Q1 requires t_r and t_f times of less than 20 ns. In the majority of applications, this should not be a problem; however, traces with high capacitance may have issues.

When shifting the XSMT pin from high to low (3.3 V to 0 V), a soft digital attenuation ramp starts. Gain steps of -1 dB occur every $1 / f_s$ from 0 dBFS to $-\infty$. This takes 104 sample periods.

Shifting the XSMT pin from low to high (0 V to 3.3V) starts a soft digital un-mute. Gain steps of 1 dB occur every $1 / f_s$ from $-\infty$ to 0 dBFS. This takes 104 sample periods.

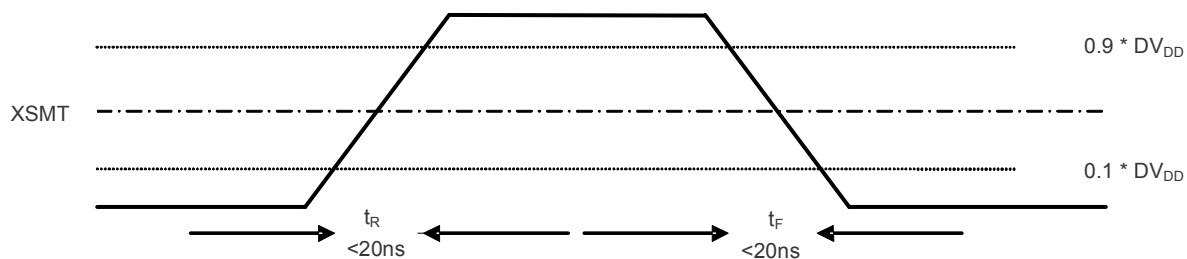


Figure 34. XSMT Timing for Soft Mute and Soft Un-Mute

Table 15. XSMT Timing Parameters

Parameters	Min	Max	Unit
Rise time (t_r)		20	ns
Fall time (t_f)		20	ns

External Power Sense Undervoltage Protection mode

The XSMT pin can alternatively monitor a system voltage, such as the 24-VDC LCD TV backlight, or 12-VDC system supply, using a potential divider created with two resistors. (See Figure 35.)

- If the XSMT pin makes a transition from 1 to 0 over 6 ms or more, the device switches into external undervoltage-protection mode. This mode uses two trigger levels.
- When the XSMT pin level reaches 2 V, the soft-mute process begins.
- When the XSMT pin level reaches 1.2 V, analog mute engages, regardless of digital audio level, and analog shutdown begins (for example, DAC circuitry powers down, and so forth).

Figure 36 is a timing diagram that shows this.

NOTE

The XSMT input-pin voltage range is from -0.3 V to $\text{DVDD} + 0.3\text{ V}$. Consider the ratio of external resistors within this input range. Any increase in power supply (such as power-supply positive noise or ripple) can pull the XSMT pin higher than $\text{DVDD} + 0.3\text{ V}$.

For example, if the PCM510x-Q1 monitors a 12-V input that a voltage divider has divided by 4, then the voltage at XSMT during ideal power supply conditions is 3 V. If the voltage spikes any higher than 14.4 V, then the voltage on XSMT exceeds 3.6 V ($\text{DVDD} + 0.3$), potentially damaging the device.

Appropriate setting of the divider allows monitoring of any dc voltage.

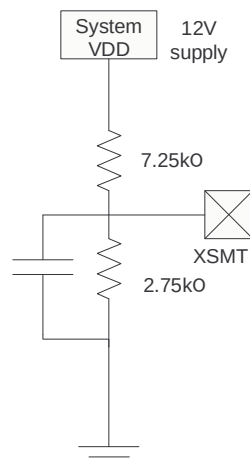


Figure 35. XSMT in External UVP Mode

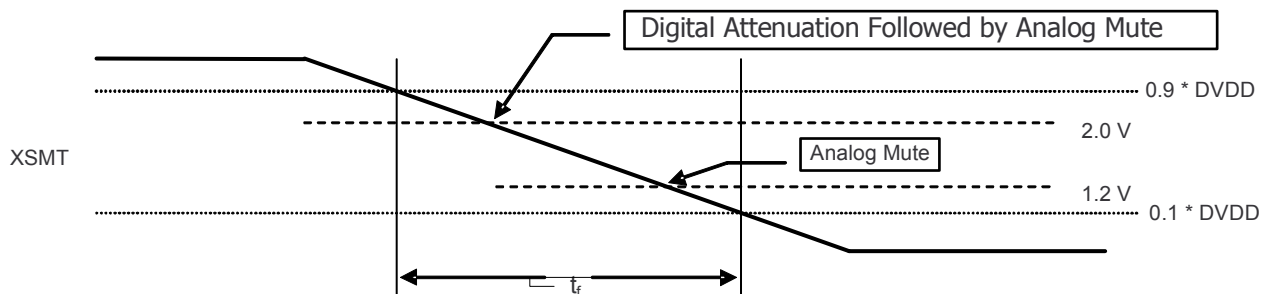


Figure 36. XSMT Timing for Undervoltage Protection

Typical Application Circuits

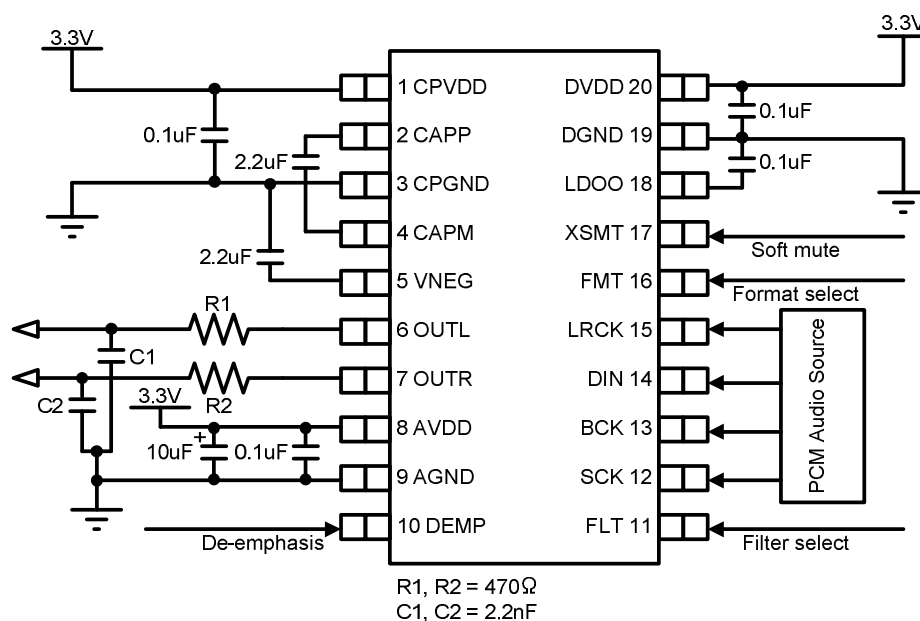


Figure 37. PCM510x-Q1 Standard PCM Audio Operation, 3.3 V

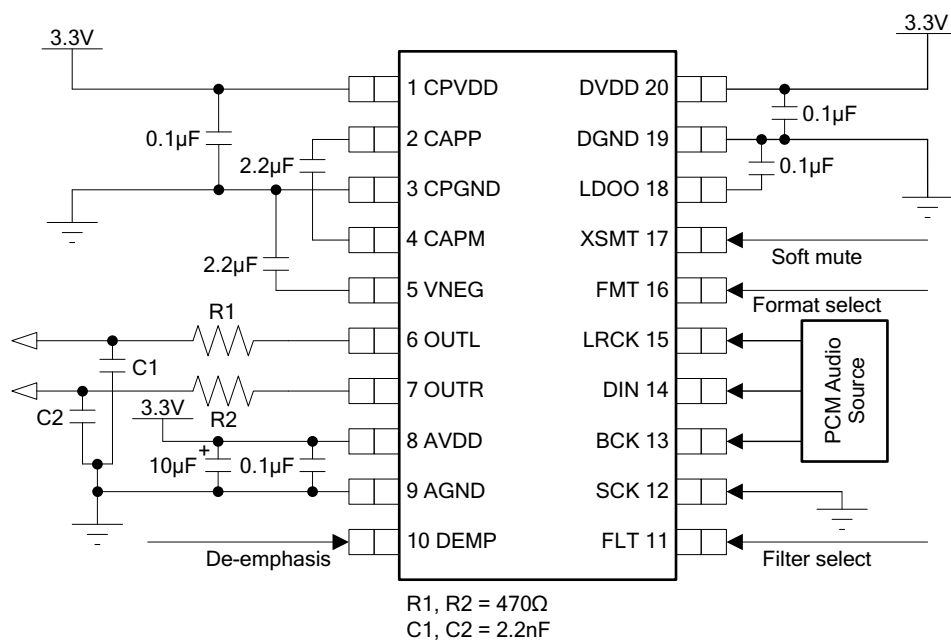


Figure 38. PCM510x-Q1 PLL Operation

Recommended Output Filter for the PCM510x-Q1

The diagram in [Figure 39](#) shows the recommended output filter for the PCM510x-Q1. The new PCM510x-Q1 next-generation current-segment architecture offers excellent out-of-band noise, making a traditional 20-kHz low-pass filter a thing of the past.

The RC settings below offer a –3-dB filter point at 153 kHz (approximately), giving the DAC the ability to reproduce virtually all frequencies through to its maximum sampling rate of 384 kHz.

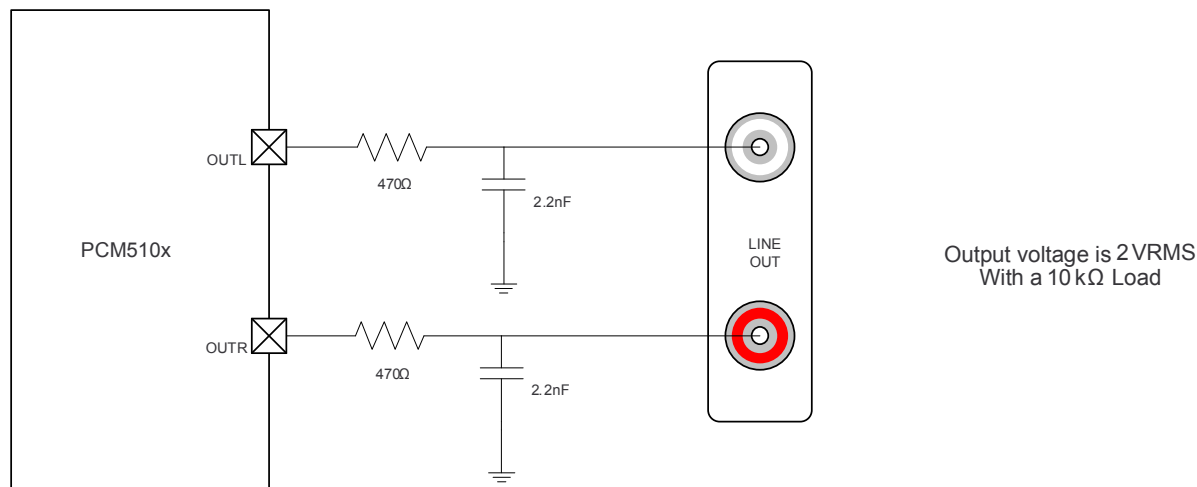


Figure 39. Recommended Low-Pass Output Filter for 10-kΩ Operation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM5102TPWRQ1	NRND	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	PCM5102Q	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

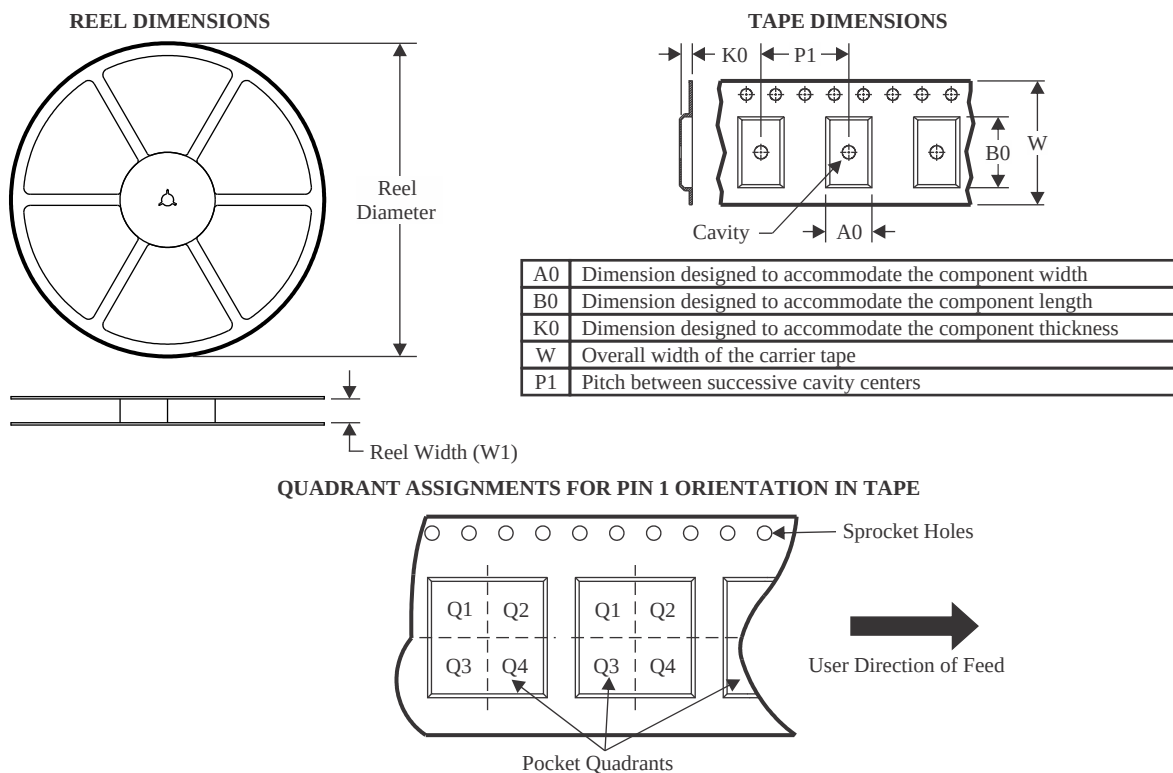
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

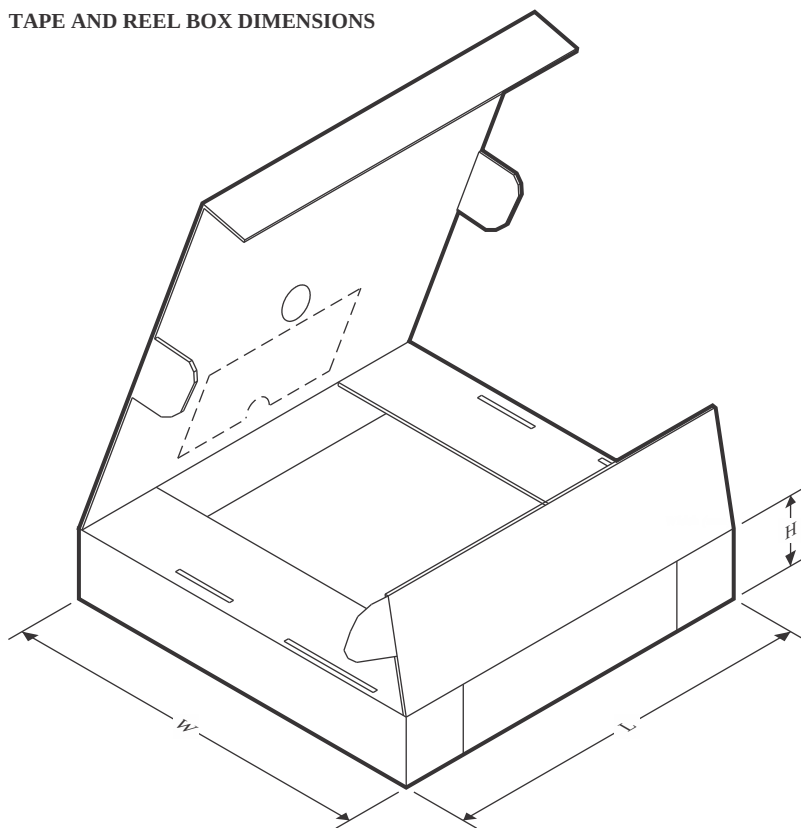
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5102TPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5102TPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

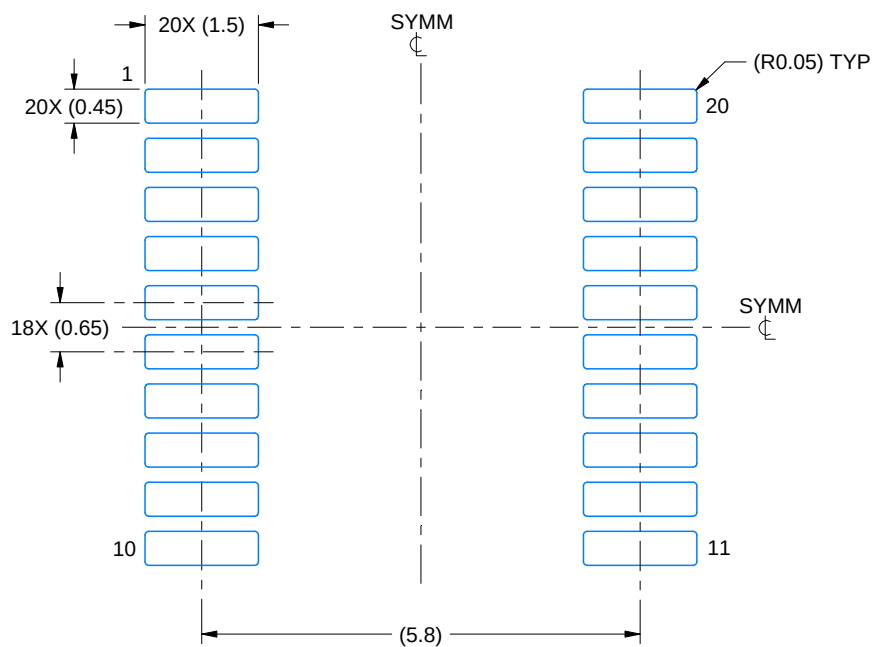


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

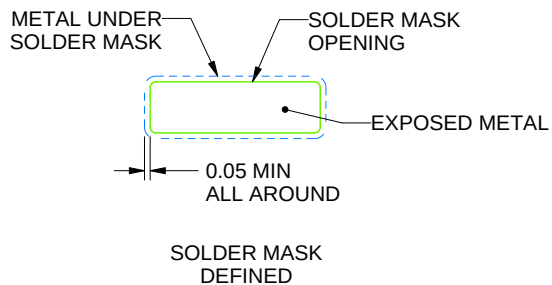
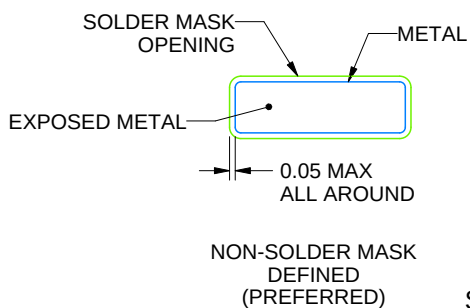
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

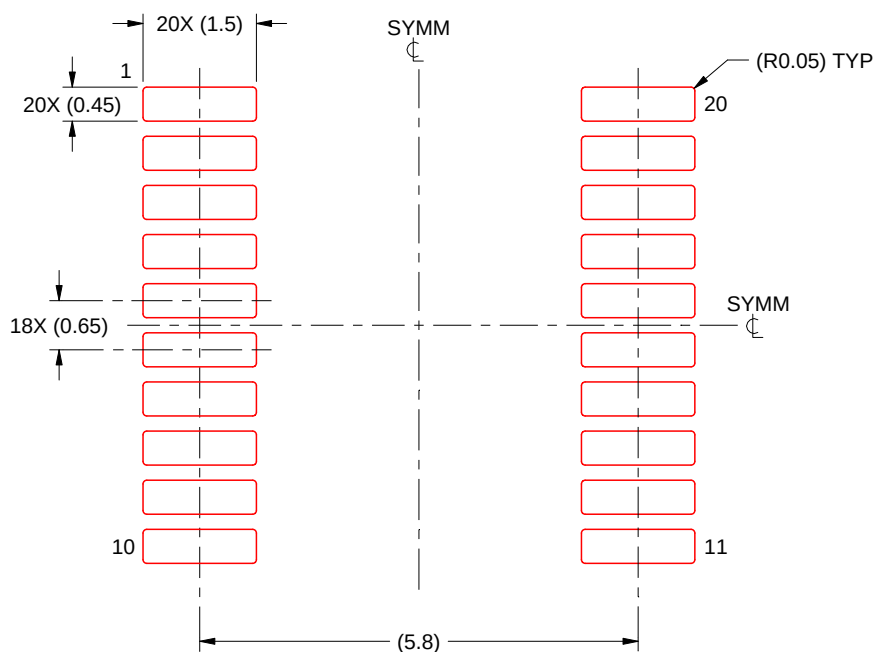
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

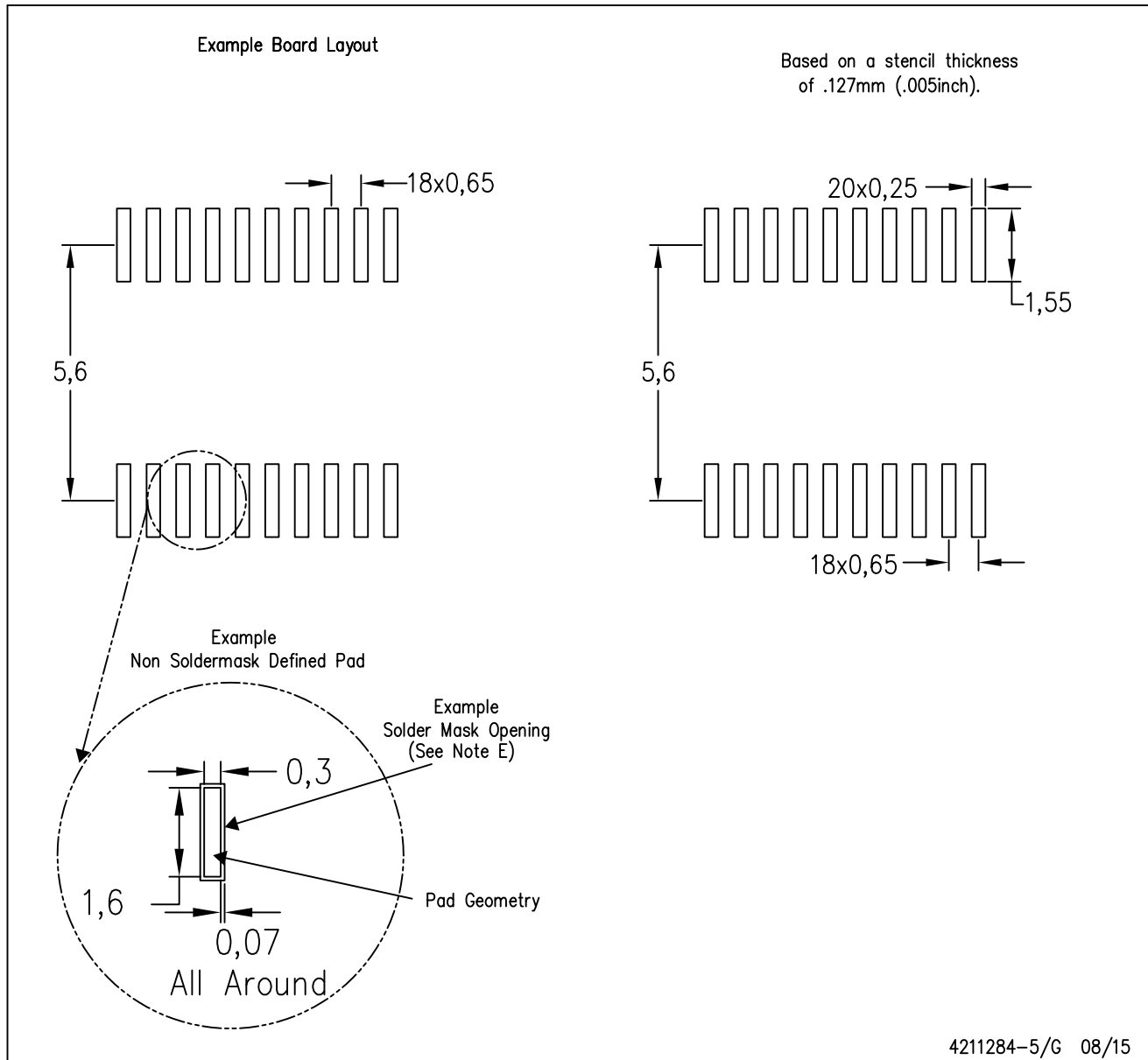
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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