DLP4710 0.47 1080p DMD

1 特性

- 0.47 英寸 (11.93mm) 对角线微镜阵列
  - 1920 × 1080 铝制微米级微镜阵列，正交布局
  - 5.4 – 微米微镜间距
  - ±17° 微镜倾斜度（相对于平面）
  - 底部照明，实现最优的效率和光学引擎尺寸
  - 偏振无关型铝微镜表面
- 32 位 SubLVDS 输入数据总线
- 专用 DLPC3439 显示控制器和 DLPA3000/DLPA3005 电源管理集成电路 (PMIC)/发光二极管 (LED) 驱动器，确保可靠运行

2 应用

- 智能全高清 (HD) 投影仪
- 移动式附件全 HD 投影仪
- 无屏幕显示器
- 交互式显示屏
- 低延迟游戏显示屏
- 头戴式显示器

3 说明

DLP4710 数字微镜器件 (DMD) 是一款数控微光机电系统 (MOEMS) 空间照明调制器 (SLM)。 当与适当的光学系统耦合时，DLP4710 DMD 可显示非常清晰的高质量图像或视频。 DLP4710 是 DLP4710 DMD、DLPC3439 显示控制器和 DLPA3000/DLPA3005 PMIC/LED 驱动器所组成的芯片组的一部分。

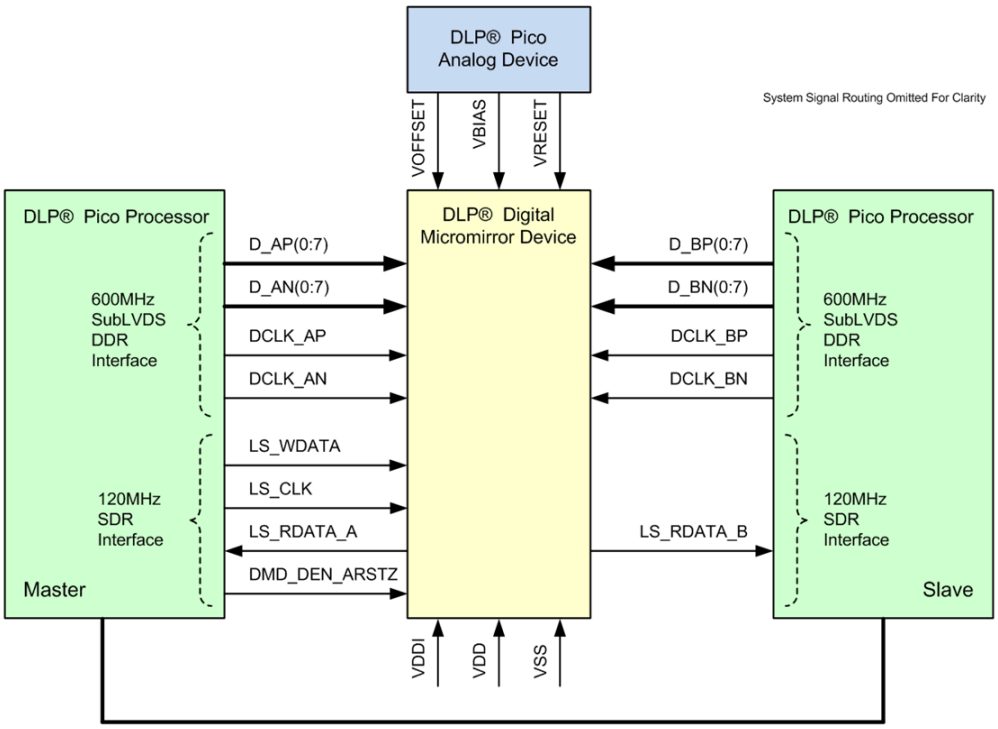
DLP4710 紧凑的物理尺寸连同控制器和 PMIC/LED 驱动器共同组成了完整的系统解决方案，从而实现了小外形尺寸、低功耗以及高分辨率 HD 显示。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLP4710	CLGA (100)	24.50mm × 11mm × 3.80mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

DLP® DLP4710 0.47 1080p 芯片组



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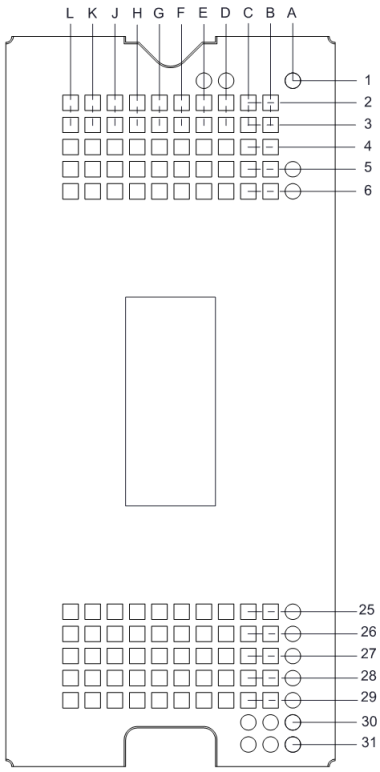
4 修订历史记录

Changes from Original (November 2014) to Revision A **Page**

- 已将器件状态从产品预览更改为量产数据并已发布完整版文档 1

5 Pin Configuration and Functions

FQL Package
100-Pin CLGA
Bottom View



Pin Functions – Connector Pins(1)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
DATA INPUTS						
D_AN(0)	G3	I	SubLVDS	Double	Data, Negative	5.01
D_AN(1)	F4	I	SubLVDS	Double	Data, Negative	2.03
D_AN(2)	E3	I	SubLVDS	Double	Data, Negative	2.41
D_AN(3)	E6	I	SubLVDS	Double	Data, Negative	4.71
D_AN(4)	J5	I	SubLVDS	Double	Data, Negative	3.23
D_AN(5)	L5	I	SubLVDS	Double	Data, Negative	3.87
D_AN(6)	G5	I	SubLVDS	Double	Data, Negative	6.32
D_AN(7)	L3	I	SubLVDS	Double	Data, Negative	1.84
D_AP(0)	H3	I	SubLVDS	Double	Data, Positive	5.01
D_AP(1)	G4	I	SubLVDS	Double	Data, Positive	2.03
D_AP(2)	E4	I	SubLVDS	Double	Data, Positive	2.41
D_AP(3)	E5	I	SubLVDS	Double	Data, Positive	4.71
D_AP(4)	J6	I	SubLVDS	Double	Data, Positive	3.23

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQL ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769 inches/ns.
Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.

Pin Functions – Connector Pins(1) (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
D_AP(5)	L6	I	SubLVDS	Double	Data, Positive	3.87
D_AP(6)	G6	I	SubLVDS	Double	Data, Positive	6.32
D_AP(7)	L4	I	SubLVDS	Double	Data, Positive	1.84
D_BN(0)	G27	I	SubLVDS	Double	Data, Negative	2.51
D_BN(1)	E26	I	SubLVDS	Double	Data, Negative	4.43
D_BN(2)	D28	I	SubLVDS	Double	Data, Negative	2.76
D_BN(3)	D26	I	SubLVDS	Double	Data, Negative	5.47
D_BN(4)	L25	I	SubLVDS	Double	Data, Negative	4.85
D_BN(5)	K25	I	SubLVDS	Double	Data, Negative	4.10
D_BN(6)	L28	I	SubLVDS	Double	Data, Negative	2.53
D_BN(7)	K27	I	SubLVDS	Double	Data, Negative	2.76
D_BP(0)	F27	I	SubLVDS	Double	Data, Positive	2.51
D_BP(1)	E27	I	SubLVDS	Double	Data, Positive	4.43
D_BP(2)	D27	I	SubLVDS	Double	Data, Positive	2.76
D_BP(3)	D25	I	SubLVDS	Double	Data, Positive	5.47
D_BP(4)	L26	I	SubLVDS	Double	Data, Positive	4.85
D_BP(5)	J25	I	SubLVDS	Double	Data, Positive	4.10
D_BP(6)	K28	I	SubLVDS	Double	Data, Positive	2.53
D_BP(7)	J27	I	SubLVDS	Double	Data, Positive	2.76
DCLK_AN	J3	I	SubLVDS	Double	Clock, Negative	3.77
DCLK_AP	K3	I	SubLVDS	Double	Clock, Positive	3.77
DCLK_BN	H26	I	SubLVDS	Double	Clock, Negative	2.98
DCLK_BP	H27	I	SubLVDS	Double	Clock, Positive	2.98
CONTROL INPUTS						
LS_WDATA	D3	I	LPSDR(1)	Single	Write data for low speed interface.	1.20
LS_CLK	C3	I	LPSDR	Single	Clock for low-speed interface	1.20
DMD_DEN_ARSTZ	B6	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	4.19
LS_RDATA_A	C6	O	LPSDR	Single	Read data for low-speed interface	3.93
LS_RDATA_B	C4	O	LPSDR	Single	Read data for low-speed interface	2.57
POWER						
VBIAS(3)	B27	Power			Supply voltage for positive bias level at micromirrors	24.51
VBIAS(3)	B4	Power				24.51
VOFFSET(3)	B2	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.	49.56
VOFFSET(3)	C29	Power				49.56
VRESET	B28	Power			Supply voltage for negative reset level at micromirrors.	24.82
VRESET	B3	Power				24.82

(3) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, VRESET. All VSS connections are also required.

Pin Functions – Connector Pins[1] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
VDD[3]	C2	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes.	
VDD	D2	Power				
VDD	D29	Power				
VDD	E2	Power				
VDD	E29	Power				
VDD	H2	Power				
VDD	H28	Power				
VDD	H29	Power				
VDD	J2	Power				
VDD	J28	Power				
VDD	J29	Power				
VDD	K2	Power				
VDD	K29	Power				
VDD	L2	Power				
VDD	L29	Power				
VDDI	E28	Power			Supply voltage for SubLVDS receivers.	
VDDI	F2	Power				
VDDI	F28	Power				
VDDI	F29	Power				
VDDI	F3	Power				
VDDI	G2	Power				
VDDI	G28	Power				
VDDI	G29	Power				

Pin Functions – Connector Pins[1] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
VSS	B25	Ground			Common return. Ground for all power.	
VSS	B26	Ground				
VSS	B29	Ground				
VSS	B5	Ground				
VSS	C25	Ground				
VSS	C26	Ground				
VSS	C27	Ground				
VSS	C28	Ground				
VSS	C5	Ground				
VSS	D4	Ground				
VSS	D5	Ground				
VSS	D6	Ground				
VSS	E25	Ground				
VSS	F25	Ground				
VSS	F26	Ground				
VSS	F5	Ground				
VSS	F6	Ground				
VSS	G25	Ground				
VSS	G26	Ground				
VSS	H25	Ground				
VSS	H4	Ground				
VSS	H5	Ground				
VSS	H6	Ground				
VSS	J26	Ground				
VSS	J4	Ground				
VSS	K26	Ground				
VSS	K4	Ground				
VSS	K5	Ground				
VSS	K6	Ground				
VSS	L27	Ground				

Pin Functions – Test Pads

NUMBER	SYSTEM BOARD
A1	Do not connect
A5	Do not connect
A6	Do not connect
A25	Do not connect
A26	Do not connect
A27	Do not connect
A28	Do not connect
A29	Do not connect
A30	Do not connect
A31	Do not connect
B30	Do not connect
B31	Do not connect
C30	Do not connect
C31	Do not connect
D1	Do not connect
E1	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

			MIN	MAX	UNIT
Supply voltage	VDD	Supply voltage for LVCMOS core logic (2) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	VDDI	Supply voltage for SubLVDS receivers (2)	–0.5	2.3	V
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode (2) (3)	–0.5	11	V
	VBIAS	Supply voltage for micromirror electrode (2)	–0.5	19	V
	VRESET	Supply voltage for micromirror electrode (2)	–15	0.3	V
	| VDDI–VDD |	Supply voltage delta (absolute value) (4)		0.3	V
	| VBIAS–VOFFSET |	Supply voltage delta (absolute value) (5)		11	V
	| VBIAS–VRESET |	Supply voltage delta (absolute value) (6)		34	V
Input voltage	Input voltage for other inputs LPSDR (2)		–0.5	VDD + 0.5	V
	Input voltage for other inputs SubLVDS (2) (7)		–0.5	VDDI + 0.5	V
Input pins	| VID |	SubLVDS input differential voltage (absolute value) (7)		810	mV
	IID	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational (8)	–20	90	°C
		Temperature – non-operational (8)	–40	90	°C
	T_{DP}	Dew Point - operating and non-operating		81	°C
	$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1 (9)		30	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(3) VOFFSET supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated by the *Micromirror Array Temperature Calculation*) or of any point along the Window Edge as defined in Figure 18. The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 18 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 18. The window test points TP2, TP3, TP4, and TP5 shown in Figure 18 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable before the DMD is installed in the final product

			MIN	MAX	UNIT
T_{stg}	DMD storage temperature		-40	85	°C
T_{DP}	Storage dew point	Long-term (1)		24	°C
		Short-term (2)		28	

(1) Long-term is defined as the usable life of the device.
(2) Dew points beyond the specified long-term dew point are for short-term conditions only, where short-term is defined as less than 60 cumulative days over the usable life of the device (operating, non-operating, or storage).

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(4)					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.7	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.7	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(5)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
$\lvert V_{DDI} – V_{DD} \rvert$	Supply voltage delta (absolute value)(6)			0.3	V
$\lvert V_{BIAS} – V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(7)			10.5	V
$\lvert V_{BIAS} – V_{RESET} \rvert$	Supply voltage delta (absolute value)(8)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(9)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(10)	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE(10)					
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value) Figure 8 , Figure 9	150	250	350	mV
V_{CM}	Common mode voltage Figure 8 , Figure 9	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage Figure 8, Figure 9	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance Figure 10	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

(1) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(2) *Recommended Operating Conditions* are applicable after the DMD is installed in the final product.
(3) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(4) All voltage values are with respect to the ground pins (VSS).
(5) VOFFSET supply transients must fall within specified max voltages.
(6) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(7) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(8) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit.
(9) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(10) Refer to the SubLVDS timing requirements in *Timing Requirements*.

Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational(11) (12) (13) (14)	0		40 to 70(13)	°C
	Array Temperature – short-term operational(12) (15)	–20		75	
T_{DP}	Dew Point - long-term average (operational and non-operational)(14)			24	°C
	Dew Point - short-term (operational and non-operational)(16)			28	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1(17)			30	°C
T_{WINDOW}	Window Temperature – operational(11) (18)			90	°C
ILL_{UV}	Illumination wavelengths < 400 nm (11)			0.68	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 400 nm and 700 nm			Thermally limited	
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2

(11) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 18 and the package thermal resistance using *Micromirror Array Temperature Calculation*.
(13) Per Figure 1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(14) Long-term is defined as the usable life of the device.
(15) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours for temperatures between the long-term maximum and 75ºC, less than 500 hours for temperatures between 0ºC and –10ºC, and less than 25 hours for temperatures between -10ºC and -20ºC.
(16) Dew points beyond the specified long-term dew point are for short-term conditions only, where short-term is defined as less than 60 cumulative days over the usable life of the device (operating, non-operating, or storage).
(17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in Figure 18. The window test points TP2, TP3, TP4, and TP5 shown in Figure 18 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(18) Window temperature is the highest temperature on the window edge shown in Figure 18. The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 18 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.

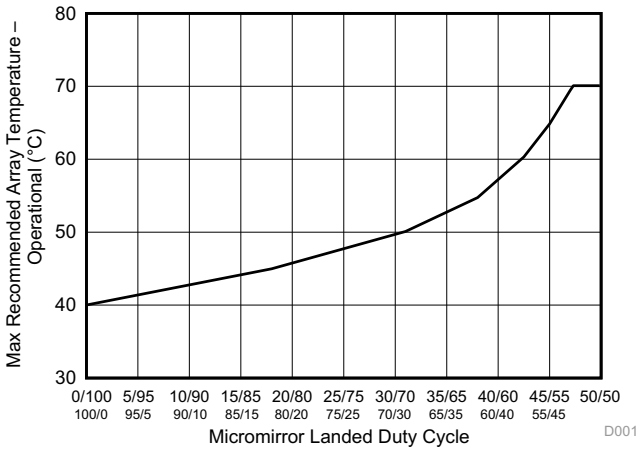


Figure 1. Max Recommended Array Temperature – Derating Curve

6.5 Thermal Information

THERMAL METRIC[1]	FQL (LGA) 100 PINS MIN	TYP	MAX	UNIT
Thermal resistance Active area to test point 1 (TP1)[1]			1.1	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS[2]	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD[3] [4]	VDD = 1.95 V			260	mA
		VDD = 1.8 V		180		
I_{DDI}	Supply current: VDDI[3] [4]	VDDI = 1.95 V			62	mA
		VDD = 1.8 V		40		
I_{OFFSET}	Supply current: VOFFSET[5] [6]	VOFFSET = 10.5 V			7.4	mA
		VOFFSET = 10 V		6.3		
I_{BIAS}	Supply current: VBIAS[5] [6]	VBIAS = 18.5 V			1.1	mA
		VBIAS = 18 V		0.9		
I_{RESET}	Supply current: VRESET[6]	VRESET = –14.5 V			5.4	mA
		VRESET = –14 V		4.4		
POWER[7]						
P_{DD}	Supply power dissipation: VDD[3] [4]	VDD = 1.95 V			507	mW
		VDD = 1.8 V		324		
P_{DDI}	Supply power dissipation: VDDI[3] [4]	VDDI = 1.95 V			120.9	mW
		VDD = 1.8 V		72		
P_{OFFSET}	Supply power dissipation: VOFFSET[5] [6]	VOFFSET = 10.5 V			77.7	mW
		VOFFSET = 10 V		63		
P_{BIAS}	Supply power dissipation: VBIAS[5] [6]	VBIAS = 18.5 V			20.35	mW
		VBIAS = 18 V		16.2		
P_{RESET}	Supply power dissipation: VRESET[6]	VRESET = –14.5 V			78.3	mW
		VRESET = –14 V		61.6		
P_{TOTAL}	Supply power dissipation: Total			536.8	804.25	mW
LPSDR INPUT[8]						
$V_{IH(DC)}$	DC input high voltage[9]		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage[9]		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage[9]		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage[9]		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	Figure 10	0.1 × VDD		0.4 × VDD	V

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (VSS).
(3) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, VRESET. All VSS connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × VDD			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz; (1080 × 240) micromirrors	400		450	pF

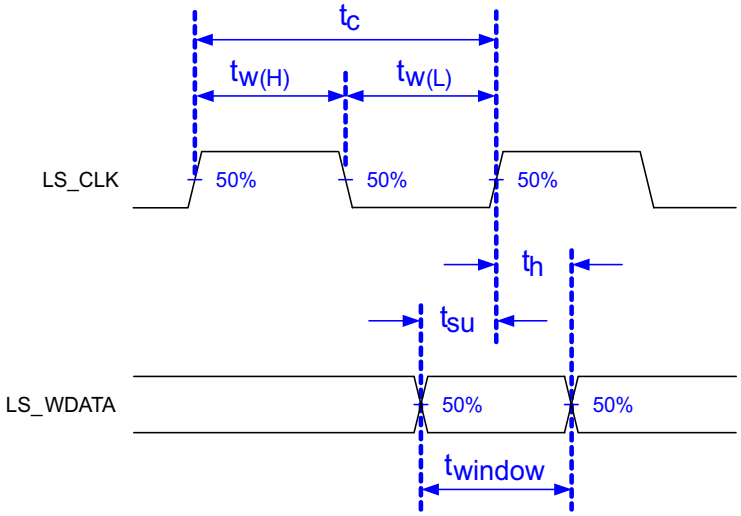
(10) LPSDR specification is for pin LS_RDATA.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(30% to 80%) × VDD, Figure 3	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × VDD, Figure 3	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × VDD, Figure 3	0.25			V/ns
t_f	Fall slew rate(2)	(80% to 20%) × VDD, Figure 3	0.25			V/ns
t_c	Cycle time LS_CLK,	Figure 2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, Figure 2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, Figure 2	3.1			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑, Figure 2	1.5			ns
t_h	Hold time	LS_WDATA valid after LS_CLK ↑, Figure 2	1.5			ns
t_{WINDOW}	Window time(1) (3)	Setup time + Hold time, Figure 2	3			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, Figure 5		0.35		ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, Figure 4	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, Figure 4	0.7	1		V/ns
t_c	Cycle time DCLK,	Figure 6	1.79	1.85		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, Figure 6	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, Figure 6	0.79			ns
t_{su}	Setup time	D(0:7) valid before DCLK ↑ or DCLK ↓, Figure 6				
t_h	Hold time	D(0:7) valid after DCLK ↑ or DCLK ↓, Figure 6				
t_{WINDOW}	Window time	Setup time + Hold time, Figure 6, Figure 7			0.3	ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(4)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in Figure 3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 3.
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.



Low-speed interface is LPSDR and adheres to the *Electrical Characteristics* and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

Figure 2. LPSDR Switching Parameters

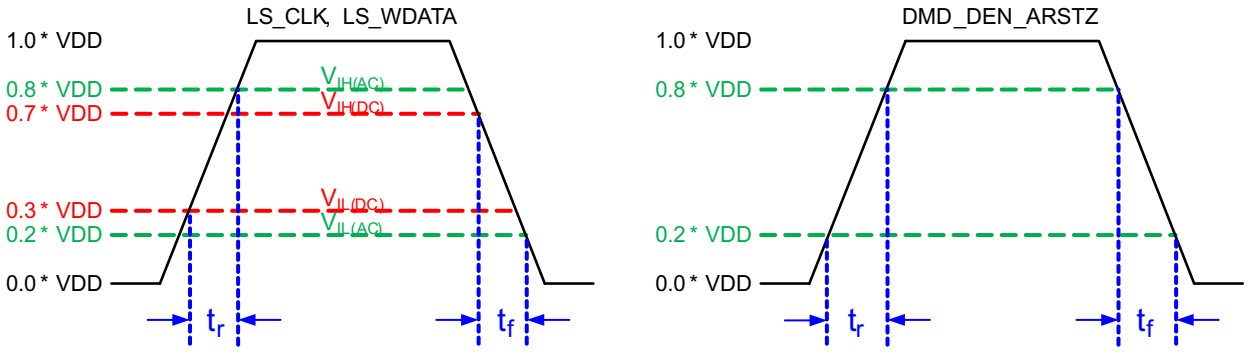


Figure 3. LPSDR Input Rise and Fall Slew Rate

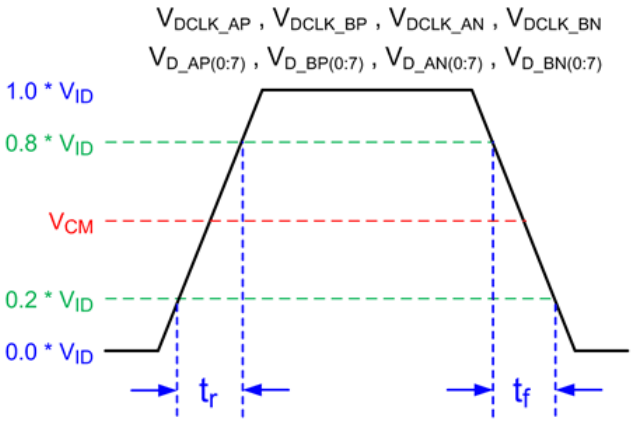


Figure 4. SubLVDS Input Rise and Fall Slew Rate

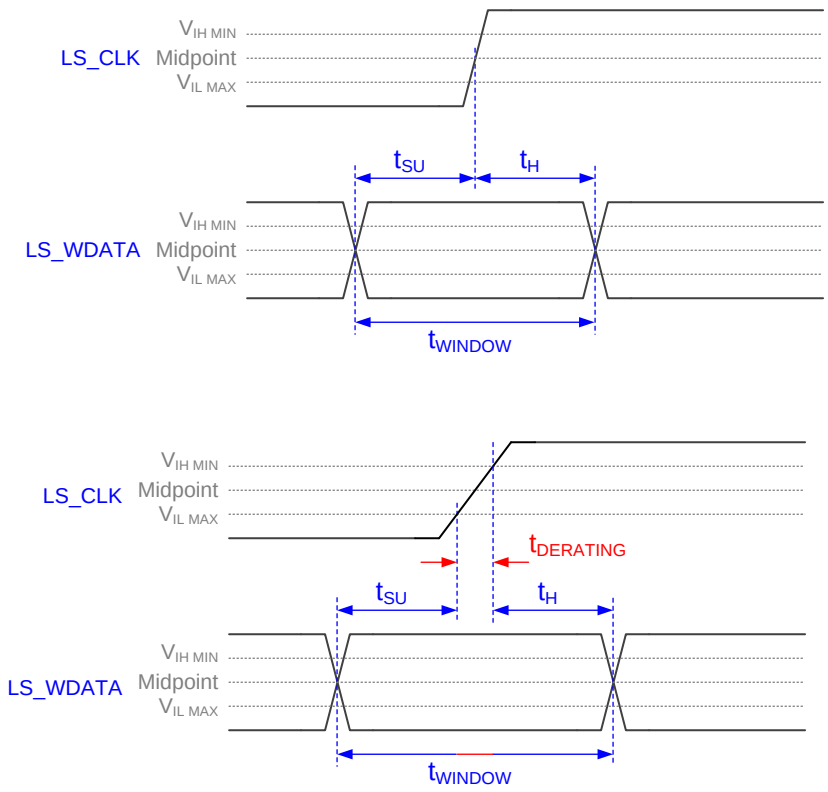


Figure 5. Window Time Derating Concept

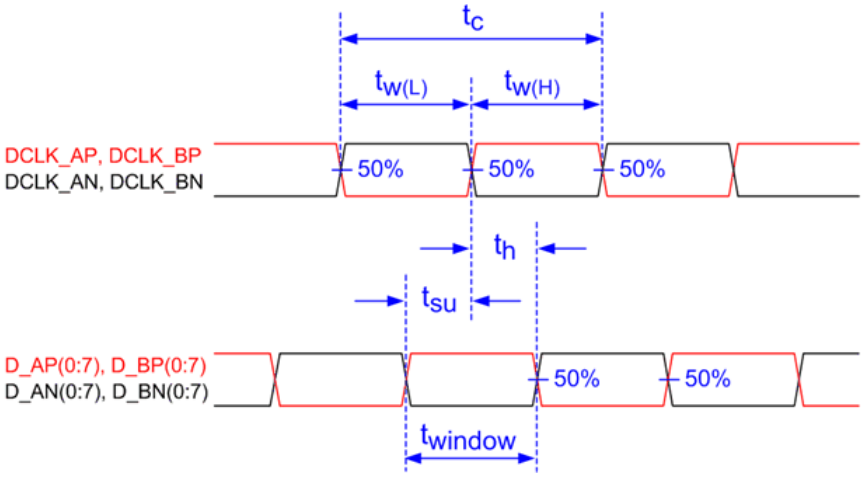
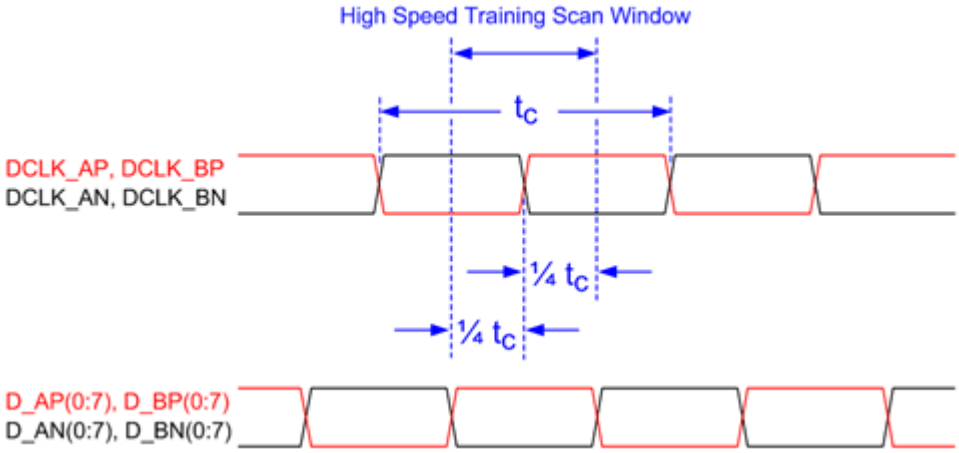


Figure 6. SubLVDS Switching Parameters



Note: Refer to *High-Speed Interface* for details.

Figure 7. High-Speed Training Scan Window

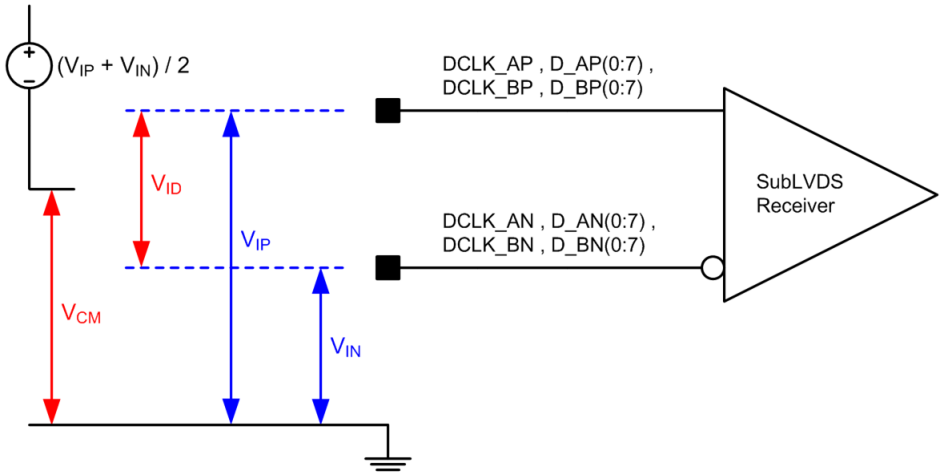


Figure 8. SubLVDS Voltage Parameters

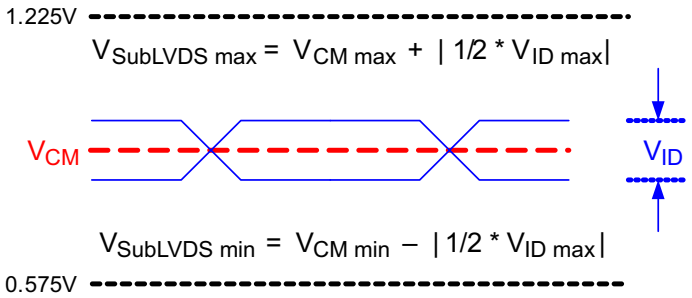


Figure 9. SubLVDS Waveform Parameters

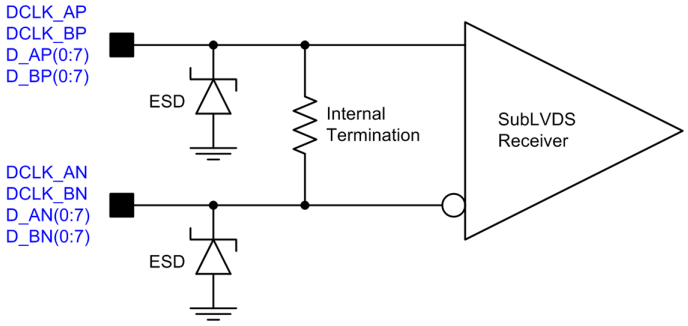


Figure 10. SubLVDS Equivalent Input Circuit

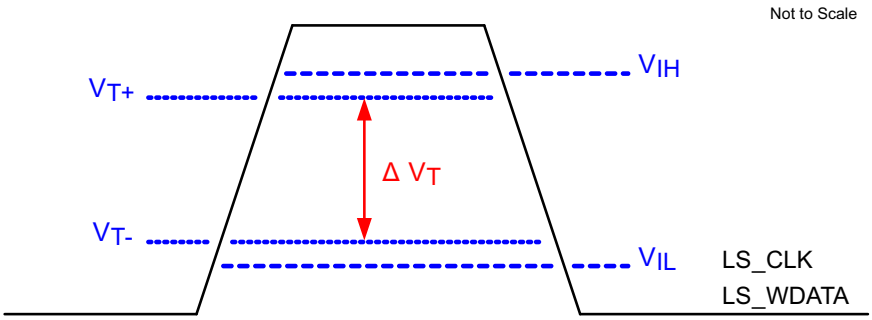


Figure 11. LPSDR Input Hysteresis

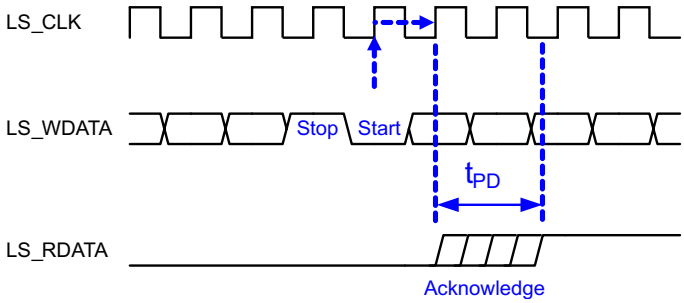
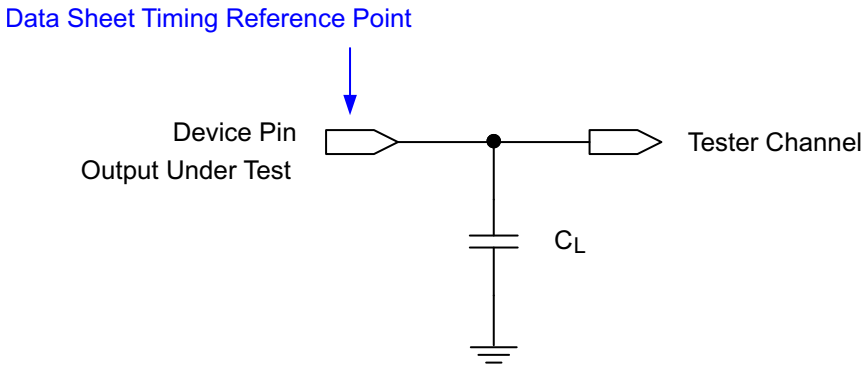


Figure 12. LPSDR Read Out



See *Timing* for more information.

Figure 13. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output. Figure 12	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
		C_L = 85 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over **Recommended Operating Conditions** unless otherwise noted.

6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:				
• Thermal Interface Area (see Figure 14)			62	N
• Clamping and Electrical Interface Area (see Figure 14)			110	N

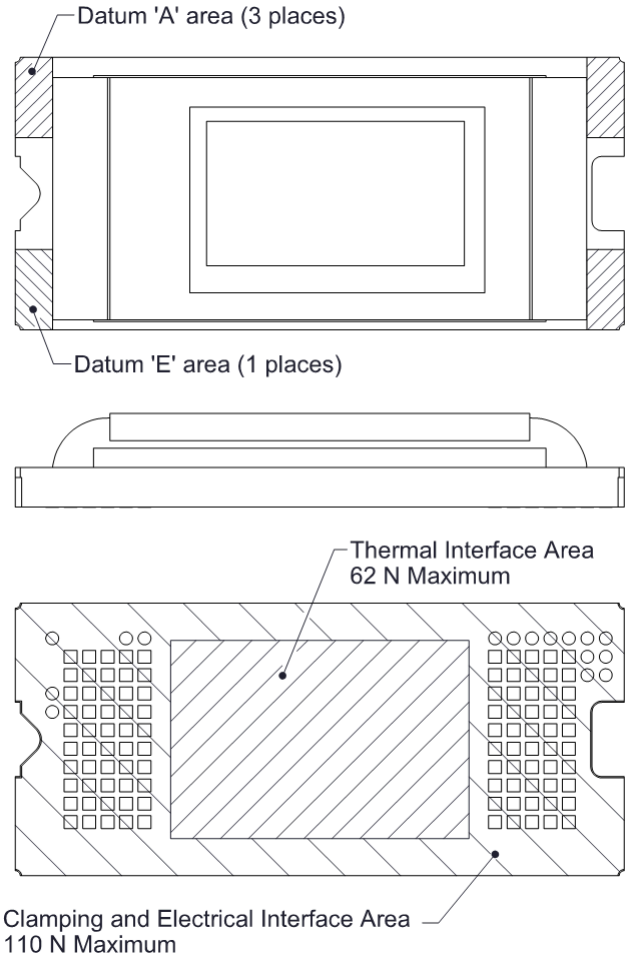


Figure 14. System Interface Loads

6.10 Physical Characteristics of the Micromirror Array

	PARAMETER		VALUE	UNIT
	Number of active columns	See Figure 15	1920	micromirrors
	Number of active rows	See Figure 15	1080	micromirrors
ε	Micromirror (pixel) pitch	See Figure 16	5.4	µm
	Micromirror active array width	Micromirror pitch × number of active columns; see Figure 15	10.368	mm
	Micromirror active array height	Micromirror pitch × number of active rows; see Figure 15	5.832	mm
	Micromirror active border	Pond of micromirror (POM) (1)	20	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

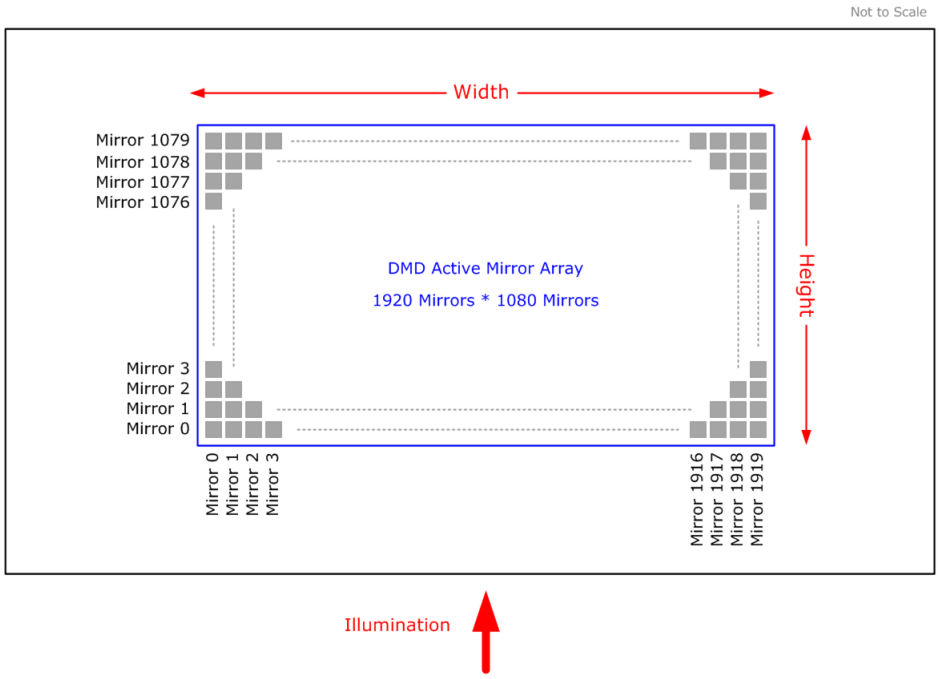


Figure 15. Micromirror Array Physical Characteristics

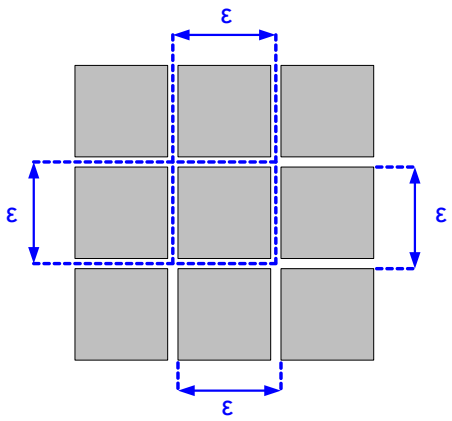


Figure 16. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		17		°
Micromirror tilt angle tolerance(2) (3) (4) (5)		–1		1	°
Micromirror tilt direction(6) (7)	Landed ON state		180		°
	Landed OFF state		270		
Micromirror crossover time	Typical Performance		1.5	4	µs
Micromirror switching time	Typical Performance			6	
Number of out-of-specification micromirrors(8)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.

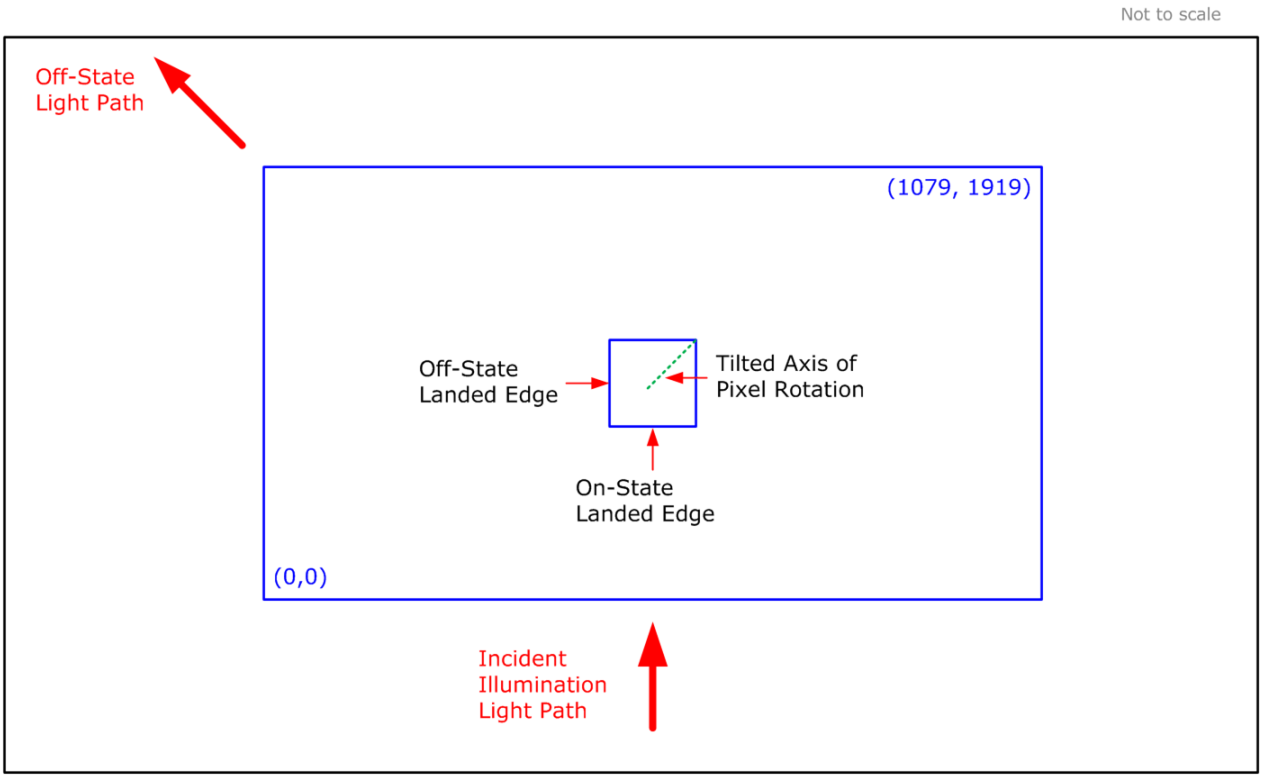


Figure 17. Landed Pixel Orientation and Tilt

6.12 Window Characteristics

PARAMETER(1)		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture(2)				See (2)	
Illumination overfill(3)				See (3)	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Window Characteristics and Optics* for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP4710 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

6.13 Chipset Component Usage Specification

The DLP4710 is a component of one or more DLP chipsets. Reliable function and operation of the DLP4710 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously

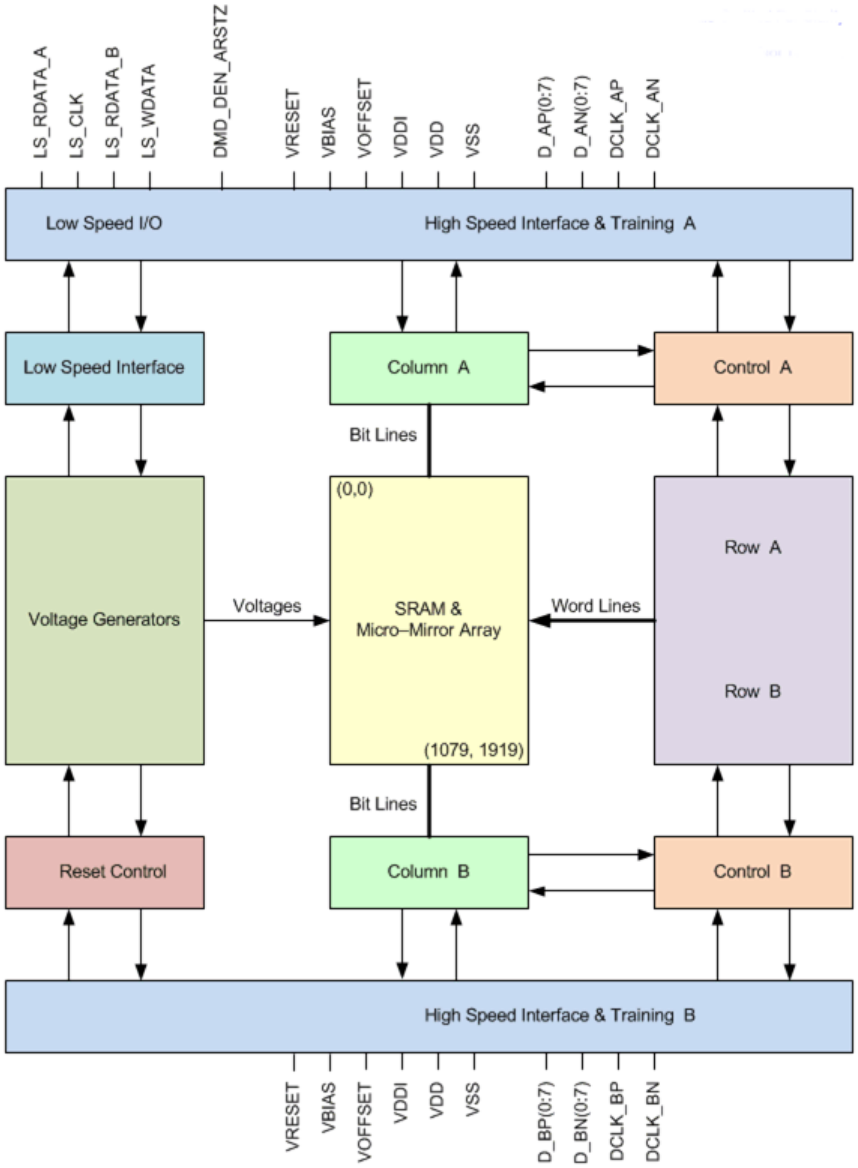
7 Detailed Description

7.1 Overview

The DLP4710 is a 0.47 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1920 columns by 1080 rows in a square grid pixel arrangement. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

DLP4710 is part of the chipset comprising of the DLP4710 DMD, DLPC3439 display controller and DLPA3000/DLPA3005 PMIC/LED driver. To ensure reliable operation, DLP4710 DMD must always be used with DLPC3439 display controller and DLPA3000/DLPA3005 PMIC/LED drivers.

7.2 Functional Block Diagram



(1) Details omitted for clarity.

7.3 Feature Description

7.3.1 Power Interface

The power management IC, DLPA3000/DLPA3005, contains 3 regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the 2 regulated DC supplies for the DLPC3439 controller.

7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3439 controller. See the DLPC3439 controller data sheet or contact a TI applications engineer.

7.5 Window Characteristics and Optics

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections:

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the ON optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.5.1.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

Window Characteristics and Optics (continued)

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

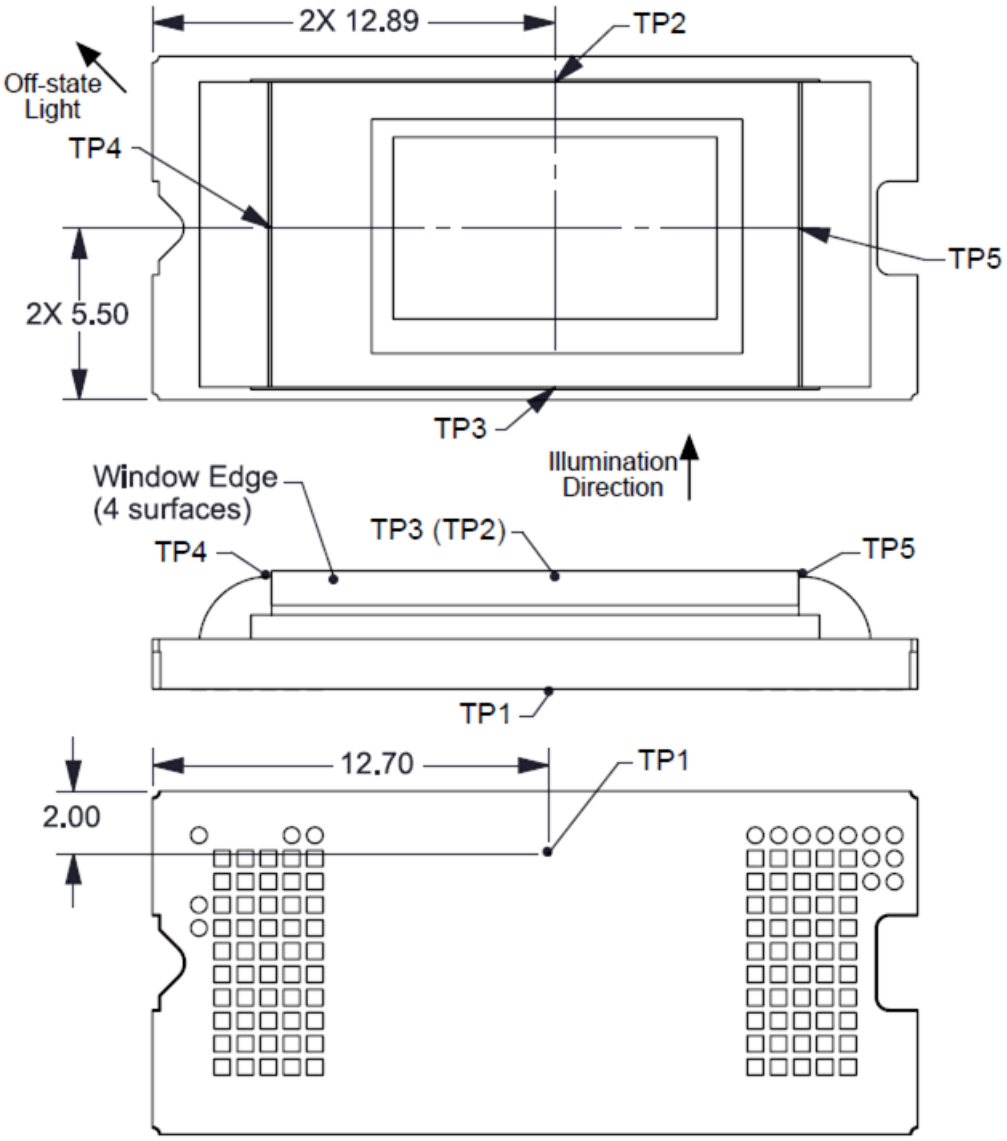


Figure 18. DMD Thermal Test Points

Micromirror Array Temperature Calculation (continued)

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (3)$$

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 18
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to outside ceramic (°C/W) specified in *Thermal Information*
- Q_{ARRAY} = Total DMD power; electrical, specified in *Electrical Characteristics* , plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W), specified in *Electrical Characteristics*
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. Refer to the specifications in *Electrical Characteristics* . Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00266 W/lm.

Sample Calculation for typical projection application:

1. $T_{CERAMIC}$ = 55°C, assumed system measurement; see *Recommended Operating Conditions* for specification limits.
2. SL = 1500 lm
3. $Q_{ELECTRICAL}$ = 1.1 W; See the table notes in *Recommended Operating Conditions* for details.
4. CL2W = 0.00266 W/lm
5. Q_{ARRAY} = 0.25 + (0.00266 × 1500) = 4.24 W
6. T_{ARRAY} = 55°C + (4.24 W × 1.1°C/W) = 59.66°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time), whereas 0/100 would indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a given long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 1.

Table 1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_%×Blue_Scale_Value)

where
Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%. represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (4)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 2.

Table 2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the Landed Duty Cycle is any applied image processing. Within the DLP Controller DLPC3439, the two functions which affect Landed Duty Cycle are Gamma and IntelliBright™.

Gamma is a power function of the form Output_Level = A × $Input\_Level^{Gamma}$, where A is a scaling factor that is typically set to 1.

In the DLPC3430/DLPC3435 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 19.

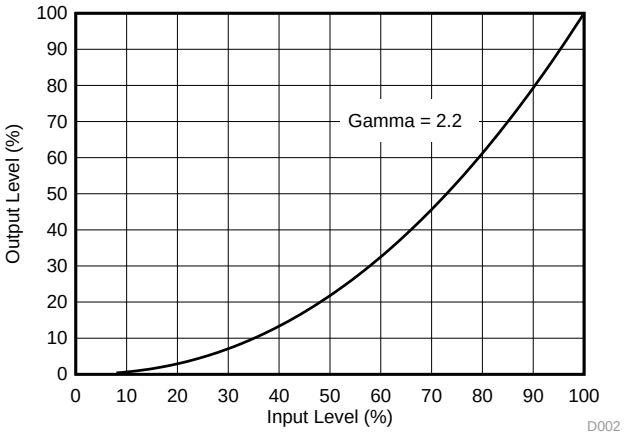


Figure 19. Example of Gamma = 2.2

From Figure 19, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while amount of gamma applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC3439 controller.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the dual DLPC3439 controllers. The new high tilt pixel in the bottom-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness constrained applications. Applications of interest include projection embedded in display devices like smartphones, tablets, cameras, and camcorders. Other applications include wearable (near-eye) displays, battery powered mobile accessory, interactive display, low-latency gaming display, and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPA3000/DLPA3005. Refer to Power Supply Recommendations for power-up and power-down specifications. To ensure reliable operation, the DLP4710 DMD must always be used with two DLPC3439 display controllers and a DLPA3000/DLPA3005 PMIC/LED driver.

8.2 Typical Application

A common application when using a DLP4710 DMD and two DLPC3439s is for creating a pico-projector that can be used as an accessory to a smartphone, tablet or a laptop. The two DLPC3439s in the pico-projector receive images from a multimedia front end within the product as shown in Figure 20.

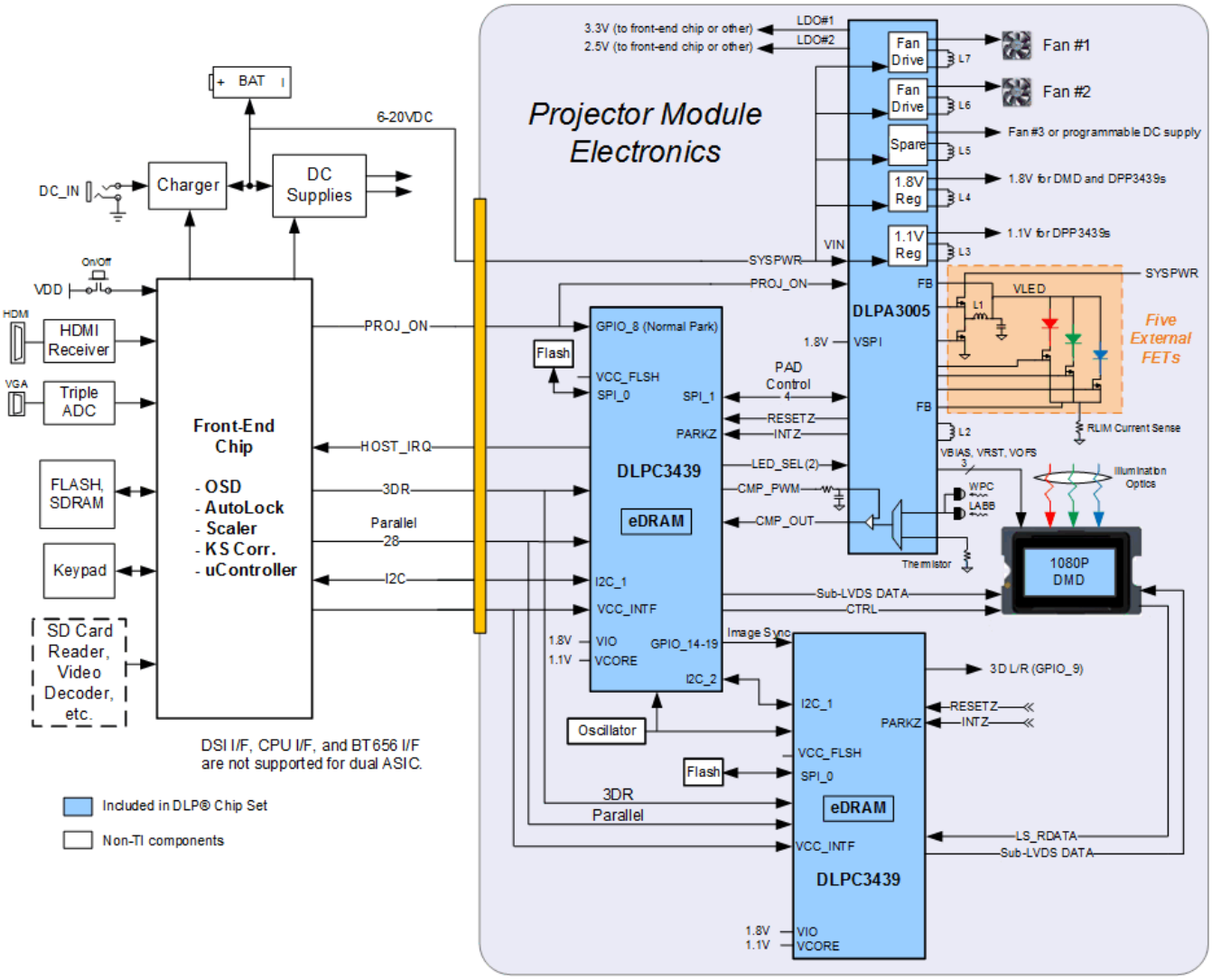


Figure 20. Typical Application Diagram

8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of a DLP4710 DMD, two DLPC3439 controllers and a DLPA3000/DLPA3005 PMIC/LED driver. The DLPC3439 controllers do the digital image processing, the DLPA3000/DLPA3005 provides the needed analog functions for the projector, and the DLP4710 DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chip set, other chips are needed. At a minimum a Flash part is needed to store the software and firmware to control each DLPC3439 controller.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

Typical Application (continued)

For connecting the DLPC3439 controllers to the multimedia front end for receiving images, a 24-bit parallel interface is used. An I2C interface should be connected to the multimedia front end for sending commands to one of the DLPC3439 controllers for configuring the DLPC3439 controller for different features.

8.2.2 Detailed Design Procedure

For connecting together the two DLPC3439 controllers, the DLPA3000/DLPA3005, and the DLP4710 DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in Figure 21. For the LED currents shown, it's assumed that the same current amplitude is applied to the red, green, and blue LEDs.

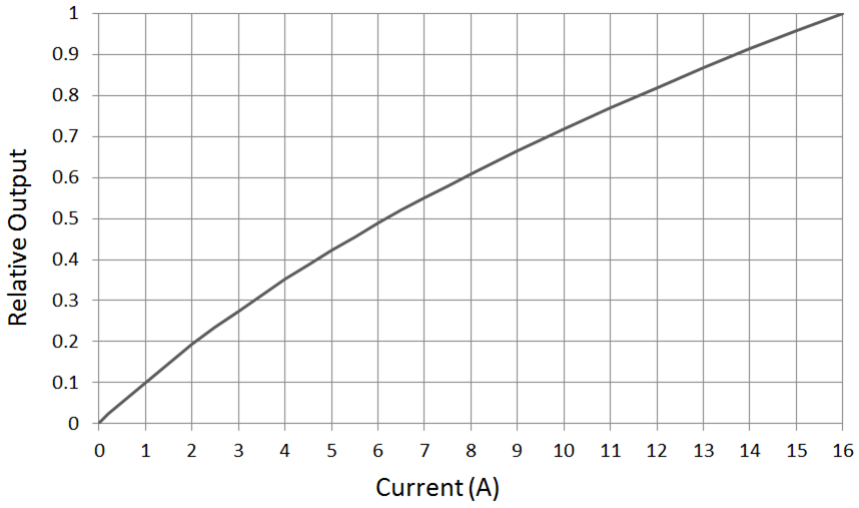


Figure 21. Luminance vs Current

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required. DMD power-up and power-down sequencing is strictly controlled by the DLPA3000/DLPA3005 devices.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 23. VSS must also be connected.

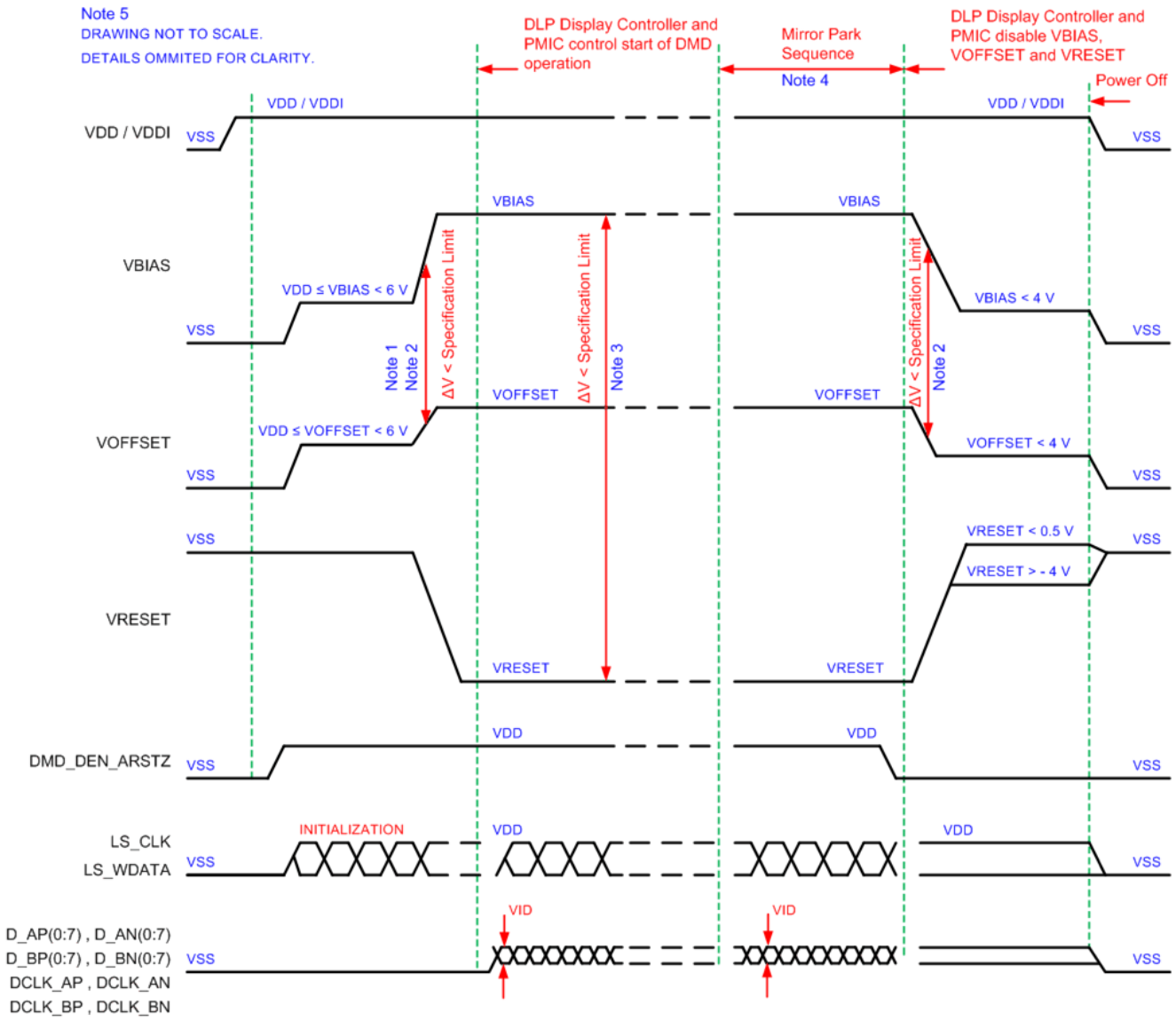
9.1 Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. Refer to Table 3 and the *Layout Example* for power-up delay requirements.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after VDD and VDDI have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 22.

9.2 Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions* (Refer to Note 2 for Figure 22).
- During power-down, the DMD's LPSDR input pins must be less than VDDI, the specified limit shown in *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 22.

9.3 Power Supply Sequencing Requirements



(1) Refer to Table 3 and Figure 23 for critical power-up sequence delay requirements.

(2) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in *Recommended Operating Conditions*. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down. Refer to Table 3 and Figure 23 for power-up delay requirements

(3) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit shown in *Recommended Operating Conditions*.

(4) When system power is interrupted, the DLPA3000/DLPA3005 initiates hardware power-down that disables VBIAS, VRESET and VOFFSET after the Micromirror Park Sequence.

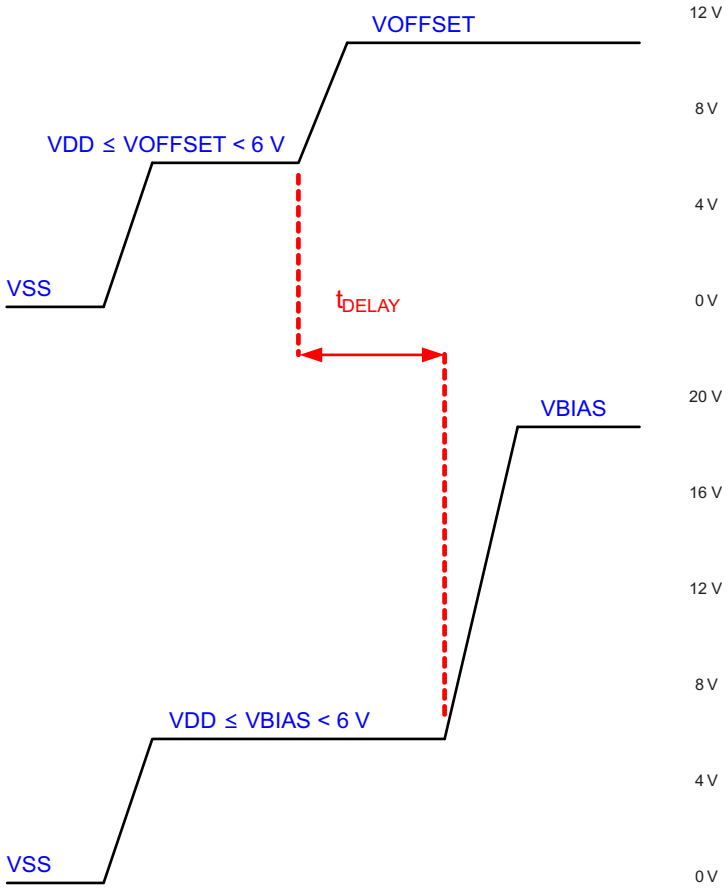
(5) Drawing is not to scale and details are omitted for clarity.

Figure 22. Power Supply Sequencing Requirements (Power Up and Power Down)

Power Supply Sequencing Requirements (continued)

Table 3. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from VOFFSET power up to VBIAS power up	2		ms
V_{OFFSET}	Supply voltage level at beginning of power–up sequence delay (see Figure 23)		6	V
V_{BIAS}	Supply voltage level at end of power–up sequence delay (see Figure 23)		6	V



Refer to Table 3 for VOFFSET and VBIAS supply voltage levels during power-up sequence delay.

Figure 23. Power-Up Sequence Delay Requirement

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and Ctrl signals between the DLPC343x controller and the DLP4710 DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer Figure 24.
- Minimum of two 220-nF decoupling capacitor close to VBIAS. Capacitor C3 and C10 in Figure 24.
- Minimum of two 220-nF decoupling capacitor close to VRST. Capacitor C1 and C9 in Figure 24.
- Minimum of two 220-nF decoupling capacitor close to VOFS. Capacitor C2 and C8 in Figure 24.
- Minimum of four 220-nF decoupling capacitor close to VDDI and VDD. Capacitor C4, C5, C6 and C7 in Figure 24.

10.2 Layout Example

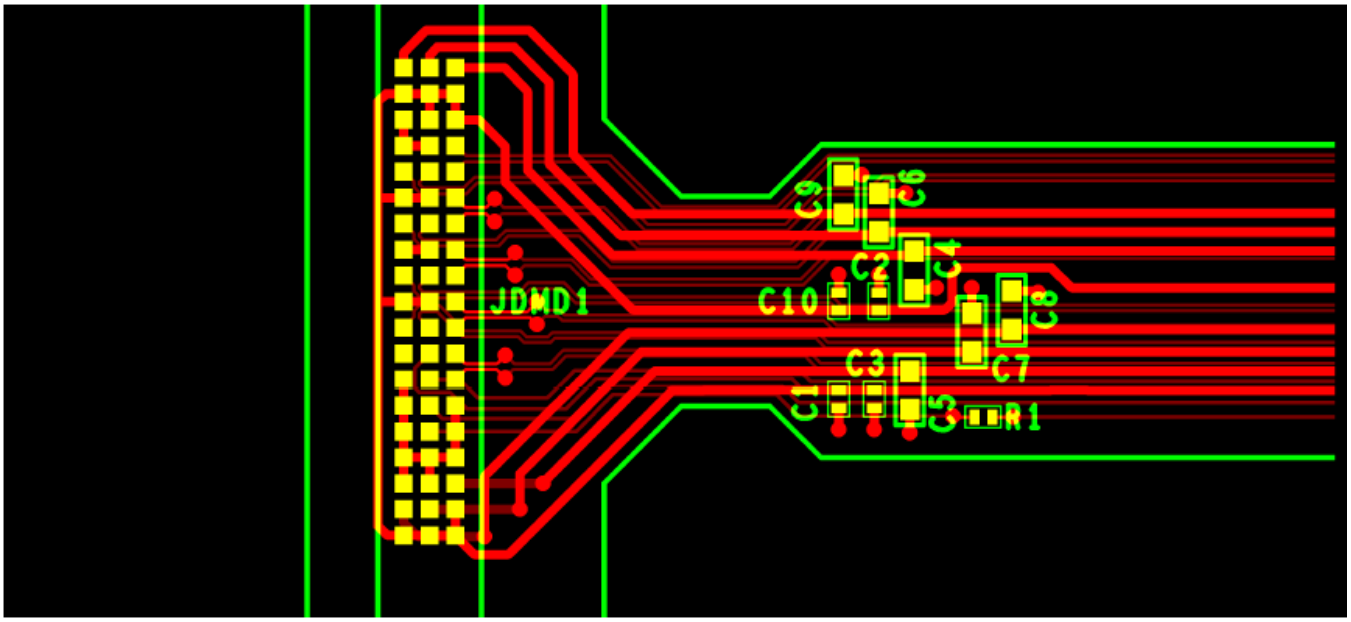


Figure 24. Power Supply Connections

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

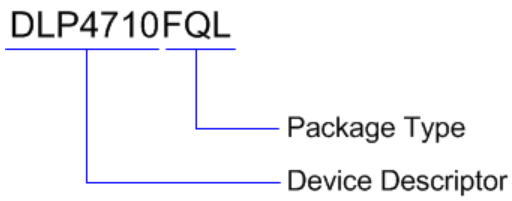


图 **25.** 部件号说明

11.1.2 器件标记

器件标记包括清晰可辨的字符串 GHJJJJK DLP4710FQL。 GHJJJJK 是批次跟踪代码。 DLP4710FQL 是器件标记。

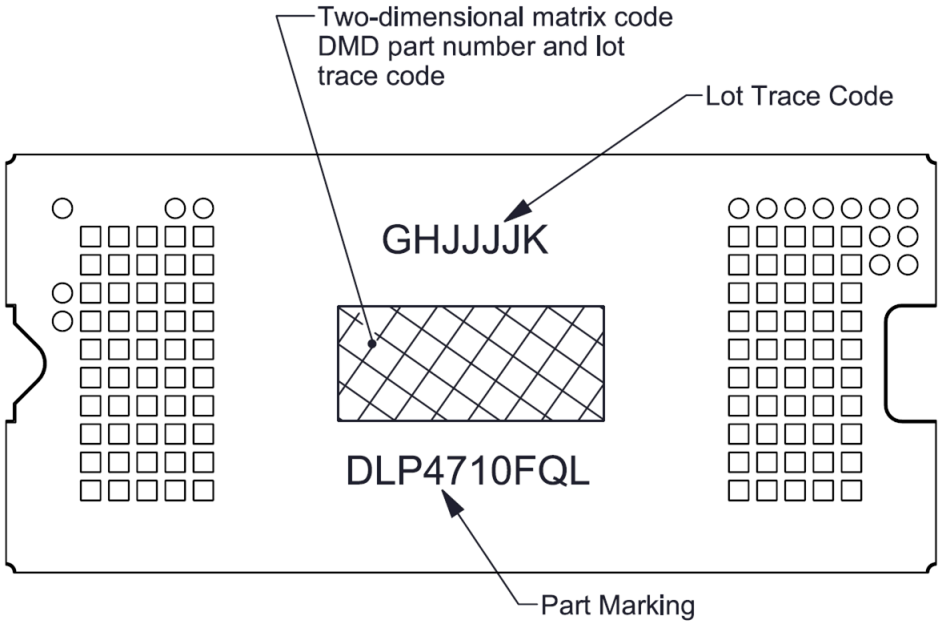


图 **26. DMD** 标记

11.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
DLP4710	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DLPC3439	请单击此处	单击此处	单击此处	单击此处	单击此处
DLPA3000	单击此处	单击此处	单击此处	单击此处	单击此处
DLPA3005	请单击此处	单击此处	单击此处	单击此处	单击此处

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

IntelliBright, E2E are trademarks of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP4710AFQL	Active	Production	CLGA (FQL) | 100	80 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	
DLP4710AFQL.A	Active	Production	CLGA (FQL) | 100	80 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	
DLP4710AFQL.B	Active	Production	CLGA (FQL) | 100	80 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	
DLP4710FQL	Obsolete	Production	CLGA (FQL) | 100	-	-			-	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

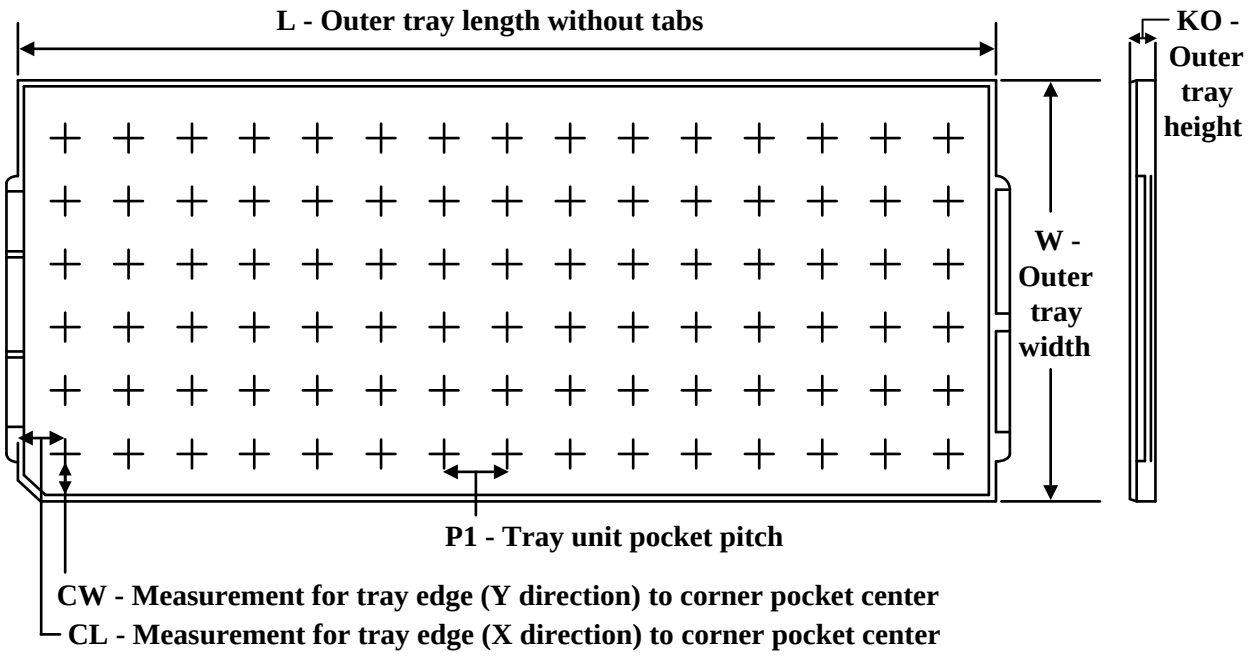
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

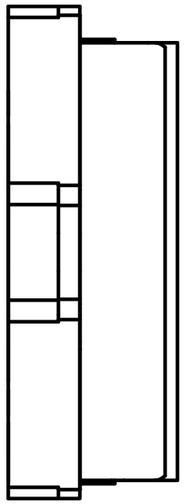
*All dimensions are nominal

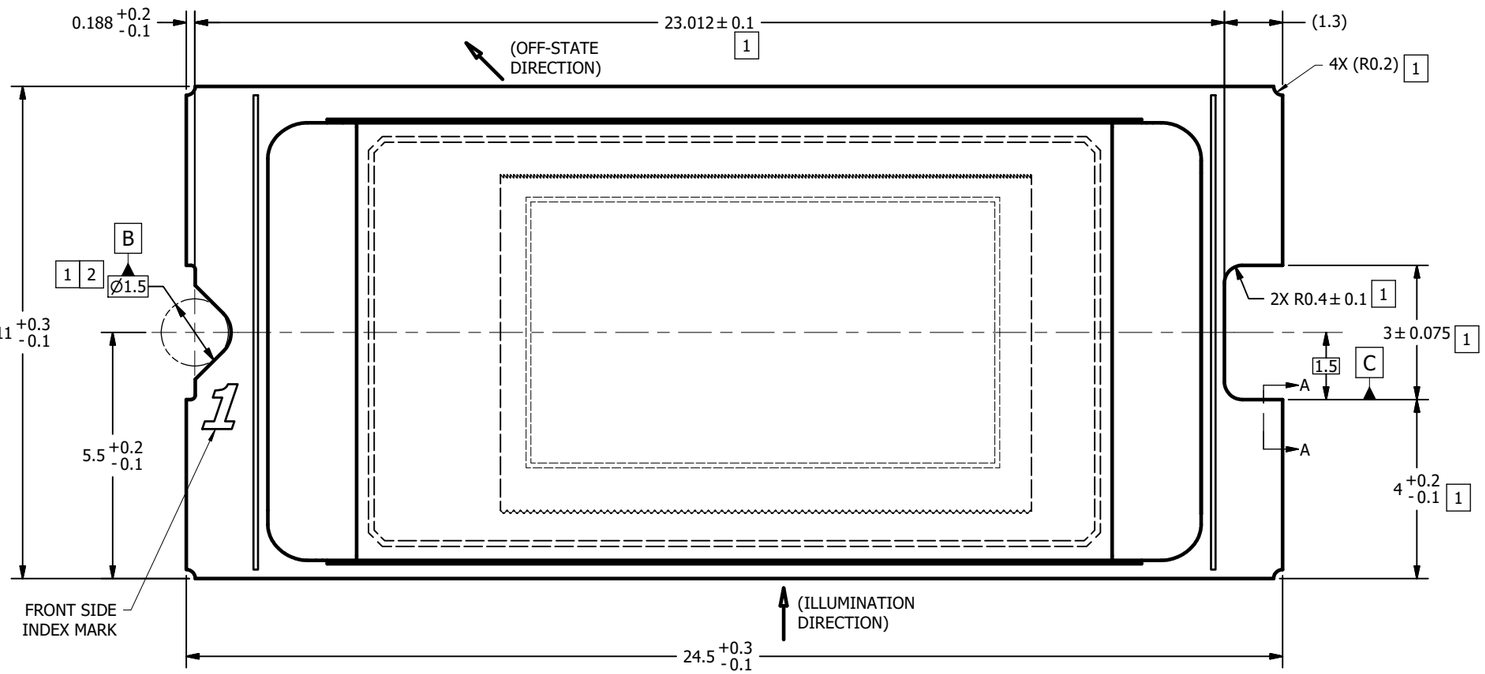
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP4710AFQL	FQL	CLGA	100	80	8 x 10	150	315	135.9	12190	28	31.5	15.45
DLP4710AFQL.A	FQL	CLGA	100	80	8 x 10	150	315	135.9	12190	28	31.5	15.45
DLP4710AFQL.B	FQL	CLGA	100	80	8 x 10	150	315	135.9	12190	28	31.5	15.45

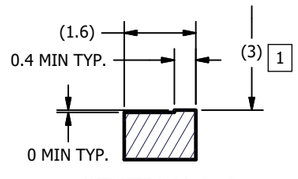
REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2140050: INITIAL RELEASE	2/20/2014	BMH
B	ECO 2140429: CORRECT DATUM C IN VIEW J-J, SH. 3	3/6/2014	BMH
C	ECO 2142093: DELETE BACK SIDE FLATNESS SPEC	5/22/2014	BMH
D	ECO 2145057: ADD "FQL PACKAGE" TO DRAWING TITLE	7/20/2016	BMH
E	ECO 2187241: ADD APERTURE SLOT PICTORIALLY	4/23/2020	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

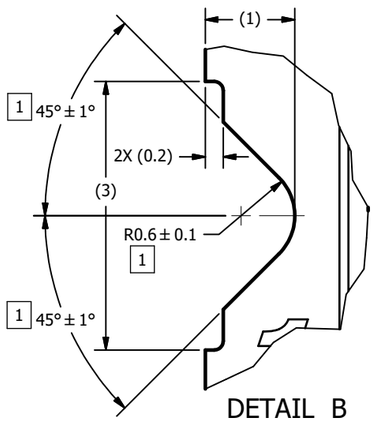
1. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
2. SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
3. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
4. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
8. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.



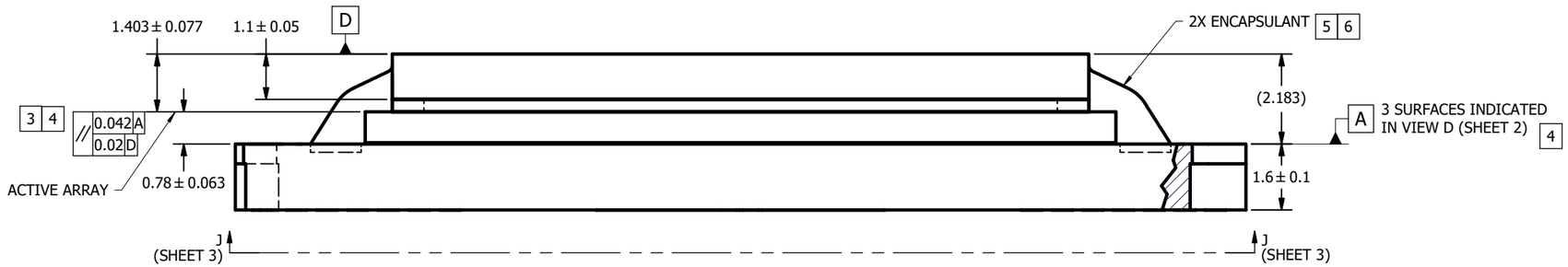




SECTION A-A
NOTCH OFFSETS



DETAIL B
V-NOTCH
SCALE 30 : 1



	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	2/20/2014
ENGINEER	B. HASKETT	2/20/2014
QA/CE	P. KONRAD	2/26/2014
CM	S. SUSI	2/25/2014
	M. DORAK	2/23/2014
APPROVED	R. LONG	2/26/2014

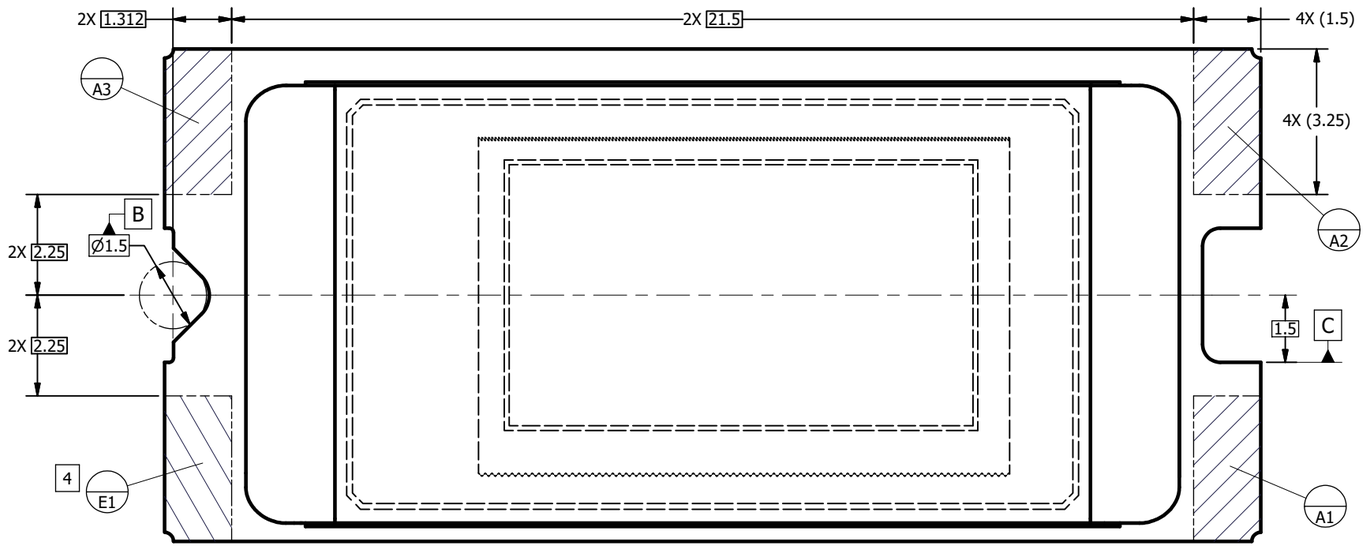
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .47 1080p SERIES 312 (FQL PACKAGE)

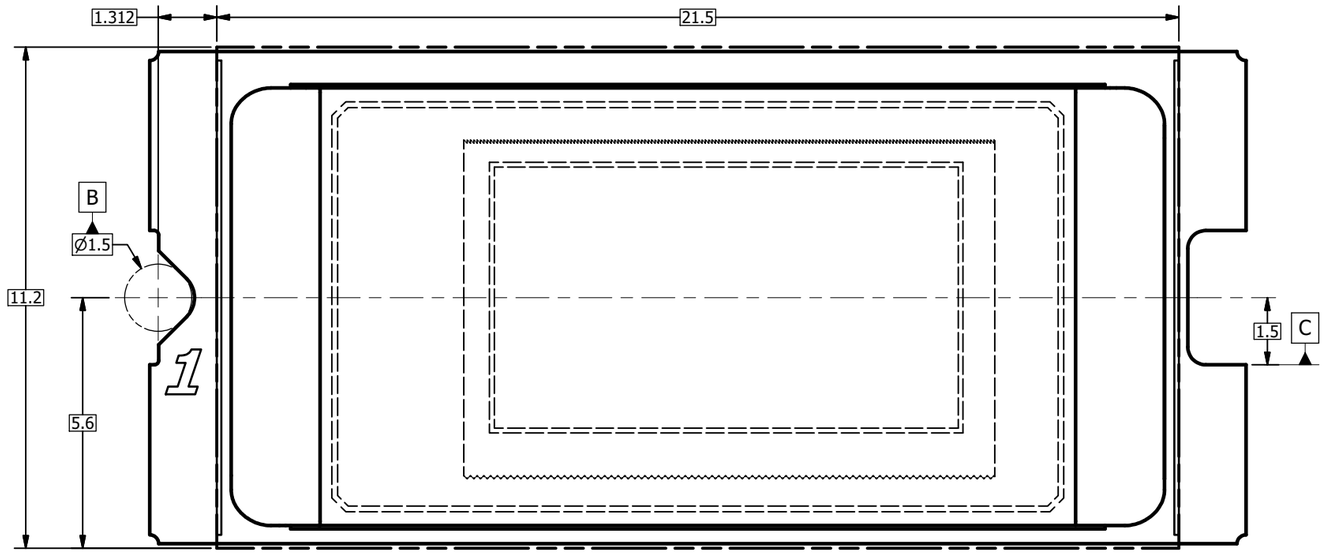
SIZE	DWG NO	REV
D	2513652	E

SCALE 15:1 SHEET 1 OF 3

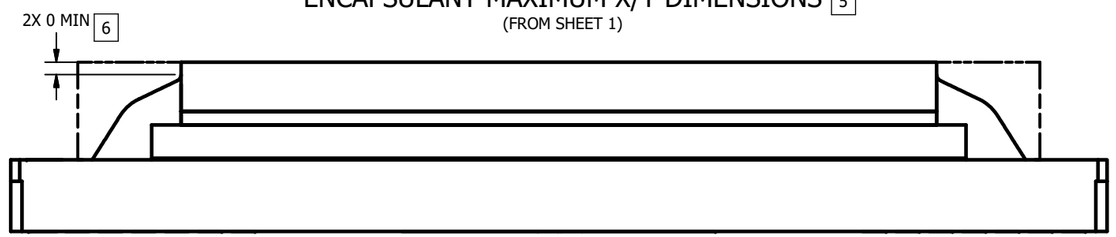
INV11-2006a



VIEW C
DATUMS A AND E
(SUBSTRATE METALLIZATION OMITTED FOR CLARITY)
(FROM SHEET 1)



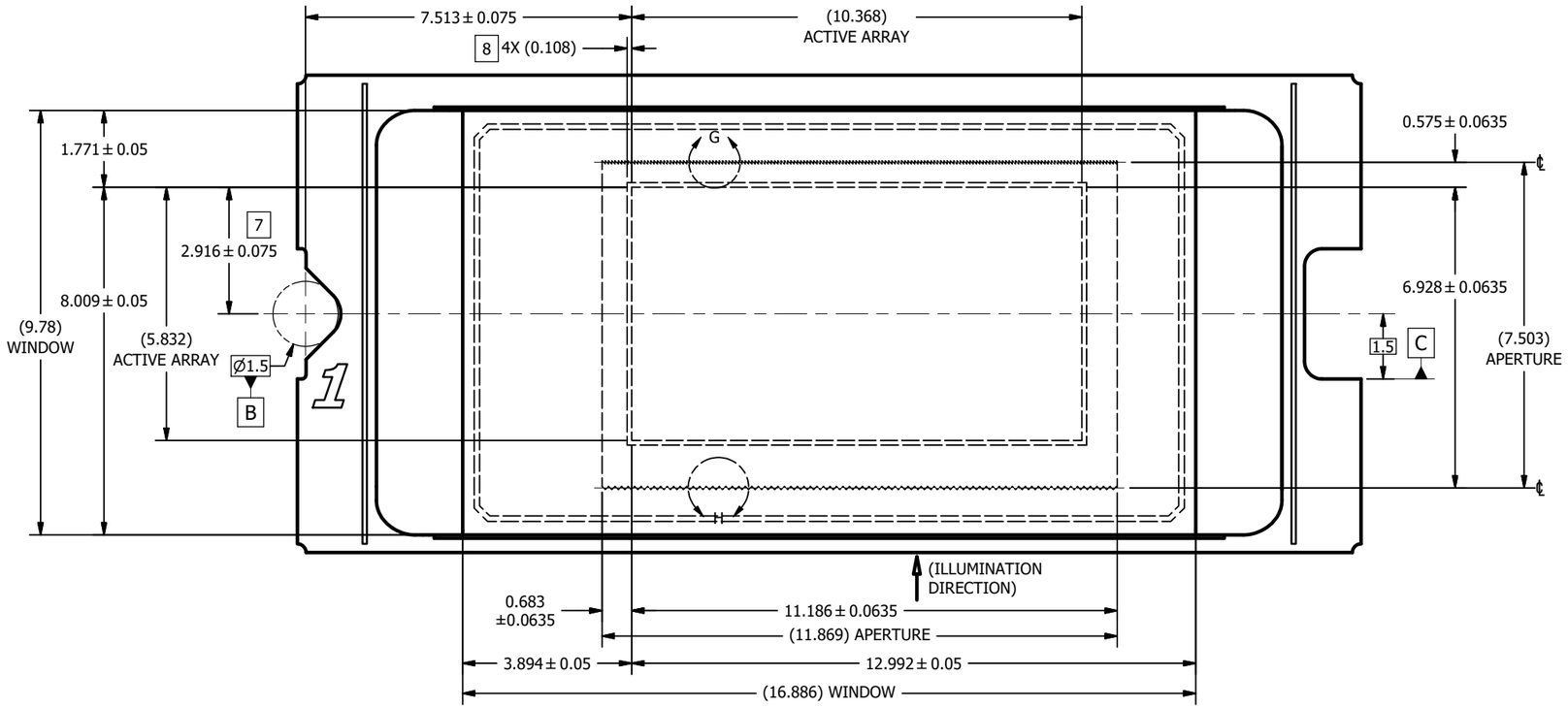
VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)



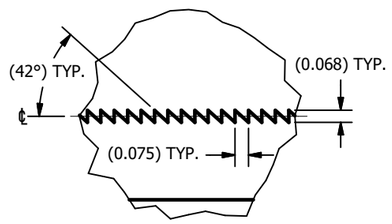
VIEW E
ENCAPSULANT MAXIMUM HEIGHT

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 2/20/2014	SIZE D	DWG NO 2513652	REV E
			SCALE	SHEET 2 OF 3	

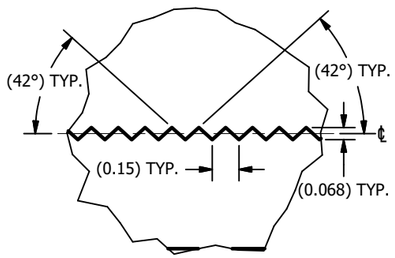
INV11-2006a



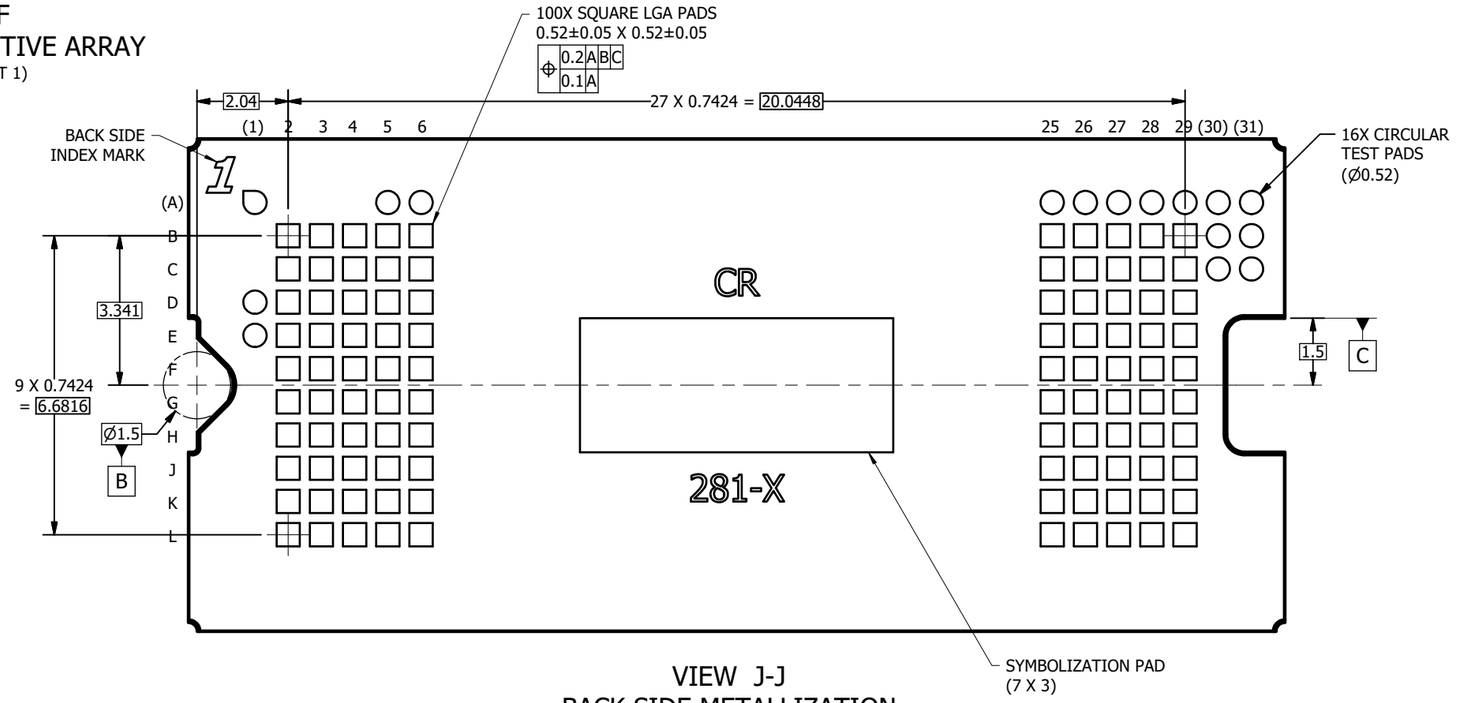
VIEW F
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL G
APERTURE TOP EDGE
SCALE 60 : 1



DETAIL H
APERTURE BOTTOM EDGE
SCALE 60 : 1



VIEW J-J
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 2/20/2014	SIZE D	DWG NO 2513652	REV E
			SCALE	SHEET 3 OF 3	

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