具有集成反极性保护功能的 TPS2662x 60V 800mA 工业电子保险丝

1 特性

- 工作电压为 4.5V 至 57V，绝对最大值为 60V
- 集成反向输入极性保护（高达 –60V）
- 集成反向输出保护，高达 –60V 输入电压（仅限 TPS26624 和 TPS26625）
- 总 RON 为 500mΩ 的集成背对背 MOSFET
- 25mA 至 870mA 可调节电流限制（870mA 时精度为 ±5%）
- 使用最少的外部组件在浪涌期间提供负载保护 (IEC 61000-4-5)
- 符合标准 A 的 EFT (IEC 61000-4-4) 性能
- 低静态电流，工作时为 400µA，关断时为 10µA
- 可调节的 UVLO、OVP 切断，输出压摆率控制
- 反向电流阻断
- 38V 固定过压钳位（仅限 TPS26622 和 TPS26623）
- 小尺寸 - 10L (3mm × 3mm) VSON
- UL2367 认证正在处理中

2 应用

- 工业电源系统
- PLC I/O 模块
- 传感器和控制
- 恒温器
- PoE 高侧保护

3 说明

TPS2662x 系列高电压电子保险丝，设计紧凑，功能丰富，且具有一整套保护功能 功能。4.5V 至 57V 的宽电源输入范围可实现对众多常用直流总线电压的控制。该器件可以承受并保护由高达 ±60V 的正负电源供电的负载。TPS26624 和 TPS26625 器件支持输入和输出反极性保护功能。集成的背对背 FET 可提供反向电流阻断功能，因此该器件适用于在电源故障和欠压条件下要求保持输出电压的系统。该器件还具备许多可调功能，可提供负载、电源和器件保护 功能 包括过流保护、输出转换率和过压保护以及欠压保护。TPS2662x 系列内部可靠的保护控制模块以及高额定电压有助于简化针对浪涌保护的系统设计。

TPS26620、TPS26622 和 TPS26624 具有闭锁功能，TPS26621、TPS26623 和 TPS26625 具有自动重试功能，用于应对过热和过流故障事件。

这些器件采用 3mm × 3mm 10 引脚 SON 封装，额定工作温度范围为 –40°C 至 +125°C。 将一页更改为整个数据表

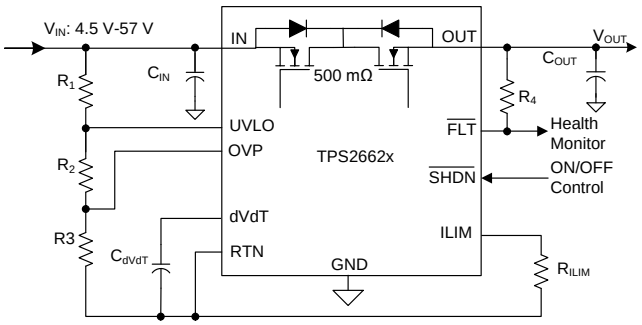
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS26620 TPS26621 TPS26622 TPS26623 TPS26624 TPS26625	SON (10)	3.00mm × 3.00mm

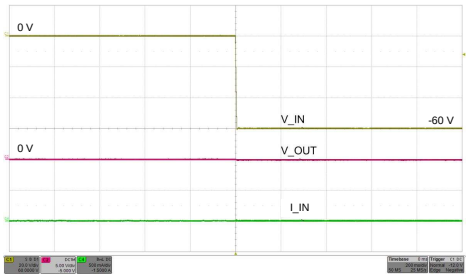
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

ADVANCE INFORMATION

简化原理图



–60V 电源时的反向输入极性保护



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4 修订历史记录

Changes from Original (October 2017) to Revision A **Page**

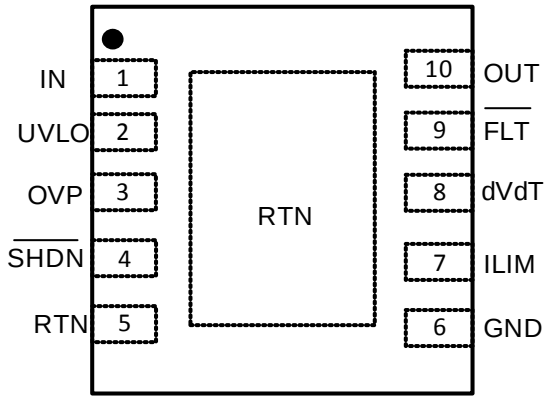
- 已更改 1

5 Device Comparison Table

PART NUMBER	OVERVOLTAGE PROTECTION	OVERLOAD and THERMAL FAULT REPINSE	REVERSE POLARITY PROTECTION
TPS26620	Overvoltage cut-off, adjustable	Latch Off	Input side
TPS26621	Overvoltage cut-off, adjustable	Auto-Retry	Input side
TPS26622	Overvoltage clamp, fixed (38 V)	Latch Off	Input side
TPS26623	Overvoltage clamp, fixed (38 V)	Auto-Retry	Input side
TPS26624	Overvoltage cut-off, adjustable	Latch Off	Input and Output side
TPS26625	Overvoltage cut-off, adjustable	Auto-Retry	Input and Output side

6 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN	Power	Input supply voltage
2	UVLO	I	Resistor programmable undervoltage lockout threshold setting input. An undervoltage event will open the internal FET. If the Undervoltage Lock Out function is not needed, the UVLO terminal must be connected to the IN terminal with a 200 kΩ resistor.
3	OVP	I	Resistor programmable overvoltage protection threshold. An overvoltage event will open internal FET. In TPS26622, connect OVP to RTN for OV clamp functionality
4	$\overline{\text{SHDN}}$	I	Shutdown PIN. Pulling it low makes the device to enter into low power shutdown mode. Cycling $\overline{\text{SHDN}}$ low and then back high resets the device that has latched off (TPS26620, TPS26622, TPS26623 only) due to a fault condition.
5	RTN	–	Reference for all internal voltages
6	GND	–	System Ground
7	ILIM	I/O	A resistor from this pin to RTN will set the overload and short circuit limit.
8	dVdT	I/O	Controls slew rate of OUT voltage. Leave open for default slew rate or tie appropriate capacitor to RTN to reduce OUT ramp rate at power ON
9	$\overline{\text{FLT}}$	O	Active Low. Fault event indicator, goes low to indicate fault condition due to UVLO, OVP, over load, reverse voltage, thermal shutdown and when $\overline{\text{SHDN}}$ is pulled low
10	OUT	Power	Output Voltage
–	Thermal Pad	–	Thermal pad. Connect Thermal pad to RTN plane for heat sinking. Do not use Thermal Pad as the only electrical connection to RTN

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, all voltages referred to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range	IN, IN–OUT	–60	60	V
	OUT (TPS26624 and TPS26625 Only)	–(60–V_{IN})	60	
	IN, IN–OUT (10 ms transient), T_A = 25 ℃	–70	70	
	[IN, OUT, $\overline{FLT}$, $\overline{SHDN}$] to RTN	–0.3	60	
	[UVLO, OVP, dVdT, ILIM] to RTN	–0.3	5	
	RTN	–60	0.3	
Sink current	$I_{\overline{FLT}}$, I_{dVdT}, $I_{\overline{SHDN}}$		10	mA
Source current	I_{dVdT}, I_{ILIM}	Internally limited		
Operating junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input voltage	4.5		57	V
OUT, $\overline{FLT}$		0		57	
UVLO, OVP, dVdT, ILIM, $\overline{SHDN}$		0		4	
ILIM	Resistance	7.5		267	kΩ
IN, OUT	External capacitance	0.1			µF
dVdT		10			nF
T_j	Operating junction temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS2662 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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Thermal Information (continued)

THERMAL METRIC[1]		TPS2662 DRC (VSON) 10 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

7.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 267 kΩ, $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN)}$	Operating input voltage		4.5		57	V
$V_{(PORR)}$	Internal POR threshold, rising			3.73	4.4	V
$V_{(PORHys)}$	Internal POR hysteresis			110		mV
$IQ_{(ON)}$	Supply current	Enabled:$V_{(\overline{SHDN})}$ = 2 V		384		µA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})}$ = 0 V		10		µA
$I_{(VINR)}$	Reverse Input supply current	$V_{(IN)}$ = –24 V, $V_{(OUT)}$ = 0 V		50	120	µA
$V_{(OVC)}$	Over voltage clamp	$V_{(IN)}$ > 40 V, $I_{(OUT)}$ = 10 mA,TPS26622, TPS26623 only	36	37.5	40	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.175	1.203	1.226	V
$V_{(UVLOF)}$	UVLO threshold, falling		1.085	1.117	1.125	V
$I_{(UVLO)}$	UVLO Input leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 3.5 V	–100	0	100	nA
				18.8	38	µA
OVER VOLTAGE PROTECTION (OVP) INPUT						
$V_{(OVPR)}$	Over-voltage threshold voltage, rising		1.175	1.203	1.226	V
$V_{(OVPF)}$	Over-voltage threshold, falling		1.085	1.117	1.125	V
$I_{(OVP)}$	OVP input leakage current	0 V ≤ $V_{(OVP)}$ ≤ 5 V	–100	0	100	nA
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Output voltage	$I_{(\overline{SHDN})}$ = 0.1 µA	2	2.781	3.3	V
$V_{(SHUTF)}$	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling		0.9	1.179		V
$V_{(SHUTR)}$	$\overline{SHDN}$ threshold, rising			1.632	1.8	V
$I_{(\overline{SHDN})}$	Input current	$V_{(\overline{SHDN})}$ = 0.4 V	–10	-2.4		µA
		$V_{(\overline{SHDN})}$ = 1.2 V		-2.3		
		$V_{(\overline{SHDN})}$ = 60 V		2.9		
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0V		1.98		µA
$R_{(dVdT)}$	dVdT discharging resistance	$\overline{SHDN}$ = 0 V, with $I_{(dVdT)}$ = 10 mA sinking		13.1		Ω
$V_{(dVdTmax)}$	dVdT maximum capacitor voltage			4.34	4.75	V
$GAIN_{(dVdT)}$	dVdT to OUT gain	$V_{(OUT)}$ /$V_{(dVdT)}$		24.6		V/V
CURRENT LIMIT PROGRAMMING (ILIM)						
$V_{(ILIM)}$	ILIM bias voltage			1		
$I_{(OL)}$	Overload current limit	$R_{(ILIM)}$ = 267 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.02	0.025	0.032	A
		$R_{(ILIM)}$ = 44.2 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.14	0.15	0.156	
		$R_{(ILIM)}$ = 26.7 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.24	0.25	0.26	
		$R_{(ILIM)}$ = 13.3 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.47	0.5	0.52	
		$R_{(ILIM)}$ = 8.25 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.76	0.8	0.83	
		$R_{(ILIM)}$ = 7.5 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.83	0.88	0.91	
$I_{(OL\_R\text{-}OPEN)}$		$R_{(ILIM)}$ = OPEN, open resistor current limit	10	15.5	26	mA
$I_{(OL\_R\text{-}SHORT)}$		$R_{(ILIM)}$ = SHORT, shorted resistor current limit	36	43	51	mA
$I_{(SCL)}$	Short-circuit current limit	$R_{(ILIM)}$ = 7.5 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 24 V		0.885		A
$I_{(FASTRIP)}$	Fast-trip comparator threshold			1.454		A
PASS FET OUTPUT (OUT)						

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Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 267 kΩ, $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON}	IN to OUT total ON resistance	0.025 A ≤ $I_{(OUT)}$ ≤ 0.8 A, T_J = 25°C, $R_{(ILIM)}$ = 7.5kΩ		478		mΩ
		0.025 A ≤ $I_{(OUT)}$ ≤ 0.8 A, T_J = 85°C, $R_{(ILIM)}$ = 7.5kΩ		626	705	
		0.025 A ≤ $I_{(OUT)}$ ≤ 0.8 A, –40ºC ≤ T_J ≤125°C, $R_{(ILIM)}$ = 7.5kΩ		478	821	
$I_{lkg(OUT)}$	OUT leakage current in off state	$V_{(IN)}$ = 60 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 0 V, Sourcing		4.38	12	µA
		$V_{(IN)}$ = 0 V, $V_{(\overline{SHDN})}$= 0V, $V_{(OUT)}$ = 24 V, Sinking		7.27	15	
		$V_{(IN)}$ = –60 V, $V_{(\overline{SHDN})}$ = 0V, V(OUT) = 0 V, sinking			25	
	OUT leakage current under output reverse polarity condition	VIN = 24 V, VOUT = –24 V, $V_{(\overline{SHDN})}$= 2 V, TP26624, TPS26625 only		IQ_{ON} + 36		
$V_{(REVTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, falling			–50		mV
$V_{(FWDTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, rising			25		mV
RTN (IC GND)						
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ pull-down resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5 mA sinking		82.3		Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 60 V	–100		100	nA
THERMAL SHUT DOWN (TSD)						
$T_{(TSD)}$	TSD threshold, rising			151		°C
$T_{(TSDhyst)}$	TSD hysteresis			13.5		°C
	Thermal fault (latch or auto-retry)	TPS26620, TPS26622, TPS26624		Latch		
		TPS26621, TPS26623, TPS26625		Auto-retry		

7.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 267 kΩ, $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN and UVLO INPUT						
UVLO turnon delay	UVLO_$t_{ON(dly)}$	UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ = Open		51		µs
		UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ > 4.7 nF, $C_{(dVdT)}$ in nF		27.4 x $C_{(dVdT)}$		µs
UVLO turnoff delay	UVLO_$t_{off(dly)}$	UVLO↓ (100 mV below $V_{(UVLOF)}$) to $\overline{FLT}$↓		6.14		µs
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
SHUTDOWN exit delay	$t_{SD(dly)}$	$\overline{SHDN}$↑ to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ = Open		156		µs
		$\overline{SHDN}$↑ to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ > 4.7 nF, $C_{(dvdt)}$ in nF		156 + 27.4 x $C_{(dVdT)}$		µs
SHUTDOWN entry delay		$\overline{SHDN}$↓ (below SHUTF) to $\overline{FLT}$↓		6.83		µs
OVER VOLTAGE PROTECTION INPUT (OVP)						
OVP exit delay	$t_{OVP(dly)}$	OVP↓ (20 mV below $V_{(OVPF)}$) to $V_{(OUT)}$ = 100 mV, TPS26620/21/24/25 Only		77		µs
OVP disable delay		OVP↑ (20 mV above $V_{(OVPR)}$) to $\overline{FLT}$↓, TPS26620/21/24/25 only		4.84		µs
CURRENT LIMIT						
Current limit switch turnoff time		$I_{(ILIM)}$ < $I_{(OUT)}$ < $I_{(FASTRIP)}$, $V_{(IN)}$ – $V_{(OUT)}$ < 2.6 V		512		ms
		$I_{(OUT)}$ > $I_{(FASTRIP)}$, $V_{(IN)}$ – $V_{(OUT)}$ < 2.6 V		1.5		µs
		$I_{(OUT)}$ > $I_{(FASTRIP)}$, 4.5 V < $V_{(IN)}$ ≤ 6V, $V_{(IN)}$ – $V_{(OUT)}$ ≥ 2.6 V			2	µs
Fast-trip comparator delay	$t_{FASTTRIP(dly)}$	$I_{(OUT)}$ > $I_{(FASTRIP)}$, 6 V < VIN ≤ 60V, $V_{(IN)}$ – $V_{(OUT)}$ ≥ 2.6 V		220	500	ns
REVERSE PROTECTION COMPARATOR						
Reverse protection comparator delay	$t_{REV(dly)}$	($V_{(IN)}$ – $V_{(OUT)}$) less than 2.6 V to FET off		3.71		µs
		($V_{(IN)}$ – $V_{(OUT)}$) ≥ 2.6 V to FET OFF		0.31		
	$t_{REV(dly)}$	($V_{(IN)}$ – $V_{(OUT)}$)↓ (100 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$↓		45		
	$t_{FWD(dly)}$	($V_{(IN)}$ – $V_{(OUT)}$)↑ (TBD mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$↑		63		
THERMAL SHUTDOWN						

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Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 267 kΩ, $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Retry delay in TSD				512		ms
OUTPUT RAMP CONTROL (dVdT)						
Output Ramp Time	t_{dVdT}	$\overline{SHDN}$↑ to $V_{(OUT)}$ = 23.9 V, with $C_{(dVdT)}$ = 22 nF		11		ms
		$\overline{SHDN}$↑ to $V_{(OUT)}$ = 4 V, with $C_{(dVdT)}$ = 22 nF		2.89		
		$\overline{SHDN}$↑ to $V_{(OUT)}$ = 23.9 V, with $C_{(dVdT)}$ = open		0.664		
FAULT FLAG ($\overline{FLT}$)						
ORP response time	t_{orpdly}	$V_{(OUT)}$ falling from $V_{(ORP\_COMP\_THRESH)}$ at -10V/µs to $\overline{FLT}$ rising edge		552		nS
PGOOD Delay	t_{PGOODF}	Falling edge		875		µs
	t_{PGOODR}	Rising edge, $C_{(dVdT)}$ = Open		1.4		ms
		Rising edge, $C_{(dVdT)}$ > 4.7 nF		TBD		µs

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8 Parameter Measurement Information

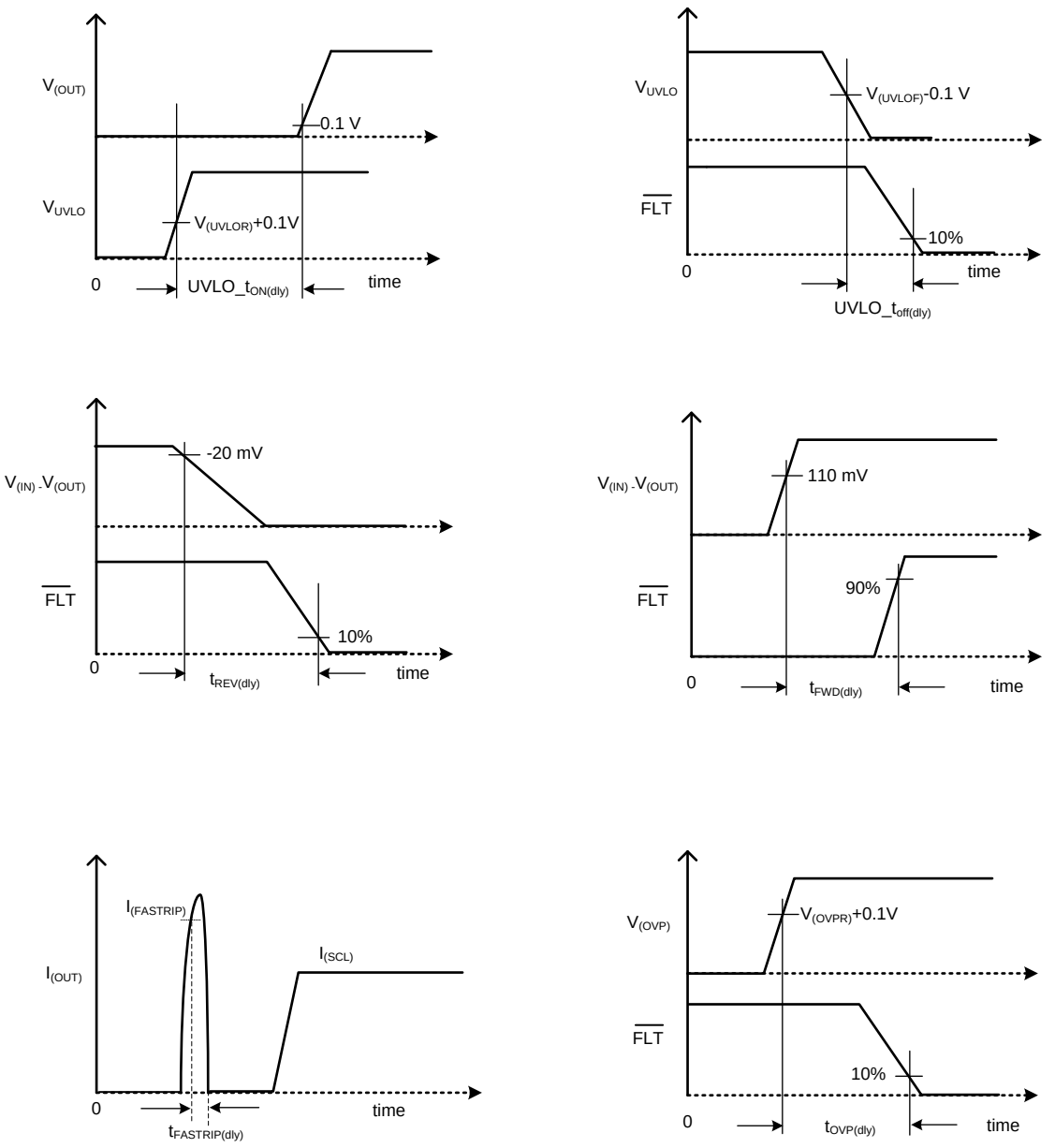

图 1. Timing Waveforms

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9 Detailed Description

9.1 Overview

The TPS2662x is a family of high voltage industrial eFuses with integrated back-to-back MOSFETs and enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 4.5 V to 57 V. The device can withstand ±60 V positive and negative supply voltages without damage. The device feature fully integrated reverse polarity protection and require zero additional power components. For hot-pluggable boards, the device provides hot-swap power management with in-rush current control and programmable output voltage slew rate features. Load, source and device protections are provided with many programmable features including overcurrent, overvoltage, undervoltage. The precision overcurrent limit (±5% at 870 mA) helps to minimize over design of the input power supply, while the fast response short circuit protection 250 ns (typical) immediately isolates the faulty load from the input supply when a short circuit is detected.

The internal robust protection control blocks of the TPS2662x along with its ±60 V rating helps to simplify the system designs for the surge compliance ensuring complete protection of the load and the device. TPS2662x devices are immune to noise tests like Electrical Fast Transients that are common in industrial applications and simplifies the system design that require criterion-A performance during this noise test.

The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault signal for the downstream system. The TPS2662x monitor functions threshold accuracy of ±3% ensures tight supervision of the supply bus, eliminating the need for a separate supply voltage supervisor chip.

The device monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected.

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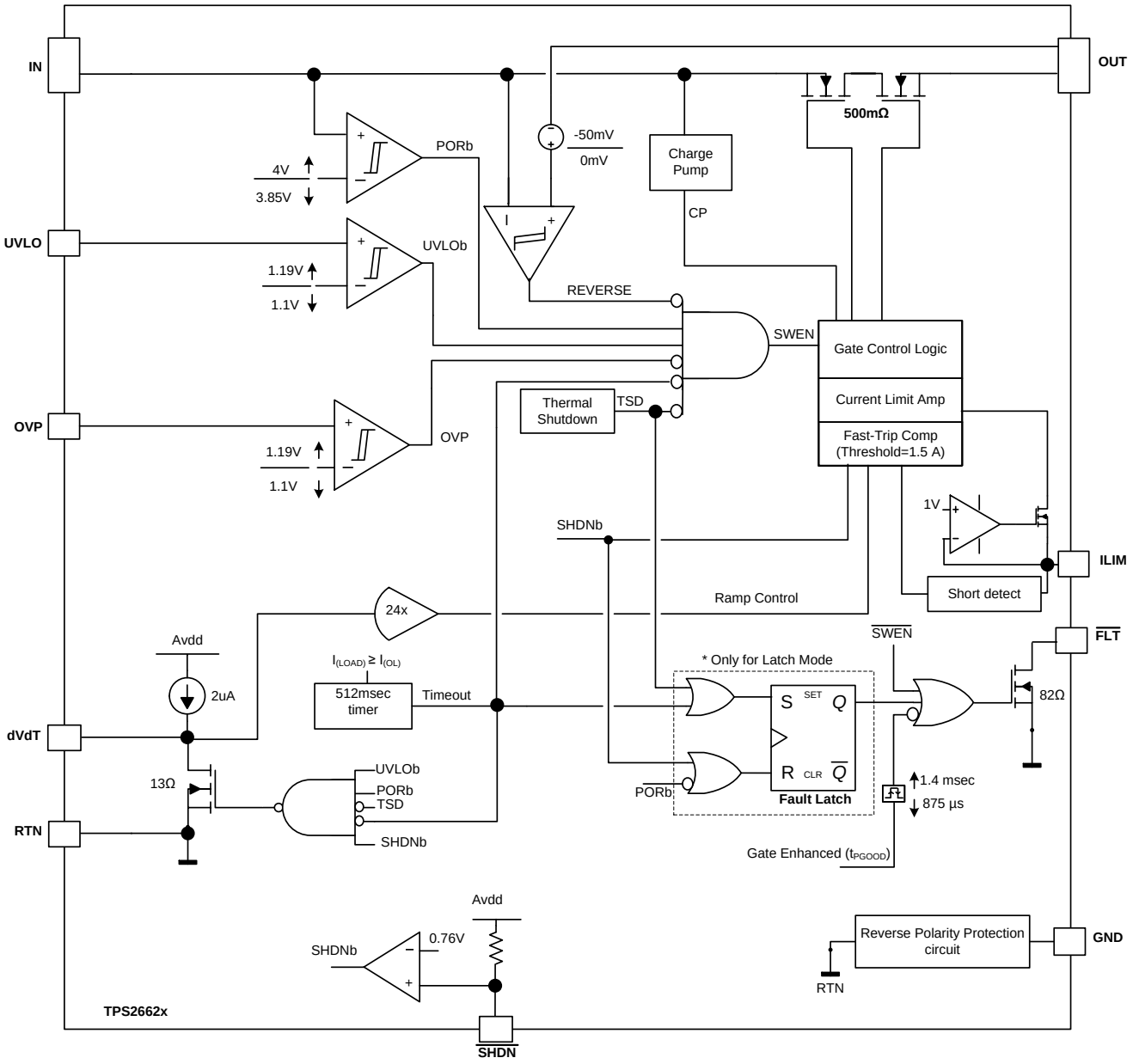
9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

This section is the undervoltage comparator input. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input power fail or input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 90 mV. To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to RTN as shown in 图 2.

Feature Description (接下页)

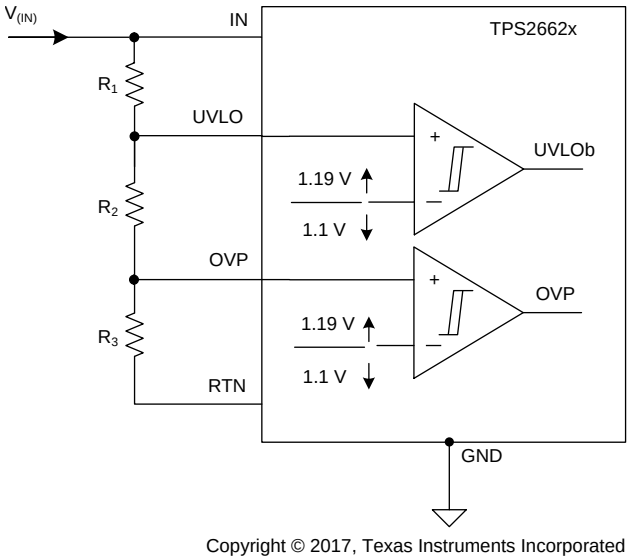


图 2. UVLO and OVP Thresholds Set by R_1, R_2 and R_3

If the Undervoltage Lockout function is not needed, the UVLO terminal must be connected to the IN terminal with a 200 kΩ resistor. The UVLO terminal must not be left floating.

9.3.2 Overvoltage Protection (OVP)

The TPS2662x family incorporate circuitry to protect the system during overvoltage conditions. The TPS26620, TPS26621, TPS26624 and TPS26625 feature overvoltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN supply to OVP terminal to RTN as shown in 图 2.

The TPS26622 and TPS26623 features an internally fixed 38 V overvoltage clamp (V_{OVC}) functionality. The OVP terminal of these devices must be connected to the RTN terminal directly. These devices clamp the output voltage to V_{OVC}, when the input voltage exceeds 38 V. During the output voltage clamp operation, the power dissipation in the internal MOSFET is $P_D = (V_{IN} – V_{OVC}) \times I_{OUT}$. Excess power dissipation for prolonged period can make the device to enter into thermal shutdown. illustrates the overvoltage clamp functionality.

9.3.3 Reverse Polarity Protection

TPS26620, TPS26621, TPS26622 and TPS26623 feature reverse input polarity protection. This feature protects the loads from negative supply voltages during field mis-wiring which is common use case in the boards having screw terminals.

TPS26624 and TPS26625 feature input as well as output reverse polarity protection. The output reverse polarity protection feature protects the on board supply from negative voltage that can appear at the output of the eFuse due to field miswiring at the output side with an external isolated power supplies.

9.3.4 Hot Plug-In and In-Rush Current Control

The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to RTN defines the slew rate of the output voltage at power-on as shown in 图 3.

ADVANCE INFORMATION

Feature Description (接下页)

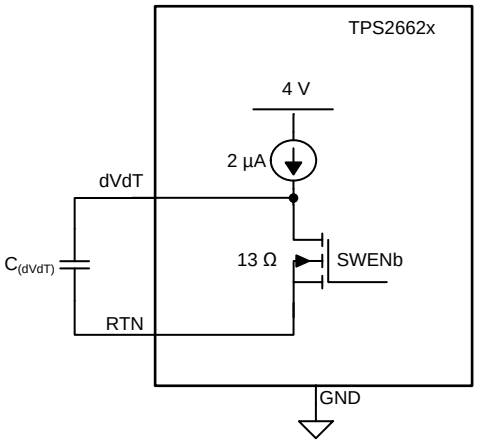


图 3. Output Ramp Up Time t_{dVdT} is Set by $C_{(dVdT)}$

The dVdT pin can be left floating to obtain a predetermined slew rate (t_{dVdT}) on the output. When the terminal is left floating, the devices set an internal output voltage ramp rate of 24 V/500 µs. A capacitor can be connected from dVdT pin to RTN to program the output voltage slew rate slower than 24 V/500 µs. Use 公式 1 and 公式 2 to calculate the external $C_{(dVdT)}$ capacitance.

公式 1 governs slew rate at start-up.

$$I_{(dVdT)} = \left(\frac{C_{(dVdT)}}{Gain_{(dVdT)}} \right) \times \left(\frac{dV_{(OUT)}}{dt} \right)$$

where

- $I_{(dVdT)}$ = 2 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$
- $Gain_{(dVdT)}$ = dVdT to V_{OUT} gain = 24 (1)

The total ramp time (t_{dVdT}) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using 公式 2.

$$t_{dVdT} = 20 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

9.3.5 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

9.3.5.1 Overload Protection

Connect a resistor across ILIM to RTN to program the over load current limit $I_{(OL)}$. During over load conditions the device regulates the current through it at $I_{(OL)}$ programmed by the $R_{(ILIM)}$ resistor as shown in 公式 3 for a maximum duration of $tCL_{(dly)}$ after which the internal FETs are turned OFF.

$$I_{OL} = \frac{6.636}{R_{ILIM}}$$

where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ (3)

ADVANCE INFORMATION

Feature Description (接下页)

During the current limit operation the output voltage droops and this may cause the device to hit the thermal shutdown threshold $T_{(TSD)}$ before $tcl_{(dly)}$. Once the thermal shutdown threshold is hit or $tcl_{(dly)}$ is lapsed, the internal FETs of TPS2662x will turn OFF. FETs in TPS26620, TPS26622 and TPS26624 remain OFF and latched. To reset the latch, cycle the $\overline{SHDN}$, UVLO or recycle the V_{IN}. TPS26621, TPS26623 and TPS26625 commences an auto-retry cycle after a retry time of 512 msec. The internal FETs turn back on in dVdT mode after this retry time. If the overload still exists then the device regulates the current at programmed current limit $I_{(OL)}$.

9.3.5.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases very rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold $I_{(FASTRIP)}$. The fast-trip comparator turns off the internal FET within 250 ns (typical), when the current through the FET exceeds $I_{(FASTRIP)}$ ($I_{(OUT)} > I_{(FASTRIP)}$), and terminates the rapid short-circuit peak current. The fast-trip threshold is internally set to 1-A. The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition.

9.3.5.3 FAULT Response

The $\overline{FLT}$ open-drain output asserts (active low) under the following conditions:

- Fault events such as undervoltage, overvoltage, over load, reverse current and thermal shutdown conditions
- The device enters low current shutdown mode when $\overline{SHDN}$ is pulled low
- During start-up when the internal FET GATE is not fully enhanced

The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry.

The $\overline{FLT}$ signal can also be used as Power Good indicator to the downstream loads like DC-DC converters. An internal Power Good (PGOOD) signal is OR'd with the fault logic. During start-up, when the device is operating in dVdT mode, PGOOD and $\overline{FLT}$ it remains low and is de-asserted after the dVdT mode is completed and the internal FET is fully enhanced. The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully enhanced before heavy load is applied by the downstream converters. Rising deglitch delay is determined by $t_{PGOOD(degl)}$ = Maximum {(875 + 20 × $C_{(dVdT)}$), t_{PGOODR}}, where $C_{(dVdT)}$ is in nF and $t_{PGOOD(degl)}$ is in µs. $\overline{FLT}$ can be left open or connected to RTN when not used. $V_{(IN)}$ falling below $V_{(PORF)}$ = 3.72 V resets $\overline{FLT}$.

9.3.5.4 IN, OUT, RTN, and GND Pins

A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended input operating voltage range is 4.5 to 57 V. $V_{(OUT)}$, in the ON condition, is calculated using 公式 4.

$$V(OUT) = V(IN) - \left(RON \times I(OUT)\right) \quad (4)$$

Where,

- RON is the total ON resistance of the internal FETs.

GND pin must be connected to the system ground. RTN is the device ground reference for all the internal control blocks. Connect the TPS2662x family support components: $R_{(ILIM)}$, $C_{(dVdT)}$ and resistors for UVLO and OVP with respect to the RTN pin. Internally, the device has reverse input polarity protection block between RTN and the GND terminal. Connecting RTN pin to GND pin disables the reverse polarity protection feature and the TPS2662x gets permanently damaged when operated under this fault event.

9.3.5.5 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FETs, if the junction temperature exceeds $T_{(TSD)}$. After the thermal shutdown event, depending upon the mode of fault response, the device either latches off or commences an auto-retry cycle 512 ms after $T_J < [T_{(TSD)} – 10°C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

ADVANCE INFORMATION

9.4 Device Functional Modes

9.4.1 Low Current Shutdown Control ($\overline{SHDN}$)

The internal FETs and the load current can be switched off by pulling the $\overline{SHDN}$ pin below 0.76 V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device as shown in 图 4 and 图 5. The device quiescent current reduces to 10 µA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must sink at least 10 µA at 400 mV. To enable the device, $\overline{SHDN}$ must be pulled up to at least 1 V. Once the device is enabled, the internal FETs turnon with dVdT mode.

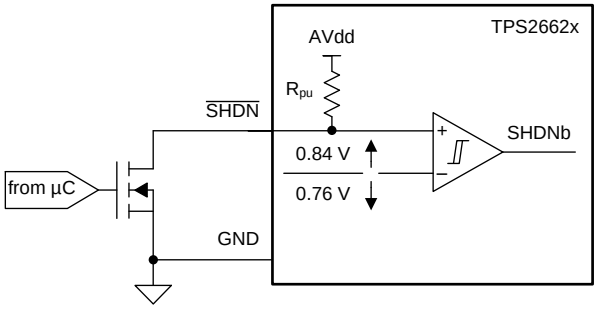


图 4. Shutdown Control

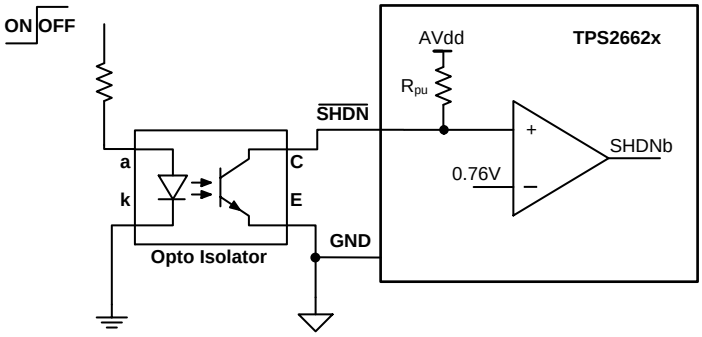


图 5. Opto-Isolator Shutdown Control

ADVANCE INFORMATION

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2662x family is an industrial eFuse, typically used for Hot-Swap and power rail protection applications. It operates from 4.5 V to 57 V with programmable current limit, overvoltage, undervoltage and reverse polarity protections. The device aids in controlling in-rush current and provides robust protection against reverse current and field miss-wiring conditions for systems such as PLC I/O modules and Sensor power supplies. The device also provides robust protection for multiple faults on the system rail.

The *Detailed Design Procedure* section can be used to select component values for the device.

10.2 Typical Application

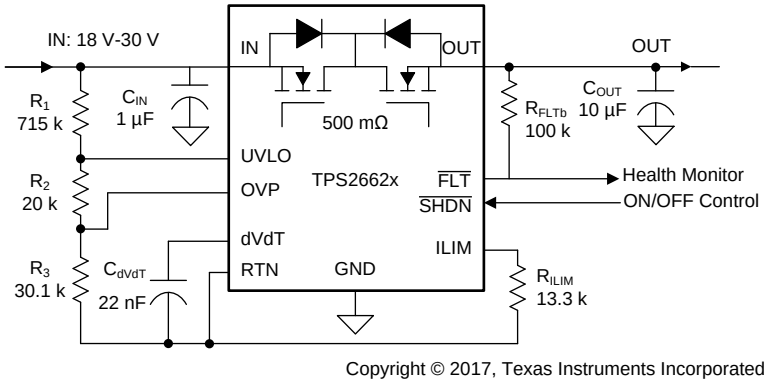


图 6. 24-V, 500m-A eFuse Input Protection Circuit for PLC I/O Module

10.2.1 Design Requirements

表 1 shows the Design Requirements for TPS2662x.

表 1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Typical input voltage	24 V
$V_{(UV)}$	Undervoltage lockout set point	18 V
$V_{(OV)}$	Overvoltage cutoff set point	30 V
$T_{(SU)}$	Start up time	10 ms
$I_{(LIM)}$	Current limit	500 mA
$C_{(OUT)}$	Load capacitance	10 µF

ADVANCE INFORMATION

10.2.2 Detailed Design Procedure

10.2.2.1 Step by Step Design Procedure

To begin the design process, the designer must know the following parameters:

- Input operating voltage range
- Maximum output capacitance
- Maximum current limit
- Load during start-up
- Maximum ambient temperature

This design procedure below seeks to control junction temperature of the device in both steady state and start-up conditions by proper selection of the output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

10.2.2.2 Programming the Current-Limit Threshold—$R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using 公式 5.

$$R_{ILIM} = \frac{6.636}{I_{LIM}} = 13.27\ k\Omega$$

where

- I_{LIM} = 500 mA (5)

Choose the closest standard 1% resistor value : $R_{(ILIM)}$ = 13.3 kΩ

10.2.2.3 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between IN, UVLO, OVP and RTN pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 公式 6 and 公式 7.

$$V_{(OVPR)} = \frac{R3}{R1 + R2 + R3} \times V_{(OV)} \quad (6)$$

$$V_{(UVLOR)} = \frac{R2 + R3}{R1 + R2 + R3} \times V_{(UV)} \quad (7)$$

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)}/(R_1+R_2+R_3)$}, it is recommended to use higher value resistance for R_1, R_2 and R_3.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20 times greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)}$ = 1.19 V and $V_{(UVLOR)}$ = 1.19 V. From the design requirements, $V_{(OV)}$ is 30 V and $V_{(UV)}$ is 18 V. To solve the equation, first choose the value of R_3 = 30.1 kΩ and use 公式 6 to solve for (R_1 + R_2) = 728.7 kΩ. Use 公式 7 and value of (R_1 + R_2) to solve for R_2 = 20.05 kΩ and finally R_1= 708.6 kΩ.

Choose the closest standard 1% resistor values: R_1 = 715 kΩ, R_2 = 20 kΩ, and R_3 = 30.1 kΩ.

10.2.2.4 Setting Output Voltage Ramp Time—(t_{dVdT})

The ramp-up capacitor $C_{(dVdT)}$ is calculated using following expression:

$$C_{dVdT} = \frac{T_{CSV}}{20 \times 10^3 \times V_{IN}}$$

where

- T_{SV} = 10 ms
- V_{IN} = 24 V (8)

ADVANCE INFORMATION

10.2.2.4.1 Support Component Selections—$R_{\overline{FLT}}$ and $C_{(IN)}$

The $R_{\overline{FLT}}$ serves as pull-up for the open-drain fault output. The current sink by this pin must not exceed 10 mA (see the *Absolute Maximum Ratings* table). Typical resistance value in the range of 10 kΩ to 100 kΩ is recommended for $R_{\overline{FLT}}$. The C_{IN} is a local bypass capacitor to suppress noise at the input. Typical capacitance value in the range of 0.1 µF to 1 µF is recommended for $C_{(IN)}$.

10.3 Do's and Don'ts

- Do not connect RTN to GND. Connecting RTN to GND disables the Reverse Polarity protection feature.
- You can connect the TPS2662x support components $R_{(ILIM)}$, $C_{(dVdT)}$, and UVLO, OVP resistors with respect to RTN pin.
- You can connect device PowerPAD to the RTN plane for an enhanced thermal performance.

ADVANCE INFORMATION

11 Power Supply Recommendations

The TPS2662x eFuse is designed for the supply voltage range of 4.5 V ≤ V_{IN} ≤ 57 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes in the designs with TPS26620, TPS26621, TPS26622, TPS26623 devices and a TVS clamp in the designs withTPS26624 and TPS26625 devices
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with 公式 9.

$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (9)$$

where

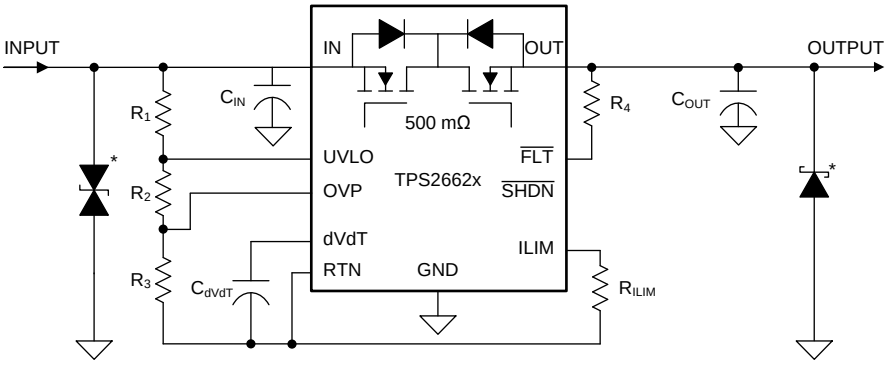
- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications it is recommended to place at least 1 µF of input capacitor to limit the falling slew rate of the input voltage within a maximum of 20 V/µs.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in 图 7.

ADVANCE INFORMATION

Transient Protection (接下页)



* Optional components needed for suppression of transients

图 7. Circuit Implementation With Optional Protection Components

ADVANCE INFORMATION

12 Layout

12.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN terminal and GND.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See 图 8 for a typical PCB layout example.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- RTN, which is the reference ground for the device must be a copper plane or island.
- Locate all the TPS2662x family support components $R_{(ILIM)}$, $C_{(dVdT)}$, UVLO, OVP resistors close to their connection pin. Connect the other end of the component to the RTN with shortest trace length.
- The trace routing for the R_{ILIM} component to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board RTN plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Designs that do not need reverse input polarity protection can have RTN, GND and PowerPAD connected together. PowerPAD in these designs can be connected to the PCB ground plane.

12.2 Layout Example

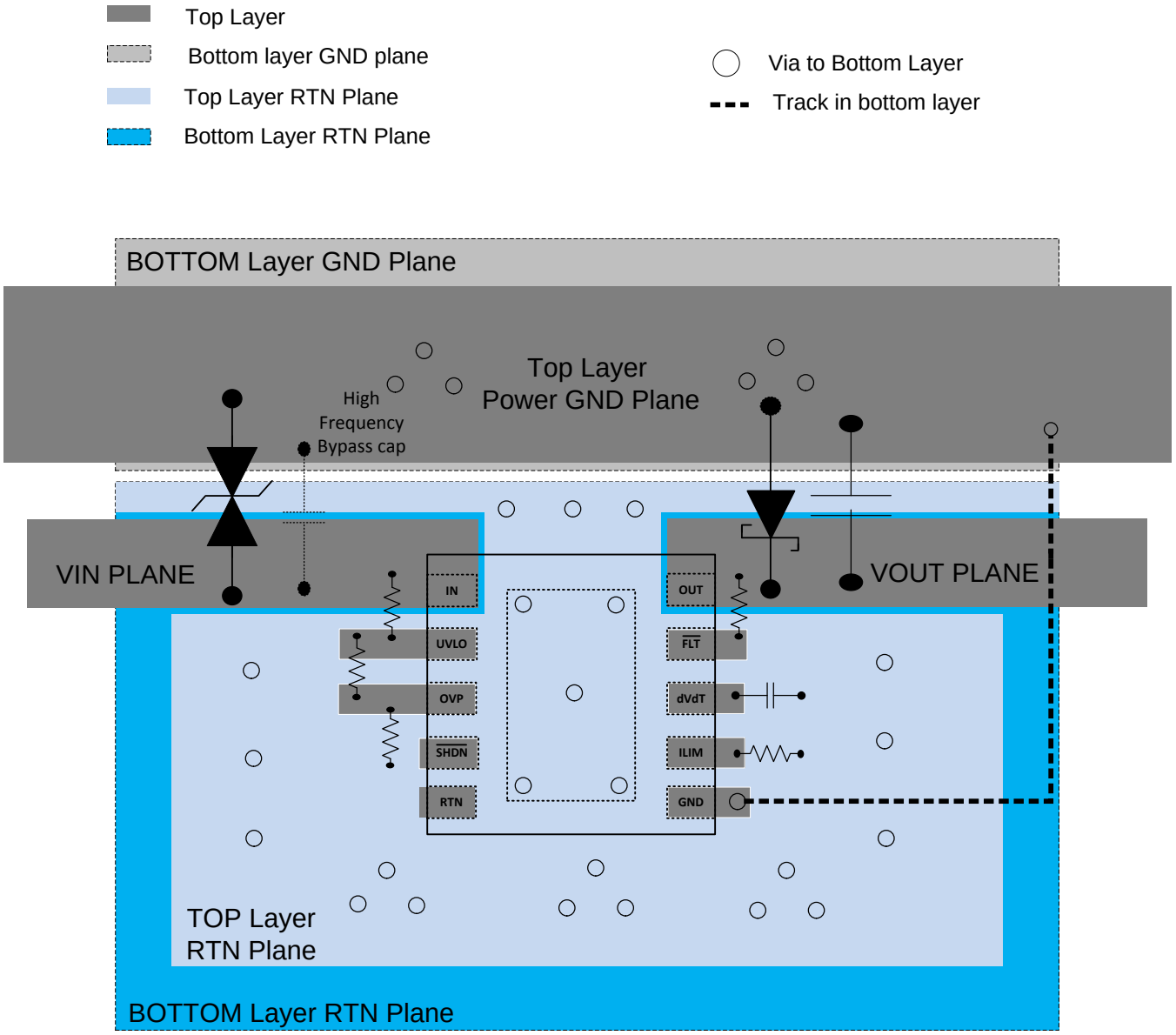


图 8. Typical PCB Layout Example With a 2 Layer PCB

ADVANCE INFORMATION

13 器件和文档支持

13.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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13.3 商标

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13.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS26620DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED00
TPS26620DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED00
TPS26620DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED00
TPS26620DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED00
TPS26621DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED01
TPS26621DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED01
TPS26621DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED01
TPS26621DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED01
TPS26621DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED01
TPS26621DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED01
TPS26622DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED02
TPS26622DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED02
TPS26622DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED02
TPS26622DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED02
TPS26623DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED03
TPS26623DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED03
TPS26623DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED03
TPS26623DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED03
TPS26624DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED04
TPS26624DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED04
TPS26624DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED04
TPS26624DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED04
TPS26624DRCTG4	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED04
TPS26624DRCTG4.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED04
TPS26625DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED05
TPS26625DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED05
TPS26625DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED05
TPS26625DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED05
TPS26625DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED05

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS26625DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED05

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

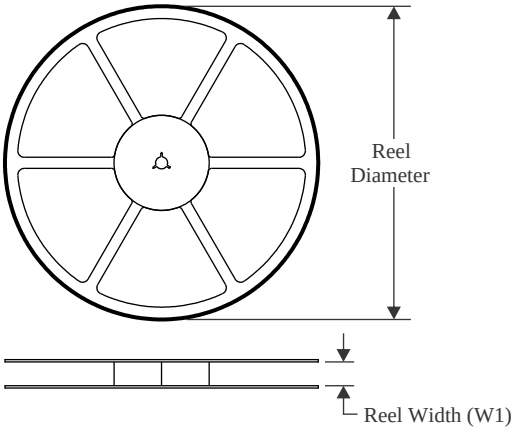
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

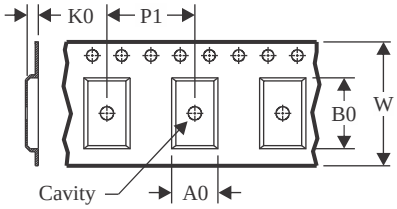
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

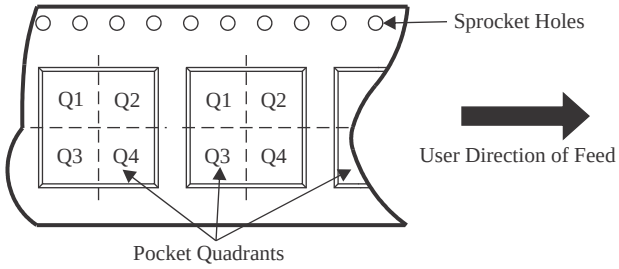


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

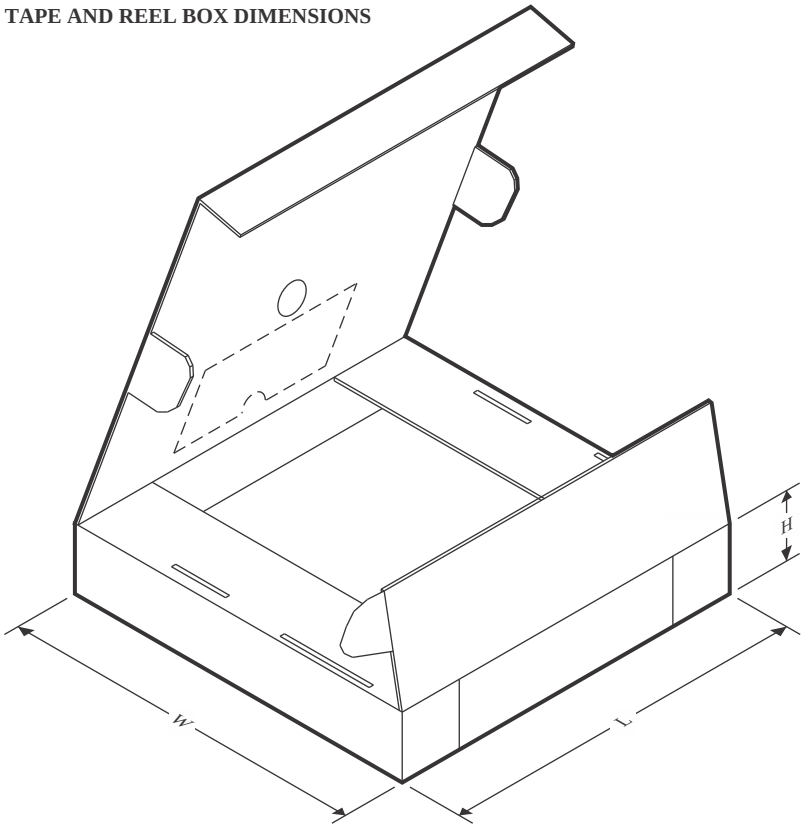
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS26620DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26620DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26621DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26621DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26621DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26622DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26622DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26623DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26623DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26624DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26624DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26624DRCTG4	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26625DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26625DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26625DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS26620DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26620DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26621DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26621DRCRG4	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26621DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26622DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26622DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26623DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26623DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26624DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26624DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26624DRCTG4	VSON	DRC	10	250	210.0	185.0	35.0
TPS26625DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26625DRCRG4	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26625DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

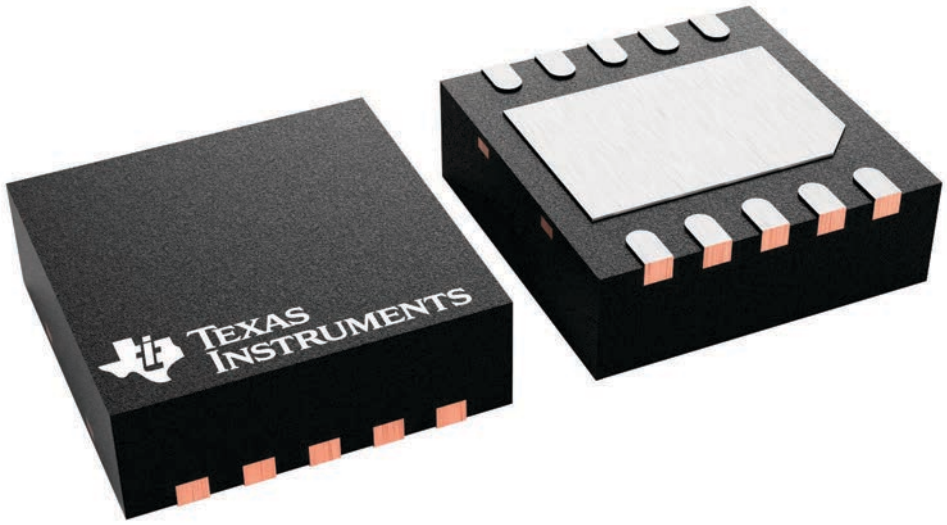
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



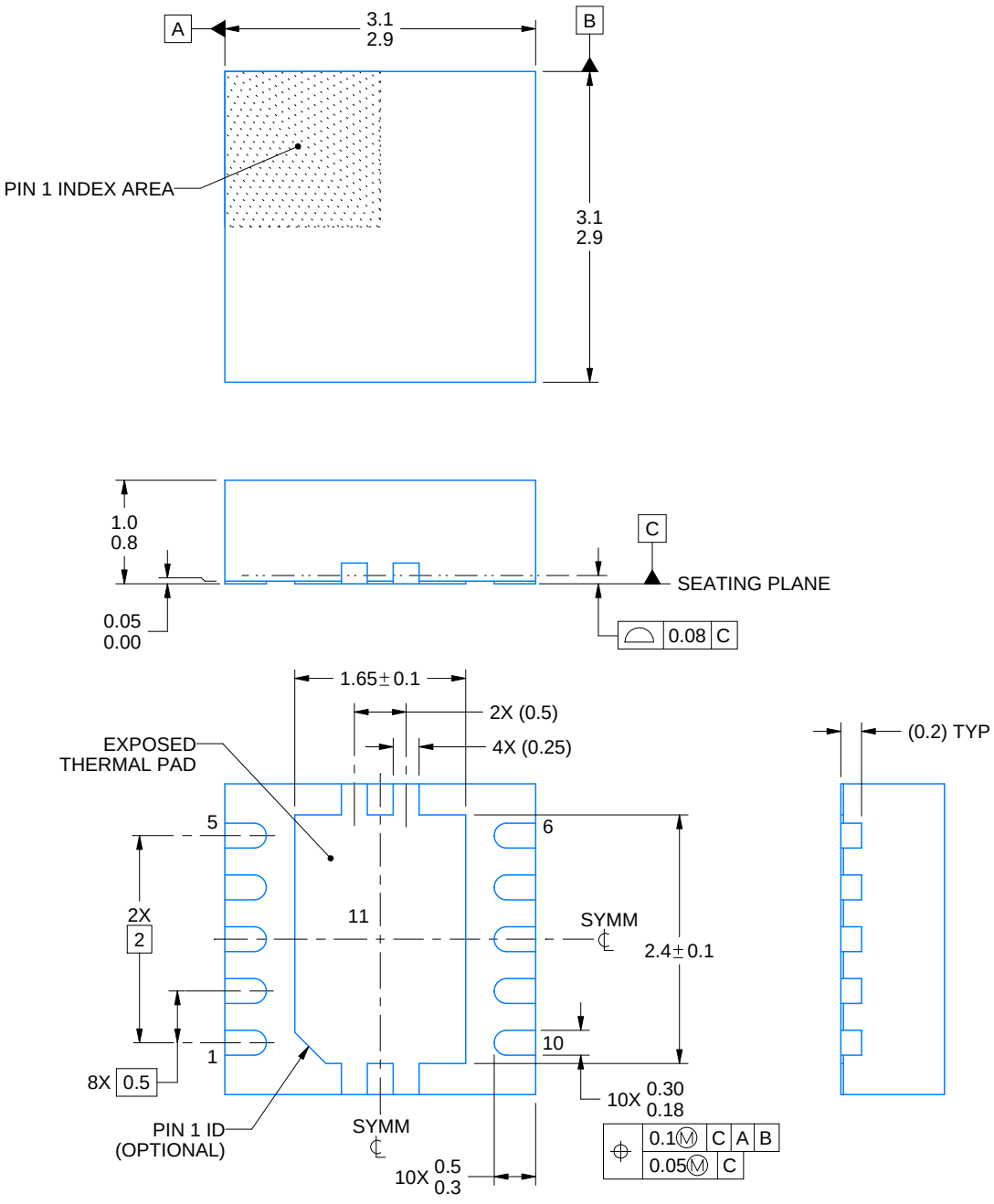
4226193/A

DRC0010J

PACKAGE OUTLINE

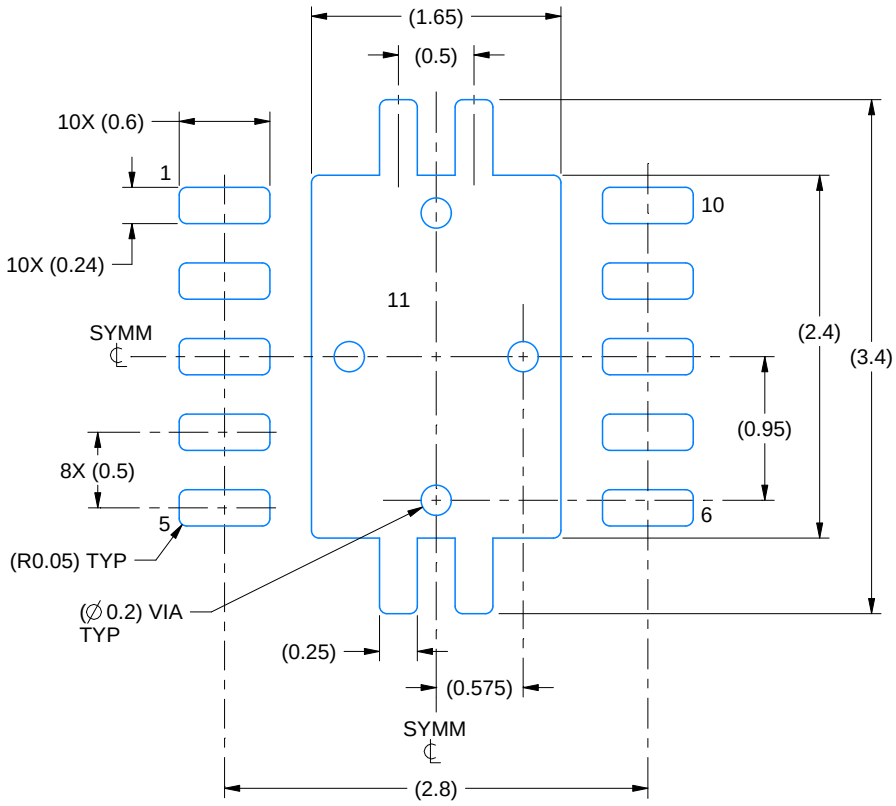
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

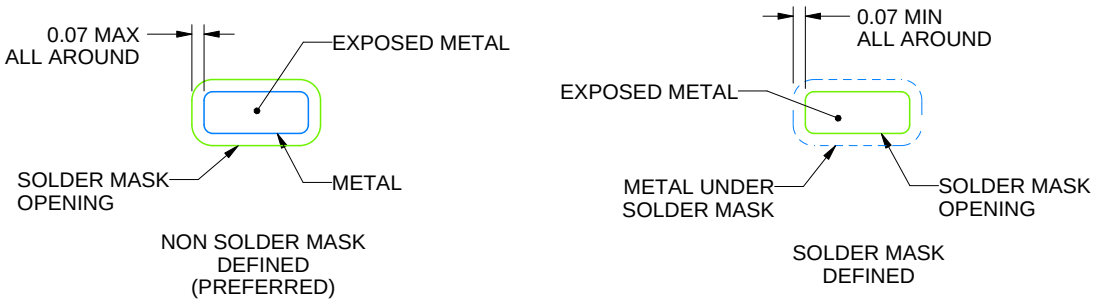


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

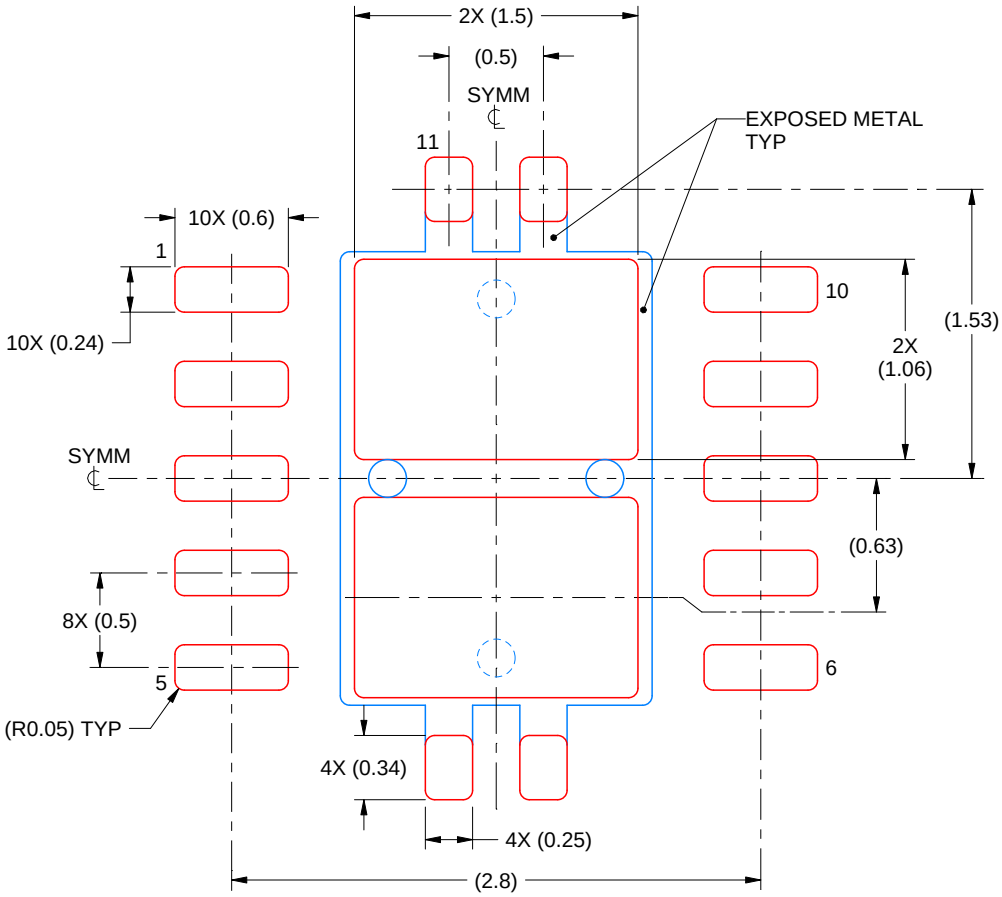
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月