# *TI Designs：TIDEP-0067*
# *66AK2Gx DSP + ARM 处理器电源解决方案参考设计*

## TI Designs

此 TI 设计是一款基于 K2G 多内核 DSP + ARM® 片上系统 (SoC) 和配套 TPS65911x 电源管理集成电路 (PMIC) 的电源参考平台。该电源解决方案设计还包含支持 12V 输入的第一级降压转换器和用于 DDR3L 存储器的 DDR 终端稳压器。该参考设计经过了测试，包括硬件参考 (EVM)、软件（处理器 SDK）和测试数据。

### 设计资源

| | |
|---|---|
| TIDEP0067 | 工具文件夹（包含设计文件） |
| 66AK2G12 | 产品文件夹 |
| TPS65911 | 产品文件夹 |
| TPS54620 | 产品文件夹 |
| TPS54429 | 产品文件夹 |
| K2G 通用 EVM | EVM 工具文件夹 |
| K2G 1GHz GP EVM | EVM 工具文件夹 |
| 适用于 K2G 的处理器 SDK | 下载软件 |

TI E2E™ Community

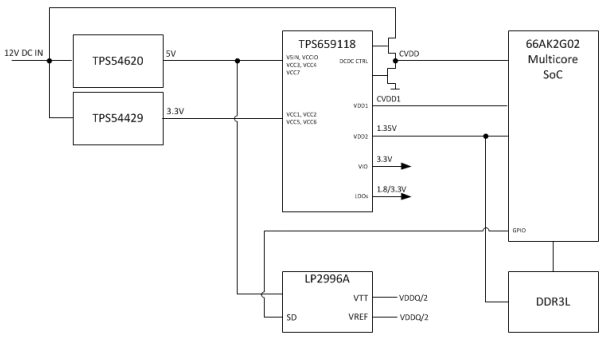
咨询我们的 E2E 专家

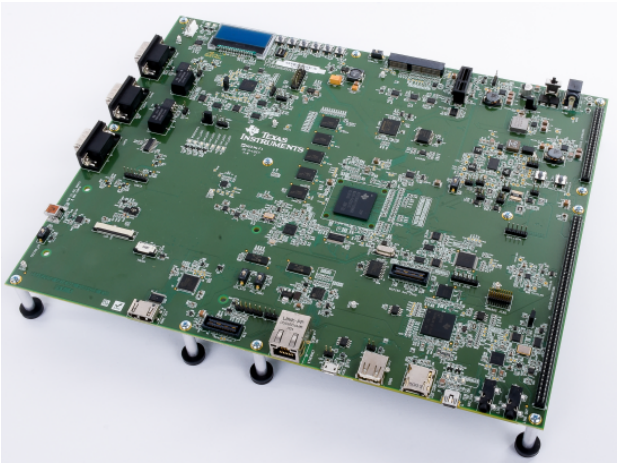
### 特性

- TPS54620 和 TPS54429：用于将 12V 输入转换为 3.3V 和 5V 输出的第一级降压转换器。
- TPS65911x 配套 PMIC，支持 SoC 和 DDR3L 存储器所需的电源定序和电源。
- TPS65911x 具有集成式实时时钟 (RTC)，适用于时间关键型 应用。
- LP2996A DDR3L 终端稳压器。

### 应用

- 汽车音频放大器
- 家用音频
- 专业音频
- 电源保护



该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

# 1 Introduction

This TI Design is a power reference platform based on the K2G Multicore DSP + Arm® System-on-Chip (SoC) and companion TPS65911x power management integrated circuit (PMIC). This power solution design also includes the first stage buck converters to support a 12 V input and the DDR termination regulator for DDR3L memory. The reference design is tested and includes hardware reference (EVM), software (Processor SDK) and test data.

# 2 K2G GP EVM Power Solution Block Diagram

The first stage buck converter devices TPS54620 and TPS54429 convert the 12-V DC input of the EVM to 5 V and 3.3 V respectively. The 5-V output from the TPS54620 provides the inputs to TPS65911x and LP2996A. The 3.3-V output form TPS54429 provides the input to TPS65911x, and 3.3-V peripheral devices on the EVM. TPS65911x provides all power supplies required for the 66K2Gx Multicore SoC, except for the 3.3-V I/O power supply.

图 1 shows the block diagram of the power solution on the K2G GP EVM.

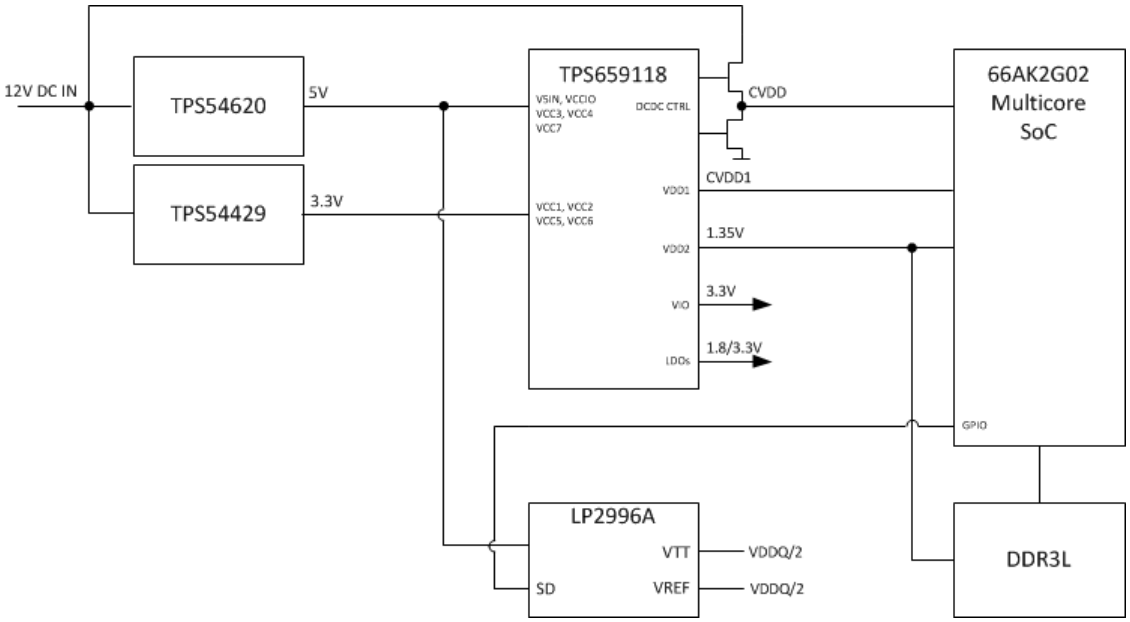



**图 1. K2G General Purpose EVM Power Solution Block Diagram**

## 3 K2G EVM Overview

The K2G GP EVM is intended to exercise the key interfaces on the K2G device. The K2G GP EVM includes the following features:

- Memory
  - 2 GB of DDR3L with ECC (32-bit data + 4-bit ECC)
  - 512 Mbit of QSPI Flash
  - 2 Gbit of NAND Flash
  - 128 Mbit of SPI Flash
  - 128 kByte of 12C EEPROM for Boot support from 12 C
  - 16 GByte eMMC
  - Micro-SD Card slot (32 GB micro-SD card included)
- Connectivity
  - Gbit Ethernet: RGMII through Micrel KSZ9031 PHY RJ45 jack
  - USB 2.0 × 2: Micro A/B connector, Host connector
  - PCIe Gen 2: Single lane card slot (root complex only)
  - COM8 connector for use with WiLink 8 modules
- Display
  - 4.3" Touch LCD display (sold seperately)
  - HDMI Tx
- Audio
  - AIC3106 stereo code
  - 3.5 mm stereo jack ×2 supports stereo analog input and output
  - All McASP signals routed to audio expansion connector
- General Purpose Serial
  - SPI and 12C ports not already used for memory, or control are routed to serial expansion connector
  - UART through RS232 chip and DB9 connector, UART over USB
- Automotive
  - MLB supported through expansion connector
  - DCAN supported through transceivers, DB9 connectors
- Emulation
  - Onboard XDS200 through mini-USB connector
  - MIPI-60 header for external emulators
  - TRACE is supported with some caveats (resistor-muxed with display signals)
- Power
  - Provided through TPS65911x PMIC – factory-programmed with K2G power-up sequence
    - 3 step-down DC–DC converters
    - 8 LDOs
    - 12C and enable signals

- Board Management Controller
  - Mainly intended for automated testing; not intended for end-products
  - May control boot modes, power-up, and more
  - Character display for system status
- Clocking
  - K2G is unique among K2 devices because the K2G generates most clocks internally, including audio frequency clocks. DDR, USB, Ethernet, and more. Clocks may be generated internally. This is the default mode on the EVM.
  - A CDCM6209 is also included and generates SYSCLK, DDR ref clock, USB clcok, and PCIe clock.

图 2 shows the K2G general purpose EVM.

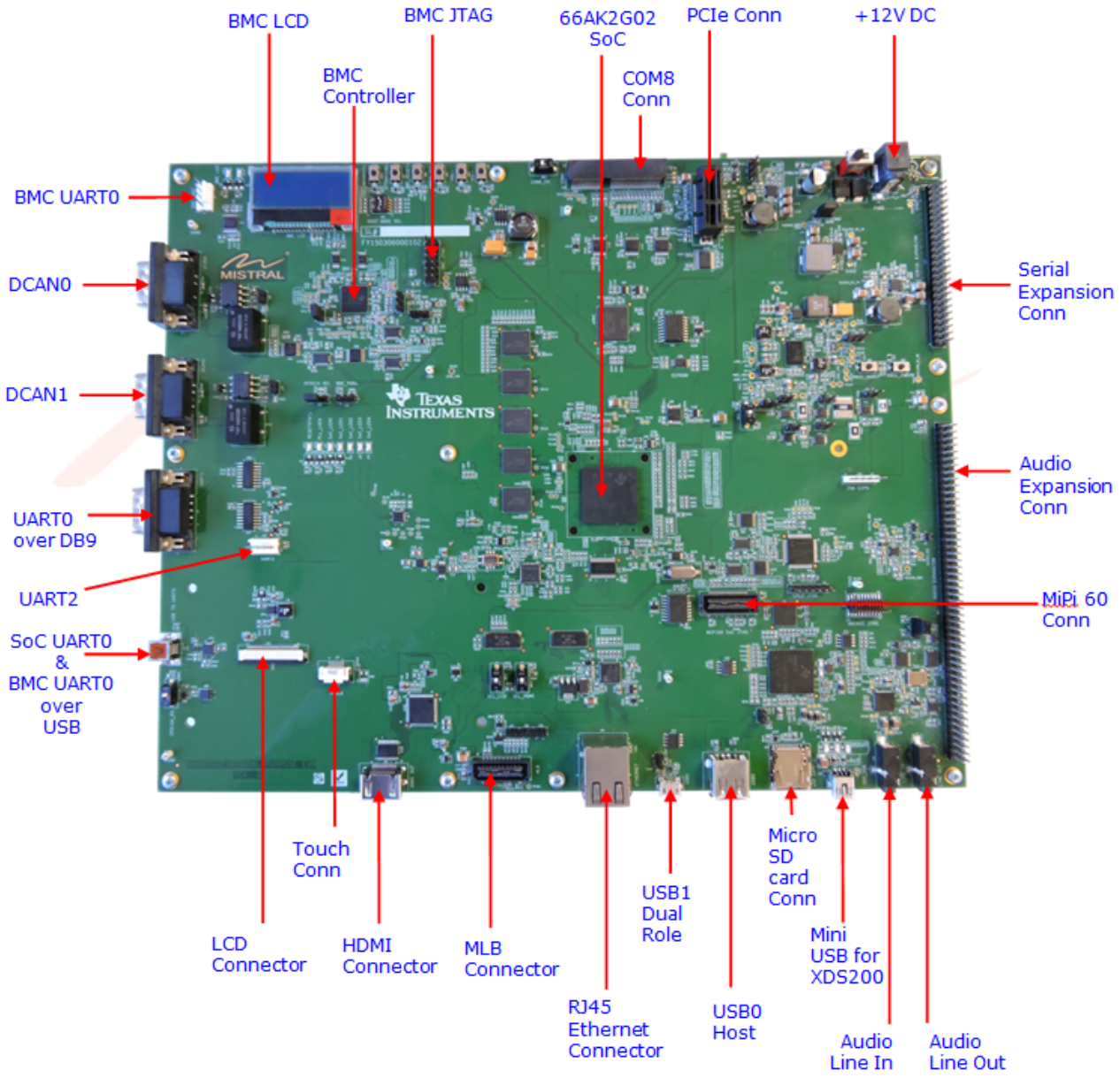



**图 2. K2G General Purpose EVM**

## 4 Software

Software for the K2G EVM is available by downloading the Processor SDK.

## 5 K2G EVM

The 66AK2Gx SoC supports the following features:

- Processor Cores and Memory
  - ARM Cortex A15 up to 1000 MHz
    - 32 KB L1D, 32 KB L1P, 512 KB, L2 cache
  - C66x DSP up to 1000 MHz
    - 32 KB L1D, 32 KB L1P, 1 MB L2
  - ECC on all memory
- Industrial and Control Peripherals
  - 2 Industrial Communication Subsystems enable cut through, real-time and low latency industrial Ethernet protocols
  - Programmable real-time I/O enables versatile field bus and control interfaces
- Security and Crypto
  - Standard secure boot with customer programmable OTP keys
  - Crypto
  - Package
    - 21 × 21 mm, 0.8-mm pitch BGA 625 pins

图 3 shows the 66AK2G12 diagram.

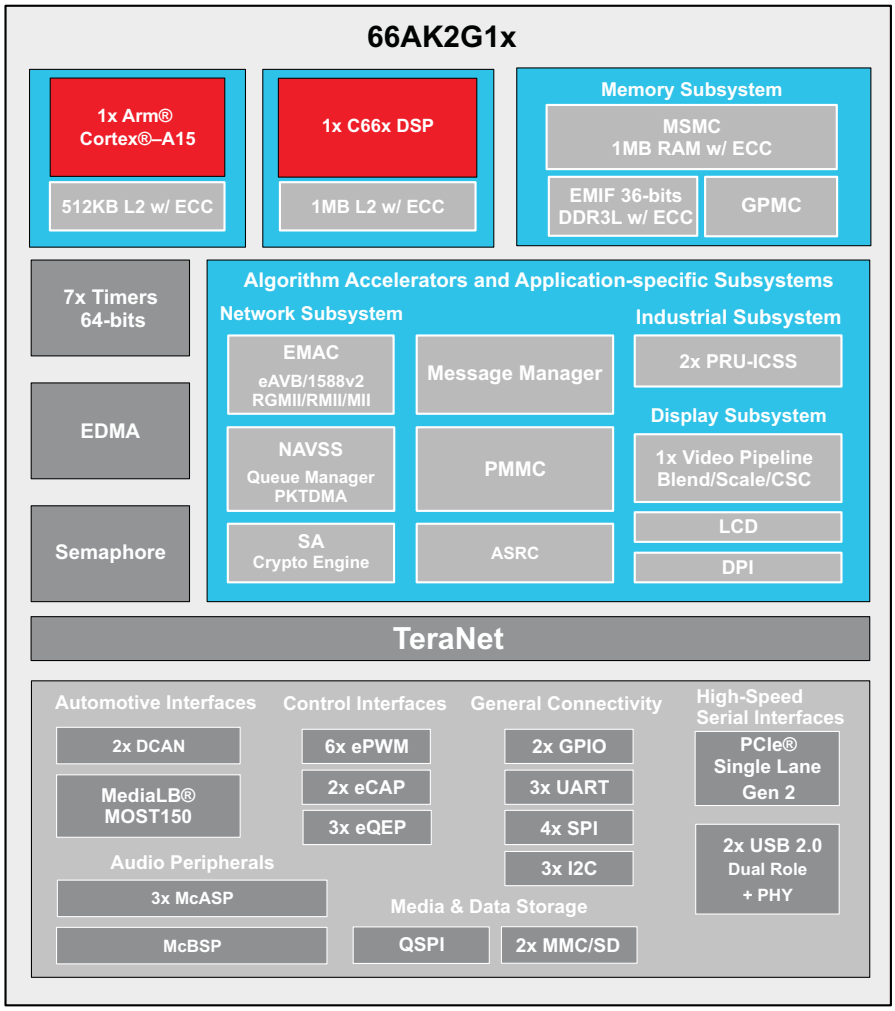





**图 3. 66AK2G12 Diagram**

# 6 TPS65911x Power Management Integrated Circuit (PMIC)

The TPS65911x is an integrated power management IC configured to operate with the 66AK2Gx SoC, combining three switch-mode buck converters, one switch-mode buck controller, and 8 linear regulators into a single BGA package. The PMIC handles power-supply sequencing and reset conditions, provides GPIO outputs for enabling external regulators or switches, and accepts i2c instructions from the processor for features such as voltage scaling and interrupt masking of various event or fault notifications. The TPS659118 is optimized to power a 66AK2G02 system, utilizing a one-time-programmable (OTP) memory configured with boot voltages, power sequencing, and other default conditions. The TPS65911A is optimized to power a 66AK2G12 system. The PMIC and processor must be connected correctly in order to meet the defined voltage, current, and sequencing requirements of the processor. A detailed lock diagram of the power management solution for the 66AK2Gx using the TPS65911x is shown in 图 4. The *TPS659118 User's Guide to Power 66AK2G02* (SWCU176) describes these connections, as well as the OTP settings defined within the PMIC. The *TPS65911A User's Guide to Power 66AK2G12* (SWCU176)

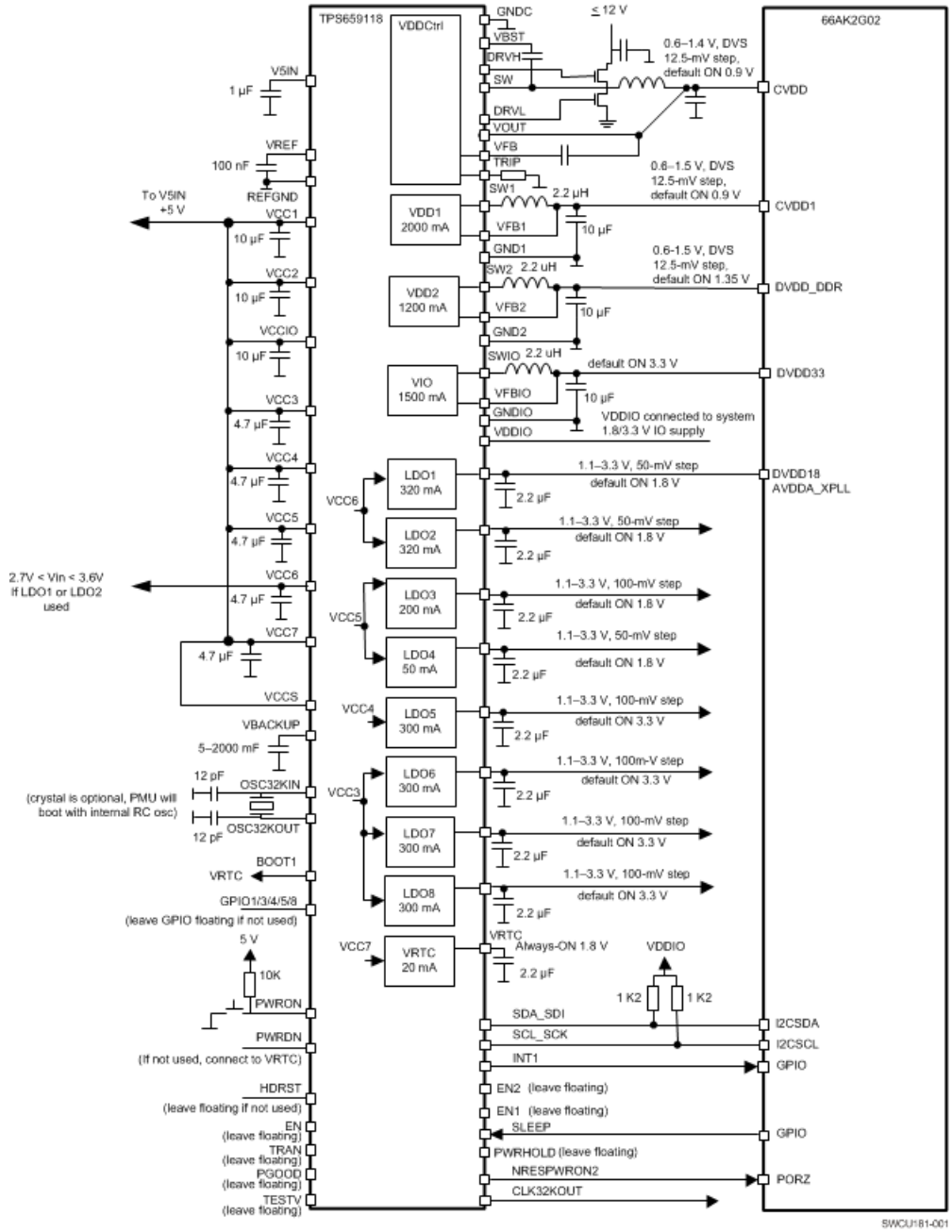



**图 4. TPS659118 PMIC with 66AK2G02**

# 7 Test Data

## 7.1 Power-Up Sequence Specification

图 5 shows the TPS65911x power-up sequencing timing.

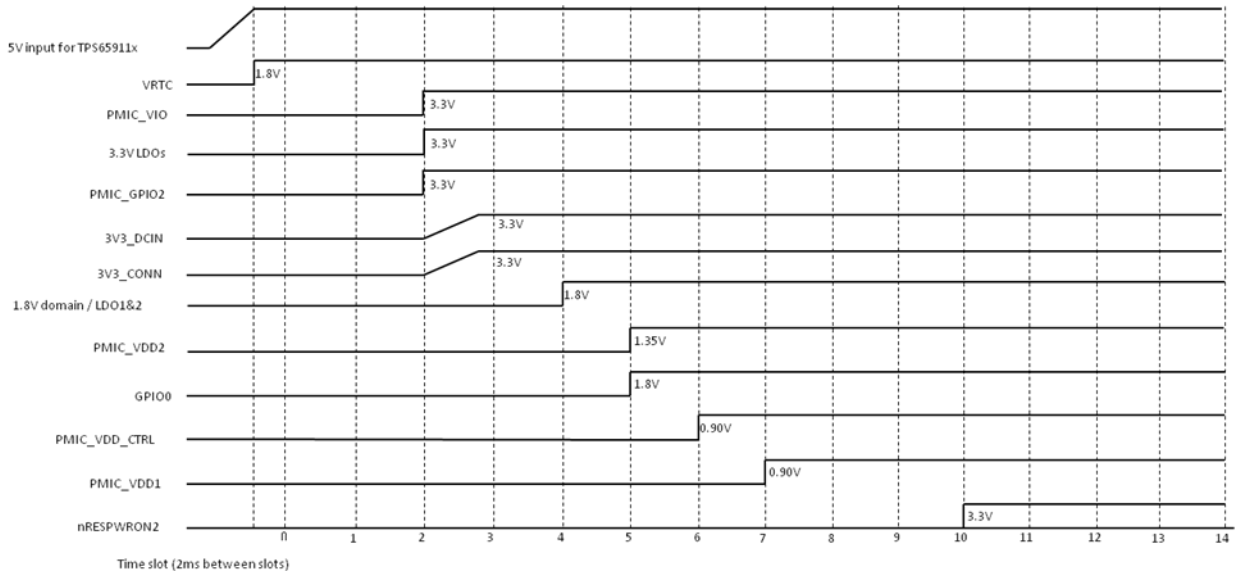



图 5. TPS65911x Power Sequencing

## 7.2 Power-Up Sequence Waveforms

The following waveforms demonstrate the power-on of the TPS65911x as required by the 66AK2Gx.

图 6 shows the power-on sequence for each of the output voltage rails and nRESPWRON2 signal respectively. The 3.3 V, 1.8 V, 1.35 V, CVDD, and CVDD1 rails turn sequentially and the nRESPWRON2 signal goes *HIGH* after all rails are *ON*.


图 6. Power-On Sequence for the TPS65911x

表 1 lists the delay time for the 3.3 V, 1.8 V, and 1.35 V processor power supplies.

表 1. Delay Time for the 3.3 V, 1.8 V, and 1.35 V Processor Power Supplies

| PLOT | EXPECTED TIMING | ACTUAL TIMING |
|---|---|---|
| 1 to 2 | N/A | 10.0 ms |
| 2 to 3 | 4.0 ms | 4.0 ms |
| 2 to 4 | 6.0 ms | 6.0 ms |
| 3 to 4 | 2.o ms | 2.0 ms |

图 7 shows the power-on sequence for the TPS65911x with nRESPWRON2.

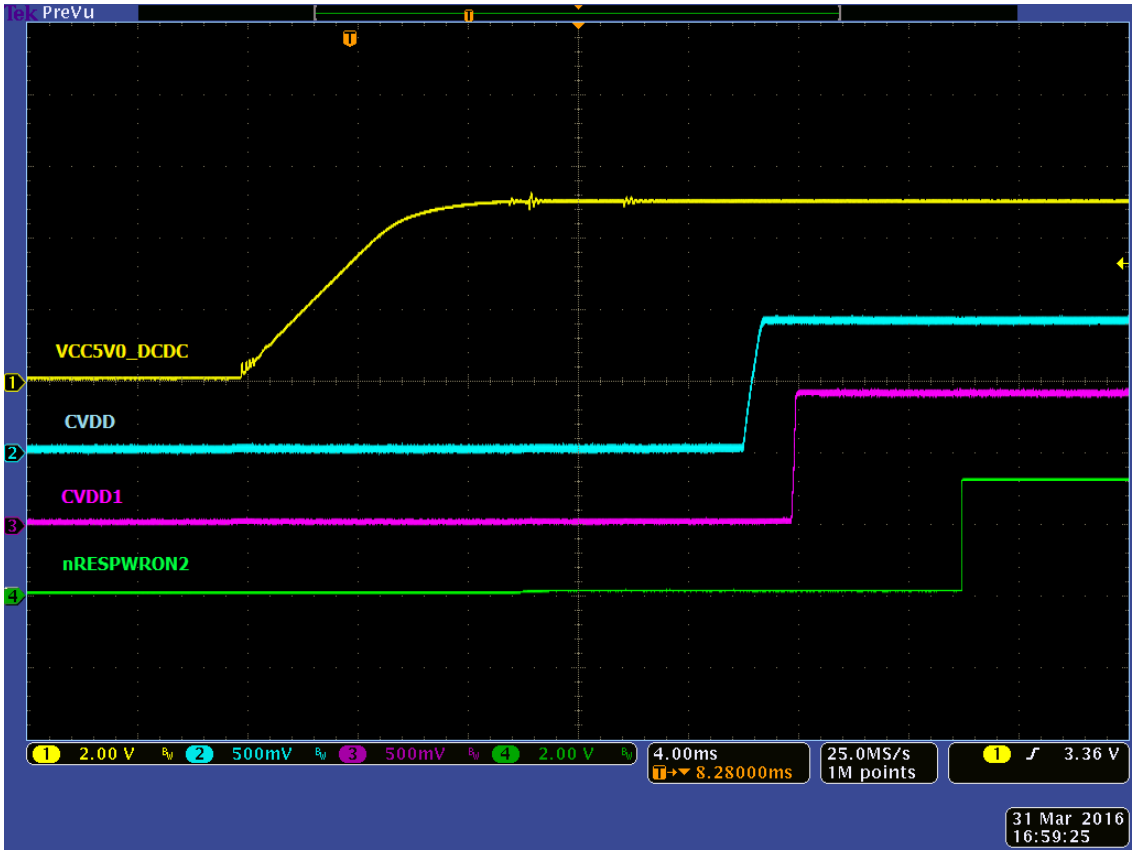



**图 7. Power-On Sequence for the TPS65911x With nRESPWRON2**

表 2 lists the delay time for the CVDD and CVDD1 processor power supplies and power on reset (POR) signal.

**表 2. Delay Time for the CVDD and CVDD1 Processor Power Supplies and Power On Reset (POR) Signal**

| PLOT | EXPECTED TIMING | ACTUAL TIMING |
|---|---|---|
| 1 to 2 | N/A | 18.4 ms |
| 2 to 3 | 2.0 ms | 2.0 ms |
| 2 to 4 | 8 ms | 8.0 ms |
| 3 to 4 | 6 ms | 6 ms |

图 8 shows the 3.3 V VIO buck converter, 3.3 V LDO5 and 1.8 V LDO1 of the TPS65911x. The 3.3 V PMIC_VIO buck converter and the 3.3 V_LDO turn *ON* simultaneously.


图 **8. Power-On Sequence for the TPS65911x Voltage Rails**

## 8 Design Files

To download the design files for TIDEP0067, see the design files at http://www.ti.com/tool/TIDEP0067.

### *8.1* *商标*

Arm is a registered trademark of ARM Limited.

# 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Original (May 2016) to A Revision | Page |
|---|---|
| • 添加了 66AK2G12 产品文件夹。 | 1 |
| • 添加了指向 EVMK2GX 工具文件夹 (1GHz K2G GP EVM) 的链接。 | 1 |
| • Changed "at 600 MHz" to "up to 1000 MHz" for both Cortex-A15 and C66x cores. | 5 |
| • Changed 66AK2G02 block diagram to 66AK2G12 block diagram. | 6 |
| • Added distinction between TPS659118 and TPS65911A. | 7 |

## 有关 TI 设计信息和资源的重要通知

德州仪器 (TI) 公司提供的技术、应用或其他设计建议、服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用； 如果您（个人，或如果是代表贵公司，则为贵公司）以任何方式下载、访问或使用了任何特定的 TI 资源，即表示贵方同意仅为该等目标，按照本通知的条款进行使用。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。

您理解并同意，在设计应用时应自行实施独立的分析、评价和 判断， 且应全权负责并确保 应用的安全性， 以及您的 应用 （包括应用中使用的所有 TI 产品）） 应符合所有适用的法律法规及其他相关要求。你就您的 应用声明，您具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。您同意，在使用或分发包含 TI 产品的任何 应用前， 您将彻底测试该等 应用 和该等应用所用 TI 产品的 功能而设计。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

您只有在为开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对 TI 资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。

TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为您辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

您同意向 TI 及其代表全额赔偿因您不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

本通知适用于 TI 资源。另有其他条款适用于某些类型的材料、TI 产品和服务的使用和采购。这些条款包括但不限于适用于 TI 的半导体产品 (http://www.ti.com/sc/docs/stdterms.htm)、评估模块和样品 (http://www.ti.com/sc/docs/sampterms.htm) 的标准条款。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122