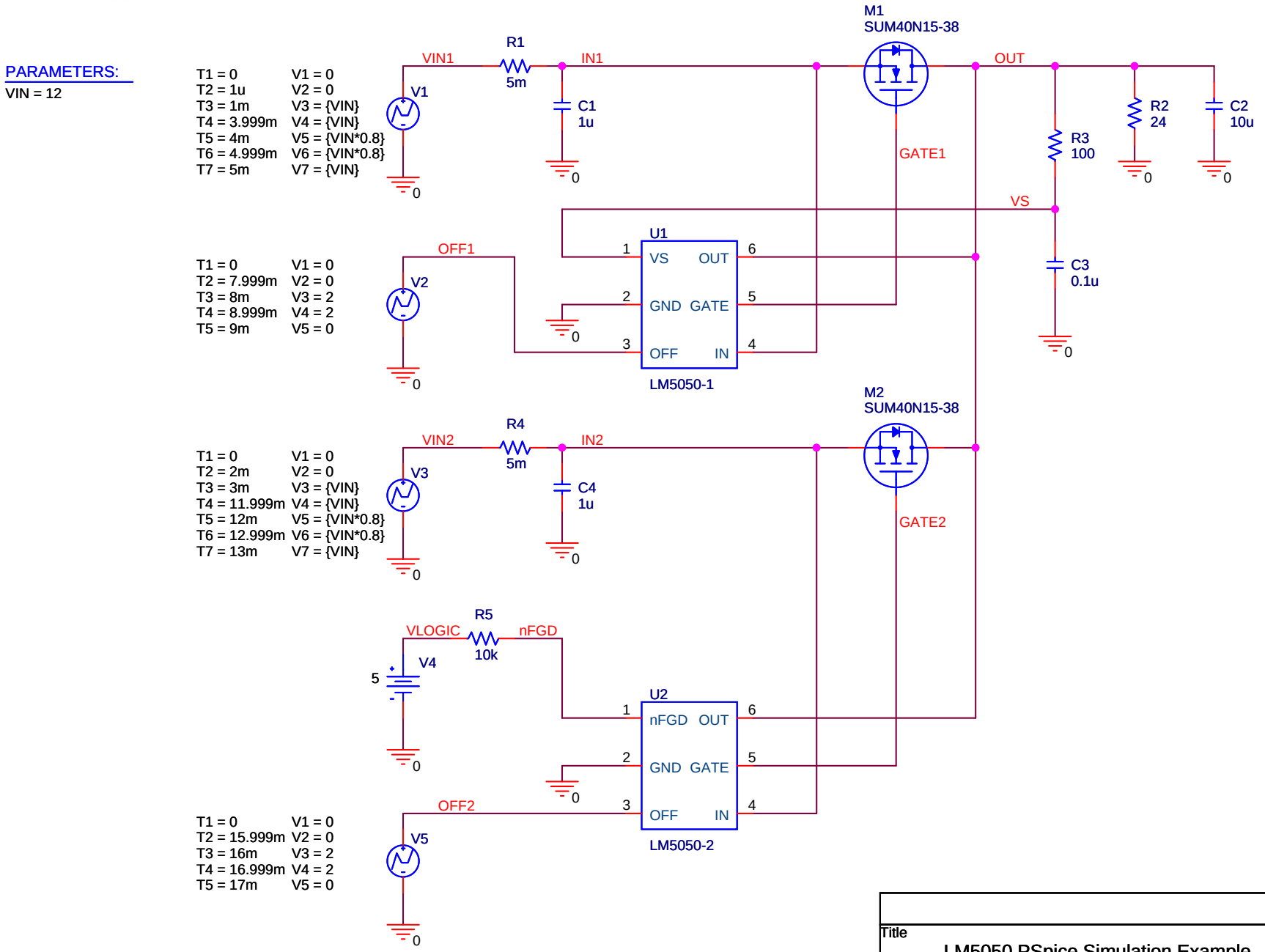
LM5050-1 and LM5050-2 High Side OR-ing FET Controllers



Title	LM5050 PSpice Simulation Example
Size A	Document Number: Model by Robert Sheehan, National Semiconductor, Santa Clara, CA
Rev A	
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LM5050-1 and LM5050-2 High Side OR-ing FET Controllers

<Introduction >
This document contains the PSPICE models and the simulation circuit example for National Semiconductor's LM5050-1 and LM5050-2.
The LM5050-1 and LM5050-2 High Side OR-ing FET Controllers operate in conjunction with external MOSFETs
as ideal rectifiers when connected in series with a power source.

<LM5050-1 Model>
The LM5050-1 model contains all of the basic features including:
- Input Operating Voltage Range 5V to 100V, Biased From VS Pin
- Current Source Gate Driver for External N-Channel MOSFET
- Gate Driver Supply Diode OR'd From IN or VS Pins
- 12V Gate Clamp with Additional Zener Protection
- 25 ns Reverse Current Comparator
- 250 ns Off Comparator
- 1.5 Ohm Gate Turn-Off Switch
- 20 mV Minimum VDS Clamp for Fast Turn-Off
- Pin Bias Currents
- Pin Reverse Voltage Diode Clamps

<LM5050-2 Model>
The LM5050-2 model contains all of the basic features including:
- Input Operating Voltage Range 6V to 100V, Biased From OUT Pin
- Current Source Gate Driver for External N-Channel MOSFET
- Gate Driver Supply From IN Pin
- 12V Gate Clamp with Additional Zener Protection
- 25 ns Reverse Current Comparator
- 250 ns Off Comparator
- 1.5 Ohm Gate Turn-Off Switch
- 20 mV Minimum VDS Clamp for Fast Turn-Off
- MOSFET Diagnostic Test Mode nFGD Pin
- Pin Bias Currents
- Pin Reverse Voltage Diode Clamps

<Assumptions and limitations>
Model & Example Assumptions:
- Temperature variations are not considered.

<Note>
- To run the simulation, a simulation profile should be added first.
- Click 'New Simulation Profile' and set the simulation time to 20 ms.
- The simulation takes less than 1 second per 20 ms simulation on a 2.4 GHz machine.

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