Solutions for Fast Charging Electric Vehicle Supply Equipment(EVSE) Design

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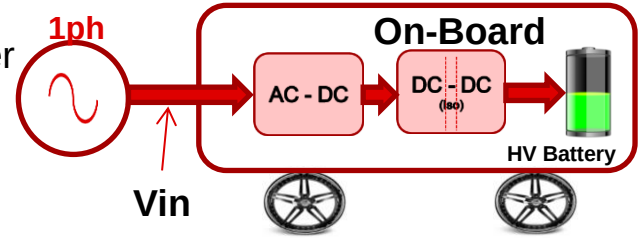
C2000 System Solutions: Digital Power

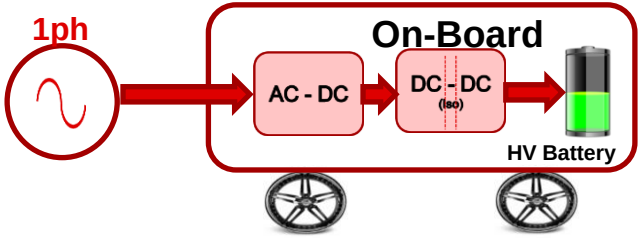
Texas Instruments

EV Chargers , typical classification and topology

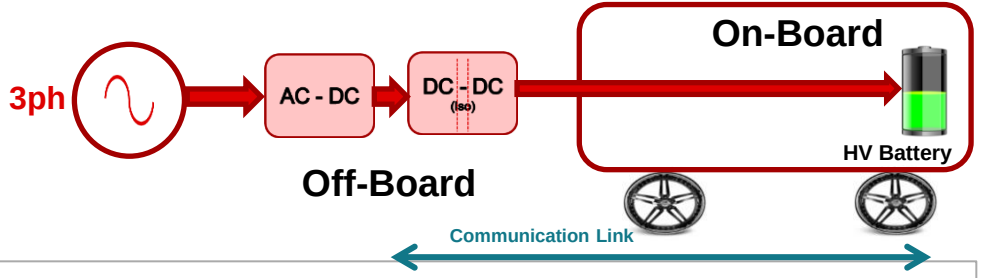
- Level 1* : Single Phase AC Charging using the on-board charger
  NEMA5-20 type outlet:
  Vin 120VAC, **Iin** 20A ~ **Pin** 2.4KW



- Level 2* : Single Phase AC charging using the on board charger
  With a NEMAL14-60 type outlet:
  Vin 120/240VAC, **Iin** 60A ~ **Pin** 14KW



- Level 3* : Three phase Off Board Charger using DC Connection
  With NEMAL15-60 type outlet
  Vin 250VAC three Phase, **Iin** 60A ~ **Pout** 45KW
  Vout: 300-600V DC



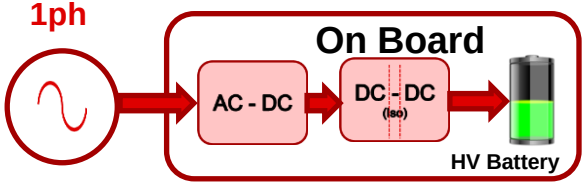
**Range per 10 min of charge

- Level described per SAEJ1772, note SAEJ1772 is incorporated in IEC6172 but level definition is different

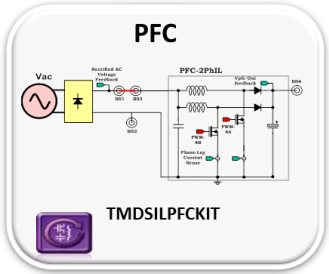
EVSE Building Blocks

Onboard charging

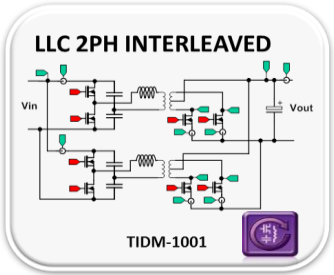
1ph

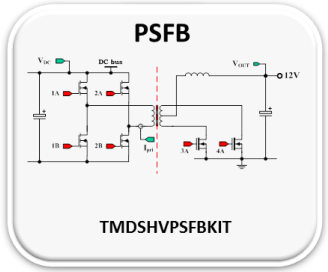


AC - DC



DC - DC (iso)

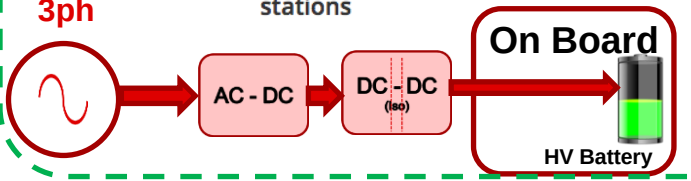




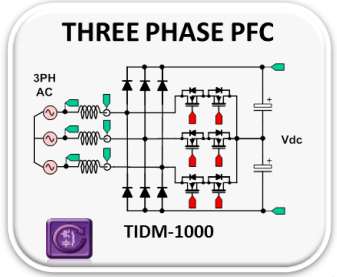
Fast Charging

Charging stations

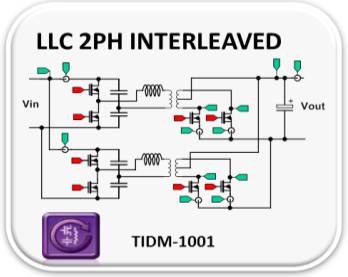
3ph

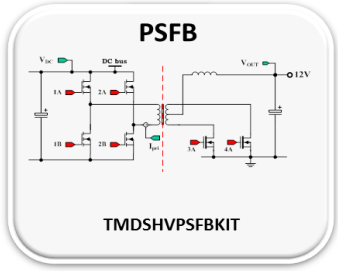


AC - DC



DC - DC (iso)



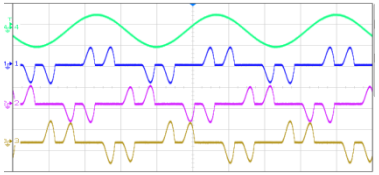


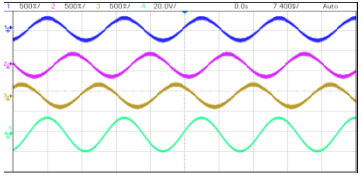
powerSUITE Enabled

Texas Instruments

Fast Charging Rectifier Solution: Three Phase PFC

- A simple three phase diode bridge draws a low power factor(PF) current and draws current with high harmonic distortion. A power factor circuit improves this current draw to be similar to a linear load, which has with high power factor and low total harmonic distortion (THD).



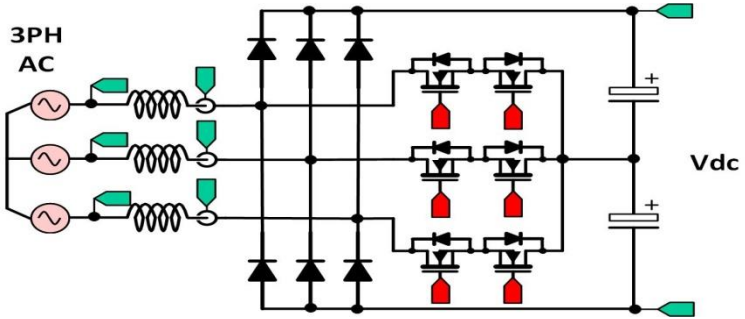


- Multiple power topologies active and passive exist for implementing three phase PFC with different advantages. Active PFC is of special interest these days as more DC type loads get added, because of it's superior power factor correction characteristics i.e. high PF, lower THD and high efficiency with the advancements in switch technology.

- **Vienna Rectifier** is a popular active PFC topology because of its
  - Inherent Three Level Switching,

  which reduces inductor size requirements
  - Lower Switching Frequency Losses
  - Switches stressed at half the output voltage
  - Low EMI

  Different variants of the Vienna rectifier exists, a popular variant is shown on the right:



TIDM-1000 : PFC 3PH VIENNA

Features

- Three Phase Power Factor Correction Rectifier Design using Vienna Rectifier controlled using C2000 MCU
- Power Spec
  - Input: 208 Vac L-L 3PH, 50Hz or
    400 Vac L-L 3PH , 60Hz
  - Output: 600V DC Nominal with 208 Vac Input
    700V DC Nominal with 400Vac Input
  - Power Max: 1.2 KW at 208Vac or
    2.4 KW at 400Vac

  Efficiency : > 98% peak efficiency
- Low total harmonic distortion (THD) < 1% (at low line)
- 50kHz PWM switching

Applications

- Off board chargers for EV
- Telecom Rectifiers
- Drives, Welding and Other industrial applications

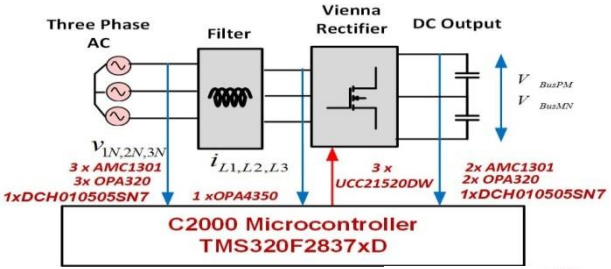
Tools & Resources

- **TI Devices**: TMS320F28377D, UCC21520DW, OPA4350UA, AMC1301, OPA320, DCH010505SN7, PTH08080WAH, TLV1117-33CDCYR, TPS71501DCKR

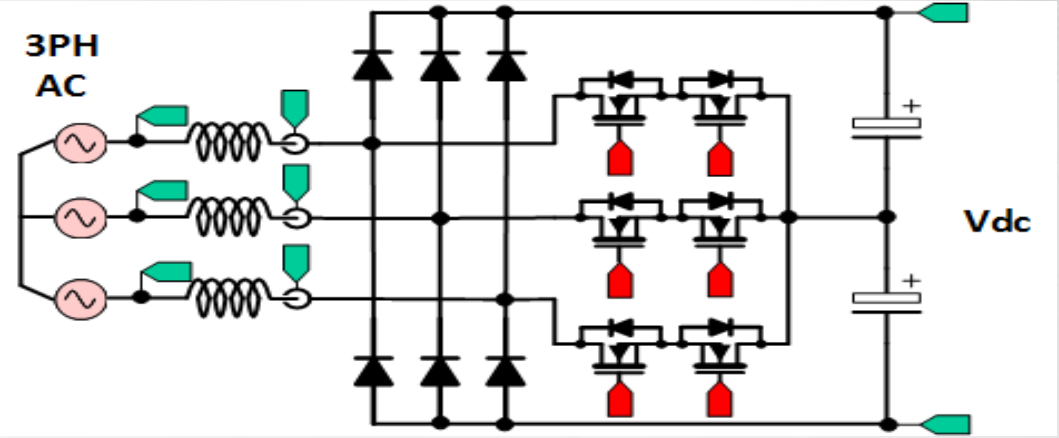
TIDM-1000

Benefits

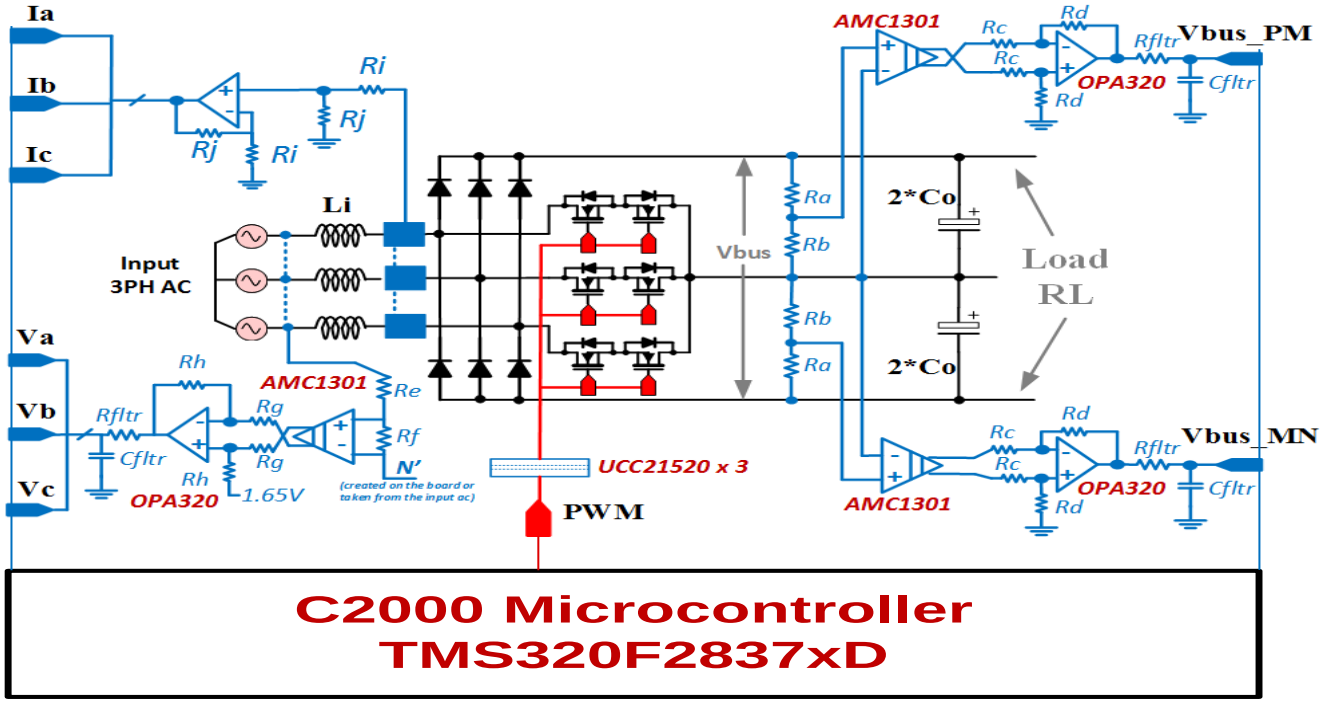
- powerSUITE enables easy adaptation of the TI Design to a custom power level and tuning of loops
- TMU accelerator enables fast control loop execution
- In built Sigma Delta Demodulators enables accurate current sensing
- On chip windowed comparators reduced components required for protection
- SFRA enables quick verification of control design



Vienna Rectifier Design



Basic Blocks for Vienna Rectifier Design

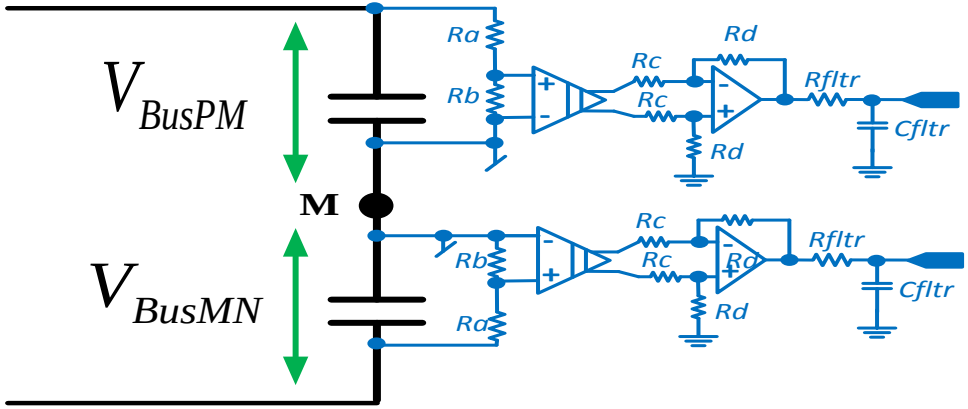


1. Sensing the System (ADC)
2. Actuating the system (PWM)
3. Controlling the system (Control Loop Design)

Isolated Bus Voltage Sensing

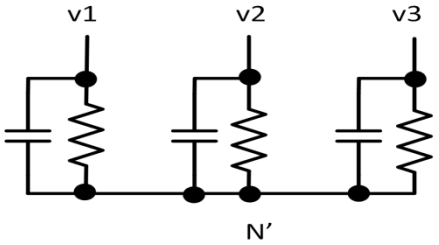
- Due to the high power nature of the applications in which Vienna Rectifier is used, isolated voltage sensing is required for the bus voltage.

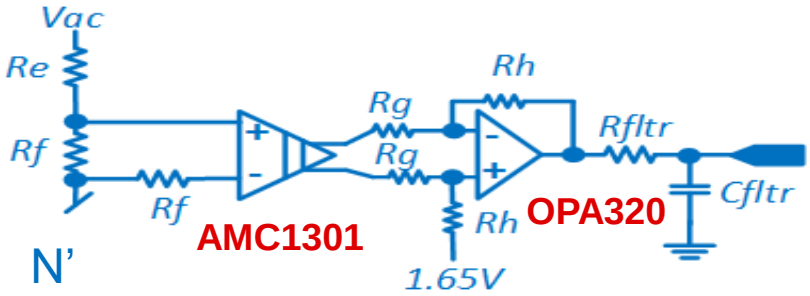
- As the bus voltage is split across two capacitors both need to be measured to enable bus balance controller.



Measuring Three Phase Voltages Line to Neutral in a Three Wire System

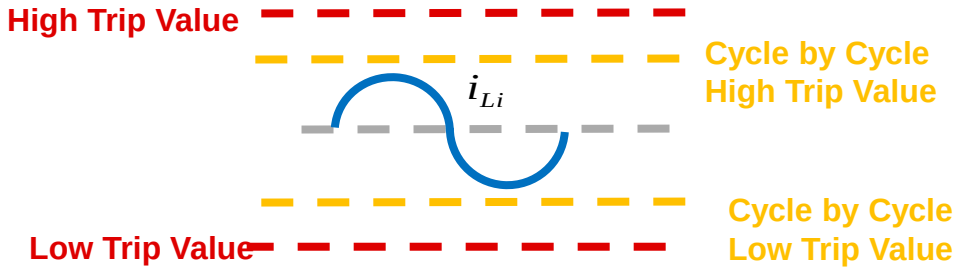
- Many three phase applications mandate use of three wire system
- Line to Neutral voltage is a critical measurement signal that is used in the control for following the input voltage, however direct neutral point connection may not be available because of application constraints.
- A virtual neutral is hence created and used for the measurement of L-N voltage using a star connection of resistors and capacitors.
- Next an isolated amplifier can then be used to measure the input ac voltages

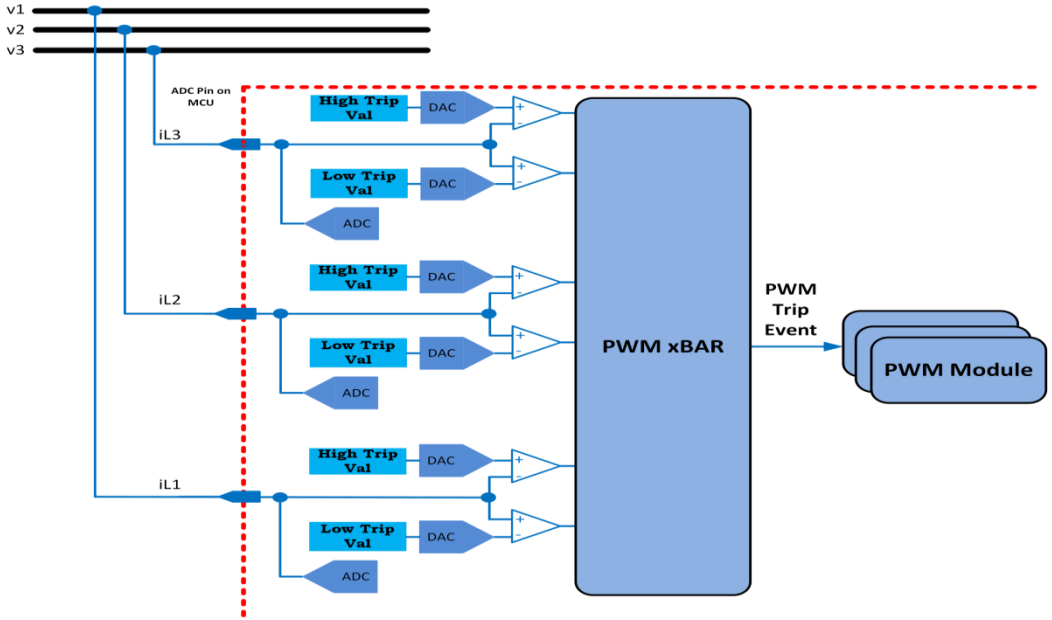




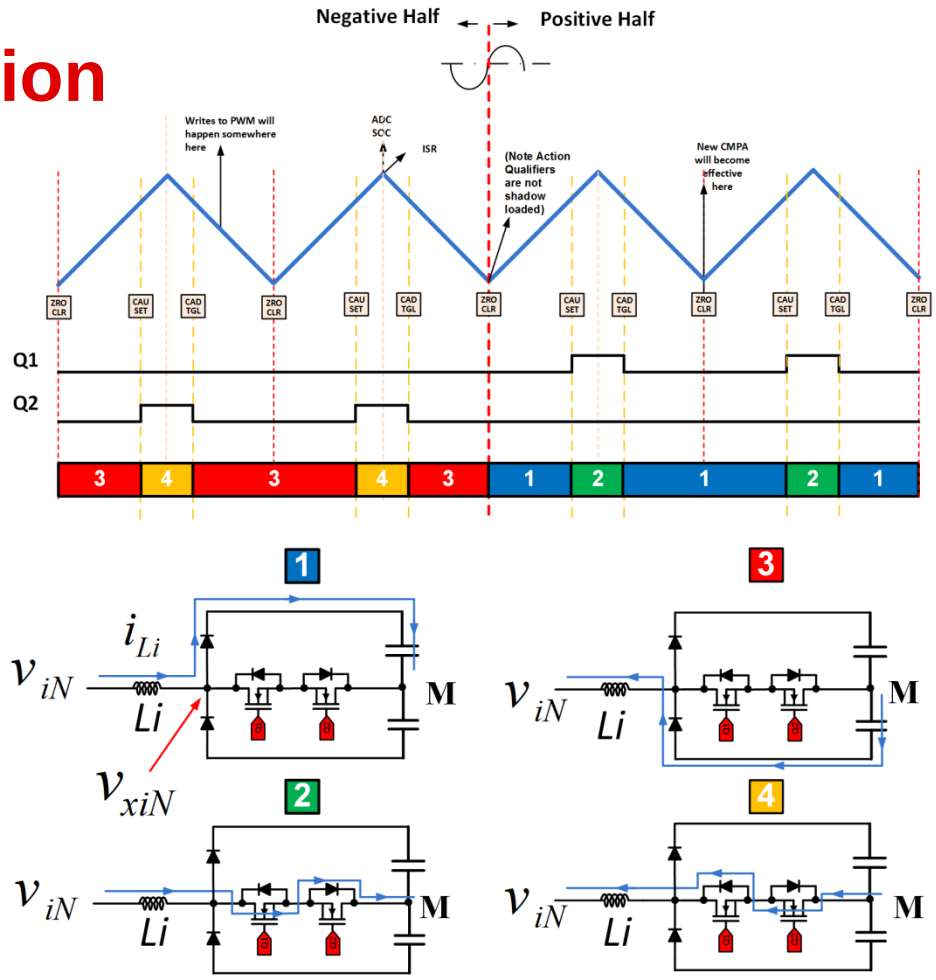
Current Protection

- Over current protection is necessary for safety purpose.
- For a three phase system it involves using multiple comparators, filters and reference generation.
- Integrated comparator subsystems in the state of the art MCUs enable addition of these features without added components on the board.
- xBAR type mechanism enables combining comparisons of three current inputs and generating signals for PWM tripping.
- Advanced features with two level of comparisons can also be implemented using additional resources or CMPSS modules.

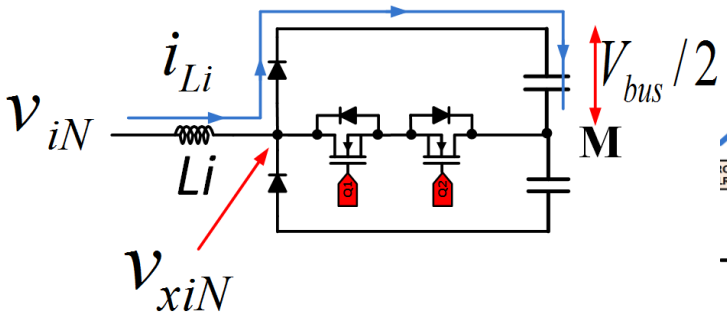


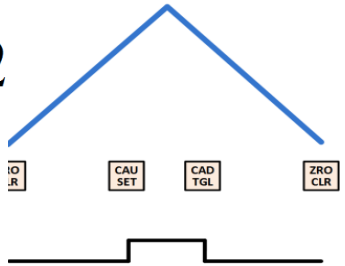


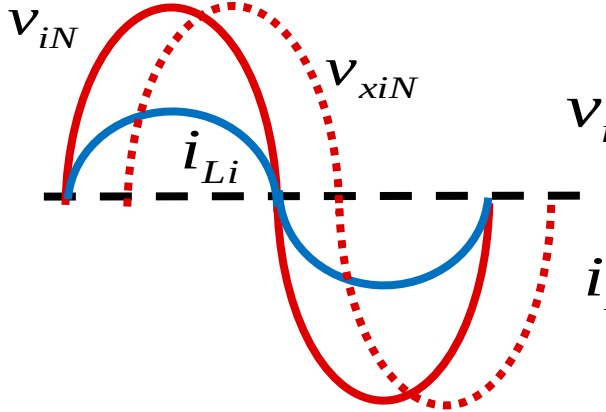
PWM Generation

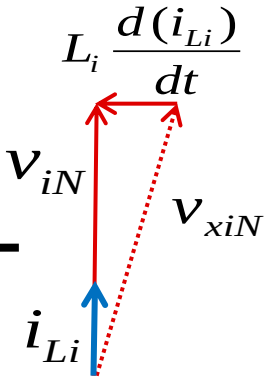


Single Phase Model of the Vienna Rectifier









- A single phase model of the Vienna Rectifier can be considered to begin understanding of the power topology
- Goal of controller is to maintain the diode bridge input voltage such that a clean unity power factor current is drawn, phasor diagram shown above.
- To achieve this, Duty cycle (D) is controlled such that the bridge input voltage is directly regulated. PWM modulation scheme is chosen appropriately to achieve this.

$$v_{xiN} = D * V_{bus}/2$$

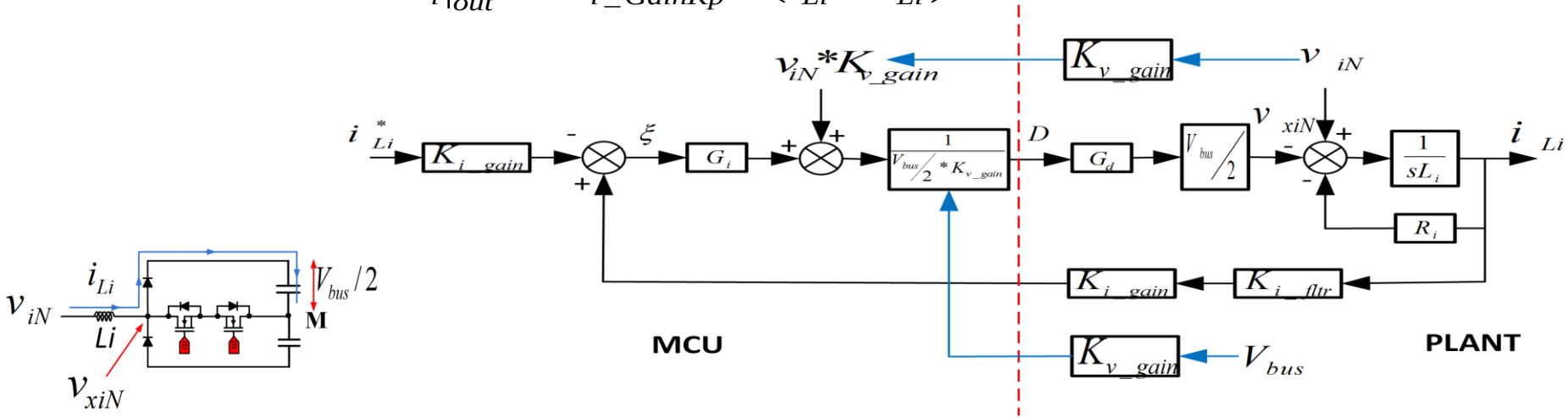
Current Loop Model

- Using Input Voltage Feedforward and DC Bus Voltage Feedforward in the current control loop structure the current loop plant is simplified as below:

$$H_{p\_i} = \frac{i_{Li}^*}{D} = \frac{1}{K_{v\_gain}} * K_{i\_gain} * K_{i\_fltr} * G_d * \frac{1}{Z_i}$$

- A simple proportional controller is used for the current control

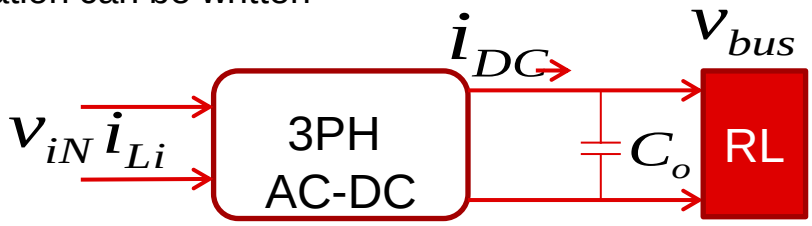
$$G_i\big|_{out} = G_{i\_GainKp} * (i_{Li} - i_{Li}^*)$$



Voltage Loop Model

Assuming efficiency of the power stage to be η following equation can be written

$$3\eta * v_{iNrms} * i_{Lirms} * = i_{DC} * v_{bus}$$



Linearizing this equation around the operating point we get

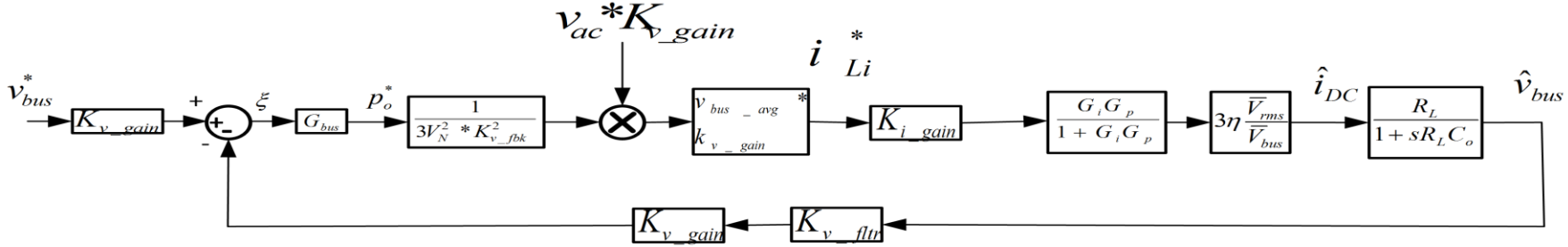
$$\hat{i}_{DC} = 3\eta \frac{\overline{V}_{Nrms}}{\overline{V}_{bus}} \hat{i}_{Li\_rms}$$

For resistive load the bus voltage and current small signal is related as

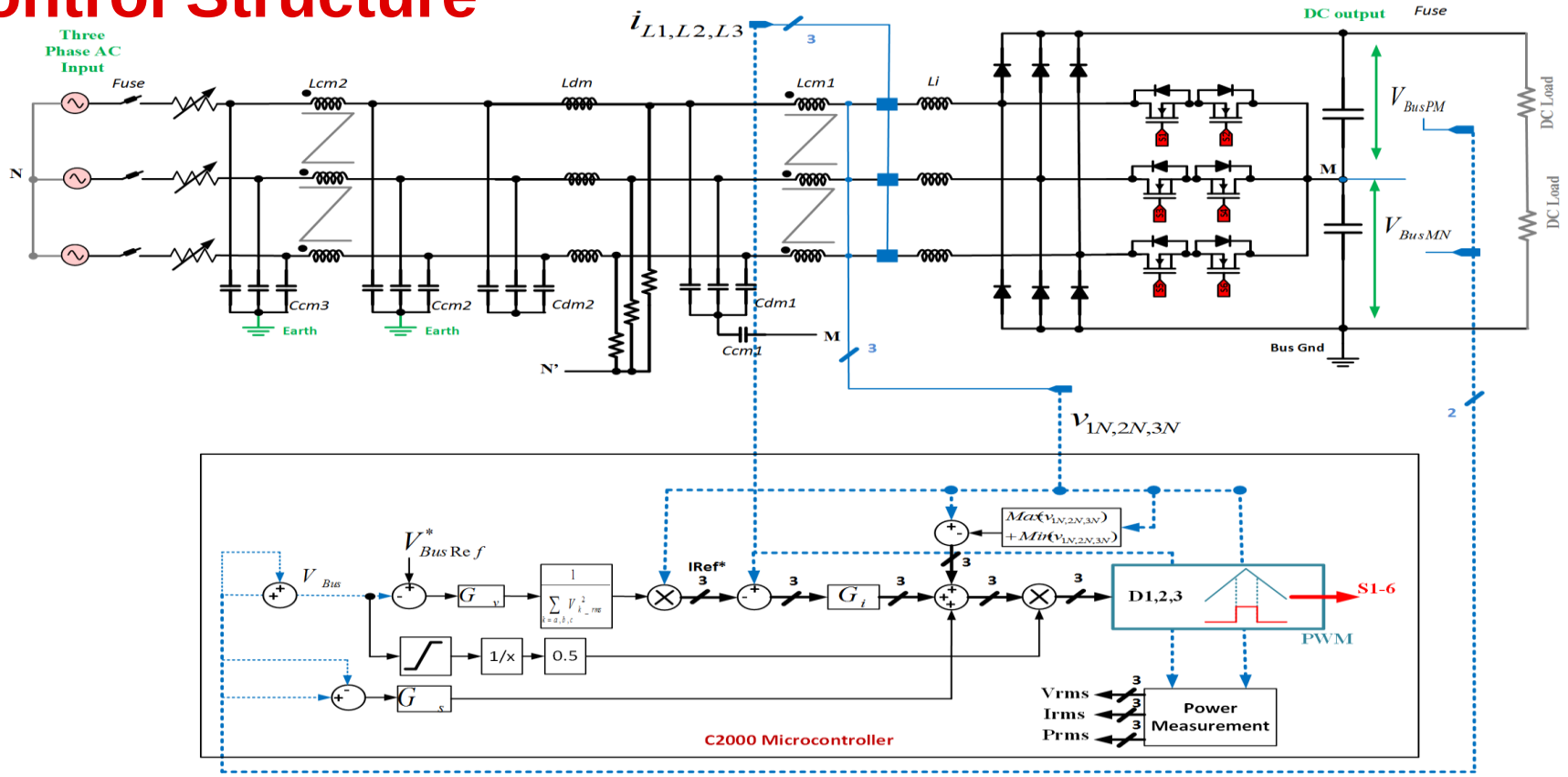
$$\hat{v}_{bus} = \frac{R_L}{1 + sR_L C_o} \hat{i}_{DC} \Rightarrow H_{Load} = \frac{\hat{v}_{bus}}{\hat{i}_{DC}}$$

With this the plant model for the voltage compensator can be written as:

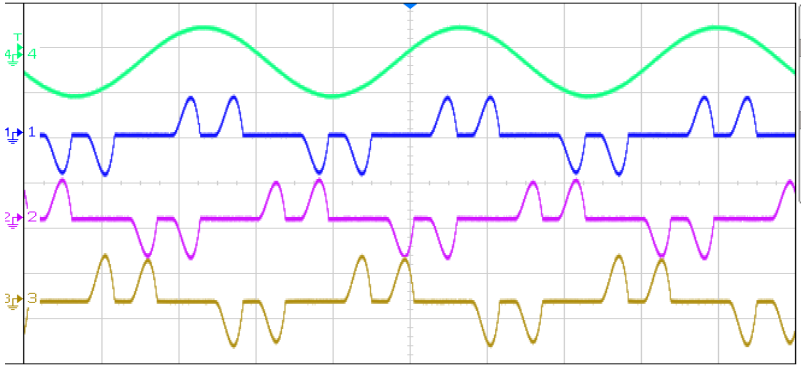
$$H_{p\_bus} = H_{load} * \eta * K_{i\_gain} * K_{v\_gain} * K_{v\_flt}$$



Control Structure

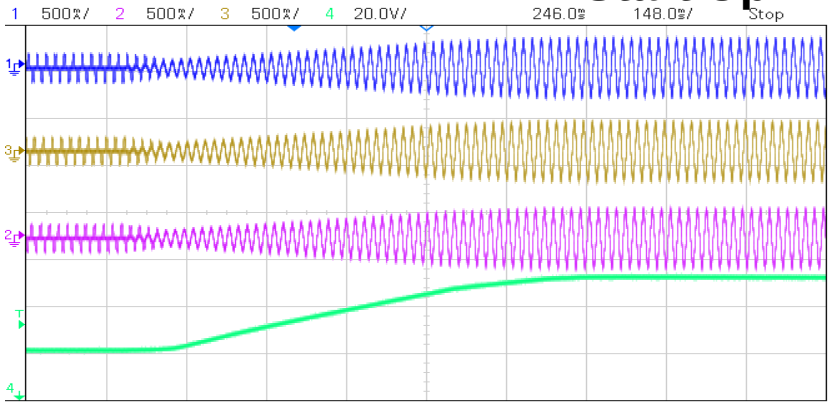


Experimental Results

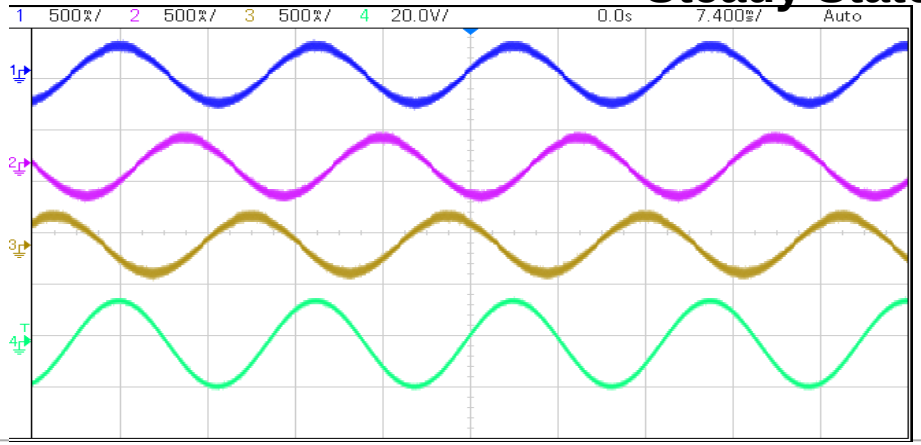


iTHD: 72.8%
PF: 0.643

Start Up

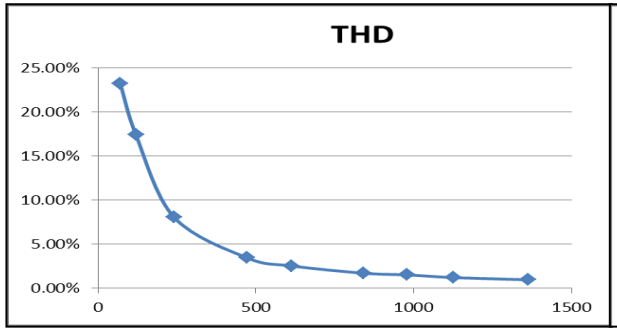


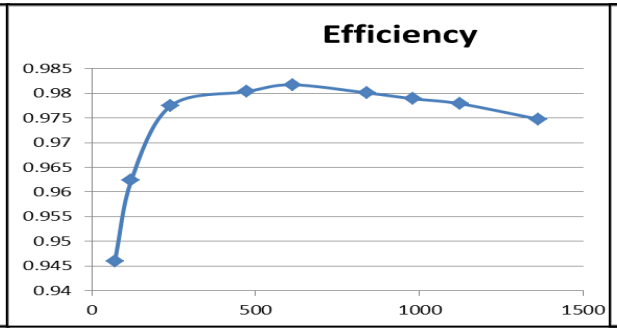
Steady State

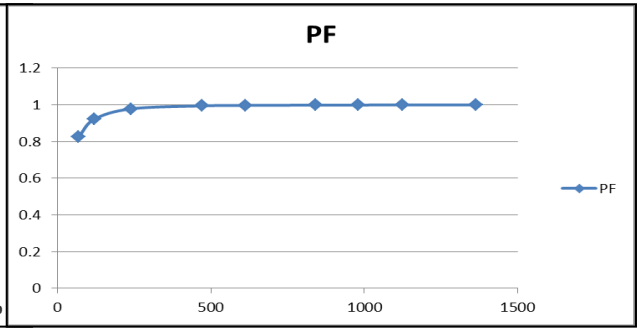


Input: 120Vrms VL-N i.e. 208Vac L-L, 60Hz
Output: 600V DC, 1.16Amps
Power: 697W
iTHD: 2.5%
PF: 0.997

Detailed Results at 208Vac / 120 VL-N

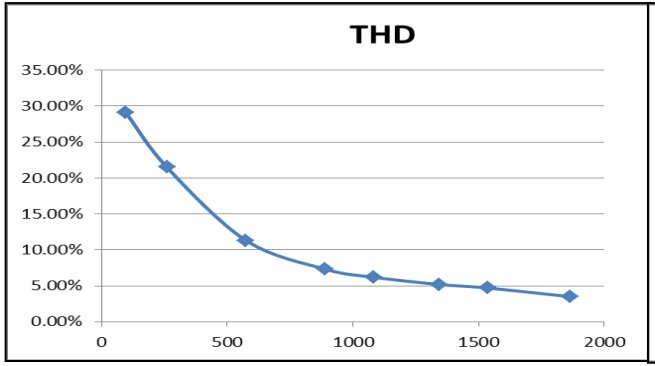


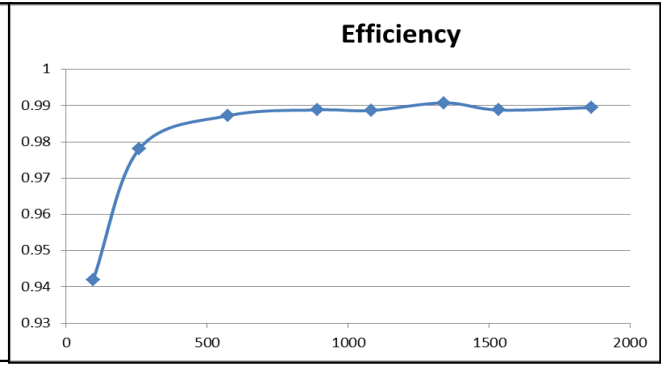


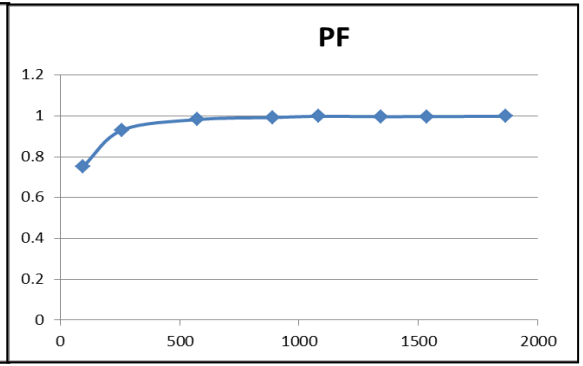


VL-N	Vout1	Vout2	VoutTotal	Pin	Iout	Pout	Efficiency	THD%	PF	%Rated Load
120	297.9	300.5	598.35	74	0.117	70.01	0.94604	23.20%	0.8263	0.061666667
120	298.6	300	598.58	124.4	0.2	119.7	0.962347	17%	0.9206	0.103666667
120	299.1	299.8	598.92	245.1	0.4	239.6	0.97743	8.09%	0.9777	0.20425
120	299.8	299	598.78	481.3	0.788	471.8	0.980342	3%	0.994	0.401083333
120	299.5	299.6	599.12	623.7	1.022	612.3	0.981723	2.54%	0.9964	0.51975
120	299.7	299.4	599.06	858.8	1.405	841.7	0.980064	1.71%	0.998	0.715666667
120	299.8	299.1	598.94	1002	1.637	980.5	0.978899	1.52%	0.9984	0.834666667
120	299.3	299.8	599.12	1151	1.878	1125	0.977879	1.22%	0.9988	0.958833333
120	300.1	298.8	598.93	1400	2.278	1364	0.974754	0.96%	0.999	1.166416667

Detailed Results at 400Vac / 230 VL-N

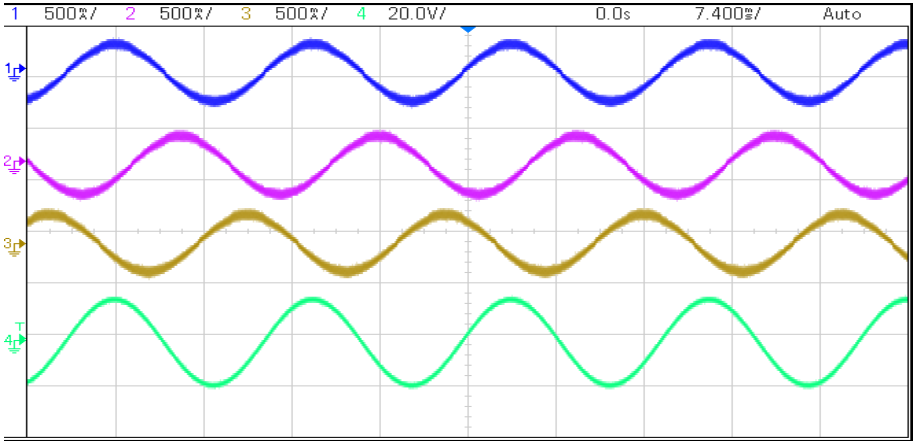






VL-N	Vout1	Vout2	VoutTotal	Pin	Iout	Pout	Efficiency	THD%	PF	%Rated Load
230	349.4	351.2	700.61	101.9	0.137	95.98	0.941939	29.10%	0.7526	0.042458333
230	349.4	351.9	701.31	265.3	0.37	259.5	0.97808	22%	0.9309	0.110541667
230	349.4	352	701.43	581.9	0.819	574.5	0.987233	11.30%	0.9823	0.242458333
230	349.5	351.8	701.29	900.7	1.27	890.6	0.988829	7%	0.9922	0.375291667
230	349.5	351.9	701.36	1095	1.543	1082	0.98867	6.20%	0.9982	0.456083333
230	349.6	351.7	701.31	1354	1.913	1342	0.990773	5.20%	0.9964	0.564208333
230	349.6	351.4	701.04	1553	2.191	1536	0.988785	4.70%	0.9972	0.64725
230	349.8	351.2	700.95	1884	2.66	1865	0.989454	3.50%	0.998	0.785166667

208 VL-L Steady State Results



Input: 120Vrms VL-N i.e. 208Vac L-L, 60Hz
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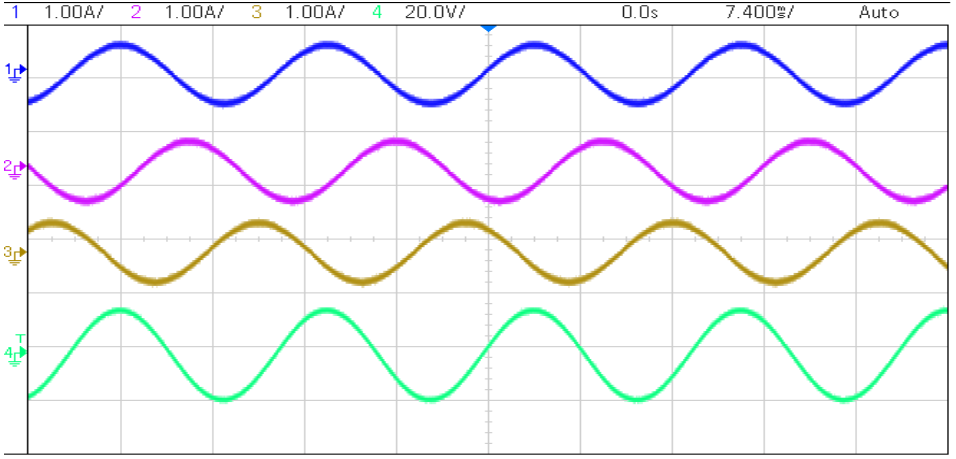
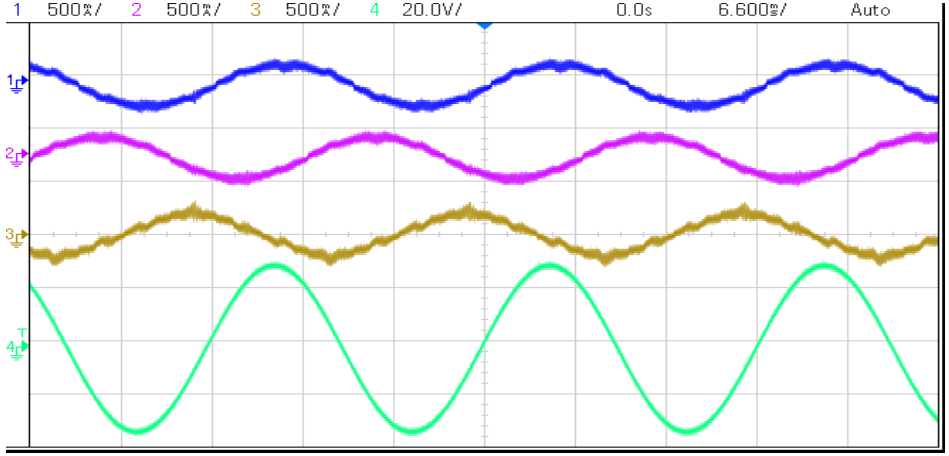
iTHD: 2.5%
PF: 0.997

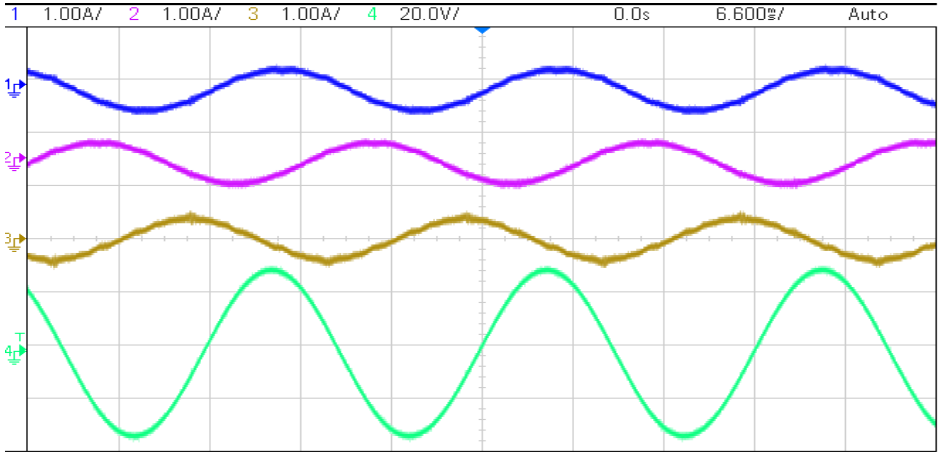


Input: 120Vrms VL-N i.e. 208Vac L-L, 60Hz
Output: 600V DC, 2.278Amps
Power: 1400W
iTHD: 0.96%
PF: 0.999

400 VL-L Steady State Results

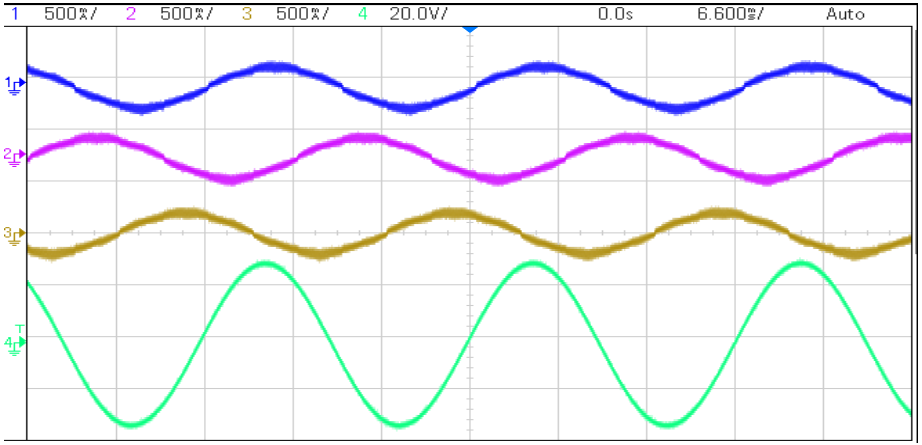


Input: 400Vac L-L, 50Hz
Output: 700V DC, 1.363Amps
Power: 960W
iTHD: 7%
PF: 0.9922

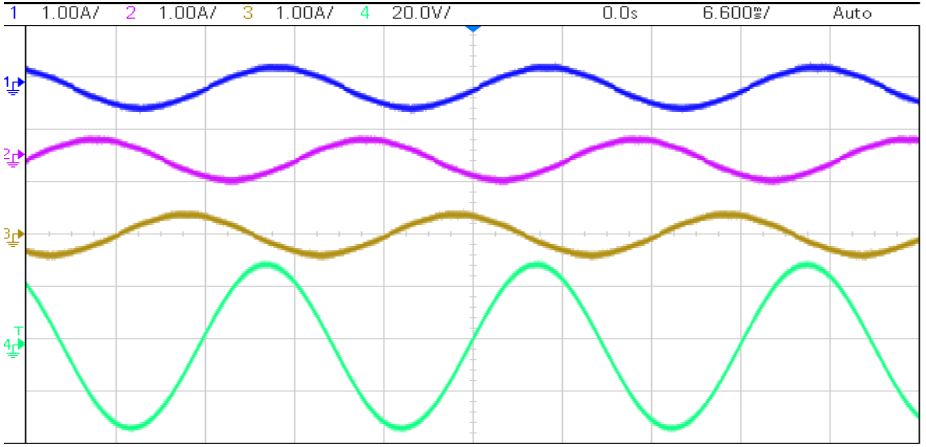


Input: 400Vac L-L, 50Hz
Output: 700V DC, 2.66Amps
Power: 1884W
iTHD: 3.5%
PF: 0.9972

400 VL-L Steady State Results (SDFM)

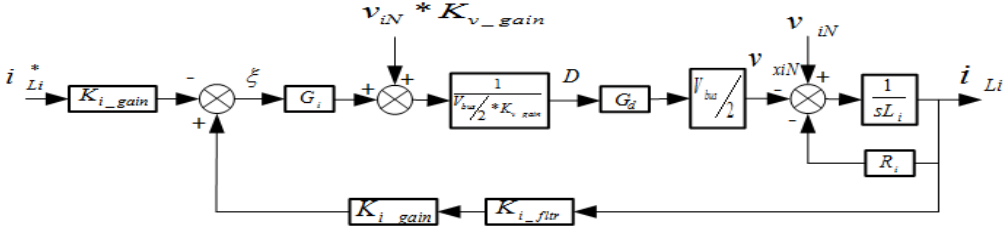


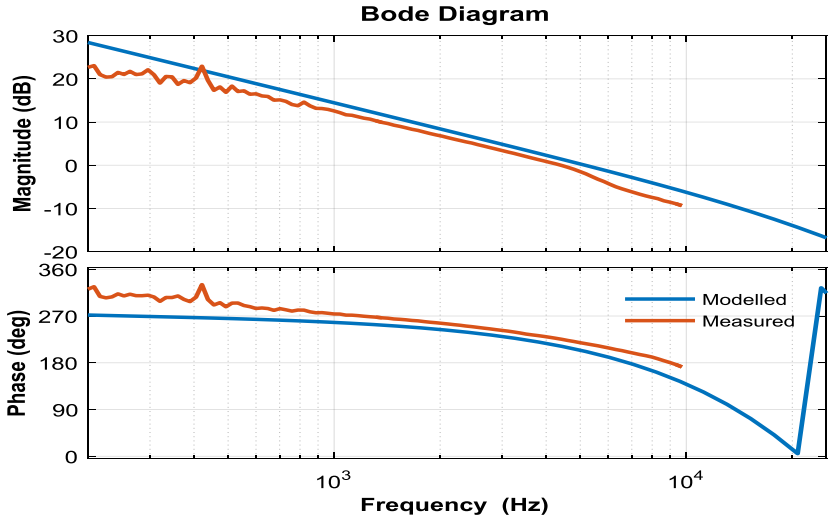
Input: 400Vac L-L, 50Hz
Output: 700V DC, 1.363Amps
Power: 960W
iTHD: 7%
PF: 0.9976

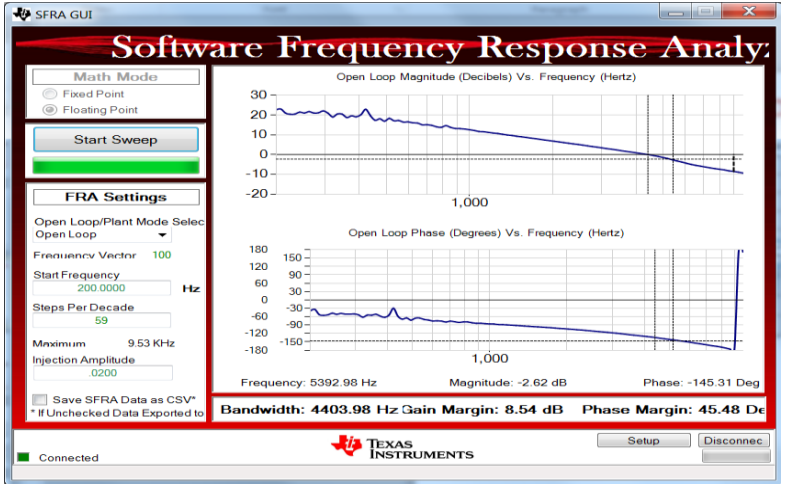


Input: 400Vac L-L, 50Hz
Output: 700V DC, 2.651Amps
Power: 1859W
iTHD: 0.85%
PF: 0.9991

Current Loop Tuning

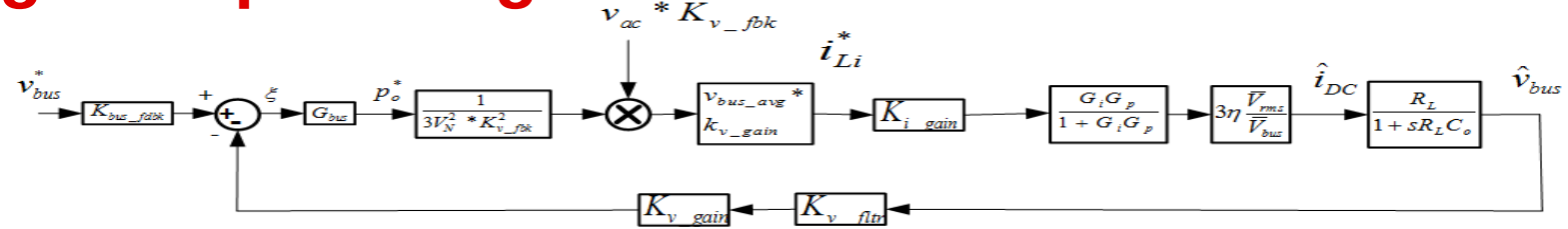


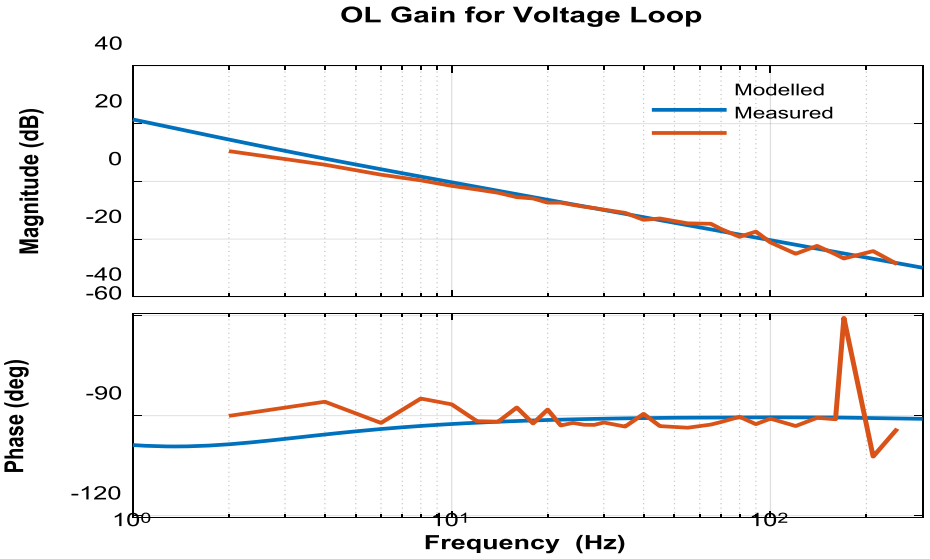


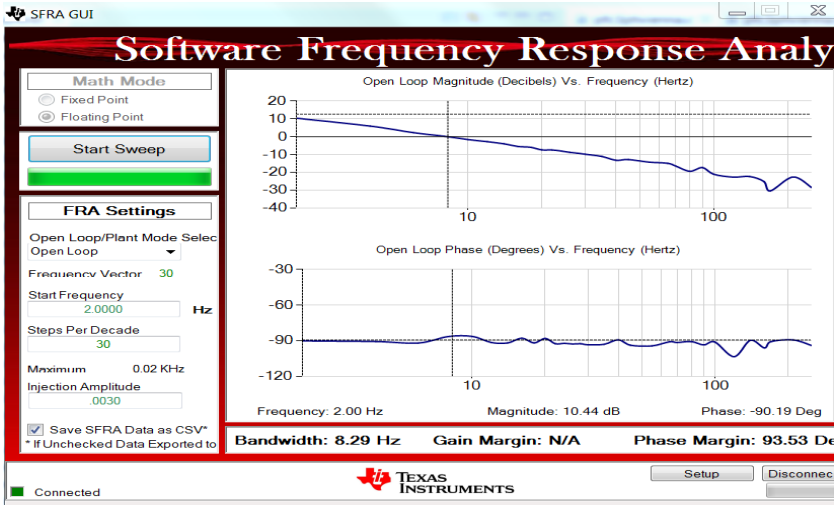


Input: 208Vac L-L, 60Hz, Output: 600V DC, 1.16Amps, Power: 697W , BUILD Level 2

Voltage Loop Tuning







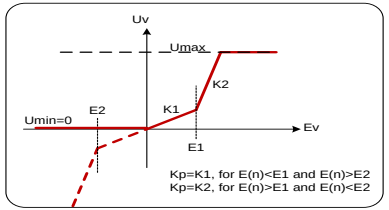
Input: 208Vac L-L, 60Hz, Output: 600V DC, 1.16Amps, Power: 697W , BUILD Level 3

Non Linear Control of Voltage Loop PFC

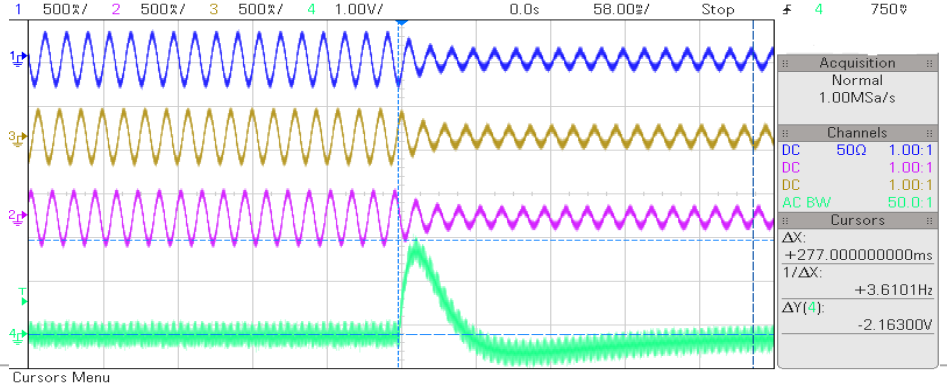
- Voltage loop requires low bandwidth for good power factor, however Dynamic response suffers hence a non-linear voltage control loop is used.

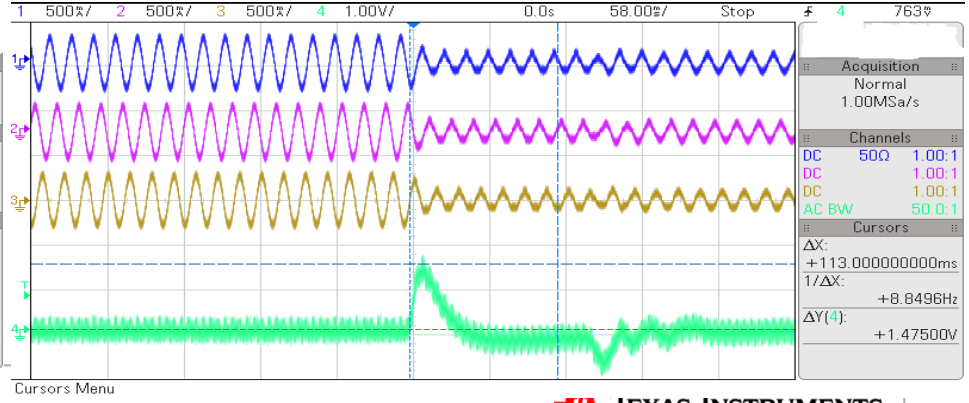
- Transient is detected by comparing voltage error, and coefficients are switched. This results in lower voltage overshoot.

$$G_v(z) = \frac{U_v}{E_v} = K_p + \frac{K_I}{1 - z^{-1}}$$



Snapshot below: Vin 208Vac, Vout 600V, Load Stepped from 245W to 745W, Overshoot reduced from 21.6V to 14.75V i.e. ***30%*** *improvement in Voltage Overshoot and Undershoot , because of non linear voltage compensator*





Software Structure

Project Structure

Settings File

"<solution>_settings.h"

Solution specific file

<solution>.h

<solutions>.c

Device specific files

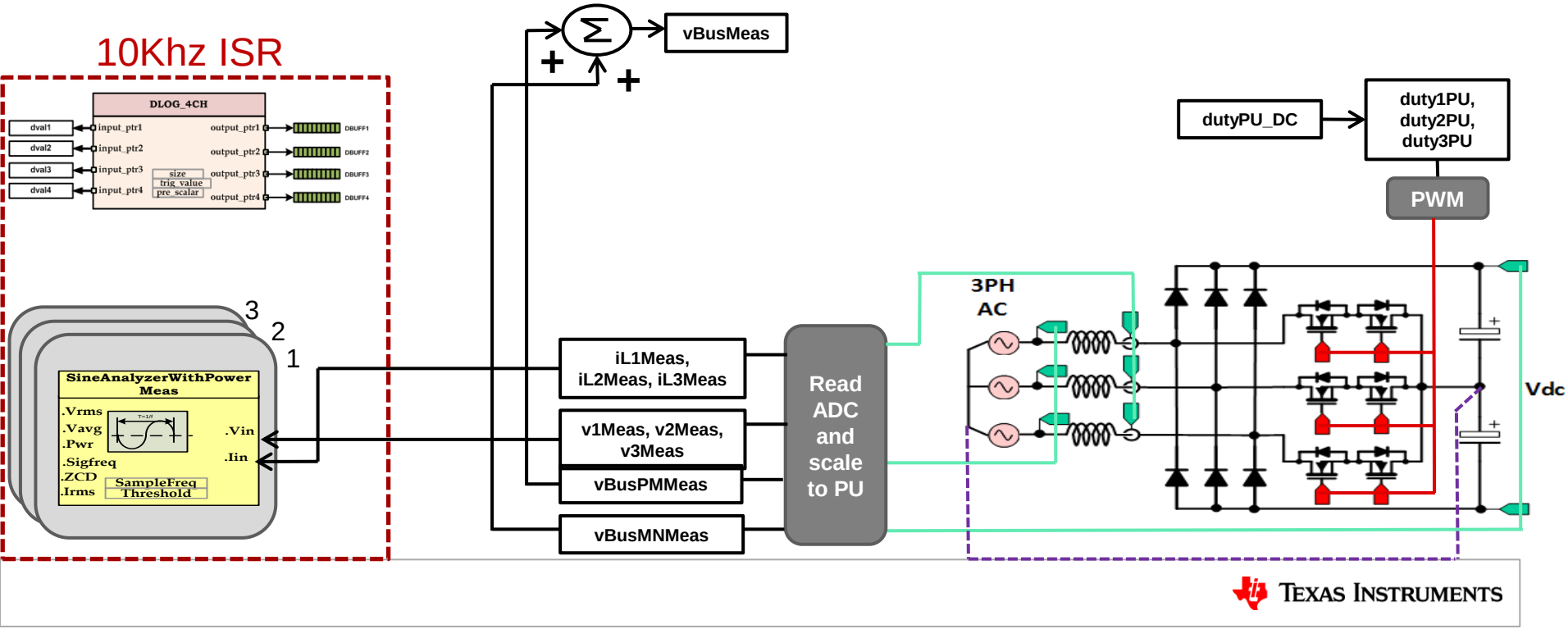
<solution>_board.h

<solution>_board.c

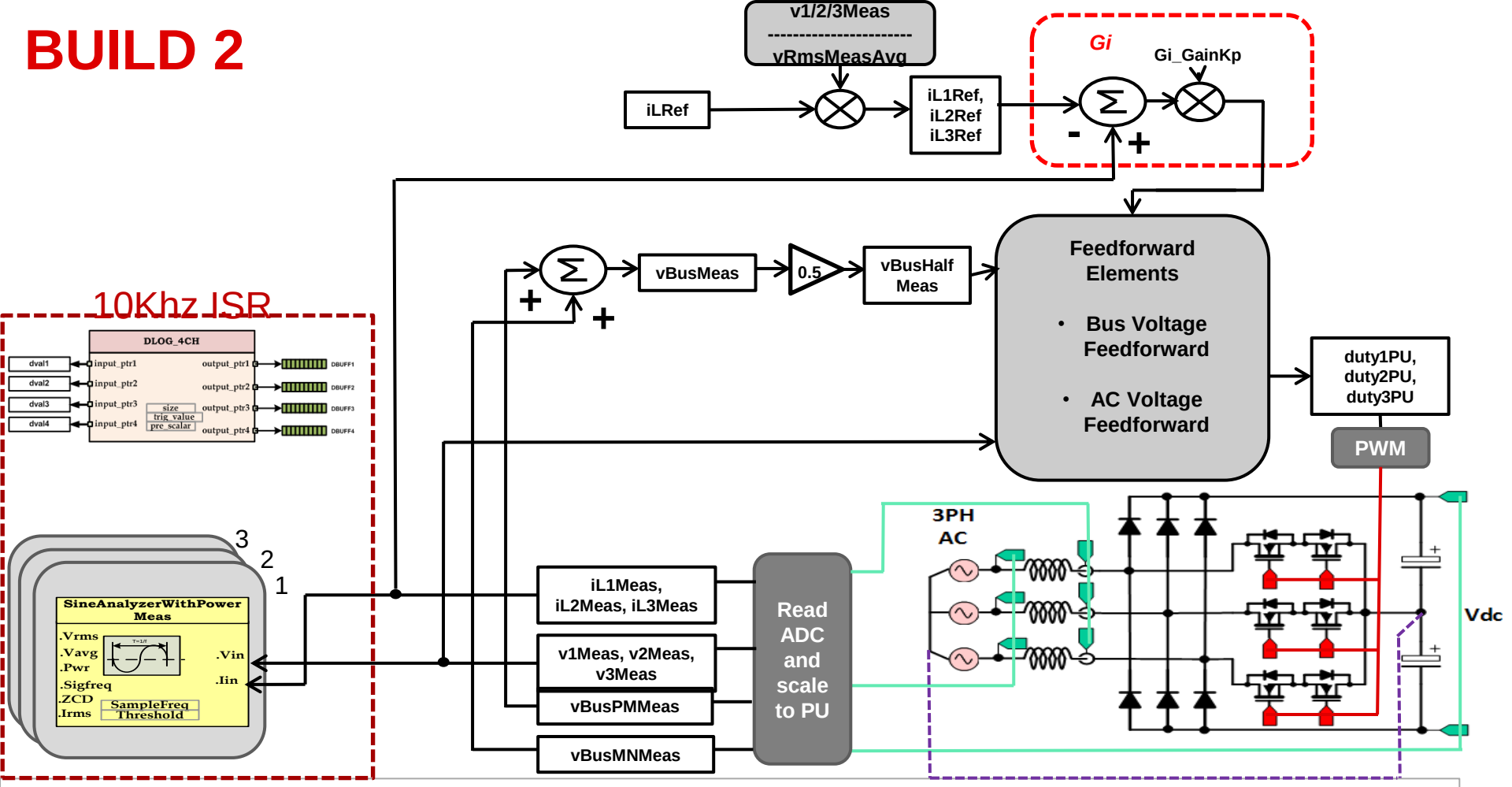
Incremental Build Levels to Simplify the Design of the System

INCR_BUILD 1: Open Loop Check
INCR_BUILD 2: Closed Current Loop
INCR_BUILD 3: Closed Voltage and Current Loop
INCR_BUILD 4: Closed Balance, Voltage and Current Loop

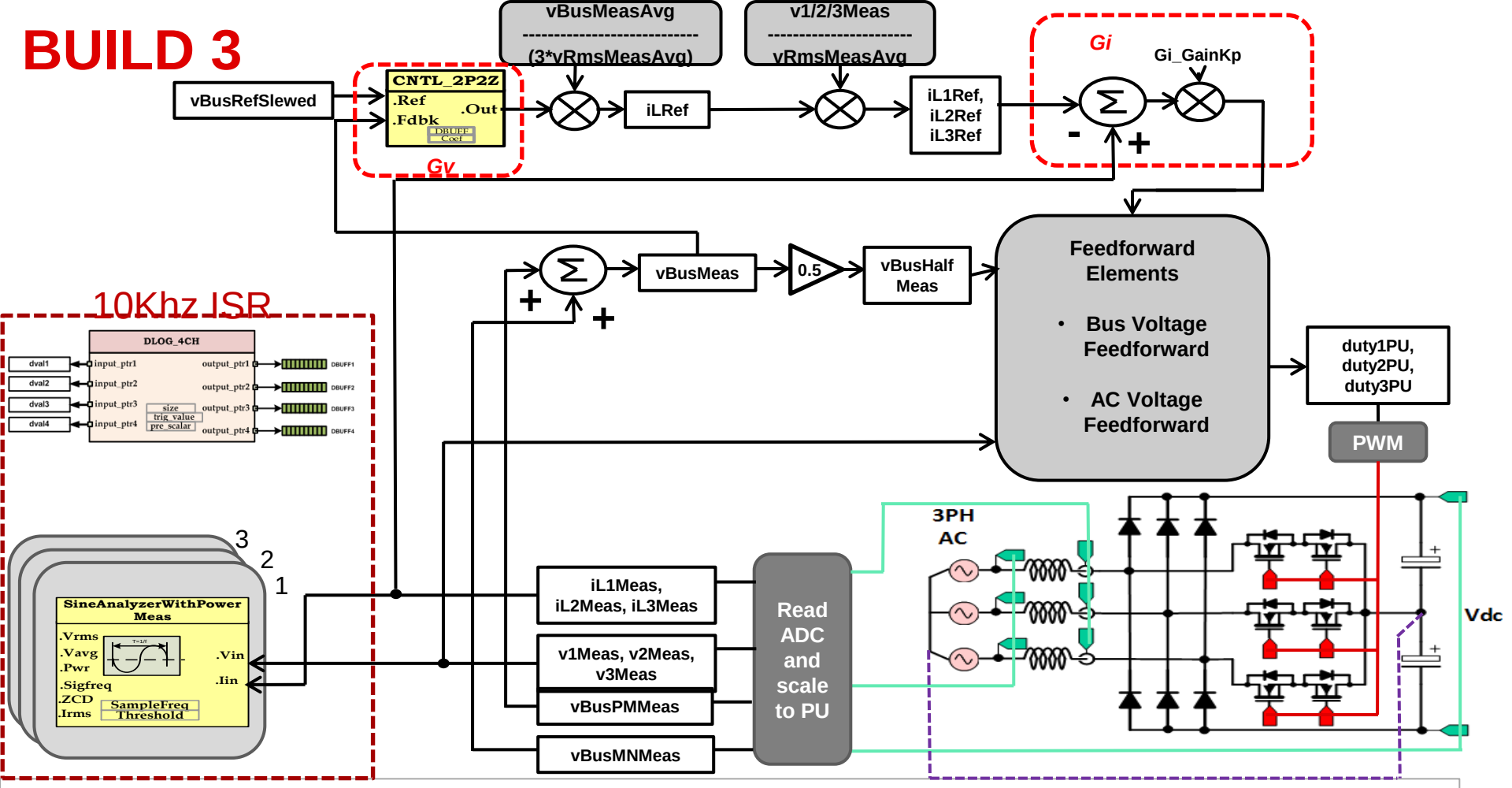
BUILD 1


10Khz ISR
DLOG_4CH
dval1
dval2
dval3
dval4
input_ptr1
input_ptr2
input_ptr3
input_ptr4
size
trig_value
pre_scalar
output_ptr1
output_ptr2
output_ptr3
output_ptr4
DBUFF1
DBUFF2
DBUFF3
DBUFF4
3
2
1
SineAnalyzerWithPower Meas
.Vrms
.Vavg
.Pwr
.Sigfreq
.ZCD
.Irms
.Vin
.Iin
SampleFreq
Threshold
vBusMeas
iL1Meas, iL2Meas, iL3Meas
v1Meas, v2Meas, v3Meas
vBusPMMeas
vBusMNMeas
Read ADC and scale to PU
dutyPU_DC
duty1PU, duty2PU, duty3PU
PWM
3PH AC
Vdc

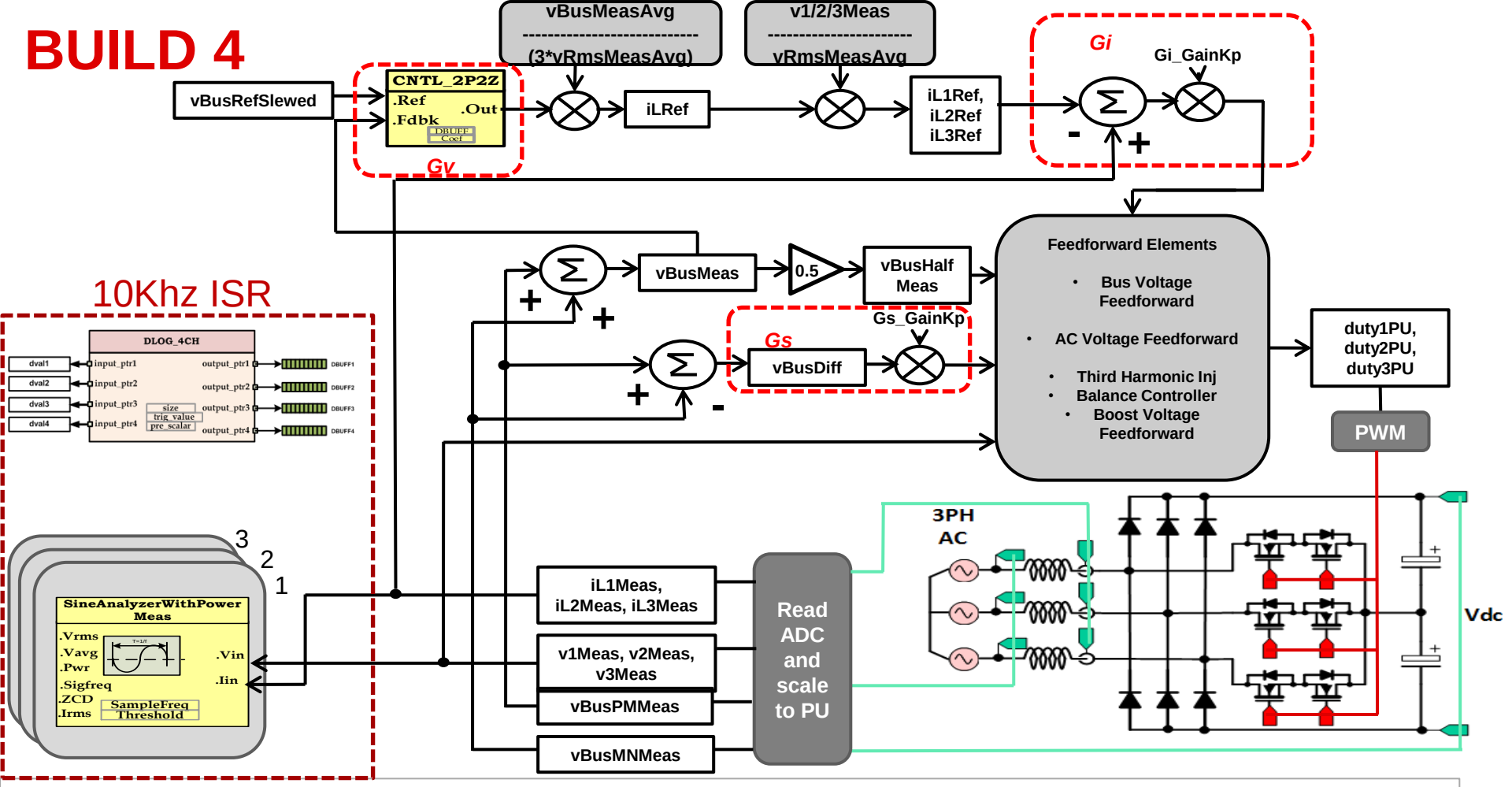
BUILD 2


v1/2/3Meas
vRmsMeasAvg
iLRef
iL1Ref,
iL2Ref
iL3Ref
Gi
Gi_GainKp
-
+
vBusMeas
0.5
vBusHalf
Meas
Feedforward
Elements
• Bus Voltage
Feedforward
• AC Voltage
Feedforward
duty1PU,
duty2PU,
duty3PU
PWM
10Khz ISR
DLOG_4CH
dval1
dval2
dval3
dval4
input_ptr1
input_ptr2
input_ptr3
input_ptr4
size
trig_value
pre_scalar
output_ptr1
output_ptr2
output_ptr3
output_ptr4
DBUFF1
DBUFF2
DBUFF3
DBUFF4
3
2
1
SineAnalyzerWithPower
Meas
.Vrms
.Vavg
.Pwr
.Sigfreq
.ZCD
.Irms
SampleFreq
Threshold
.Vin
.Iin
iL1Meas,
iL2Meas, iL3Meas
v1Meas, v2Meas,
v3Meas
vBusPMMeas
vBusMNMeas
Read
ADC
and
scale
to PU
3PH
AC
Vdc

BUILD 3


vBusMeasAvg
(3*vRmsMeasAvg)
v1/2/3Meas
vRmsMeasAvg
Gi
Gi_GainKp
vBusRefSlewed
CNTL_2P2Z
.Ref
.Fdbk
.Out
DBUFF Coef
Gv
iLRef
iL1Ref,
iL2Ref
iL3Ref
vBusMeas
0.5
vBusHalf Meas
Feedforward Elements
• Bus Voltage Feedforward
• AC Voltage Feedforward
duty1PU,
duty2PU,
duty3PU
PWM
10Khz ISR
DLOG_4CH
dval1
dval2
dval3
dval4
input_ptr1
input_ptr2
input_ptr3
input_ptr4
output_ptr1
output_ptr2
output_ptr3
output_ptr4
DBUFF1
DBUFF2
DBUFF3
DBUFF4
size
trig_value
pre_scalar
3
2
1
SineAnalyzerWithPower Meas
.Vrms
.Vavg
.Pwr
.Sigfreq
.ZCD
.Irms
.Vin
.Iin
SampleFreq
Threshold
iL1Meas,
iL2Meas, iL3Meas
v1Meas, v2Meas,
v3Meas
vBusPMMeas
vBusMNMeas
Read ADC and scale to PU
3PH AC
Vdc

BUILD 4


vBusMeasAvg
(3*vRmsMeasAvg)
v1/2/3Meas
vRmsMeasAvg
vBusRefSlewed
CNTL_2P2Z
.Ref
.Fdbk
.Out
DBUFF Coef
Gv
iLRef
iL1Ref,
iL2Ref
iL3Ref
Gi
Gi_GainKp
vBusMeas
0.5
vBusHalf Meas
Gs
Gs_GainKp
vBusDiff
Feedforward Elements
Bus Voltage Feedforward
AC Voltage Feedforward
Third Harmonic Inj
Balance Controller
Boost Voltage Feedforward
duty1PU,
duty2PU,
duty3PU
PWM
10Khz ISR
DLOG_4CH
dval1
dval2
dval3
dval4
input_ptr1
input_ptr2
input_ptr3
input_ptr4
output_ptr1
output_ptr2
output_ptr3
output_ptr4
size
trig_value
pre_scalar
DBUFF1
DBUFF2
DBUFF3
DBUFF4
3
2
1
SineAnalyzerWithPower Meas
.Vrms
.Vavg
.Pwr
.Sigfreq
.ZCD
.Irms
.Vin
.Iin
SampleFreq
Threshold
iL1Meas,
iL2Meas, iL3Meas
v1Meas, v2Meas,
v3Meas
vBusPMMeas
vBusMNMeas
Read ADC and scale to PU
3PH AC
Vdc

References

- Digital Current Controller for a 1 MHz, 10 kW Three-Phase VIENNA Rectifier, Michael Hartmann, Power Electron. Syst. Lab., ETH Zurich, Zurich, Switzerland , Simon D. Round, Hans Ertl, Johann W. Kolar, IEEE Transaction on Power Electronics, Volume 24, Issue 11, Pg. 2496-2508

Links

- TIDM-1000 – Vienna Rectifier Based Three Phase PFC Reference Design
- TMS320F28377D – Dual Core 32-bit Real Time Controller
- controlSUITE™ – Software and Development Tools for C2000™ MCUs
- powerSUITE – SFRA User Guide and documentation(included in controlSUITE™ download)
- Code Composer Studio for C2000™ – IDE for C2000™ MCUs