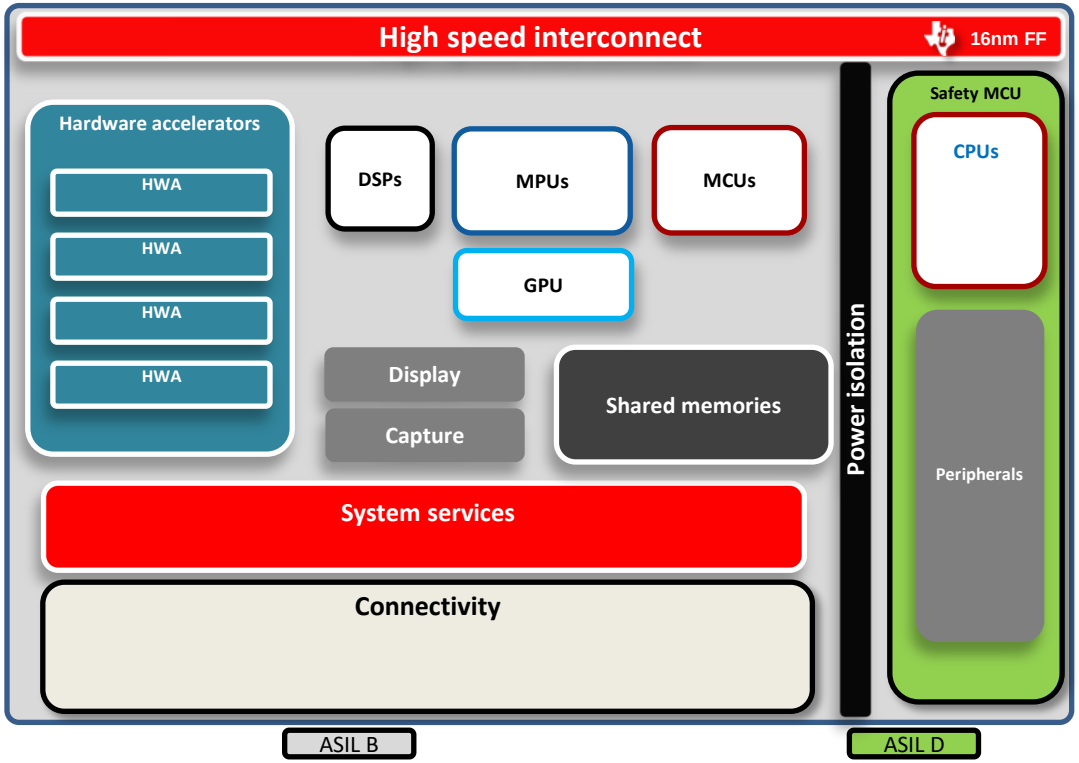
Jacinto™ 7 processors: Overview of key SoC subsystems and features for automotive applications

Overview agenda

- Key features and benefits
- Heterogeneous processing cores
- Application-specific hardware accelerators
- Device management architecture
- Memory architecture & data movement
- Safety and isolation features
- Virtualization features
- Security features
- Power management features
- Network connectivity
- Flash and storage
- Serial connectivity



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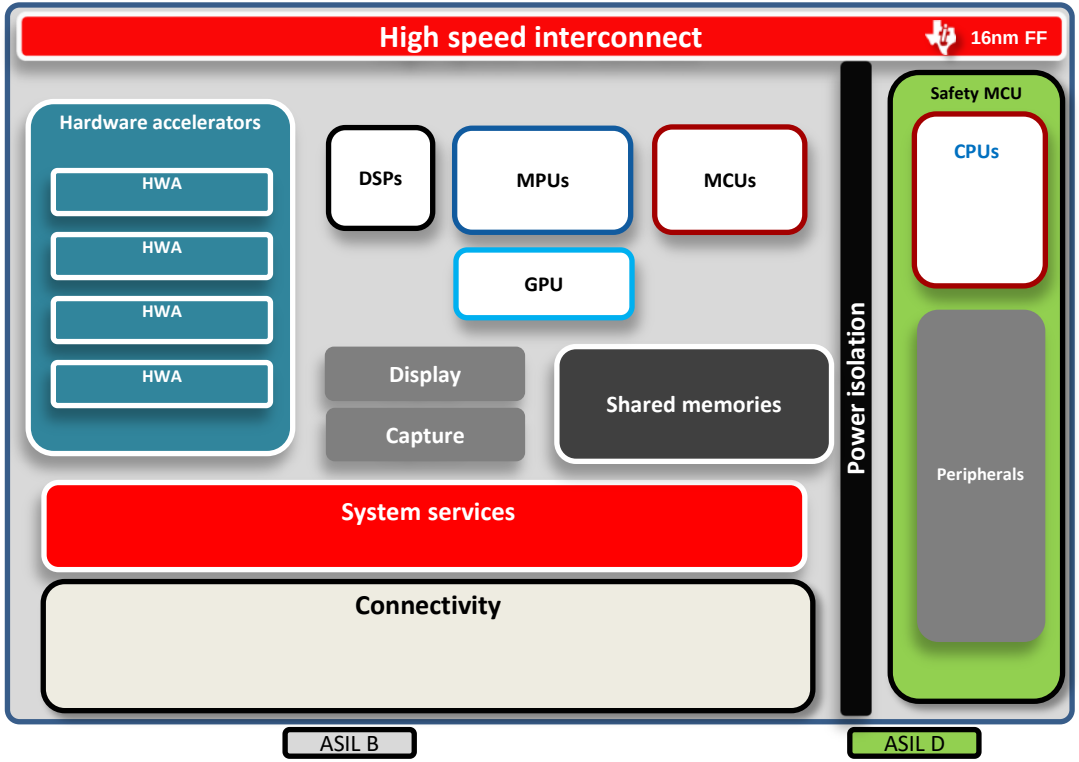
Key features and benefits

- High-performance, highly-integrated, peripheral-rich processors enable key automotive applications.
- Mature, high-quality 16FF process technology provides full automotive support.
- Key differentiated hardware acceleration for networking, imaging and deep learning.
- Bottom-up architecture focusing on coherent resource sharing while maintaining isolation for security and safety.
- Integrated Safety Micro Controller Unit (MCU) for reduced system cost facilitating mixed safety applications and managing power.
- Scalable hardware and software platform with high commonality is provided across the processor family.



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Heterogeneous processing cores

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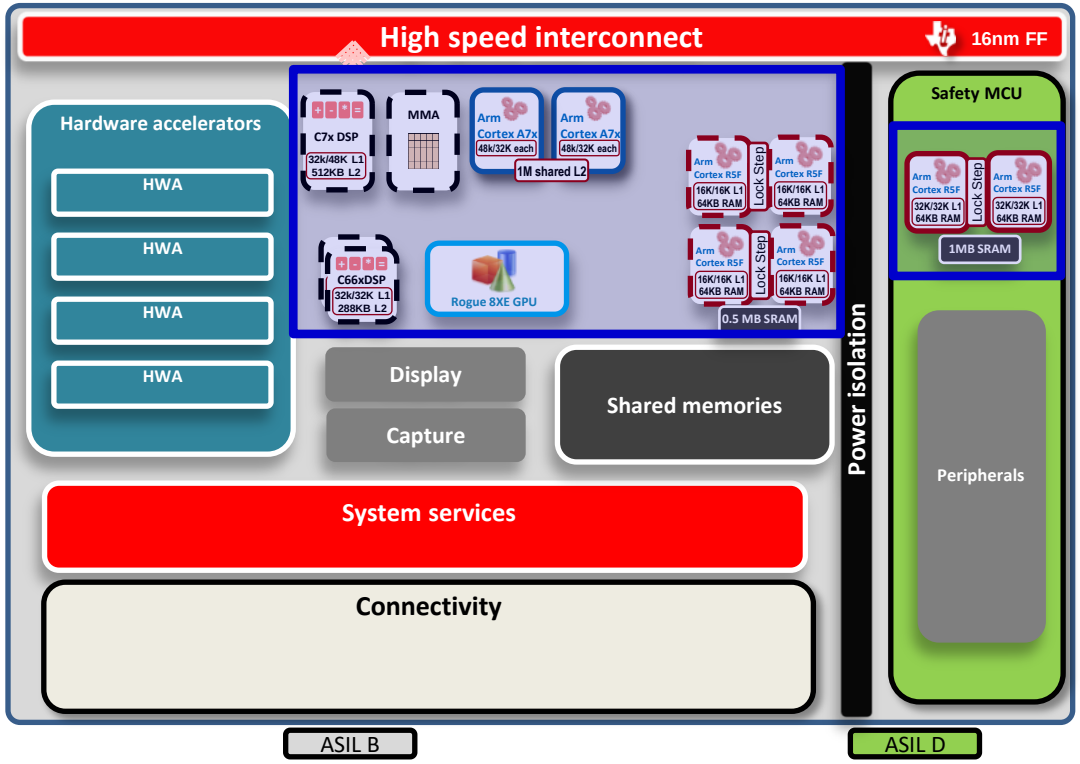

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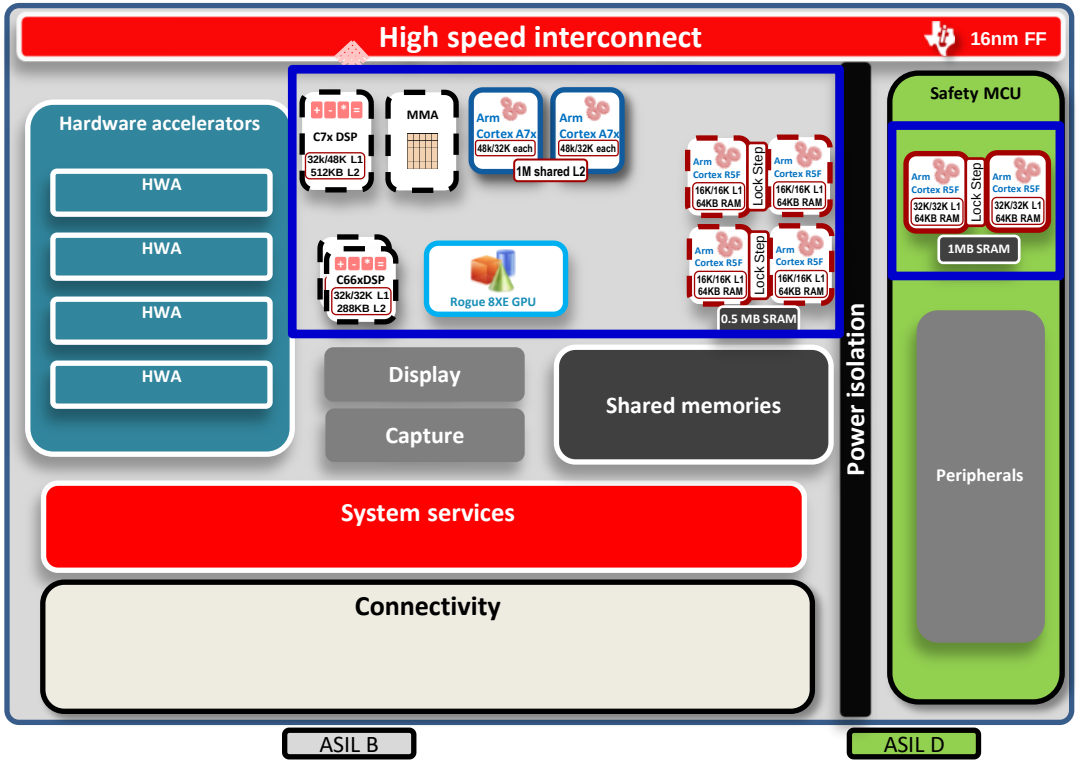
Heterogeneous processing cores

- Microprocessing Unit (MPU):
  - Arm® Cortex®-A72 dual SMP up to 2 GHz
    - Cache coherence with system cache
- Microcontroller Unit (MCU):
  - Arm® Cortex®-R5F dual clusters:
    - Lock-step or split mode up to 1 GHz
    - 2x clusters in main 1x in Safety MCU
- Digital Signal Processors (DSP):
  - TI C71x true 64 bit DSP up to 1 GHz
    - 4-30x performance of previous gen
    - Dual-path CPU with both 64-bit scalar and 512-bit vector operations
    - Math Multiply Accelerator (MMA) for deep learning
    - Cache coherence with system cache
  - TI C66x DSP up to 1.3 GHz
- Graphics Processing Unit (GPU):
  - PowerVR 8XE series GE8430 from Imagination Technologies



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Application-specific hardware accelerators

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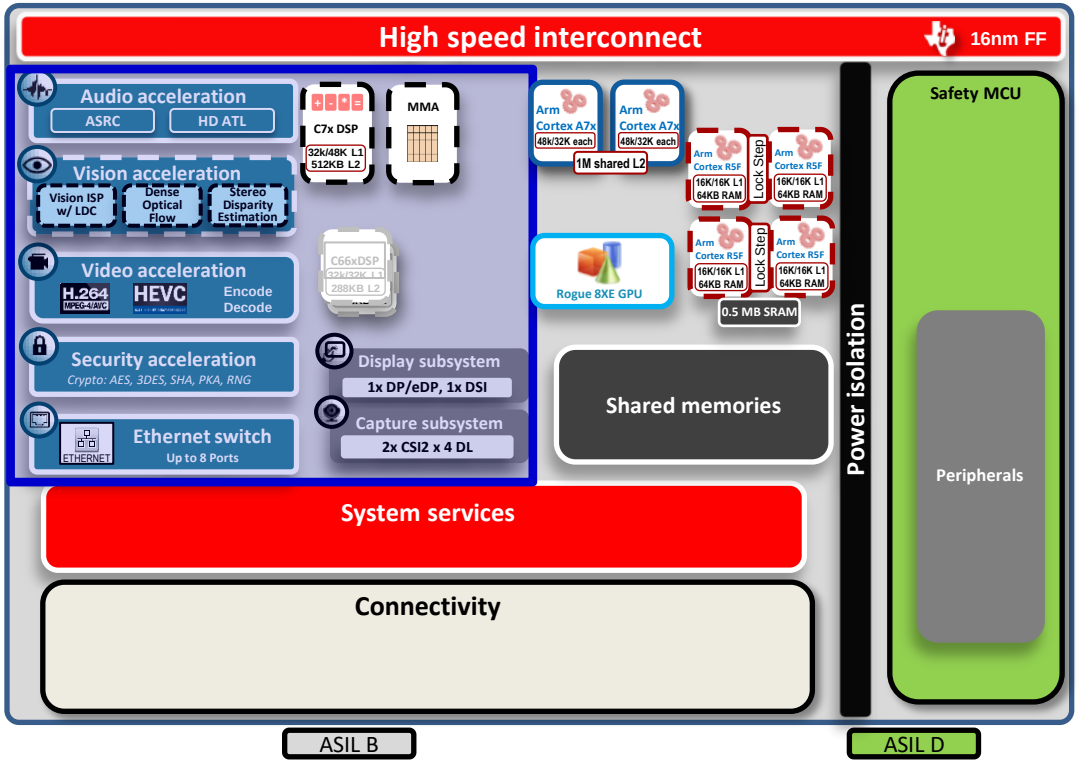

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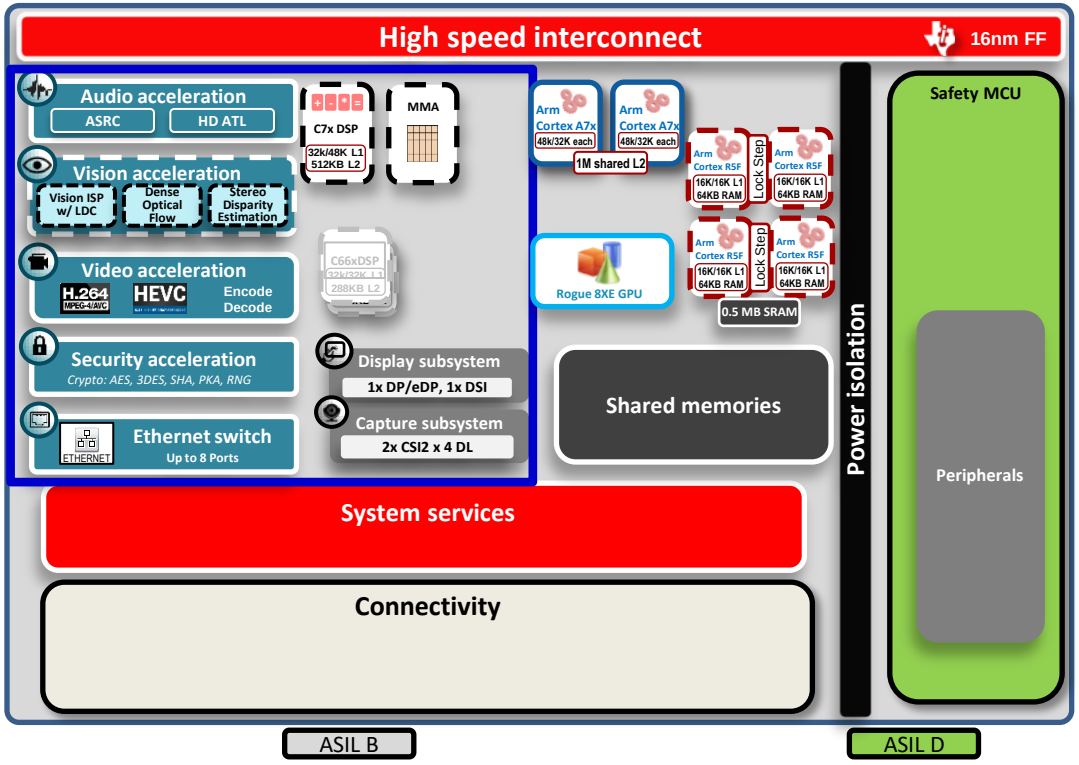
Application-specific hardware accelerators

- Capture and vision acceleration:
  - Vision Pre-Processing Accelerator (VPAC)
    - 7th generation TI imaging processor
  - Depth and Motion Perception Accelerator (DMPAC)
    - High-resolution stereo depth engine
    - Dense optical flow
  - Pixel-processing tuned to improve effective CNN-based deep learning performance
- Deep learning acceleration:
  - C71x DSP with MMA accelerator
  - Optimized memory system to minimize DDR bandwidth and device count
- Display subsystem:
  - Safety isolation and freeze frame detect
- Video acceleration:
  - Multi-format decode up to 4k60 and encode up to 1080p60



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Device management architecture

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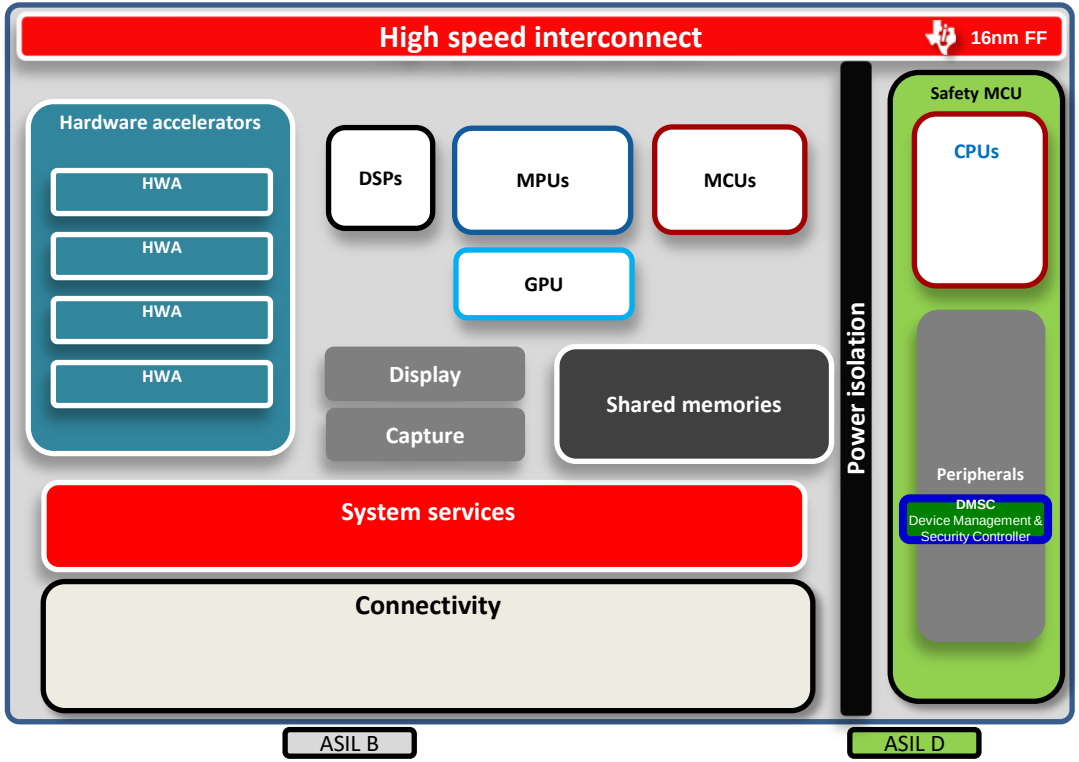

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Memory architecture and data movement

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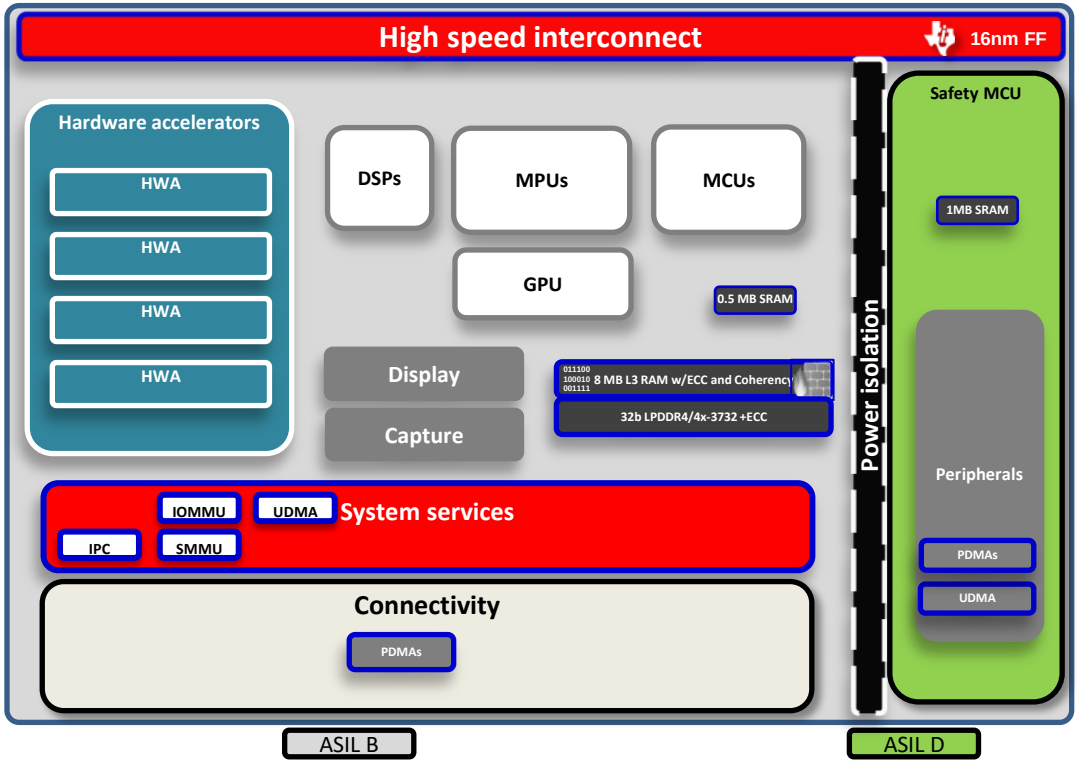

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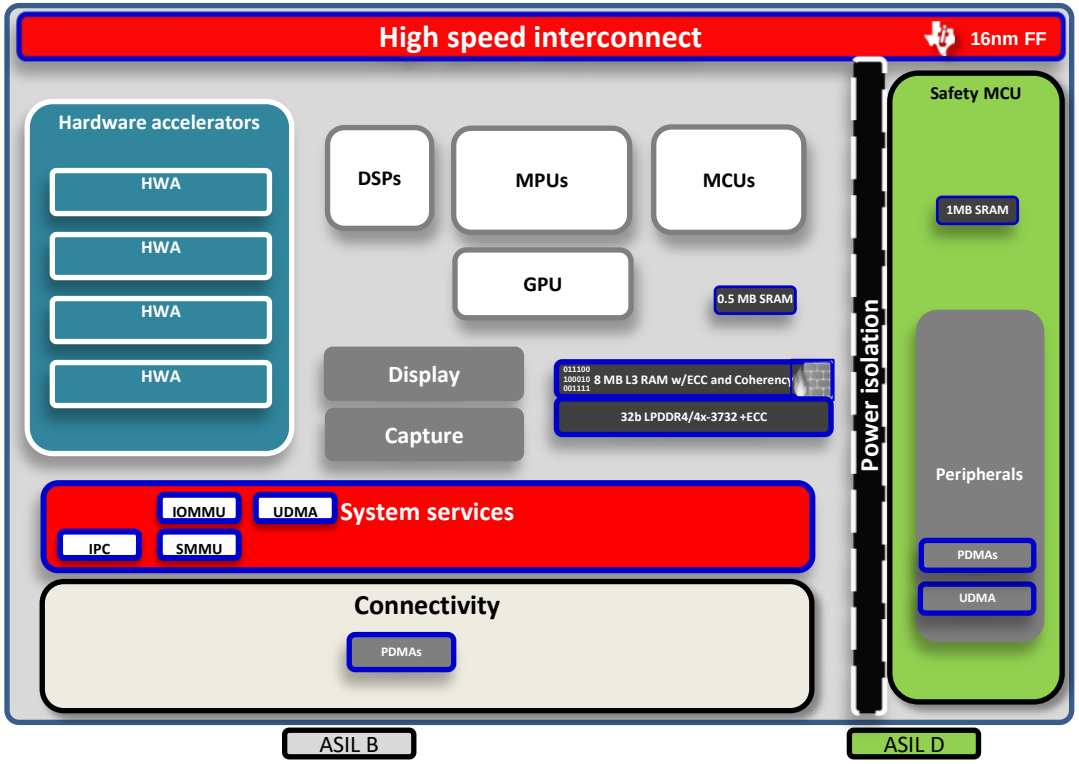
Memory architecture and data movement

- Optimized 3-level memory system:
  - Level 1 and 2 caches on CPUs
  - Up to 8 Mbyte shared L3 cache with coherence provided by Multi-core Shared Memory Controller (MSMC)
  - LPDDR4/4X up to DDR3733 plus inline ECC with context cache
- Multiple DMA for memory movement:
  - Data Routing Unit (DRU) for deep learning paging
  - Unified DMA (uDMA) in both Main and Safety MCU domains
- Efficient SoC bus fabric:
  - Traffic prioritization and quality of service (QoS) features
  - Virtualization support accessible to most cores and peripherals



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Safety and isolation features

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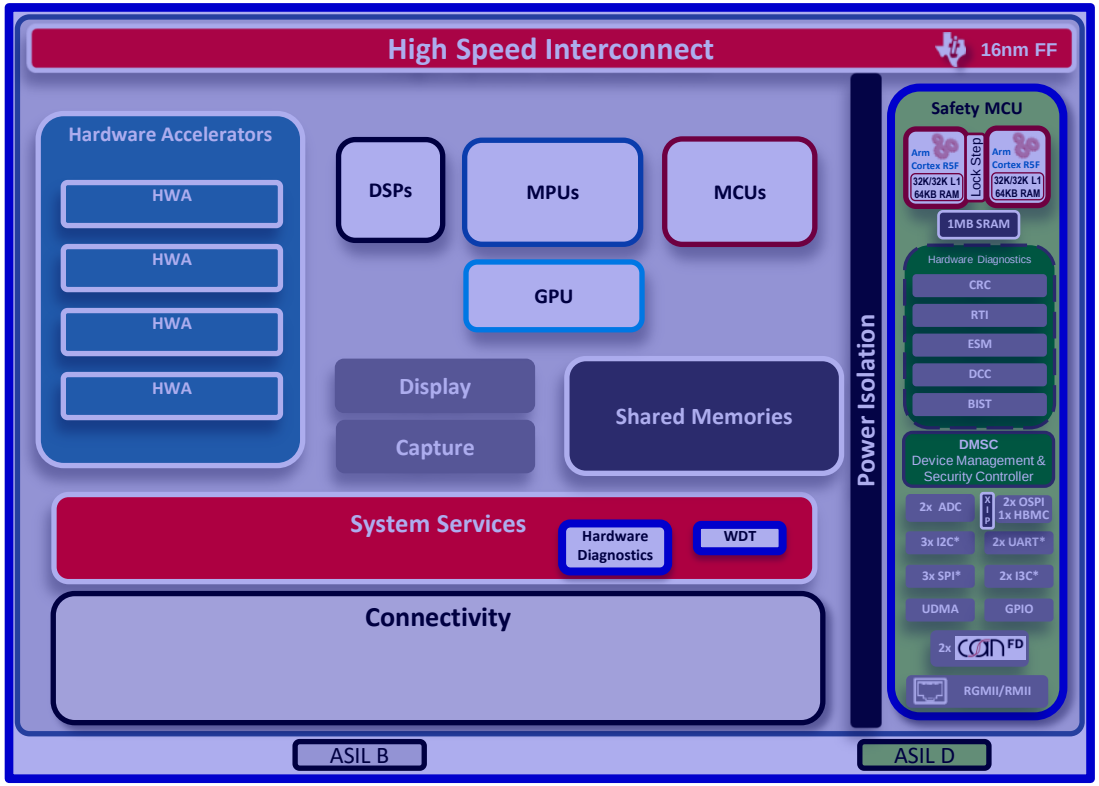

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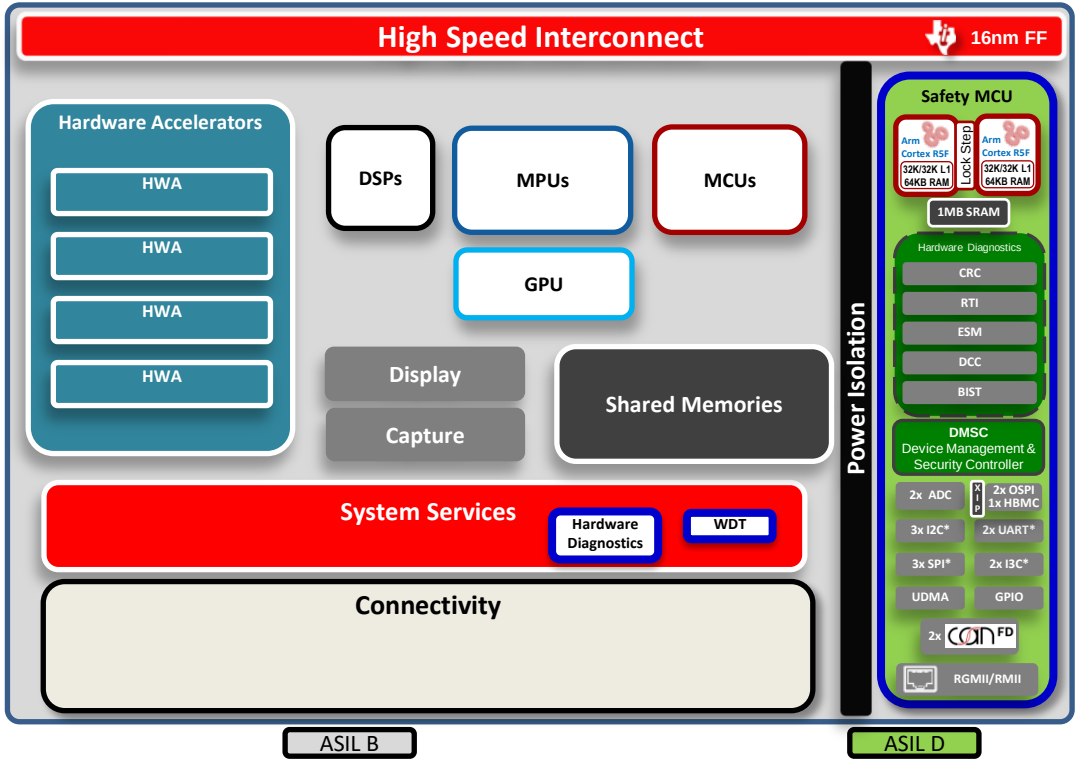
Safety and isolation features

- Safety MCU:
  - Targeting ASIL-D systems
  - Voltage, clock and reset isolated with lock-step R5, DMA and full peripheral set
  - Safety timeout gaskets to safety access main domain
  - Safe and secure execute in place (XIP) from external flash
- Diagnostics support (both domains):
  - Voltage and temperature monitors
  - Flexible clock monitoring
  - Dedicated CRC-calculating DMAs
  - Built-in self-test (BIST) and power-on self-test (POST)
  - ADC for external monitoring
- Other safety features:
  - ECC on all critical memories
  - Windowed watchdog timers on all cores



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Virtualization features

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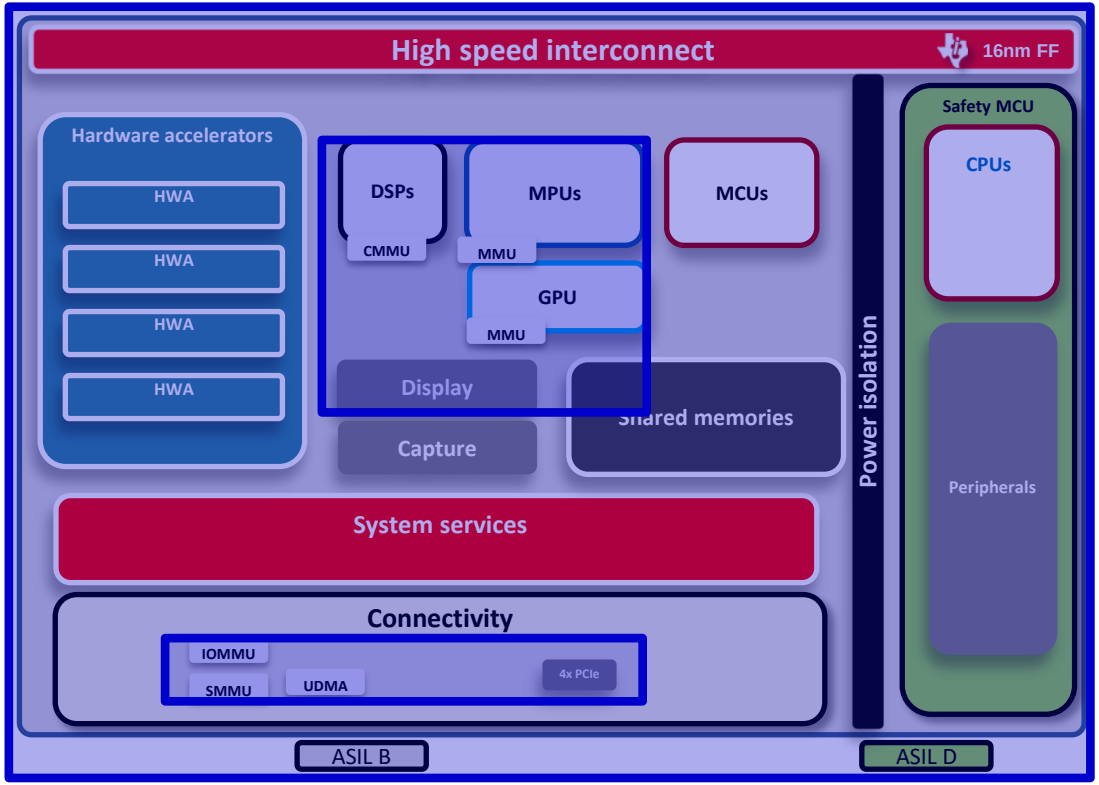

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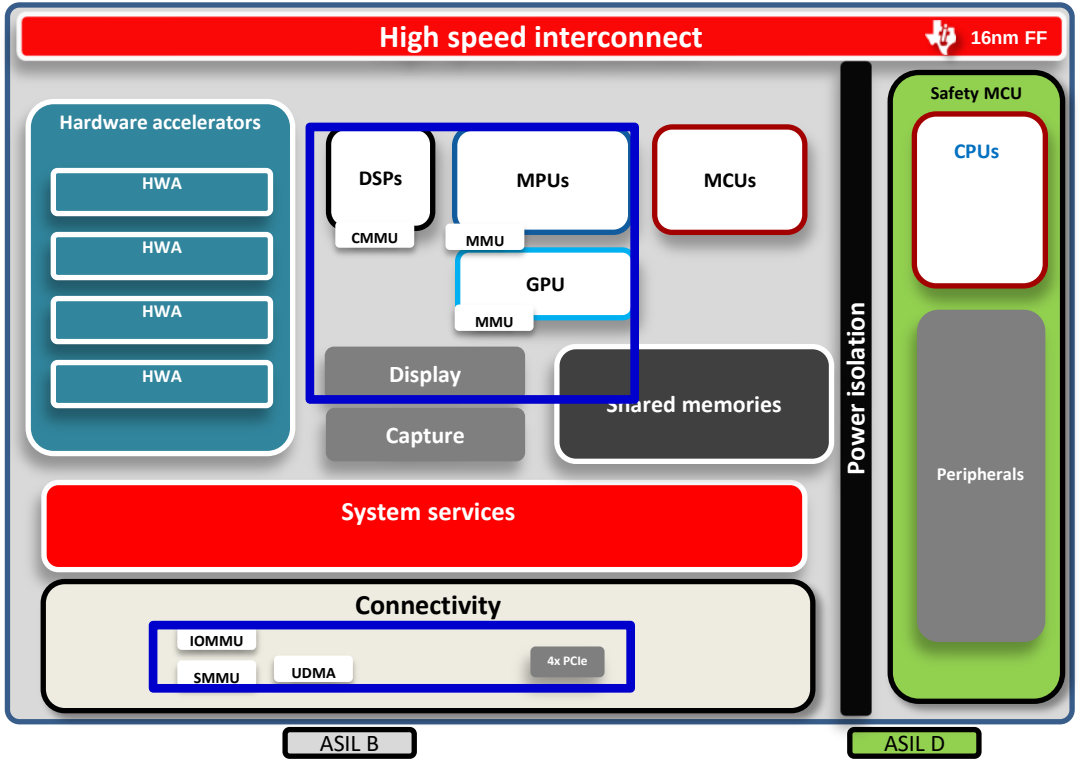
Virtualization features

- Memory Management Unit (MMU):
  - CPU 2-stage MMUs for primary cores
- IO-MMU:
  - System MMU (sMMU):
    - Standard ARMv3 SMMU 2-stage system MMU
  - TI IO-MMU:
    - Peripheral Virtualization Unit (PVU)
    - Page-based Address Translator (PAT)
    - Provides 2 stage of “real-time” IOMMU
- Peripheral support:
  - PCIe Single-Root I/O Virtualization (SRIOV)
  - DSS-virtualized ownership of pipe and overlay management
  - GPU virtual resource manager
  - Arm Generic Interrupt Controller (GIC-500)



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Security management features

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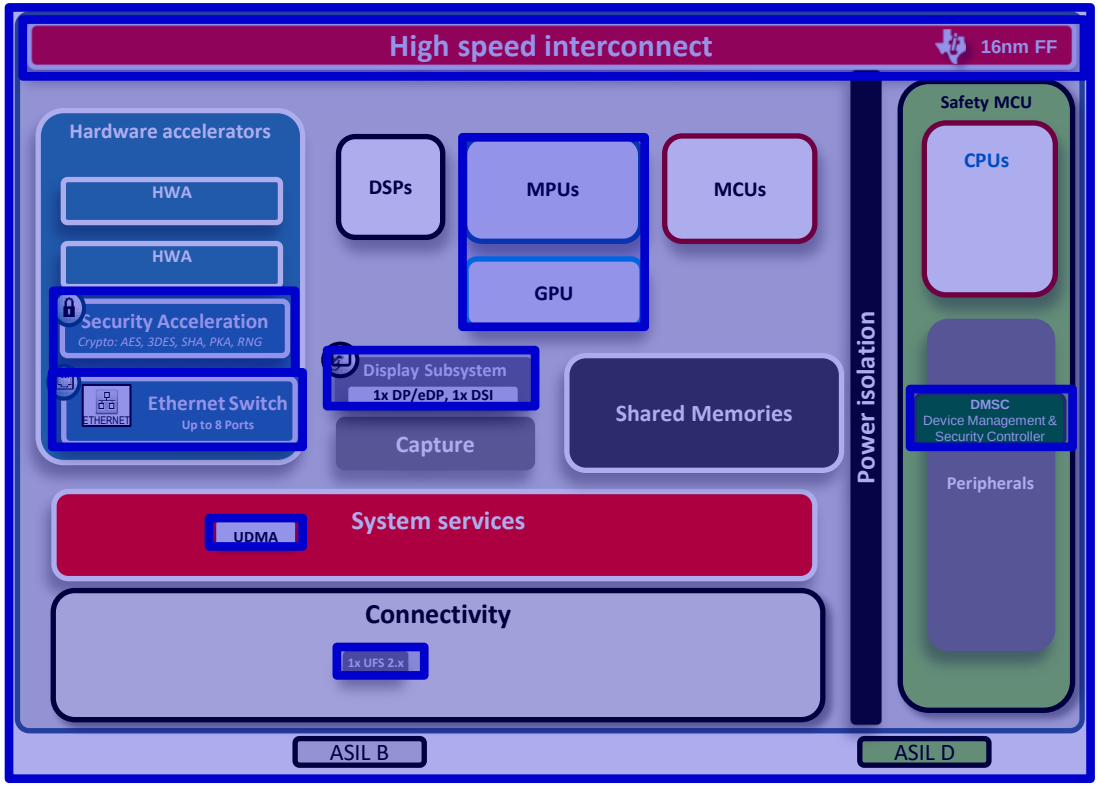

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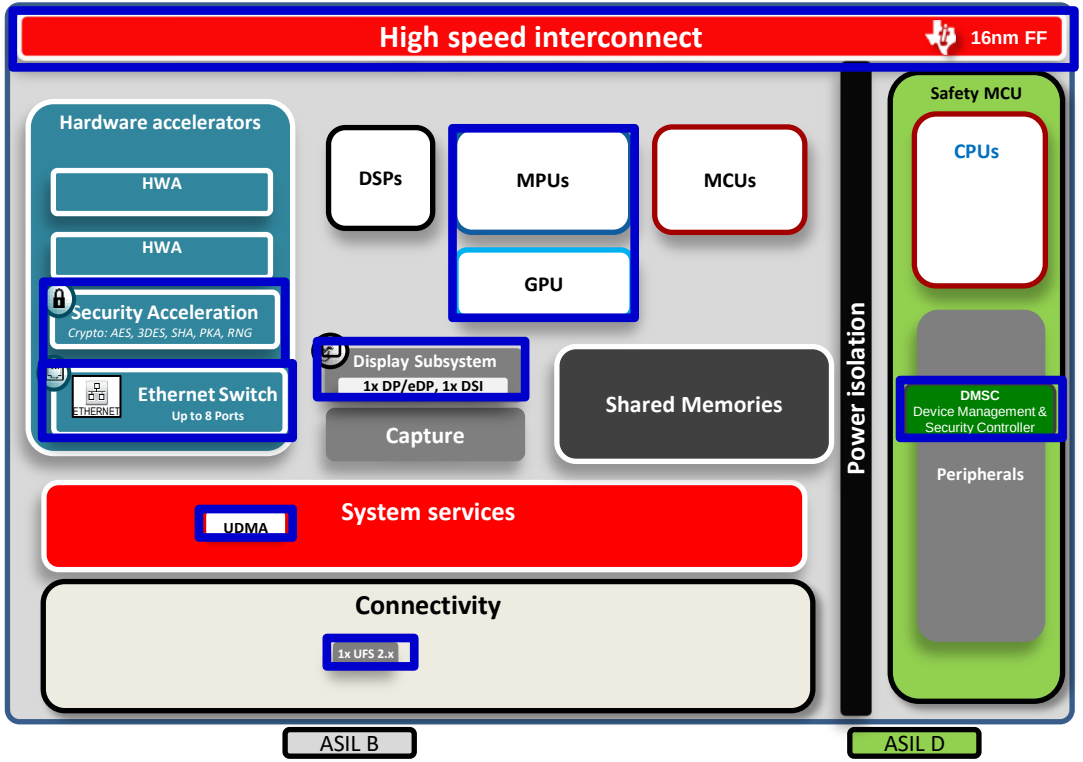
Security management features

- Secure boot and runtime security:
  - Customer-securable device
  - Secure execution from flash (on-the-fly authentication)
- DMSC (Arm Cortex-M3) security manager
- Full endpoint protection via firewalls
- Cryptography acceleration:
  - Both Main and Safety MCU domains
  - Multiple algorithms implemented in hardware: SHA2, AES, etc.
- Embedded IP features:
  - GPU, DSS security isolation
  - Display, UFS embedded crypto
- ARM Trustzone for trusted execution environment on A72



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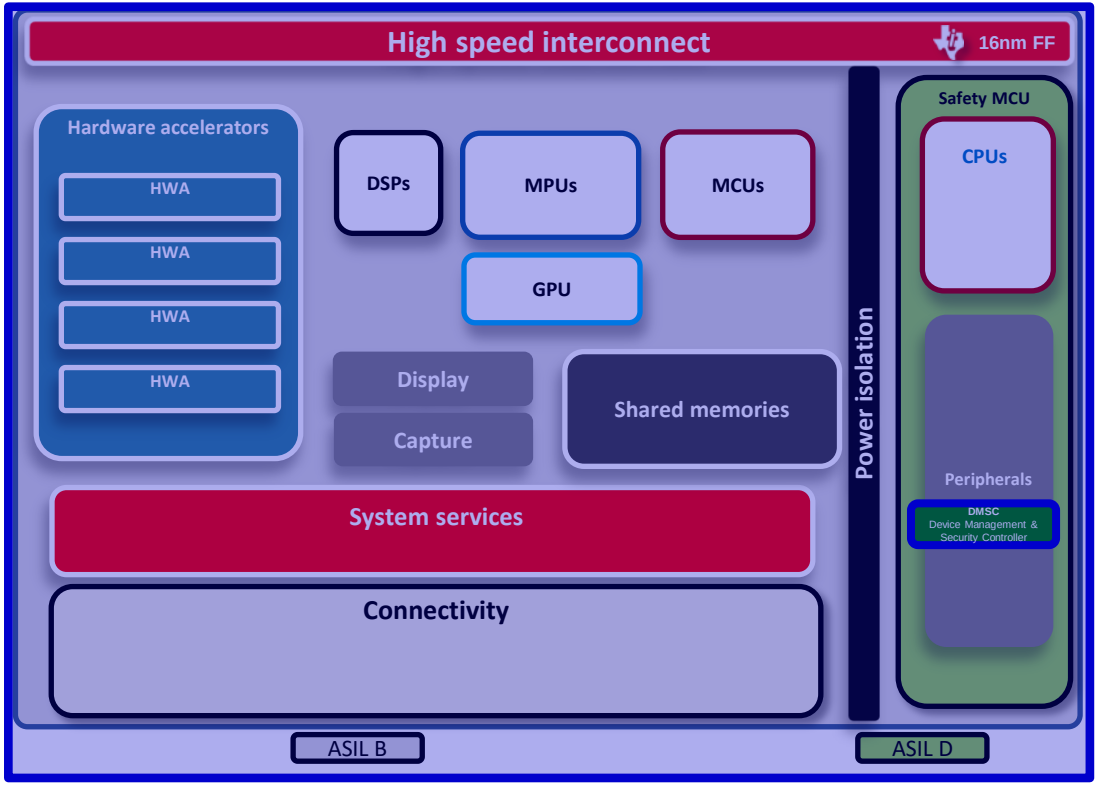

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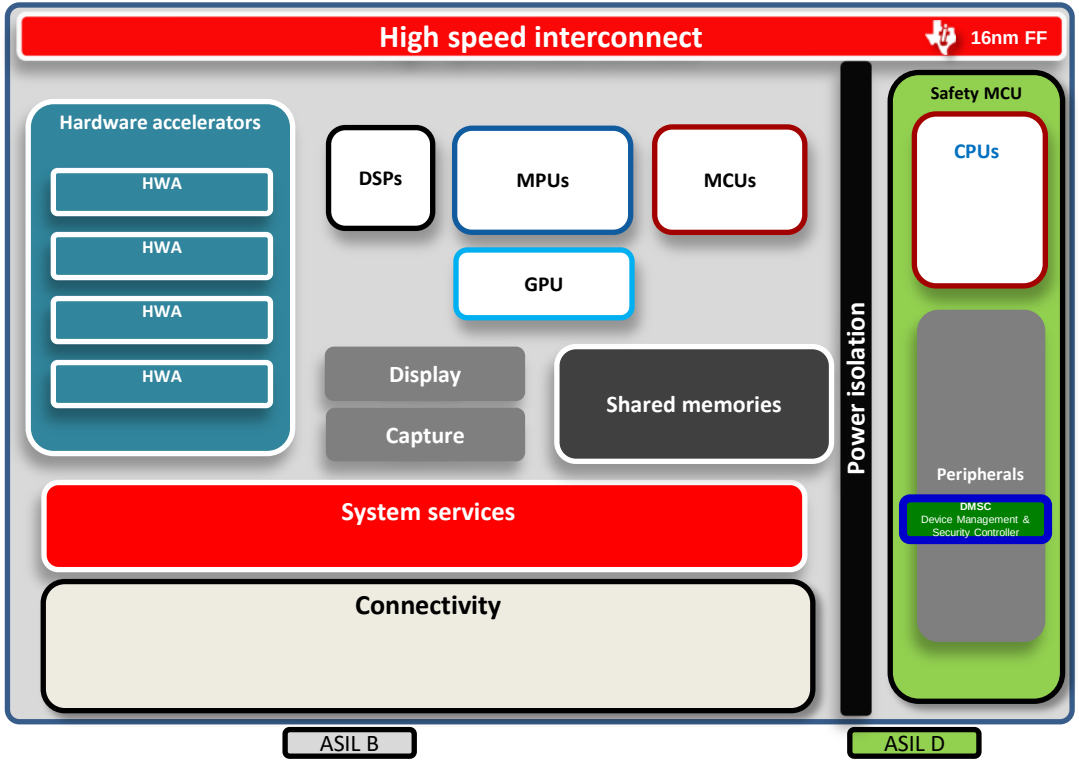
Power management features

- Voltage domains (AVS, power modes):
  - Adaptive voltage scaling for main CPUs
  - Shut off Main domain during MCU-only mode
- Power domains:
  - Internally-switched domains on major core/IP
- Clocking control:
  - Multiple PLL for fine-grain clock control
  - Dynamic Frequency Scaling (DFS)
  - Clock gating (SW and automatic)
- Power management IP features:
  - Power-OK (POK) voltage detectors
  - Power Glitch Detectors (PGD)
  - Temperature sensors
  - Thermal diode
  - DDR suspend to RAM



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Network connectivity

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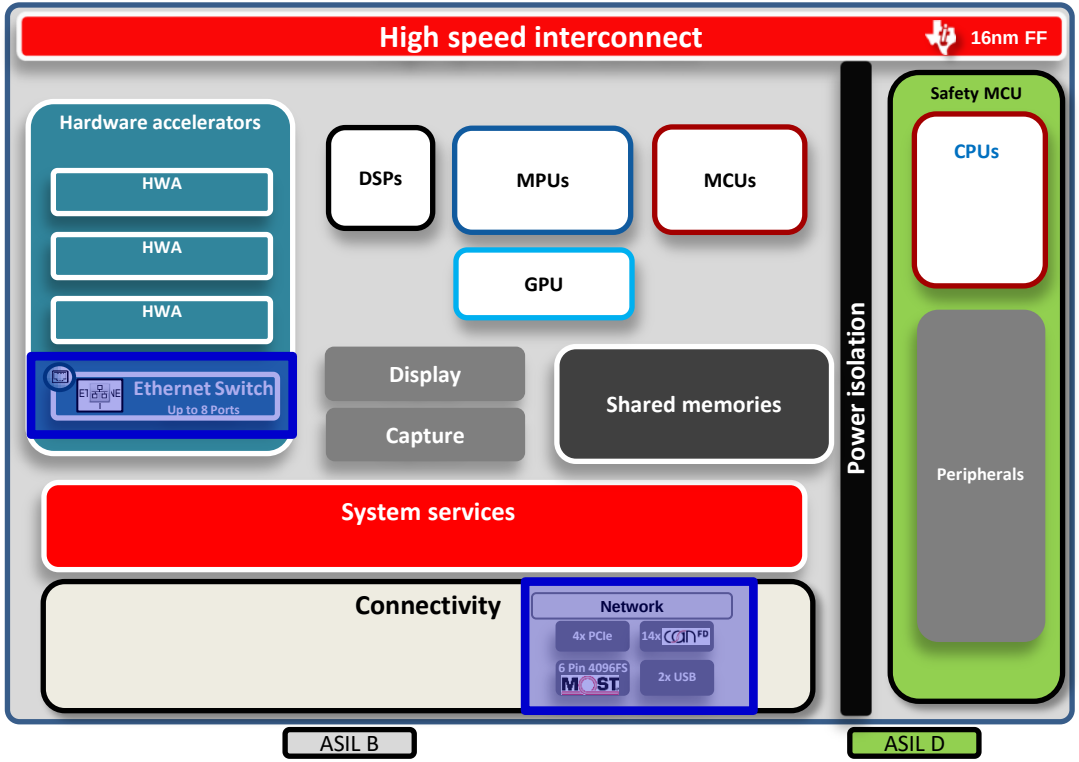

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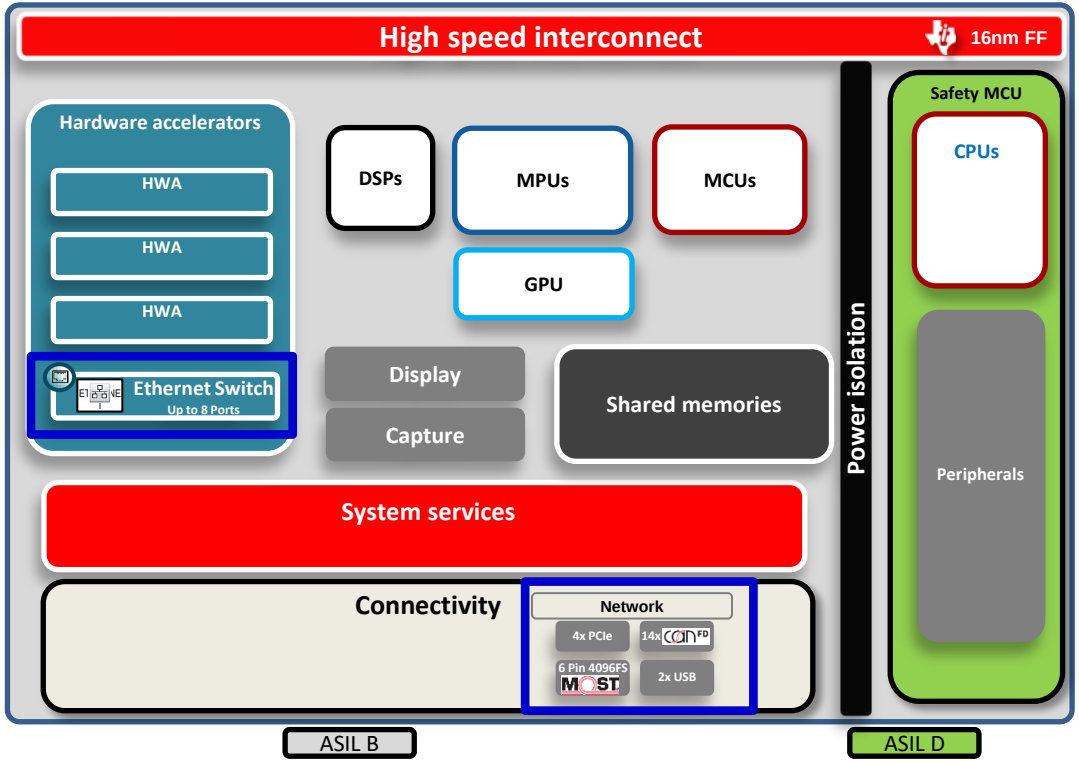
Network connectivity

- Ethernet switch:
  - Up to eight 1Gbps ports (SGMII, RGMII, RMII or QSGMII) plus 1 port on Safety MCU
  - Hardware classification and traffic shaping at full 1Gbps line rate
  - Reset isolation with packet forwarding
  - TSN and AVB support
  - Eliminates external switch replacement
- PCIe:
  - Up to 4x links with configurable width
  - Root complex or Endpoint support
  - SR-IOV support for virtualization
  - Port-to-port direct for non-transparent bridging eliminates external switch
- Up to 16 or more CAN-FD interfaces
- Two USB3.0 with dual role and Type-C switch
- One Media-LB interface to MOST150 controller



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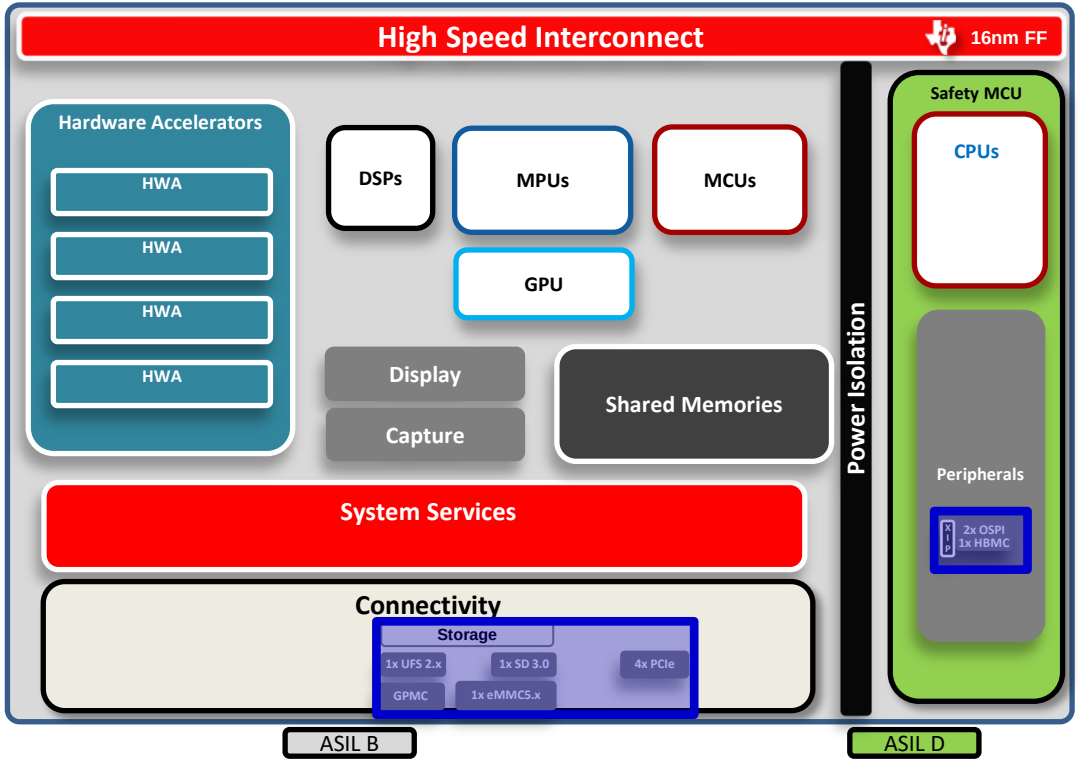

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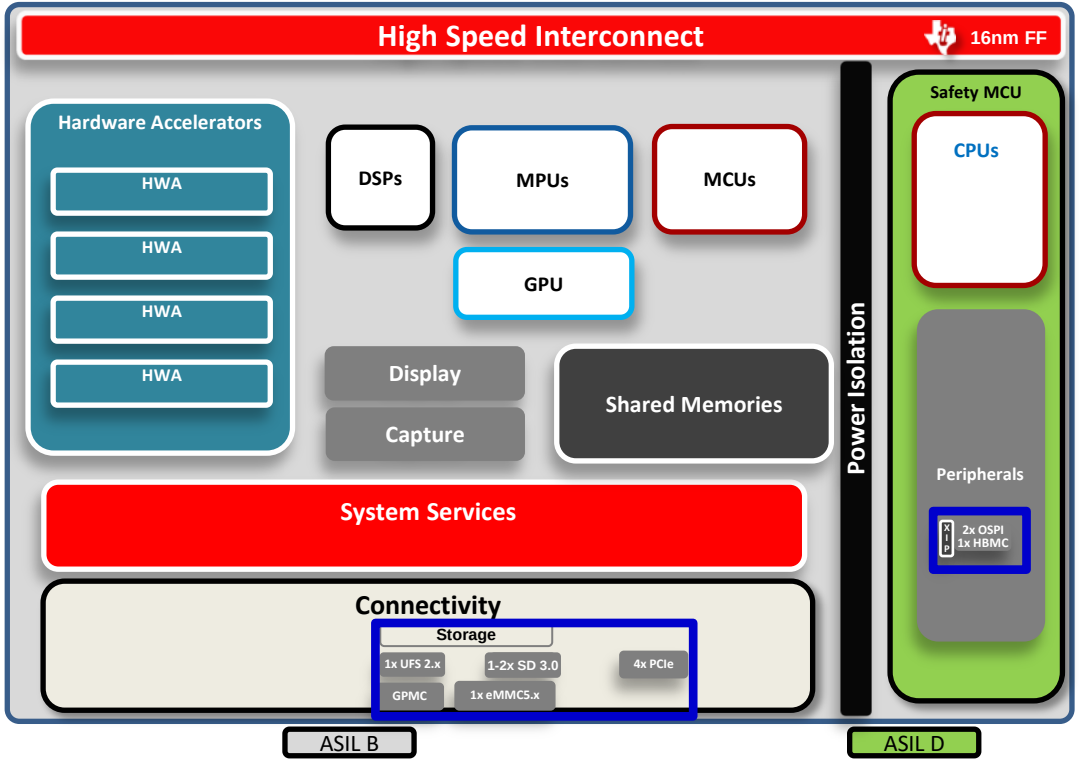

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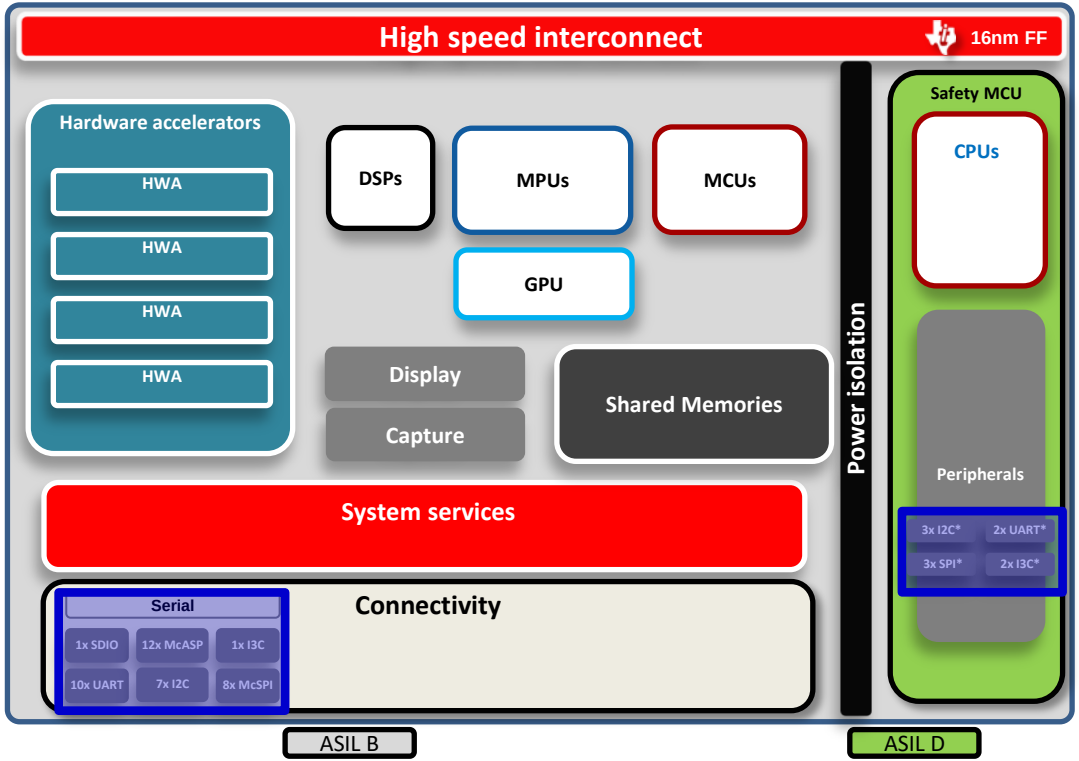

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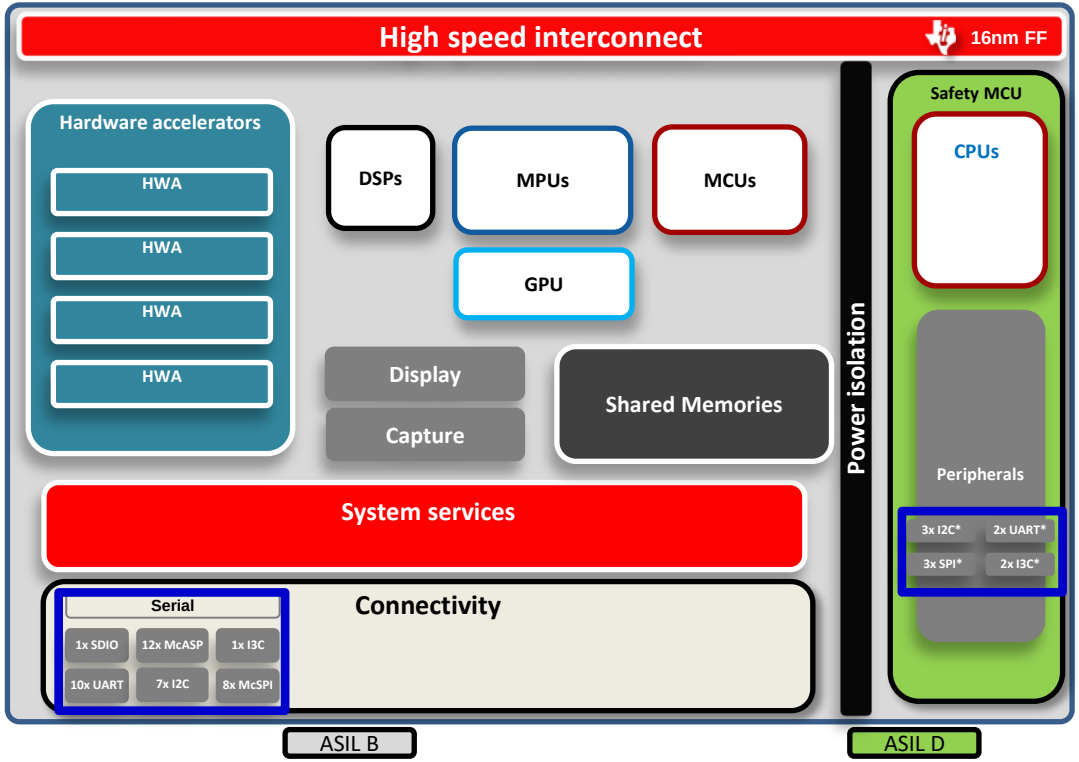

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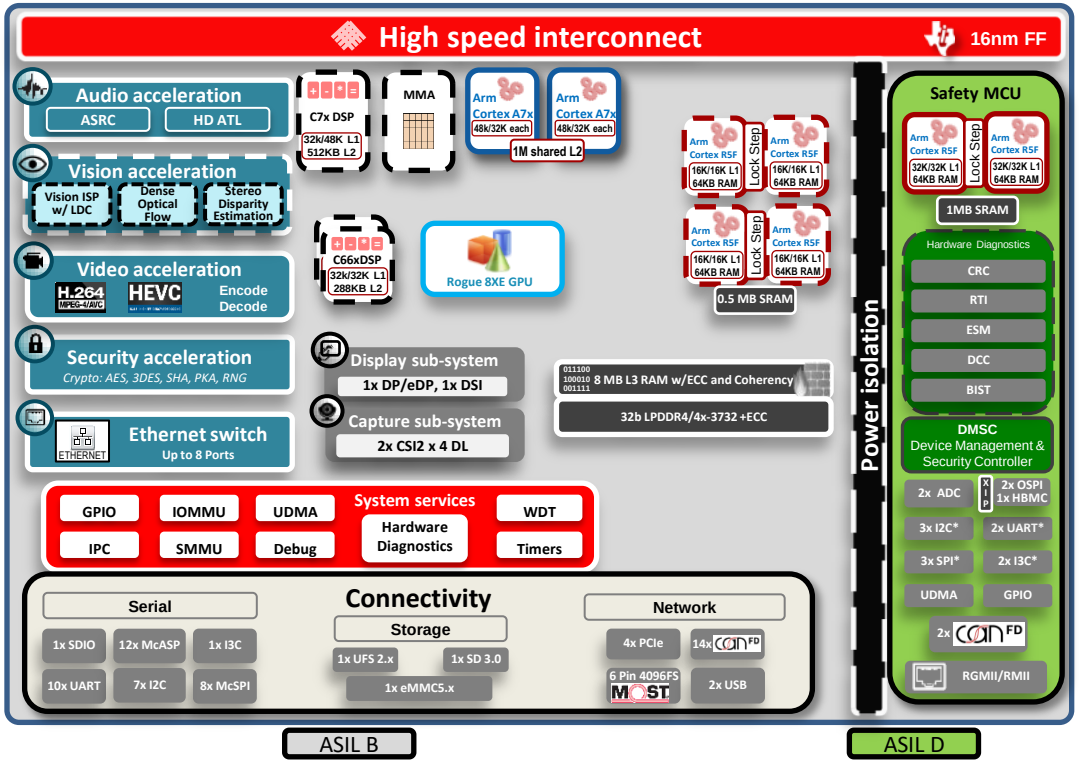

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For more information

- For more training on Jacinto 7 processors: http://training.ti.com/jacinto7
- Download Processor SDK Automotive for Jacinto 7 processors: http://www.ti.com/tool/PROCESSOR-SDK-DRA8X-TDA4X
- Order TDA4VM Jacinto Automotive processors for ADAS & autonomous vehicles: http://www.ti.com/product/TDA4VM
- Order the TDA4VMx evaluation module: http://www.ti.com/tool/TDA4VMXEVM
- Order DRA829V Jacinto Automotive processors for gateway & vehicle compute: http://www.ti.com/product/DRA829V
- Order the DRA829Vx evaluation module: http://www.ti.com/tool/DRA829VXEVM
- For questions regarding topics covered in this training, visit the processors support forum at the TI E2E Community website: https://e2e.ti.com