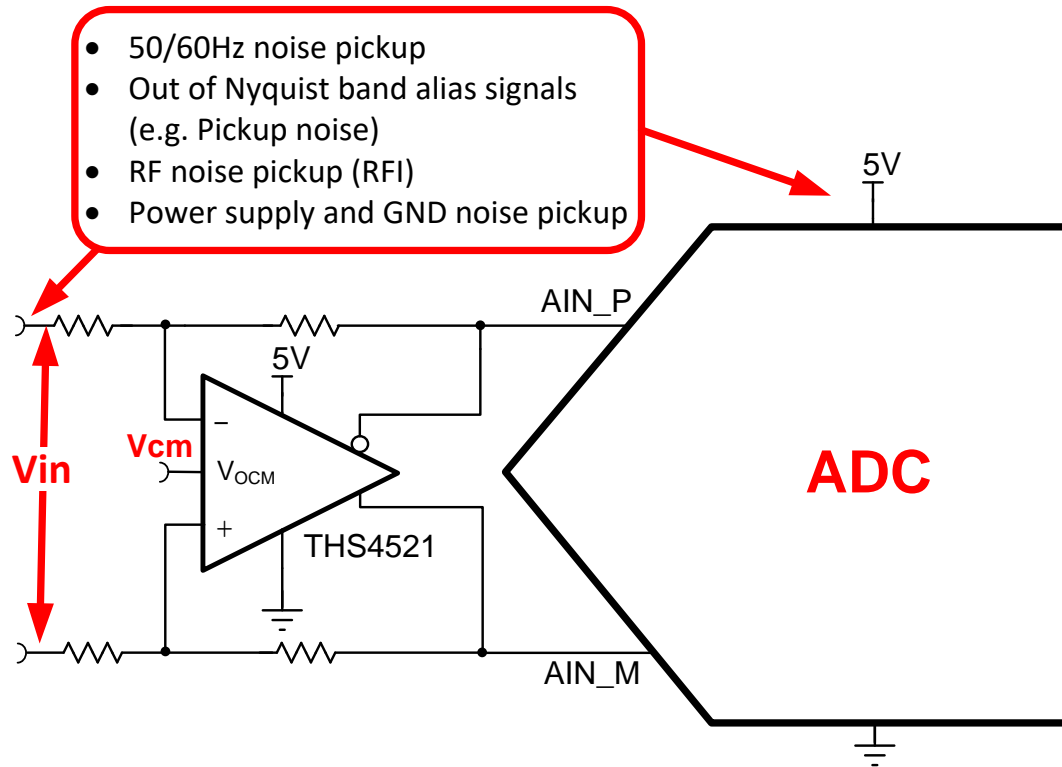# Noise & Drive Considerations SAR and Delta-Sigma ADCs

TI Precision Labs – ADCs

Created by Art Kay and Ryan Andrews

Presented by Ryan Andrews

Introducing Extrinsic Noise: ΔΣ and SAR ADCs

- 50/60Hz noise pickup
- Out of Nyquist band alias signals (e.g. Pickup noise)
- RF noise pickup (RFI)
- Power supply and GND noise pickup

5V

AIN_P

5V

Vcm

V_{OCM}

Vin

THS4521

ADC

AIN_M

TEXAS INSTRUMENTS

50/60Hz filter

Sampling rate = 20 sps
Max input f = 10Hz
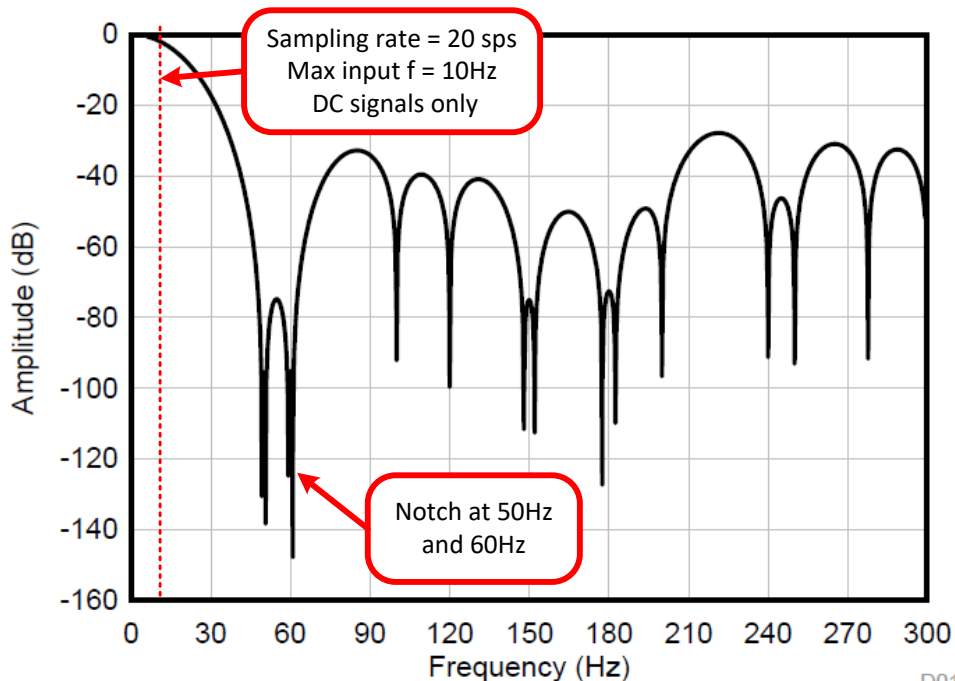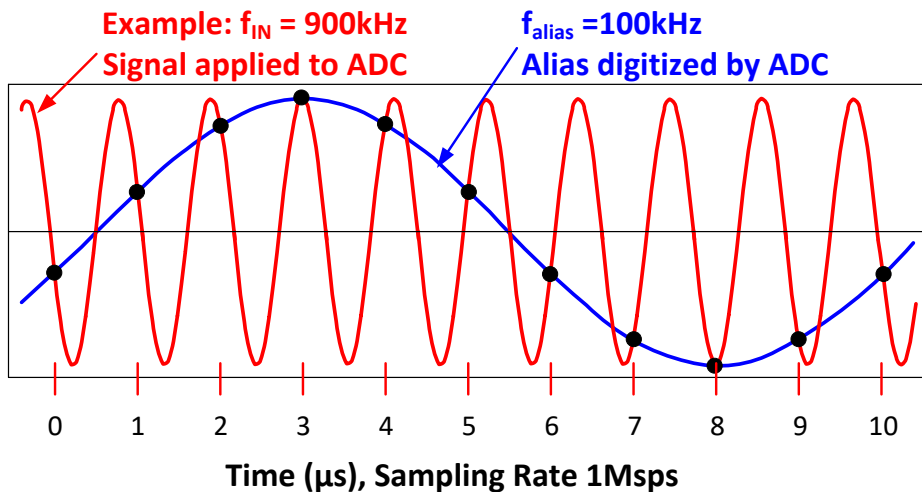DC signals only

Notch at 50Hz and 60Hz

Figure 89. FIR Frequency Response (20 SPS)
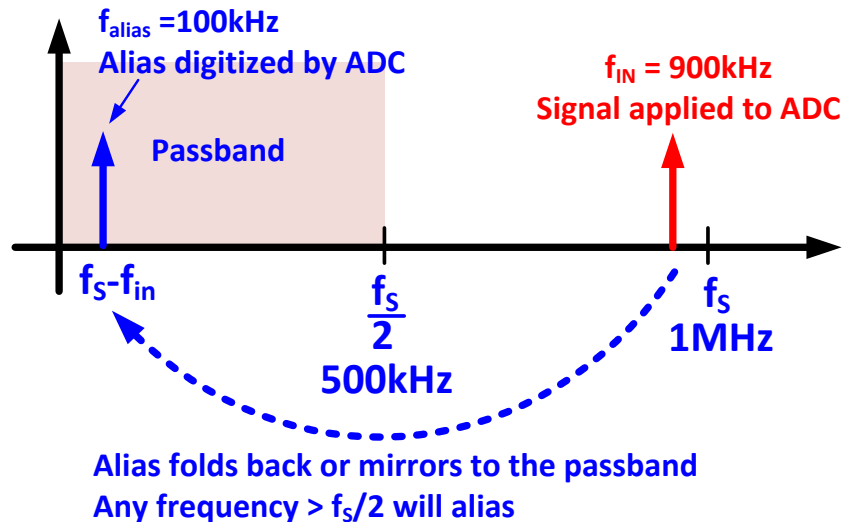
50/60Hz notch digital filter
- The notch on a Sinc filter can be tuned to 50Hz or 60Hz
- A more sophisticated FIR filter can have two notches that cancel both 50 and 60Hz (see example shown).
- This filter significantly reduces power line noise pickup.

TEXAS INSTRUMENTS

Aliasing – The Concept

Time Domain

Example: f_{IN} = 900kHz
Signal applied to ADC

f_{alias} =100kHz
Alias digitized by ADC

Time (µs), Sampling Rate 1Msps

Frequency Domain

f_{alias} =100kHz
Alias digitized by ADC

f_{IN} = 900kHz
Signal applied to ADC

Passband

f_S-f_{in}

$\dfrac{f_S}{2}$
500kHz

f_S
1MHz

Alias folds back or mirrors to the passband
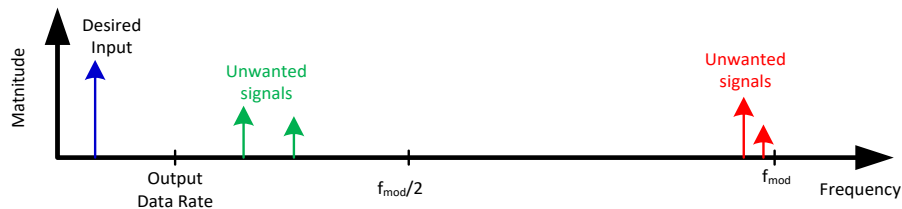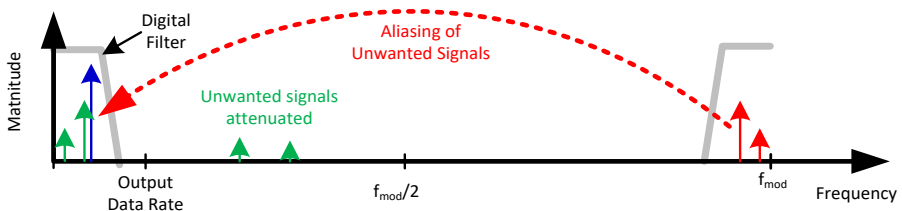Any frequency > f_S/2 will alias

Who's affected and who's not?

– **SAR** → Always need anti-aliasing filter as there is no digital filter. Multi-order analog filter may be required.

– **Delta-Sigma** → The anti-aliasing filter requirement on a delta sigma may be simplified by digital filter
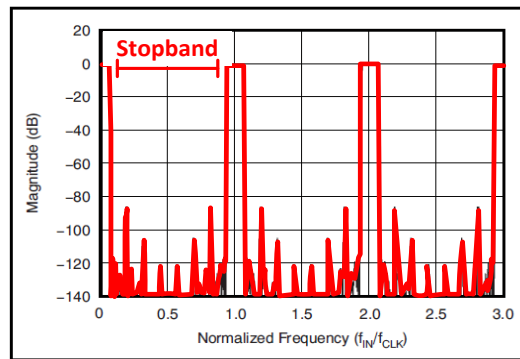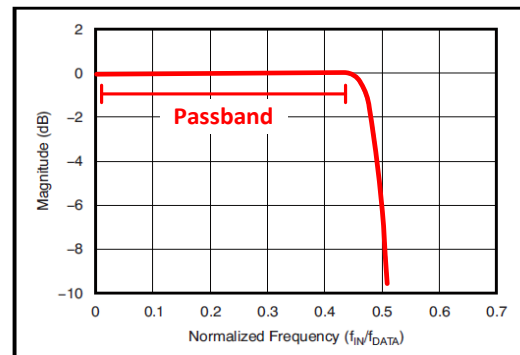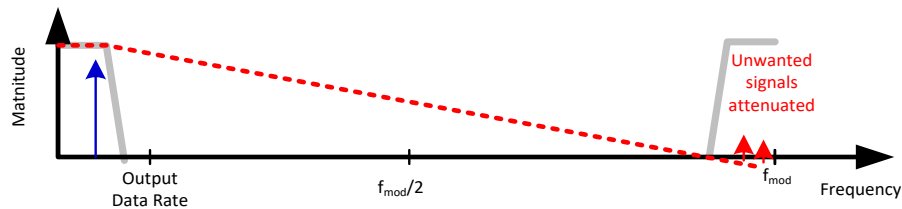
ΔΣ Antialiasing filter

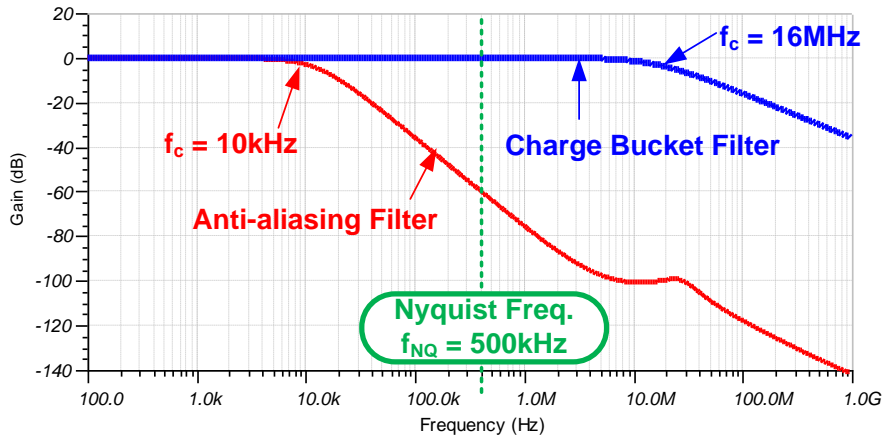# ΔΣ Antialiasing filter

Simple RC antialiasing filter

$$f_{c(CM)} = \frac{1}{2\pi(R_{in1})C_{cm1}}$$

$$f_{c(CM)} = \frac{1}{2\pi(100\Omega)(0.1nF)}$$
$$= 15.9MHz$$

$$f_{c(dif)} = \frac{1}{2\pi(2R_{in1})(C_{dif}+½Ccm_1)}$$

$$f_{c(dif)} = \frac{1}{2\pi(200\Omega)(1.05nF)}$$
$$= 0.758MHz$$

SAR Anti-aliasing Filter Design (fs = 1MHz)

Front End EMI & RFI Rejection

- Additional filters you may find include:
  - Some SAR and Delta-Sigma ADCs include a front-end RC filter for EMI purposes
  - Some include multi-order low-pass filters before an amplifier
- Depending on frequencies of out-of-band signals, Delta-Sigma ADC's digital filters can help attenuate these out-of-band signals

Delta-Sigma ADC
First order LPF RC for EMI immunity
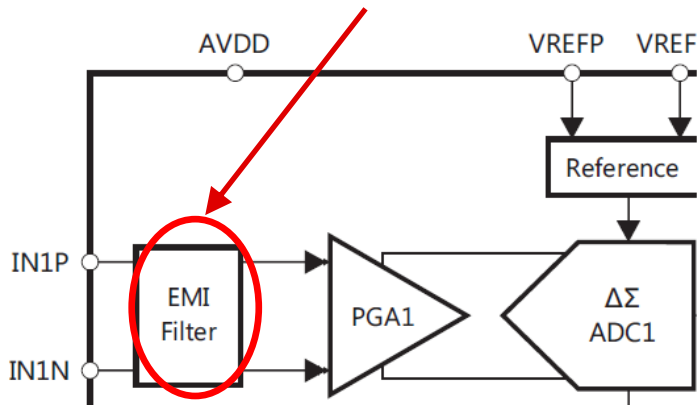
SAR ADC
Second-order LPF for Anti-Aliasing

Introducing Intrinsic Noise: ΔΣ and SAR ADCs

- Thermal input noise of ADC
- Jitter noise of clock source
- Voltage reference noise
- Quantization noise

Voltage Reference

AIN_P

5V

Thermal Noise

ADC

Vcm

V_OCM

Vin

PD

THS4521

AIN_M

Jitter noise

Clock

TEXAS INSTRUMENTS
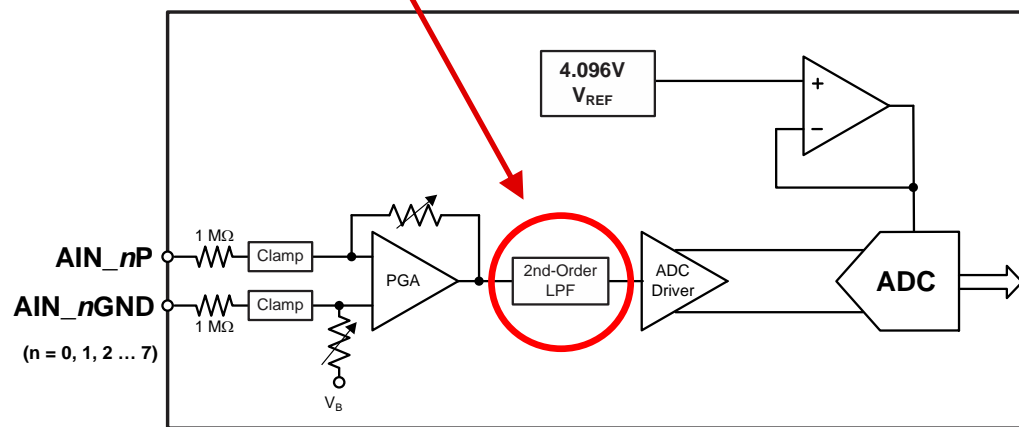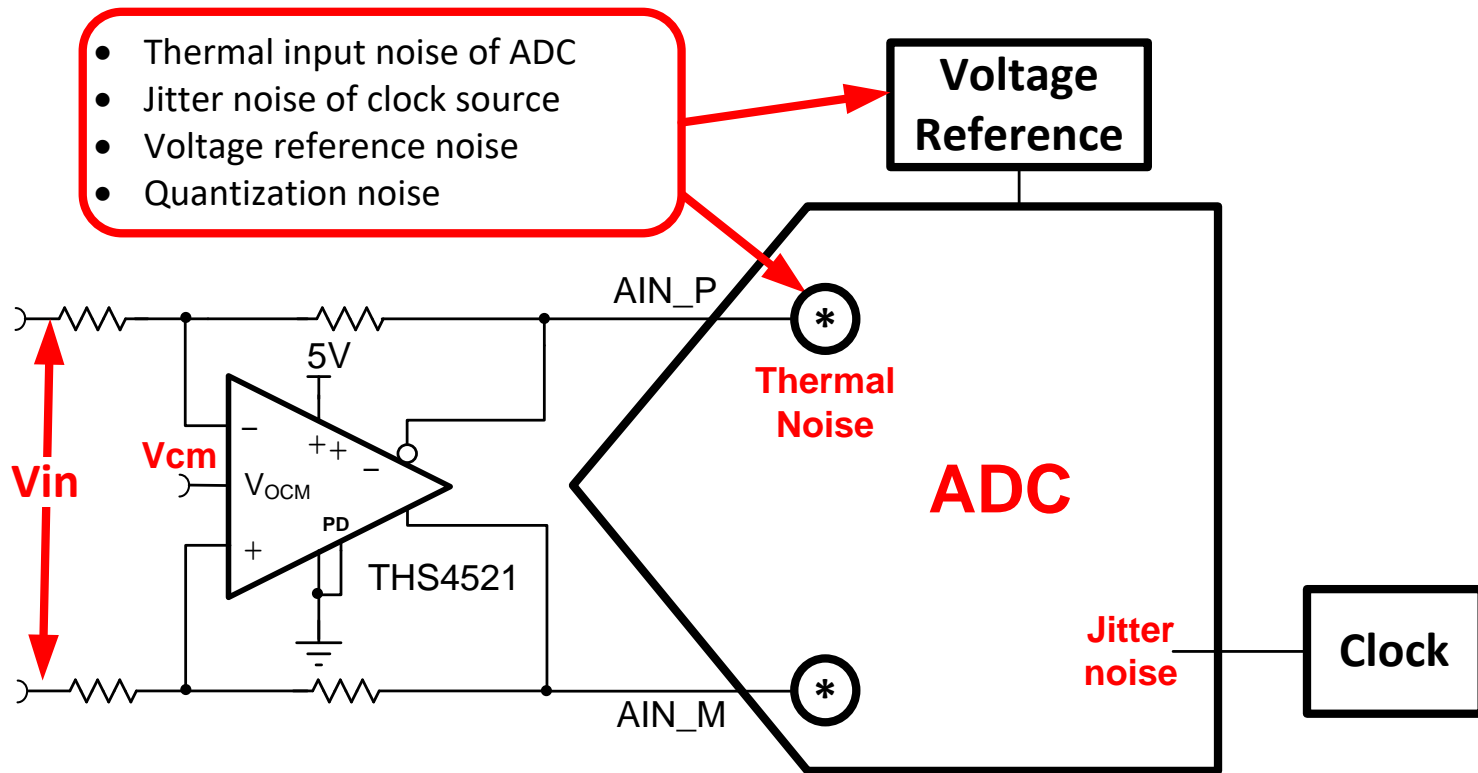
ADC Noise Sources: Clock Jitter

- Jitter is the conversion clock sample-to-sample variation
- Behavior is random following Gaussian distributions
- CLK source jitter and ADC aperture delay will both contribute to clocking error

CLK edge Variation

How Clock Jitter Effects ADCs

Voltage Measurement Error

- Data converters use clock edge or CONVST edge to control sample point
  - Deviation in sample point create measurement error
  - Effect: Noise floor of FFT will rise increasing system noise
- Acceptable clock jitter is dependent on:
  - Target SNR
  - Target Fin
  - OSR (Delta-Sigma only)

ΔΣ term only
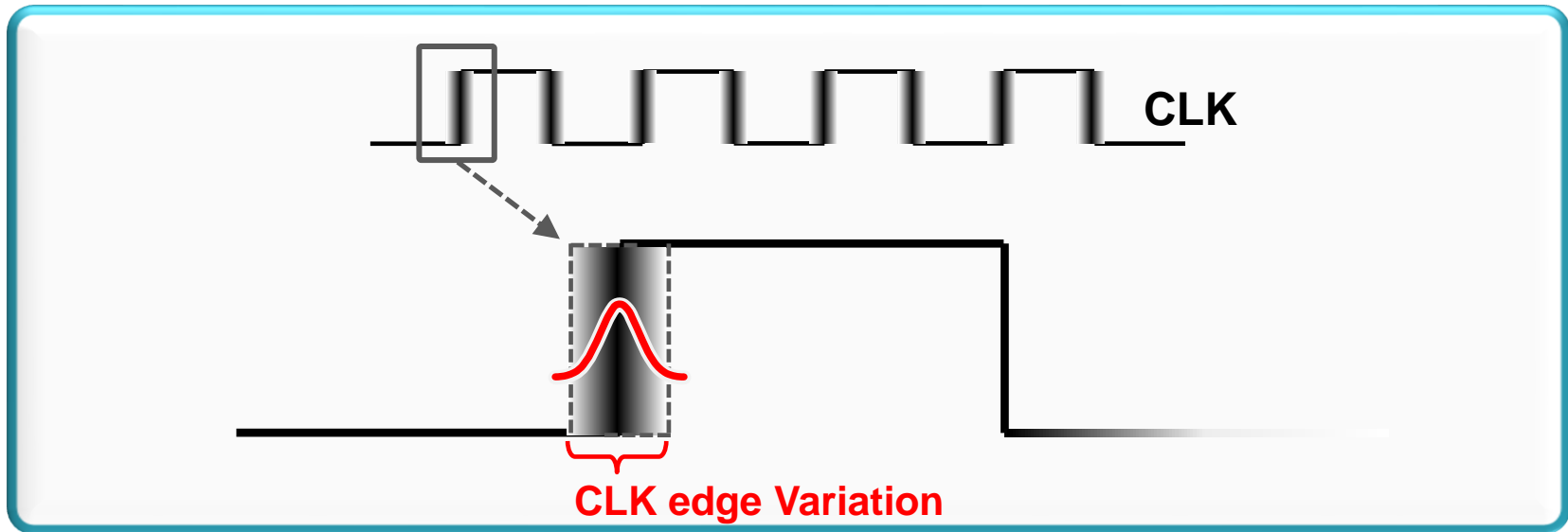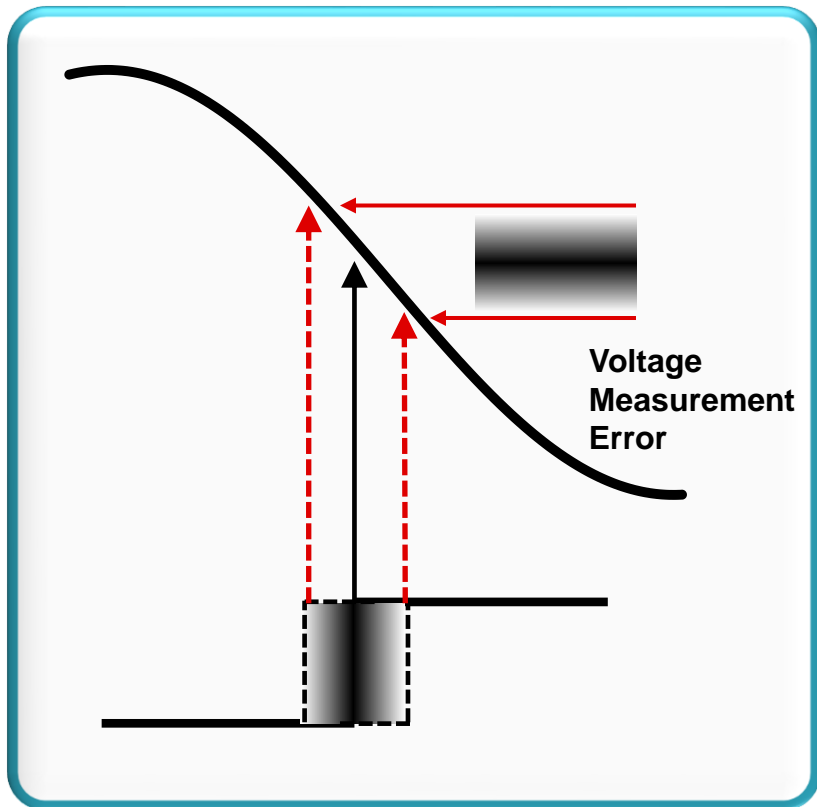
$$SNR = -20 * \log(2 * \pi * f_{in} * t_{jitter}) + \boxed{10 * \log(OSR)}$$

Jitter Sensitivity in SAR vs ΔΣ ADC

SAR SNR vs Jitter

ΔΣ SNR vs Jitter @ OSR = 128

$$SNR = -20 * \log(2 * \pi * f_{in} * t_{jitter})$$

$$SNR = -20 * \log(2 * \pi * f_{in} * t_{jitter}) + 10 * \log(OSR)$$

ΔΣ Oversampling and Noise Shaping

In general, filter order and cutoff frequency limit total noise

Sinc3 digital filter

Noise not rejected by filter

Noise rejected by filter

$F_m/2$

TEXAS INSTRUMENTS

Ultra low noise DC optimized ΔΣ example

ADS1262			
DATA RATE	FILTER MODE	Noise G = 32 (μV_{RMS})	BW -3dB (Hz)
2.5 SPS	FIR	0.011	1.2
2.5 SPS	SINC1	0.008	1.10
2.5 SPS	SINC3	0.006	0.65
10 SPS	FIR	0.023	4.7
10 SPS	SINC1	0.018	4.43
10 SPS	SINC3	0.014	2.62

Figure 91. FIR Frequency Response (10 SPS)

Figure 84. Sinc Frequency Response (10 SPS)

Wideband delta-sigma vs. SAR

ADS1675 ΔΣ	
DATA RATE	Noise (μV_{RMS})
125 kSPS	6.17
250 kSPS	7.44
500 kSPS	9.66
1000 kSPS	12.99
2000 kSPS	18.64
4000 kSPS	44.02

ADS8900B SAR	
DATA RATE	Noise (μV_{RMS})
0 to 1000kSPS	23

ADS1675 ΔΣ	
DATA RATE	SNR (dB)
125 kSPS	107
2000 kSPS	97
4000 kSPS	92

ADS8900B SAR	
DATA RATE	SNR (dB)
250 kSPS	104.5
500 kSPS	104.5
1000 kSPS	104.5

Noise wideband ΔΣ vs SAR

- ΔΣ uses noise shaping and digital filter to reduce noise
- ΔΣ digital filter bandwidth is adjusted to match data rates
- SAR has same noise for all sampling rate (no digital filter)
- SNR for ΔΣ will depend on sampling rate, OSR, and filter. SNR for SAR is not dependent on sampling rate

Quantization Noise vs. Thermal Noise
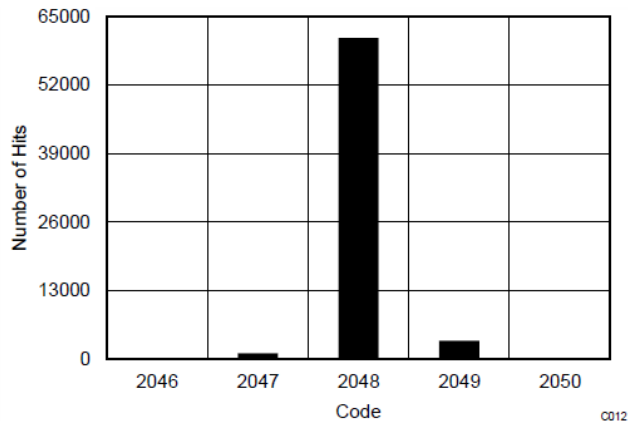
Quantization Noise
Dominant
ADS7042, SAR
12 Bit, 1MSPS
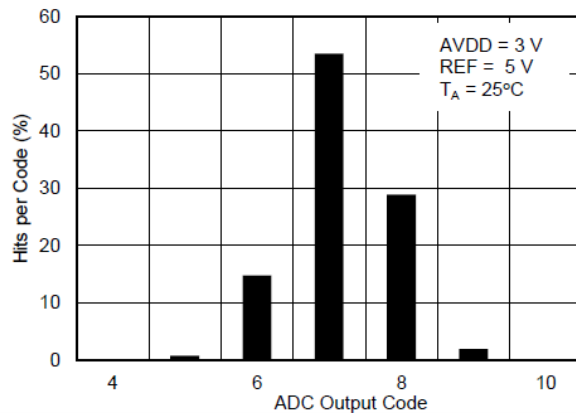
Both Thermal Noise
& Quantization Noise
ADS8881, SAR
18 Bit, 1MSPS
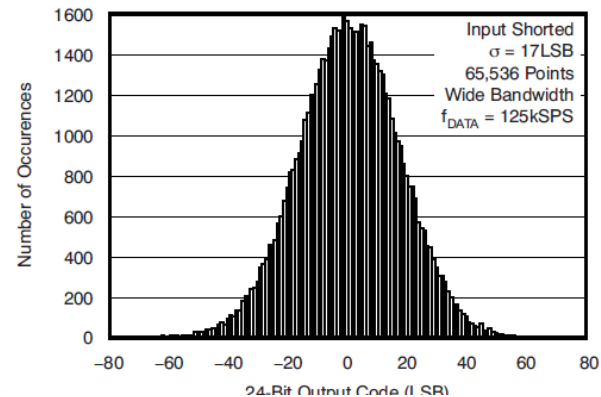
Thermal Noise
Dominant
ADS1675, $\Delta\Sigma$
24 Bit, 125kSPS

Introducing ∆Σ and SAR ADC drive considerations

- When is the reference buffer needed?
- When is the driver Amp needed?
- How do SAR and ∆Σ differ

Voltage Reference

AIN_P

5V

Vcm

V_{OCM}

Vin

THS4521

ADC

AIN_M
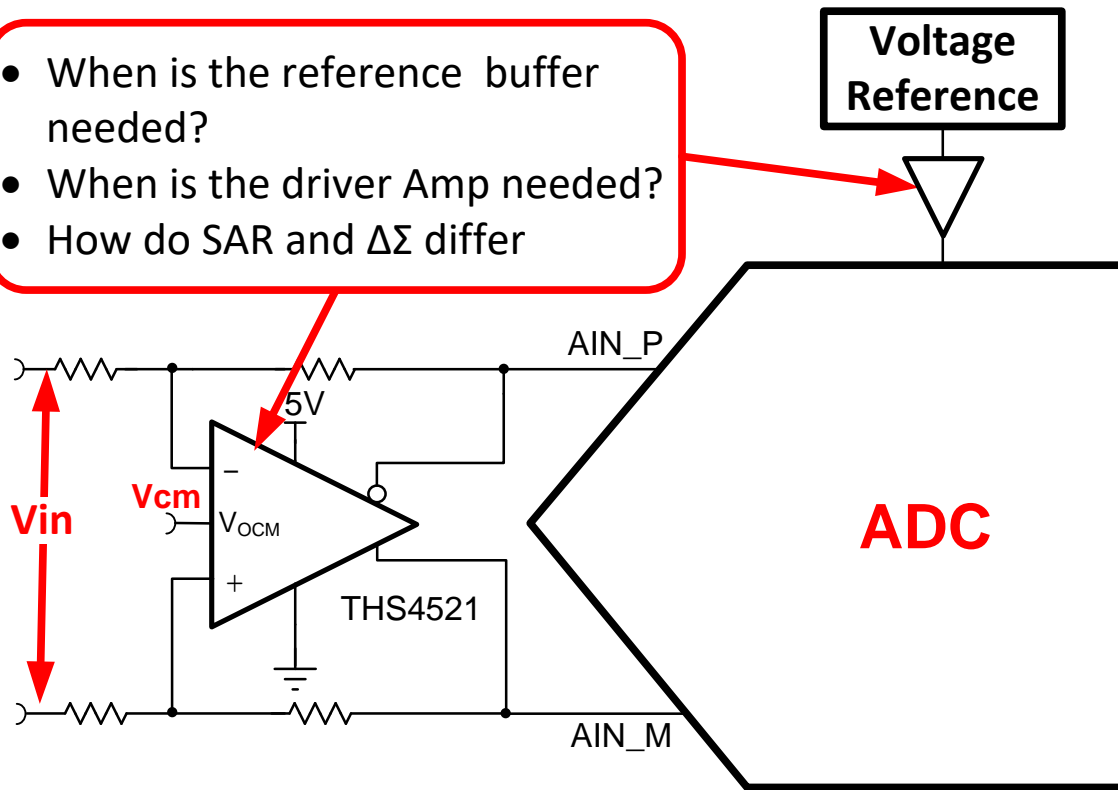
Direct Drive vs. Buffered
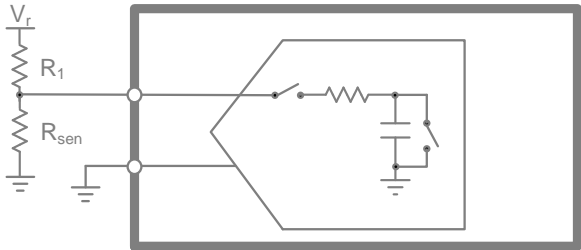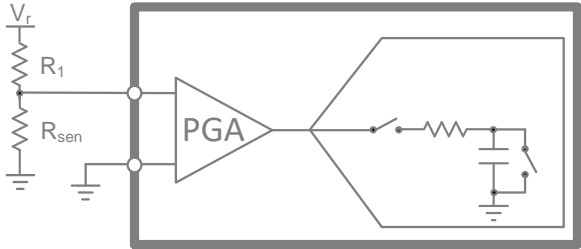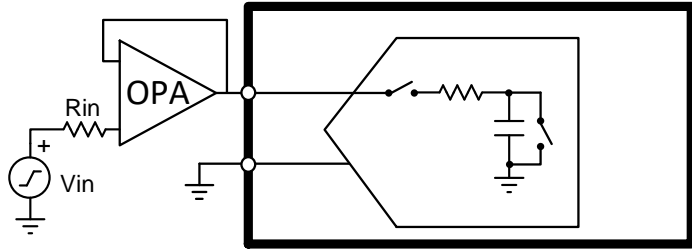
External Buffer
- Buffer is normally needed for high sampling rates to quickly and accurately charge the sample and hold capacitor to its final value.
- Amplifier may be used to attenuate or amplify a signal to match the input range.
- Match impedances

Direct Drive vs. Buffered
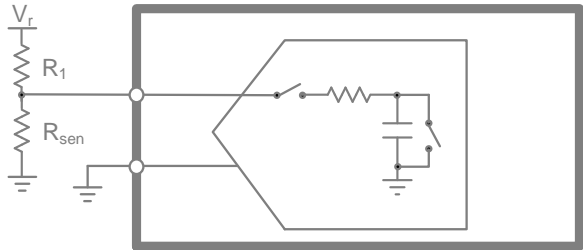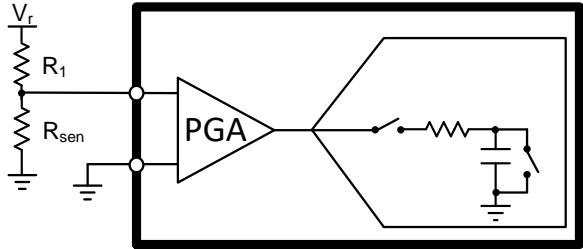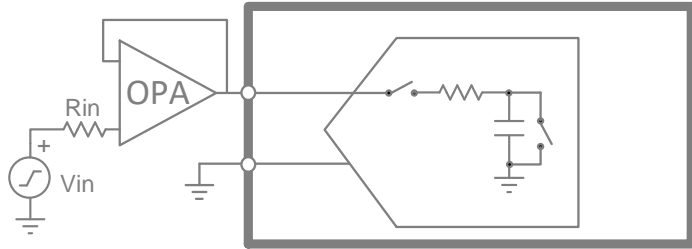
Integrated PGA
- Integrated PGA can be used in place of external amplifier (generally on ΔΣ)
- Typically the wide bandwidth applications use external amplifiers.

TEXAS INSTRUMENTS

Direct Drive vs. Buffered
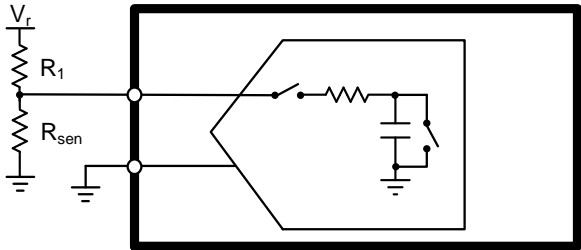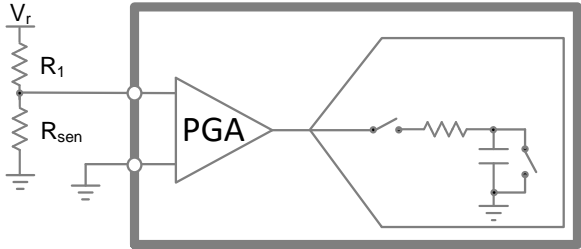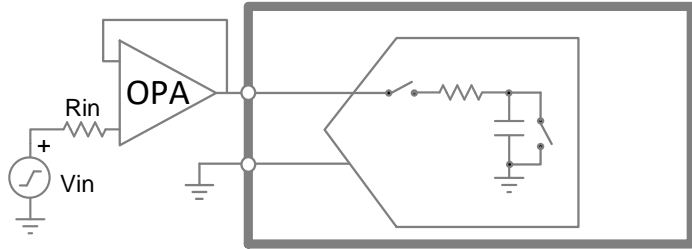
Direct Drive
- Direct drive can be used a lower sampling rates
- For direct drive, the external sensor impedance will impact the sample and hold settling.

Buffered – what bandwidth is required?
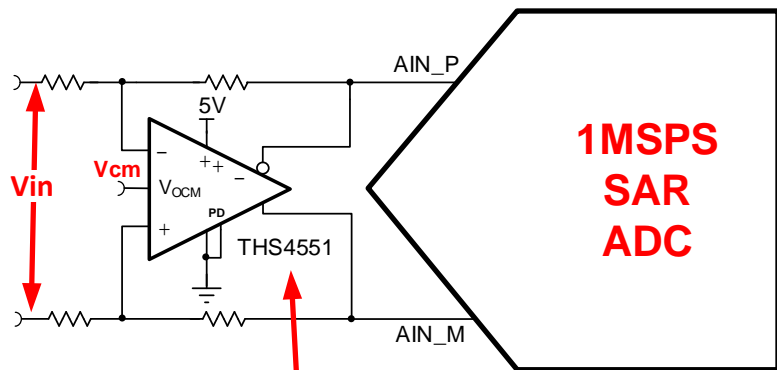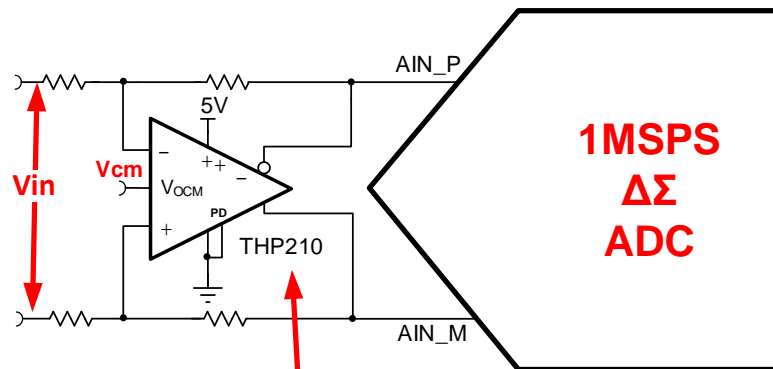
THS4551
- BW = 150MHz
- Iq = 1.35mA
- Vos = 175µV, ΔVos/ΔT = 1.8µV/C
- Ib = 1µA

THP210
- BW = 9.2MHz
- Iq = 0.95mA
- Vos = 40µV, ΔVos/ΔT = 0.35µV/C
- Ib = 2nA

Reference buffered required?
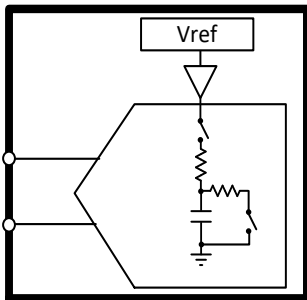
Reference integrated into ADC

Vref

Wide bandwidth buffer integrated into reference

REF6050

External wide bandwidth buffer

REF5050

OPA320

Wide bandwidth buffer integrated into ADC

REF5050

No wide bandwidth buffer. Lower sampling rate

REF5050
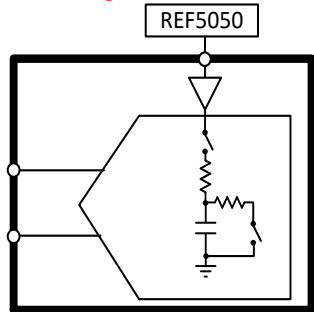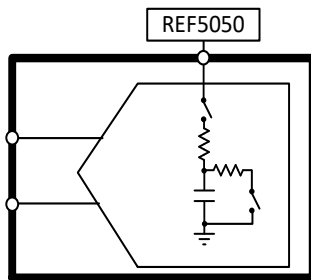
Reference buffer requirement
- For high sampling rates, a wide bandwidth may be required
- The buffer may be external, integrated in the reference, or integrated in the ADC.
- Reference buffer is not required for low sampling rates
- Both SAR and $\Delta\Sigma$ will both use direct drive or buffered configurations.

Thanks for your time! Please try the quiz.

Questions: SAR & Delta-Sigma Introduction

1. (T/F) SAR converters commonly have digital filters that can be used to reject 60Hz noise.
   a. True
   b. False

2. (T/F) A simple first-order RC filter can be used for the delta-sigma anti-aliasing filter, but a more complex active filter is typically required for SAR.
   a. True
   b. False

Questions: SAR & Delta-Sigma Introduction

3. (T/F) Clock jitter acts as a noise source. The impact of this noise source does not depend on the input signal frequency.

    a. True

    b. False

4. (T/F) Oversampling can be used to reduce clock jitter noise.

    a. True

    b. False

Questions: SAR & Delta-Sigma Introduction

5. The _____ converter typically has lower noise for lower sampling rates.
    a. Delta-Sigma
    b. SAR
    c. Both Delta-Sigma and SAR have lower noise for lower sampling rates.

6. An input buffer may be required to _____.
    a. Scale the input level
    b. Match impedances
    c. Drive the input sample and hold for accurate settling
    d. All of the above
    e. Option a and b are correct

Noise & Drive Considerations
SAR and Delta-Sigma ADCs
TI Precision Labs – ADCs

Created by Art Kay and Ryan Andrews

Presented by Ryan Andrews

Hello, and welcome to the TI Precision Lab series covering noise and ADC drive considerations for both SAR and delta-sigma converters. In the last video, we looked in detail at digital filters and latency considerations. In this video, we will focus on how SAR and delta-sigma converters are different from a noise perspective. We will also take a short look at input signal drive and voltage reference drive circuits for both topologies.

Introducing Extrinsic Noise: ΔΣ and SAR ADCs

- 50/60Hz noise pickup
- Out of Nyquist band alias signals (e.g. Pickup noise)
- RF noise pickup (RFI)
- Power supply and GND noise pickup

5V

AIN_P

5V

Vcm

V_{OCM}

Vin

−

+

THS4521

ADC

5V

AIN_M
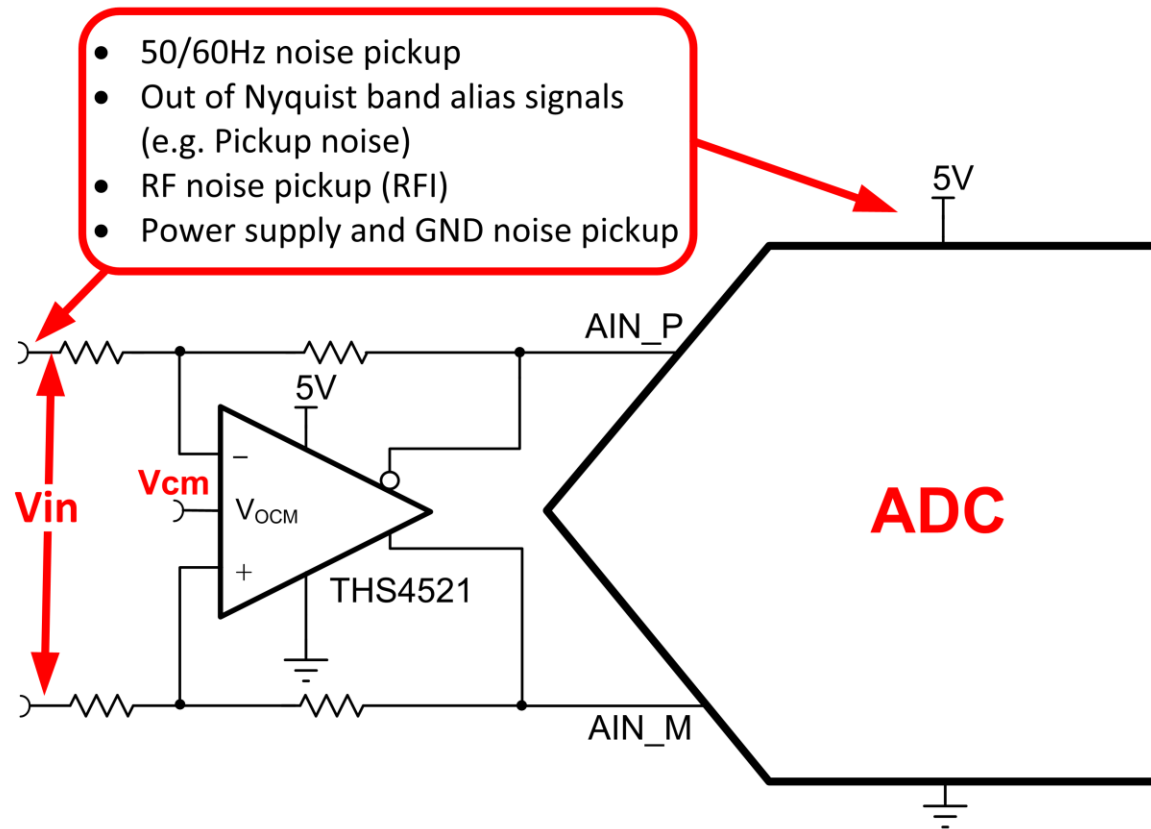
This topic will cover both intrinsic and extrinsic noise sources for SAR and delta-sigma converters. Intrinsic noise is naturally occurring and is generated by the circuit components themselves. Extrinsic noise is noise picked up from other circuits and even the outside world. Intrinsic noise normally has a Gaussian distribution, but extrinsic noise does not have a Gaussian distribution. First we will cover extrinsic noise.

Some common types of extrinsic noise that can impact an ADC system are 50 or 60Hz power line pickup, alias signals, RF noise, and power supply noise. Throughout this video, we will highlight any differences that may exist between SAR and delta-sigma converters.

50/60Hz filter
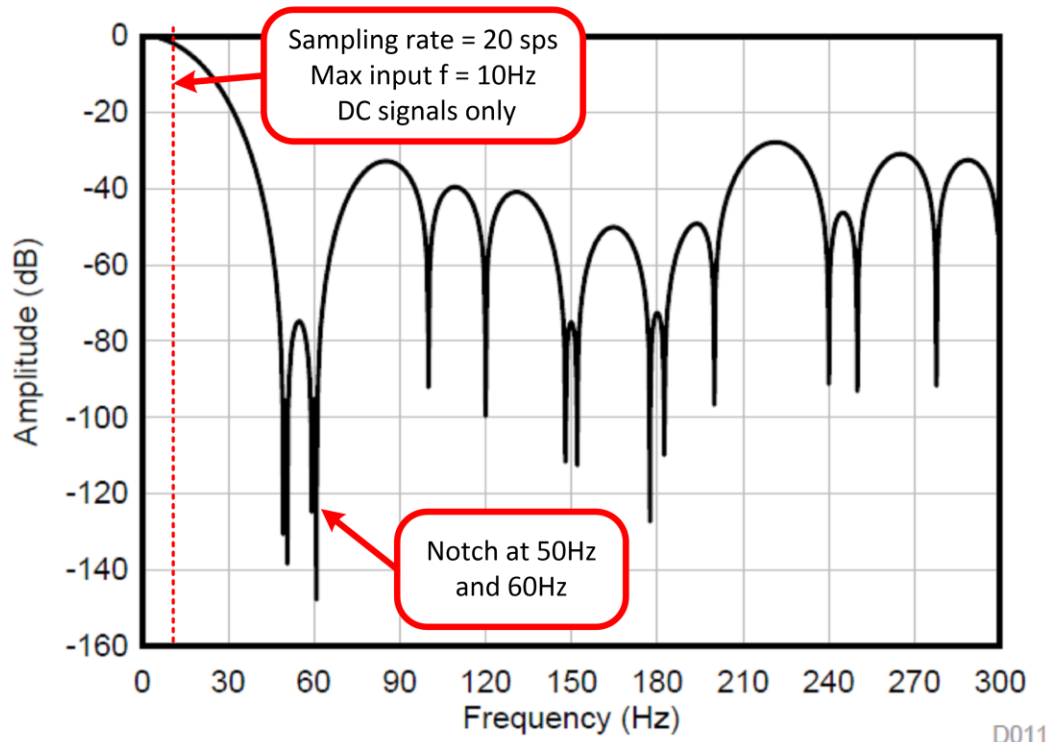
Figure 89. FIR Frequency Response (20 SPS)

50/60Hz notch digital filter
- The notch on a Sinc filter can be tuned to 50Hz or 60Hz
- A more sophisticated FIR filter can have two notches that cancel both 50 and 60Hz (see example shown).
- This filter significantly reduces power line noise pickup.

TEXAS INSTRUMENTS

Even for very low frequency systems, 50 and 60Hz noise can be an issue. Some delta-sigma converters have a special low latency filter that is specifically designed to reject both 50 and 60Hz signals. This type of filter has a similar response to a Sinc filter, but includes an extra notch at both 50 and 60 Hz. Thus, a product using this filter does not need to be customized to work in a specific region. This kind of operation is not found in SAR converters as they do not contain digital filters and are not usually optimized for DC operation.
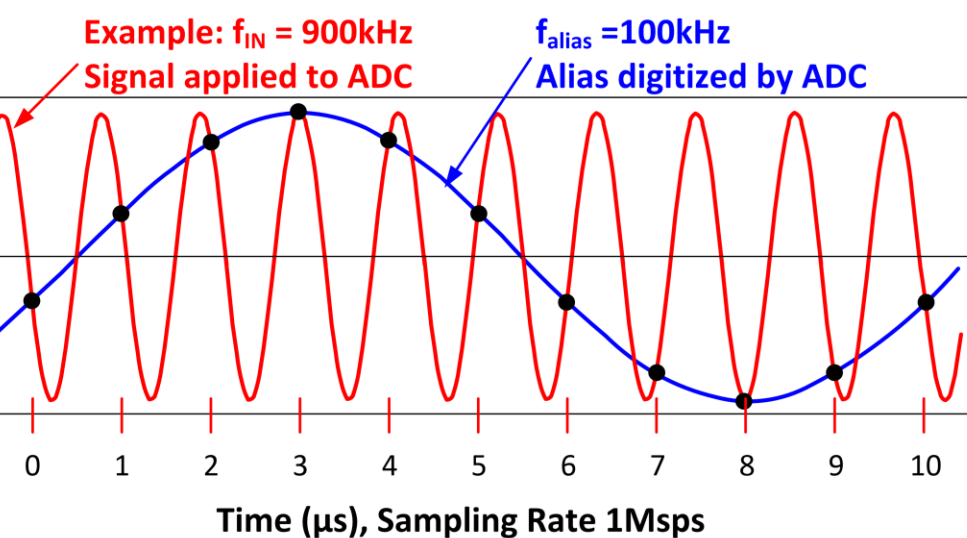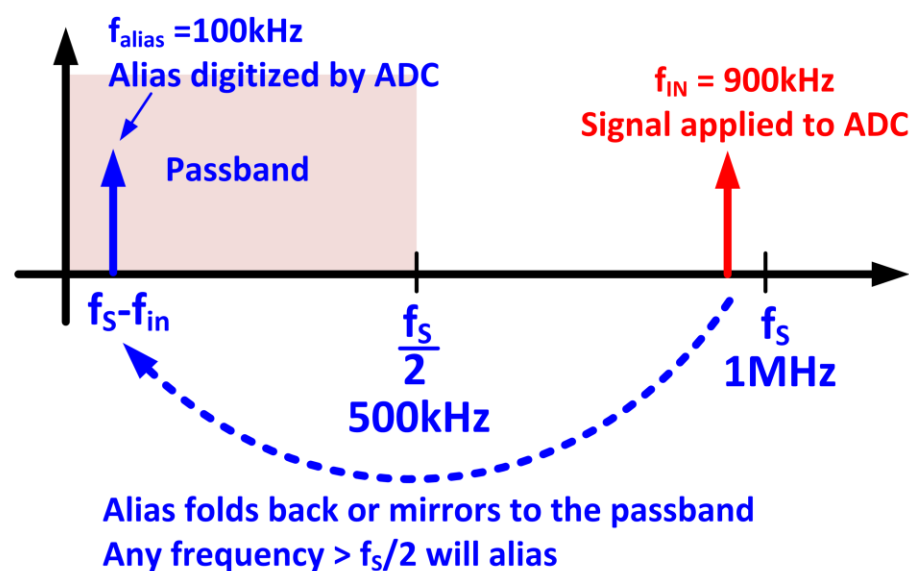
3

Aliasing – The Concept

Time Domain

Example: f_{IN} = 900kHz
Signal applied to ADC

f_{alias} =100kHz
Alias digitized by ADC

0	1	2	3	4	5	6	7	8	9	10

Time (µs), Sampling Rate 1Msps

Frequency Domain

f_{alias} =100kHz
Alias digitized by ADC

f_{IN} = 900kHz
Signal applied to ADC

Passband

f_S-f_{in} $\dfrac{f_S}{2}$ f_S
                    500kHz   **1MHz**

Alias folds back or mirrors to the passband
Any frequency > f_S/2 will alias

Who's affected and who's not?

- **SAR** → Always need anti-aliasing filter as there is no digital filter. Multi-order analog filter may be required.

- **Delta-Sigma** → The anti-aliasing filter requirement on a delta sigma may be simplified by digital filter

TEXAS INSTRUMENTS

Aliasing is an effect by which a sampled high frequency signal appears as a low frequency signal called an "alias". This alias is indistinguishable from other low frequency signals that are not aliases and we generally want to avoid them. To prevent aliasing, we must consider the Nyquist criteria, which states that the input signal frequency must be kept below the one-half the sampling frequency. Any input signal with a frequency greater that one-half the sampling frequency will create aliases.

The graph on the left shows aliasing in the time domain. The sampling rate for this example is 1MSPS, so the Nyquist frequency is 500kHz. The input frequency, shown in red, is 900kHz, which violates the Nyquist criteria, and consequently, there will be an alias. The blue signal is the 100-kHz alias. You can see how sampling the input frequency at 1MSPS generates the alias in the time domain.

The graph on the right shows the same aliasing example in the frequency domain. The red input signal at 900kHz aliases back to the first Nyquist zone. The frequency of the alias is at the sampling rate minus the input frequency ($f_{alias} = f_s - f_{in}$). Again, remember that any frequency above fs/2 will cause an alias.

4

ΔΣ Antialiasing filter

Input Signal and Noise pickup

Aliasing and attenuation of noise

External antialiasing filter Single pole RC
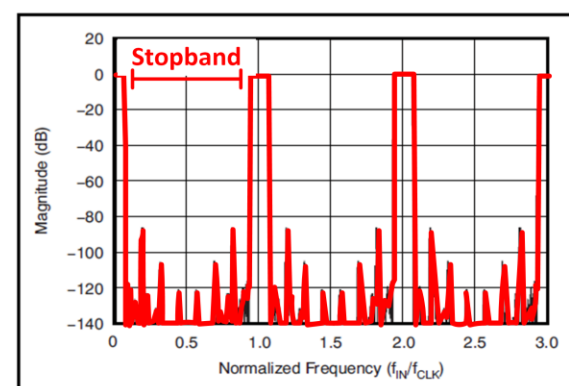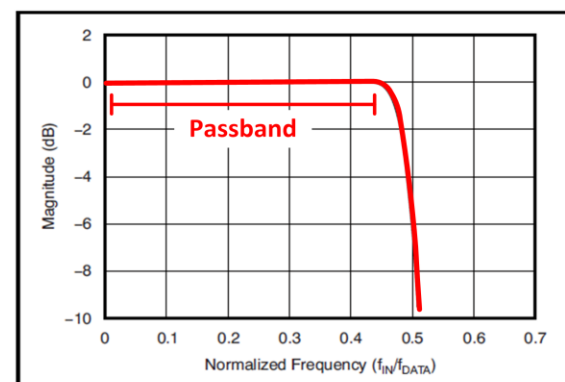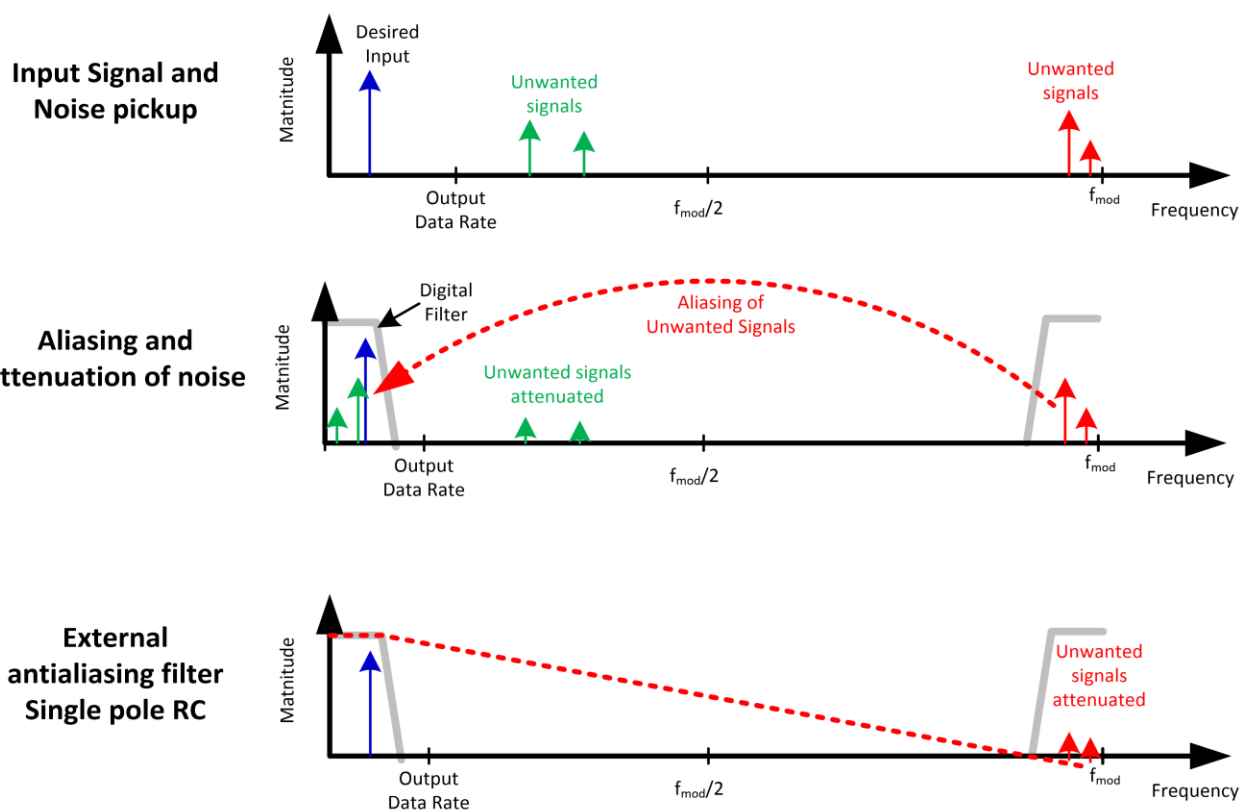
This slide explains the anti-aliasing requirements for delta-sigma converters.

Beginning with the top figure, unwanted noise signals can occur at frequencies greater than the output data rate of the delta-sigma converter. If these signals are left unfiltered, they will alias into the ADC's passband. The passband for a delta-sigma converter can be as wide as one-half the output data rate, as shown in the top-right image.

A delta-sigma converter will have digital filters that can help minimize the anti-aliasing requirement. This is shown in the middle figure. The digital filter in gray attenuates the green noise signals in the filter's stopband. However, it is important to realize that the digital filter will also alias or reflect at multiples of the modulator frequency, labeled "fMOD." If the unwanted noise pick-up is near the modulator frequency, it will be left unfiltered and reflect into the passband. That is what is happening with the red noise signals. These signals occur near the modulator frequency beyond the stopband, so they are inside the *aliased* digital filter passband and will be reflected into the passband.

The way to avoid this problem is to use a simple external RC filter. This filter will have first-order, low-pass response that rolls off gradually and attenuate the high-frequency noise near the modulator frequency to minimize any aliasing issues. Let's look at component selection for this RC filter in the next slide.
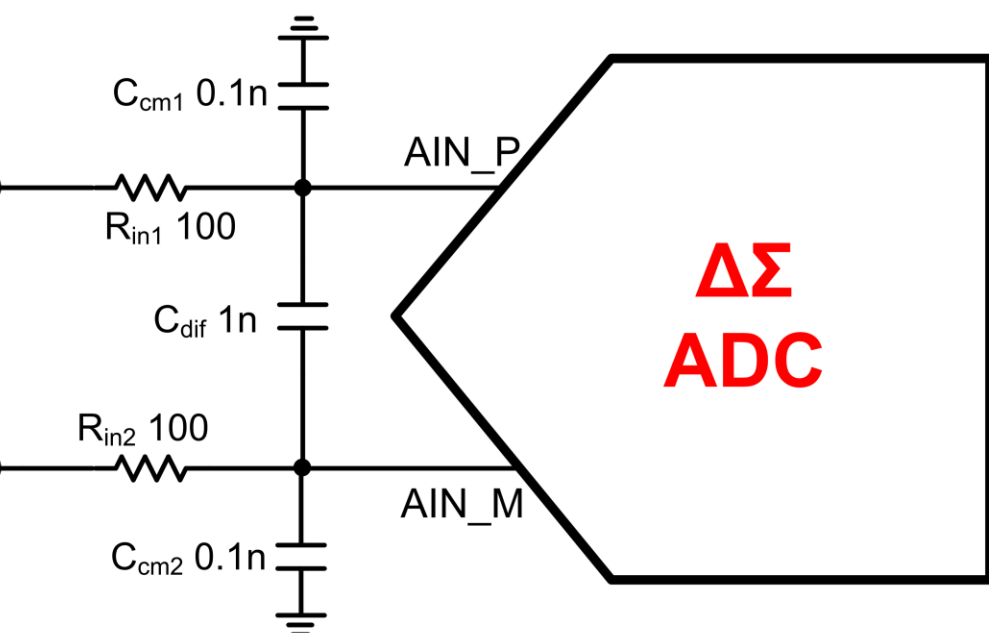
5

ΔΣ Antialiasing filter

Simple RC antialiasing filter

$$f_{c(CM)} = \frac{1}{2\pi(R_{in1})C_{cm1}}$$

$$f_{c(CM)} = \frac{1}{2\pi(100\Omega)(0.1nF)}$$

$$= 15.9MHz$$

$$f_{c(dif)} = \frac{1}{2\pi(2R_{in1})(C_{dif}+\frac{1}{2}Ccm_1)}$$

$$f_{c(dif)} = \frac{1}{2\pi(200\Omega)(1.05nF)}$$

$$= 0.758MHz$$

This slide shows the most common antialiasing filter topology used with delta-sigma converters.

Note that the common-mode capacitors from each input to ground are 10 times smaller than the differential capacitor. This is a common approach as mismatch in common-mode capacitance due to component tolerance will convert common-mode signals to differential signals. Using the smaller common-mode capacitor values sets the cutoff frequency higher than the differential filter. This assures that any signals that are translated from common-mode to differential will be attenuated by the differential filter.

This topic will be covered in more detail in a later video series. For now, the main point is the understand that the delta-sigma antialiasing filter is very simple. Now, for comparison, let's look at a typical antialiasing filter for a SAR converter.

SAR Anti-aliasing Filter Design (fs = 1MHz)
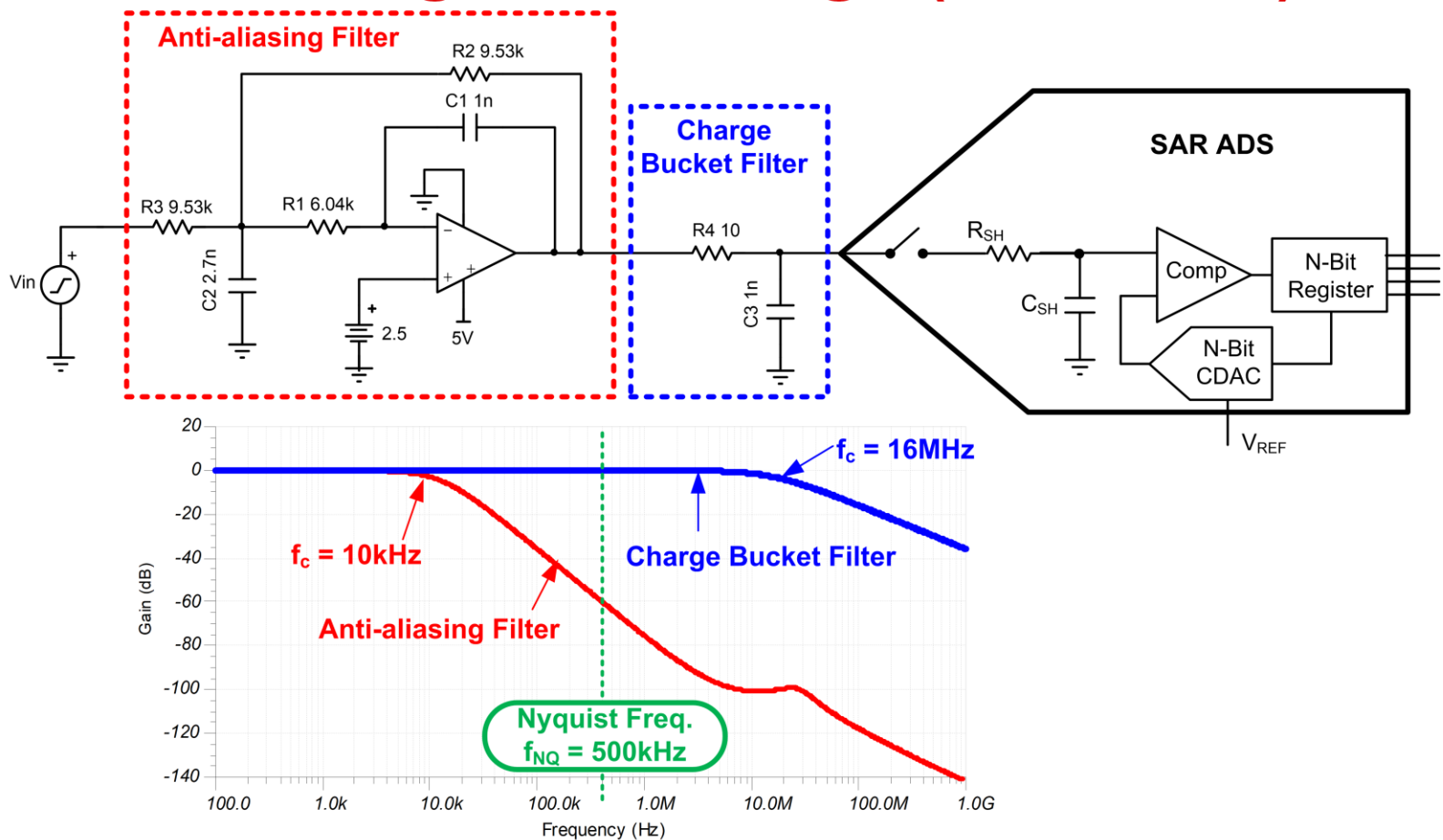
Here we show a typical SAR system with an anti-aliasing filter, and a charge bucket filter.

The charge bucket filter is used to absorb transient charge kickback from the SAR input sample-and-hold circuit. In a later video series, we cover this topic in great detail, but for now you should understand that this filter is not designed to be an anti-aliasing filter. Generally, the cutoff frequency of this filter will be set to 10 or 20 times the sampling frequency of the ADC, whereas an antialiasing filter needs to have a cutoff less than half the sampling frequency to be effective. In this example, you can see that the charge bucket filter cutoff is set to 16MHz, even though the sampling frequency is 1MHz.

In this example, the antialiasing filter is an active second-order low-pass filter with a cutoff frequency of 10 kHz. This filter has an attenuation of 60dB at the Nyquist frequency, so it functions as an effective antialiasing filter.

An important point here is that the SAR typically does not have an integrated digital filter, so an external active filter that has significant attenuation at the Nyquist frequency is required to prevent aliasing. The delta-sigma converter, on the other hand, always has an integrated digital filter, so the antialiasing requirements are significantly relaxed.

Front End EMI & RFI Rejection

- Additional filters you may find include:
  - Some SAR and Delta-Sigma ADCs include a front-end RC filter for EMI purposes
  - Some include multi-order low-pass filters before an amplifier
- Depending on frequencies of out-of-band signals, Delta-Sigma ADC's digital filters can help attenuate these out-of-band signals

Delta-Sigma ADC
First order LPF RC for EMI immunity
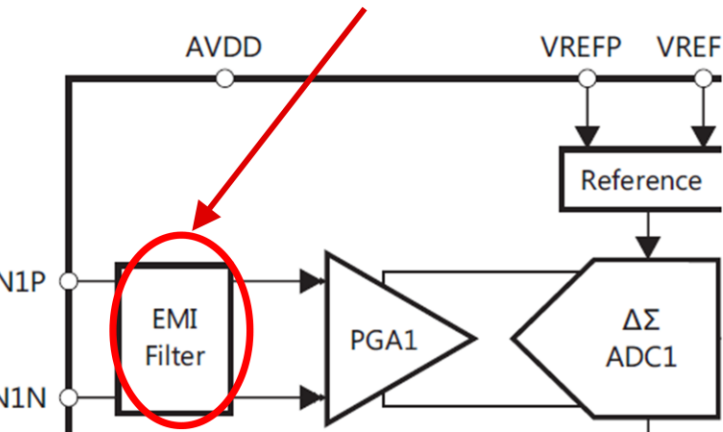
SAR ADC
Second-order LPF for Anti-Aliasing
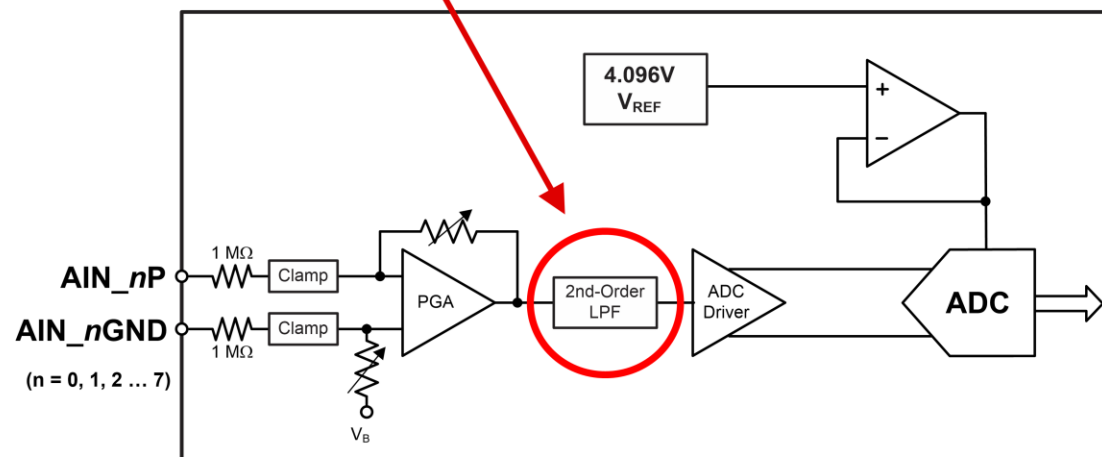
TEXAS INSTRUMENTS

One last comment on ADC filtering. Some products will include integrated filters. For example, the Delta Sigma converter shown on the left includes an RF frequency filter to protect against electromagnetic interference or EMI. This filter is effective at frequency's in the hundreds of Mega-Hertz to Giga-Hertz. It minimizes the effect of RF frequencies on the Delta-Sigma's PGA. Even though the PGA bandwidth is significantly lower than RF frequencies, noise pick-up in this frequency range can cause large shifts in the amplifier's offset. So, the filter effectively minimizes the effect of RF noise pick-up.

The SAR converter shown to the right incorporates an integrated anti-aliasing filter into the design. This is very helpful as no external anti-aliasing filter is now required. In fact, this design incorporates an internal PGA, reference, and reference buffer, so that the complete signal chain is contained in one device.

This concludes the section on extrinsic noise. Now we will look at intrinsic noise.

Introducing Intrinsic Noise: ΔΣ and SAR ADCs

- Thermal input noise of ADC
- Jitter noise of clock source
- Voltage reference noise
- Quantization noise

Voltage Reference

AIN_P

Thermal Noise

ADC

Vin

Vcm

V_{OCM}

5V

++

PD

THS4521

AIN_M

Jitter noise

Clock
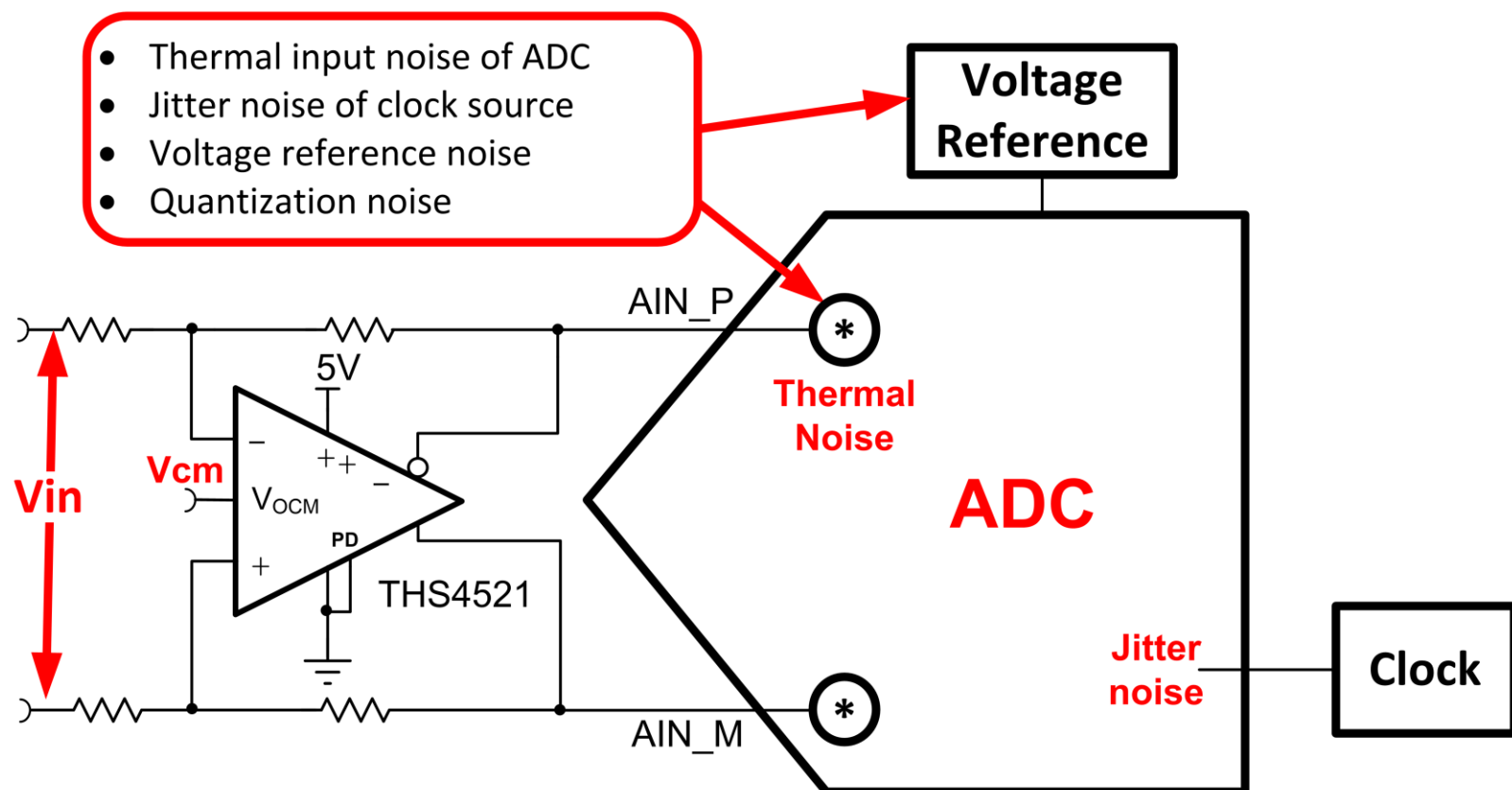
Intrinsic noise is naturally occurring noise that is generated by the circuit components themselves. This noise typically has a Gaussian distribution and the noise levels can be predicted through calculations or simulations. Some examples of intrinsic noise are thermal noise, jitter noise from a clock source, voltage reference noise, and quantization noise.

Since the clock jitter noise and other thermal noise sources are all Gaussian, they are indistinguishable from one another and can be combined using the root sum of squares.

ADC Noise Sources: Clock Jitter KA2

- Jitter is the conversion clock sample-to-sample variation
- Behavior is random following Gaussian distributions
- CLK source jitter and ADC aperture delay will both contribute to clocking error

CLK

CLK edge Variation

TEXAS INSTRUMENTS
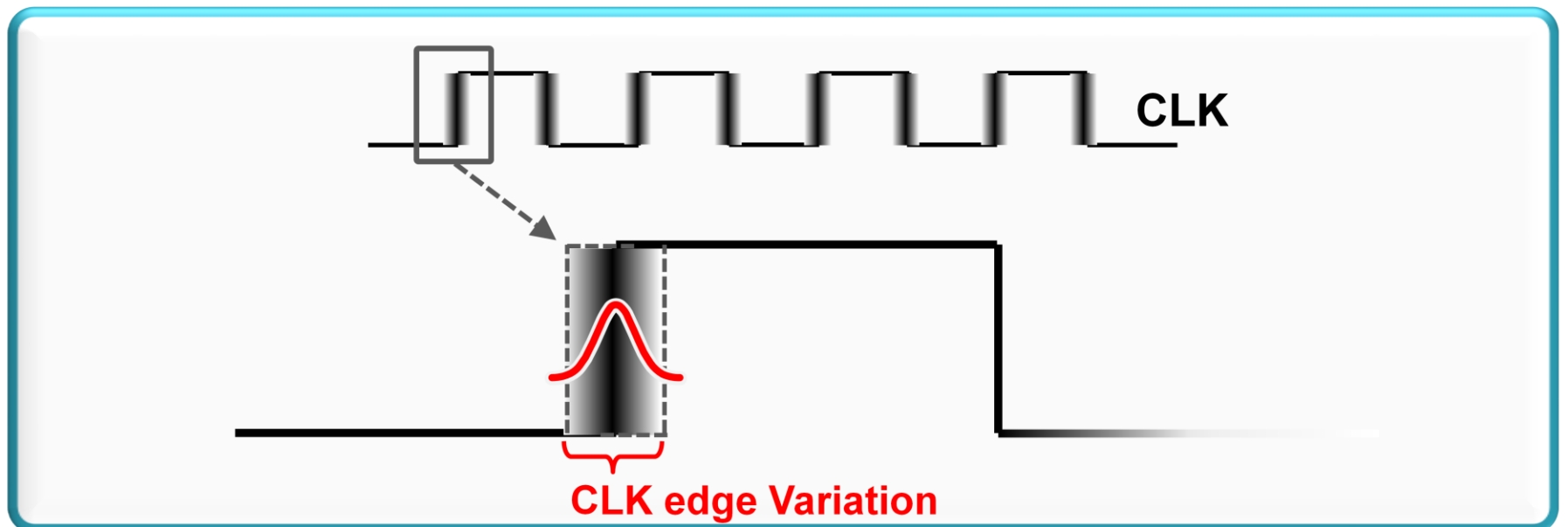
Here we will first define clock jitter and in the next slide, we will see how clock jitter translates to noise in an ADC system.

Clock jitter is random variations in the timing edges of the clock source. Note that this variation has a Gaussian distribution. Depending on the quality of the clock source, this jitter can be minimized. An expensive precision Phase Lock Loop or PLL can limit the jitter to very low levels. Clock jitter errors are mainly limited to AC type errors because the jitter affects the aperture delay in an ADC.

How Clock Jitter Effects ADCs

Voltage Measurement Error

- Data converters use clock edge or CONVST edge to control sample point
  - Deviation in sample point create measurement error
  - Effect: Noise floor of FFT will rise increasing system noise
- Acceptable clock jitter is dependent on:
  - Target SNR
  - Target Fin
  - OSR (Delta-Sigma only)

ΔΣ term only

$$SNR = -20 * \log(2 * \pi * f_{in} * t_{jitter}) + \boxed{10 * \log(OSR)}$$

This slide shows how jitter in the clock can affect the ADC accuracy. In simple terms, the point in time at which the signal is captured will vary from sample to sample. This produces a voltage variation that looks like white noise superimposed on the input signal, shown here as a sine wave. As a result, clock jitter raises the noise floor in an FFT.

Inspecting the formula shows that higher frequency input signals or larger clock jitter increases this error. It makes sense that higher frequency signals are more susceptible to clock jitter as the slope of the waveform you are capturing is more steep, so the error will be greater for a fixed amount of jitter. Also, a larger jitter time clearly introduces more error as well since the conversion result has more time to deviate from the actual value desired sample point.

Finally, the equation at the bottom calculates the best-case signal-to-noise ratio considering only clock jitter. Notice that oversampling has the effect of averaging the jitter out. Thus, the best-case signal-to-noise ratio due to clock jitter is improved by a factor of 10*log(OSR). This is only applicable for delta-sigma converters.

Jitter Sensitivity in SAR vs ΔΣ ADC

SAR SNR vs Jitter

ΔΣ SNR vs Jitter @ OSR = 128

$$SNR = -20 * \log(2 * \pi * f_{in} * t_{jitter})$$

$$SNR = -20 * \log(2 * \pi * f_{in} * t_{jitter}) + 10 * \log(OSR)$$

TEXAS INSTRUMENTS

This slide graphs the signal-to-noise ratio as a function of frequency and jitter. As expected the signal-to-noise ratio gets worse for higher frequency signals, and also for larger clock jitter. Also, you can see that the oversampling ratio shifts the signal-to-noise ratio up by a factor 10*log (OSR).

For lower input signal frequencies, jitter may not be a significant issue. On the other hand, for high frequency devices, jitter may be the fundamental limiting factor to performance. The high-speed data converter video series covers the topic of jitter in great detail. For now, the goal is to emphasize that the delta-sigma converter uses oversampling, so it has some inherent immunity to jitter issues. Typically, most SAR converters do not use oversampling, so the graph on the left is more pertinent to SAR converters.

ΔΣ Oversampling and Noise Shaping

In general, filter order and cutoff frequency limit total noise

Sinc3 digital filter

Noise not rejected by filter

Noise rejected by filter

$F_m/2$
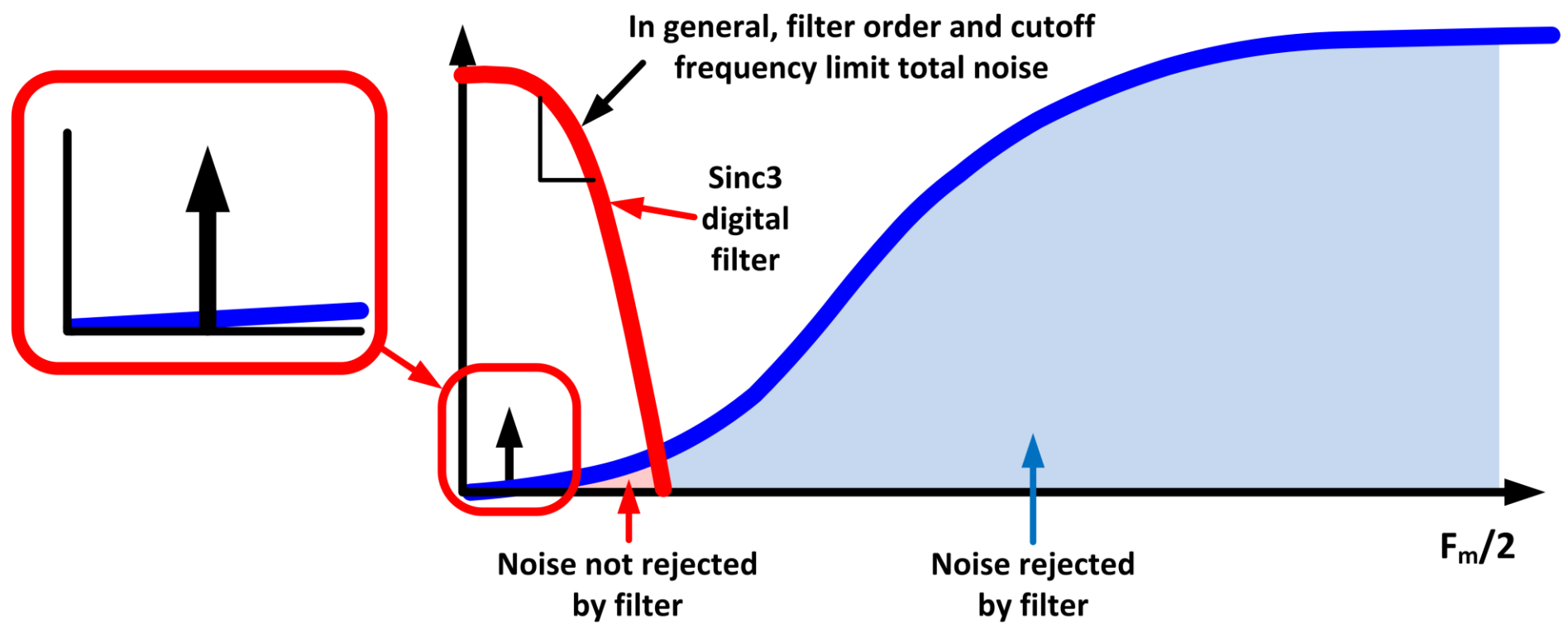
In the previous two videos, we discussed noise shaping and digital filters in detail for delta-sigma converters. Noise shaping minimizes the quantization noise near the signal of interest, and the digital filter eliminates much of the high-frequency noise. This method allows for excellent low-noise performance on delta-sigma converters, but is not a feature used in SAR converters.

In the next slide, we will look at the noise performance for a precision DC optimized delta-sigma converter.

Ultra low noise DC optimized ΔΣ example

ADS1262			
DATA RATE	FILTER MODE	Noise G = 32 (μV_{RMS})	BW -3dB (Hz)
2.5 SPS	FIR	0.011	1.2
2.5 SPS	SINC1	0.008	1.10
2.5 SPS	SINC3	0.006	0.65
10 SPS	FIR	0.023	4.7
10 SPS	SINC1	0.018	4.43
10 SPS	SINC3	0.014	2.62

Figure 91. FIR Frequency Response (10 SPS)

Figure 84. Sinc Frequency Response (10 SPS)

TEXAS INSTRUMENTS

Here we show the noise specifications for the ADS1252 delta-sigma converter. This device uses a low latency filter that is optimized for low frequency or DC inputs. The sampling rates shown in this example are 2.5 SPS and 10 SPS. The table lists the noise levels for three different filter types: FIR, SINC1, and SINC3. The table also shows the associated 3dB bandwidth for each filter.

The main point here is that low bandwidth and high order filters minimize the noise, as you would expect. Also, it should be emphasized that the lowest noise option in this example has a total integrated noise if 6 nVrms. This is incredibly low noise as converters and amplifiers can have total noise in the microvolts range or higher. Of course, this makes sense when you consider that the bandwidth is 0.65Hz. So for this example, the converter is optimized to measure a very low frequency signal with minimal noise error.

Wideband delta-sigma vs. SAR

ADS1675 ΔΣ	
DATA RATE	Noise (μV_{RMS})
125 kSPS	6.17
250 kSPS	7.44
500 kSPS	9.66
1000 kSPS	12.99
2000 kSPS	18.64
4000 kSPS	44.02

ADS8900B SAR	
DATA RATE	Noise (μV_{RMS})
0 to 1000kSPS	23

ADS1675 ΔΣ	
DATA RATE	SNR (dB)
125 kSPS	107
2000 kSPS	97
4000 kSPS	92

ADS8900B SAR	
DATA RATE	SNR (dB)
250 kSPS	104.5
500 kSPS	104.5
1000 kSPS	104.5

Noise wideband ΔΣ vs SAR
- ΔΣ uses noise shaping and digital filter to reduce noise
- ΔΣ digital filter bandwidth is adjusted to match data rates
- SAR has same noise for all sampling rate (no digital filter)
- SNR for ΔΣ will depend on sampling rate, OSR, and filter. SNR for SAR is not dependent on sampling rate

TEXAS INSTRUMENTS

Here we compare and contrast a SAR converter with a wide bandwidth delta-sigma converter. It would not make sense to compare the last example to a SAR as a SAR would never have it's bandwidth limited to just a few hertz. On the other hand, the wide bandwidth delta-sigma converter will have more similar specifications and applications to the SAR.

First, notice that the noise for the ADS1675 delta-sigma converter scales with data rate. This is because the associated digital filter will also adjust with data rate. For this example, the data rate ranges from 125kSPS to 4000kSPS and the associated noise ranges from 6 uVrms to 44 uVrms.

Notice that the SAR sampling rate can be adjusted from 0 to 1000kSPS, but it's associate noise is a constant 23uVrms regardless of the sampling rate. This is because the SAR does not have an integrated digital filter, and any noise on the input will alias back into the Nyquist band, regardless of the sampling rate.

At the bottom of the slide, you can see the same phenomena with signal-to-noise ratio or SNR. Since noise for the delta-sigma converter scales with data rate, so does SNR. Conversely, for the SAR, the SNR is constant and independent of the data rate.

Quantization Noise vs. Thermal Noise
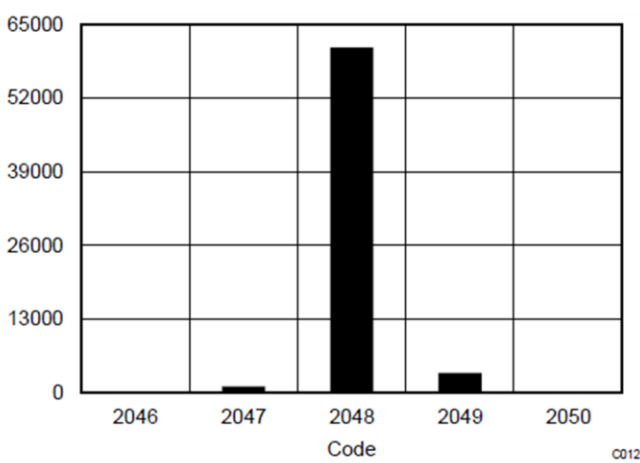
**Quantization Noise
Dominant
ADS7042, SAR
12 Bit, 1MSPS**
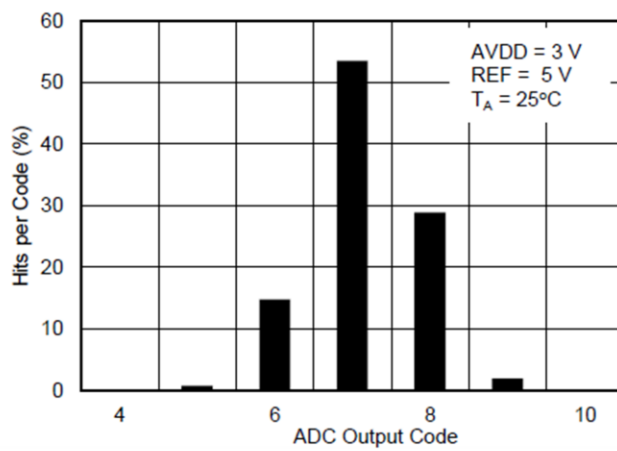
**Both Thermal Noise
& Quantization Noise
ADS8881, SAR
18 Bit, 1MSPS**

**Thermal Noise
Dominant
ADS1675, $\Delta\Sigma$
24 Bit, 125kSPS**

TEXAS INSTRUMENTS

In general, the ADC noise will be a combination of thermal and quantization noise. The DC input histogram is a good indication of which noise source is dominate in a particular a device.

A single column in the histogram indicates that the device is dominated by quantization noise, as shown on the left. A Gaussian distribution in the histogram indicates that the device is dominated by thermal noise, as shown on the right.

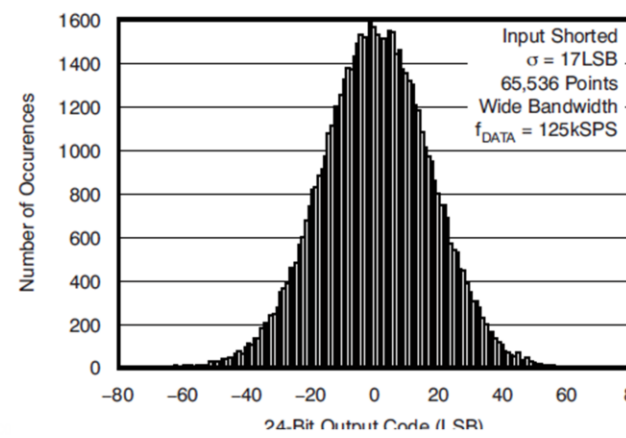For low resolution devices, the LSB size is relatively large compared to any thermal noise, so low resolution devices tend to be dominated by quantization noise. The example shown on the left is a 12-bit SAR converter, but delta-sigma converters with resolution less than 16 bits will also be dominated by quantization noise.

For intermediate resolution devices, the noise will be a mixture of both thermal and quantization noise. SAR converters will often fall into this category.

High resolution devices tend to be dominated by thermal noise. This is especially true for wideband devices as the noise is not limited by a filter. This example shows a wide bandwidth delta-sigma converter, and you can see that the noise clearly follows a Gaussian distribution, so the device is dominated by thermal noise. Note that a DC optimized delta-sigma running at a very low sampling rate may have very low thermal noise, so the histogram would show a combination of thermal and quantization noise similar to the graph in the middle.

Introducing ΔΣ and SAR ADC drive considerations

- When is the reference buffer needed?
- When is the driver Amp needed?
- How do SAR and ΔΣ differ

Voltage Reference

ADC

AIN_P

AIN_M

Vin

Vcm

V_{OCM}

5V

THS4521

TEXAS INSTRUMENTS
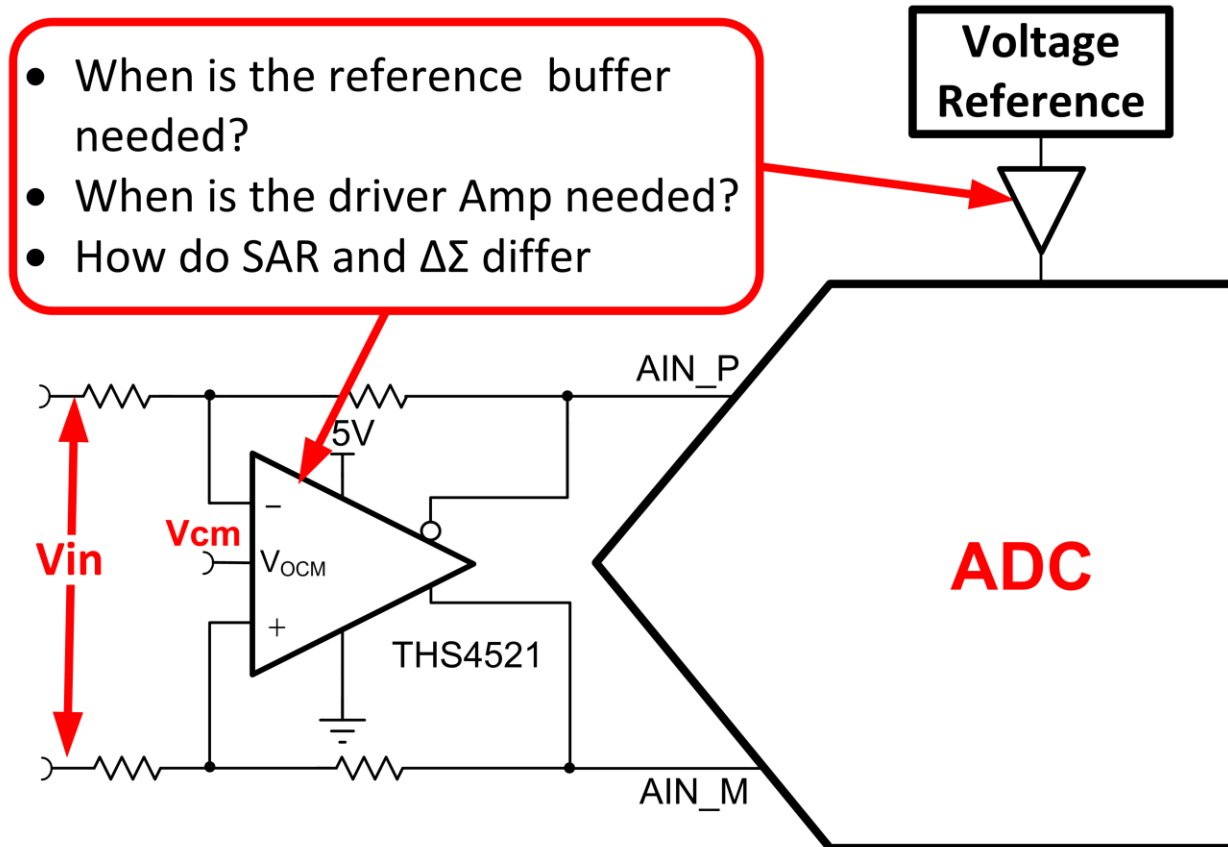
Now that we have covered noise, let's move on to an new topic. In this section we will consider when amplifiers are required to drive the input of ADCs and to buffer the voltage reference input. Here we are just providing a brief overview and later we have multiple videos covering this topic in great detail. The goal here is to provide some general insight into how drive requirements may differ between SAR and delta-sigma converters.

Direct Drive vs. Buffered
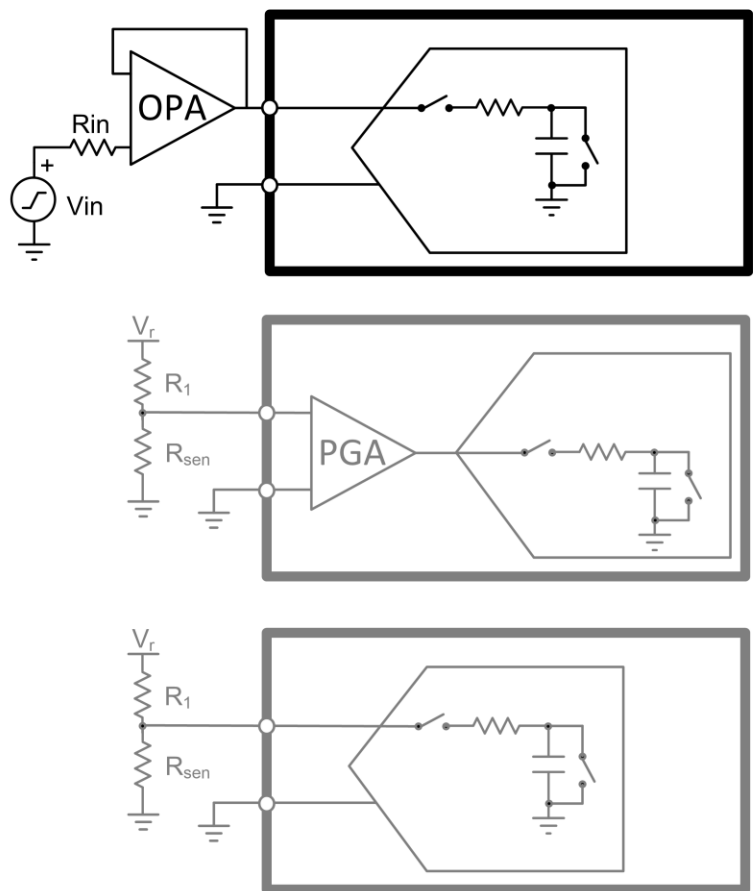
External Buffer
- Buffer is normally needed for high sampling rates to quickly and accurately charge the sample and hold capacitor to its final value.
- Amplifier may be used to attenuate or amplify a signal to match the input range.
- Match impedances

First let's consider the options for connecting signals to an ADC. The figure at the top of the slide illustrates the case where an external amplifier is used to buffer the ADC input. The amplifier is often used for wide bandwidth SAR and delta-sigma applications, where it is needed to absorb the charge kickback from the internal switch-capacitor sampling circuit. Amplifiers may also be used in cases where the input signal chain needs to attenuate or amplify the sensor output to match it to the ADC input range. Finally, the amplifier can help to increase the input impedance to match high impedance sensors.

Direct Drive vs. Buffered
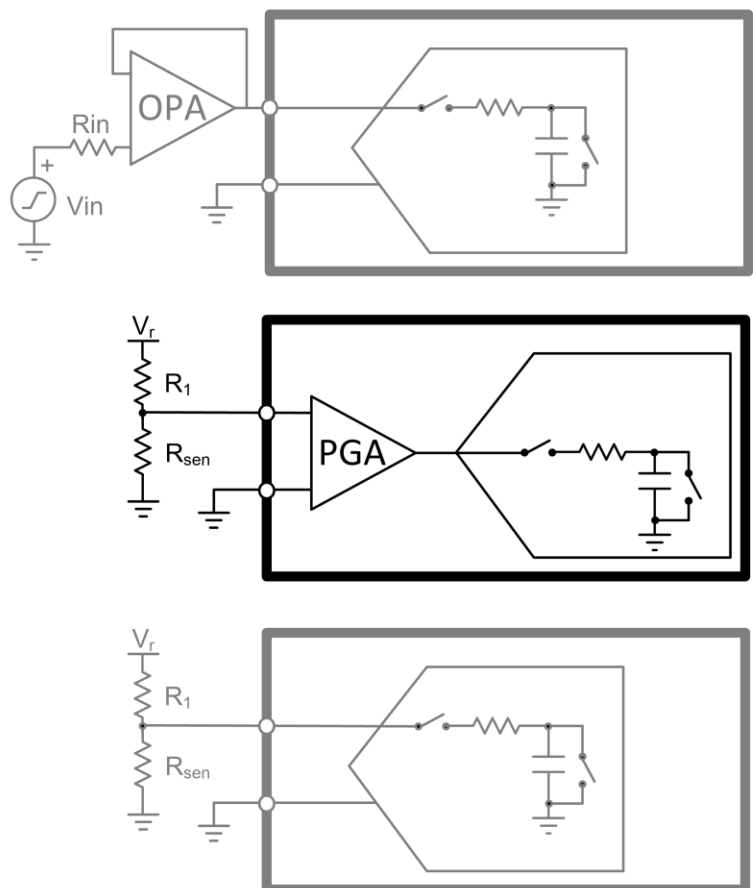
Integrated PGA
- Integrated PGA can be used in place of external amplifier (generally on ΔΣ)
- Typically the wide bandwidth applications use external amplifiers.

The next case to consider is where a programmable gain amplifier, or PGA, is integrated into the ADC. In this case, the external amplifier is not needed. The integrated PGA is very common in delta-sigma converters, but can be found on some SAR converters as well. Typically, this kind of internal feature is used for the lower bandwidth applications, while wide bandwidth applications use discrete external amplifiers.

Direct Drive vs. Buffered
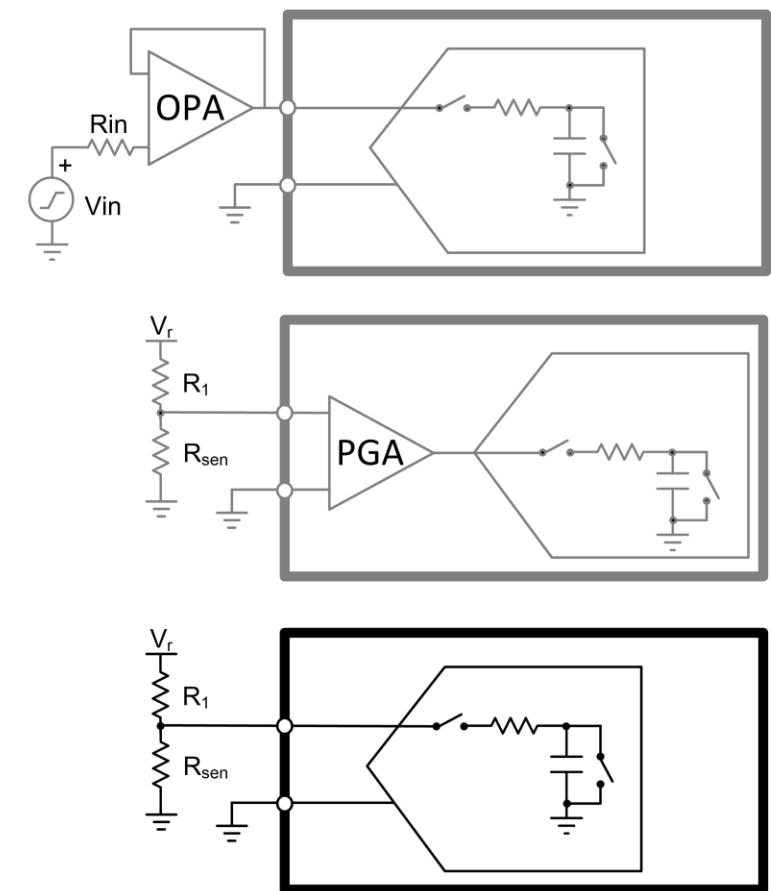
Direct Drive
- Direct drive can be used a lower sampling rates
- For direct drive, the external sensor impedance will impact the sample and hold settling.

The last case is where the data converter does not have an integrated PGA, but the sensor is directly connected to the switch-capacitor input. Both SAR and delta-sigma converters can use this approach. Typically this is used for low frequency applications. In this case the internal switch-capacitor circuit will need to charge up and settle through the source impedance of the sensor.

All three methods are valid approaches and will be used according to the system bandwidth, and sensor specifications. Let's take a closer look at the first case, and compare SAR and delta-sigma requirements.

Buffered – what bandwidth is required?
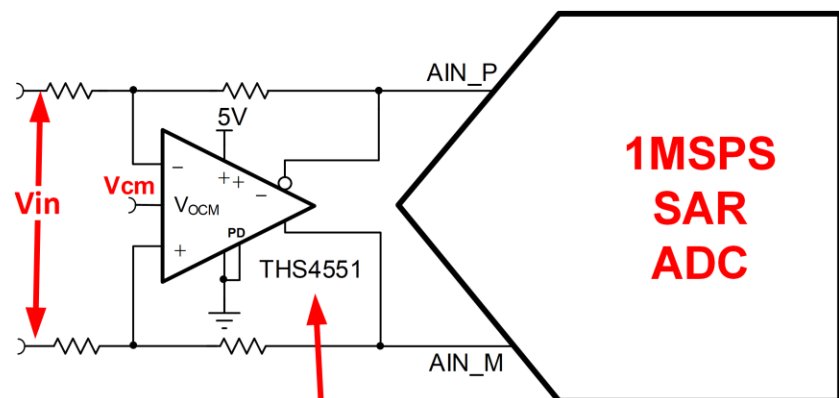
THS4551
- BW = 150MHz
- Iq = 1.35mA
- Vos = 175µV, ΔVos/ΔT = 1.8µV/C
- Ib = 1µA

THP210
- BW = 9.2MHz
- Iq = 0.95mA
- Vos = 40µV, ΔVos/ΔT = 0.35µV/C
- Ib = 2nA

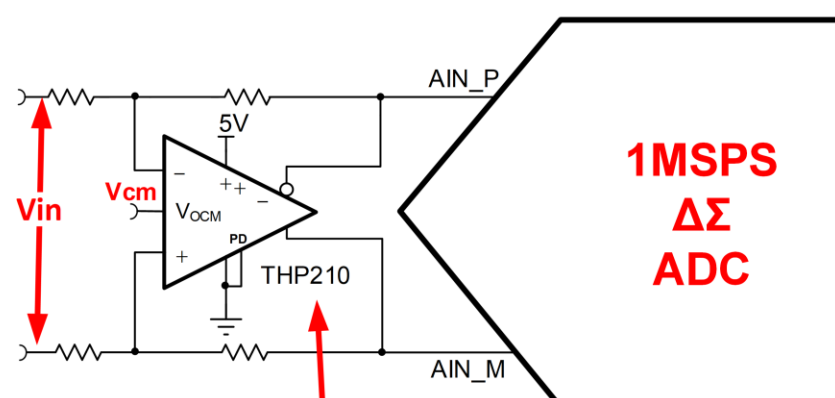Here we compare a wide bandwidth delta-sigma converter to a SAR converter. Both cases require an external amplifier to drive the switch-capacitor input. Frequently, this external amplifier needs to have a bandwidth substantially wider than the sampling rate for best performance.

In the example on the left, the SAR converter uses a fully differential amplifier with a 150-MHz bandwidth, even though the sampling rate is only 1 MSPS. This is not unusual as the switch-capacitor input to the SAR has transients that are much faster than the 1-MHz sampling rate.

Some wide bandwidth delta-sigma converters, on the other hand, may use an internal "pre-charge" buffer that helps to alleviate the some of the charge kickback. This type of configuration may still require an external amplifier, but the bandwidth requirement can be substantially reduced. This isn't always the case, and you need to consult the device data sheet to see what the requirements are. Again, this topic is covered in detail in later videos.

Reference buffered required?
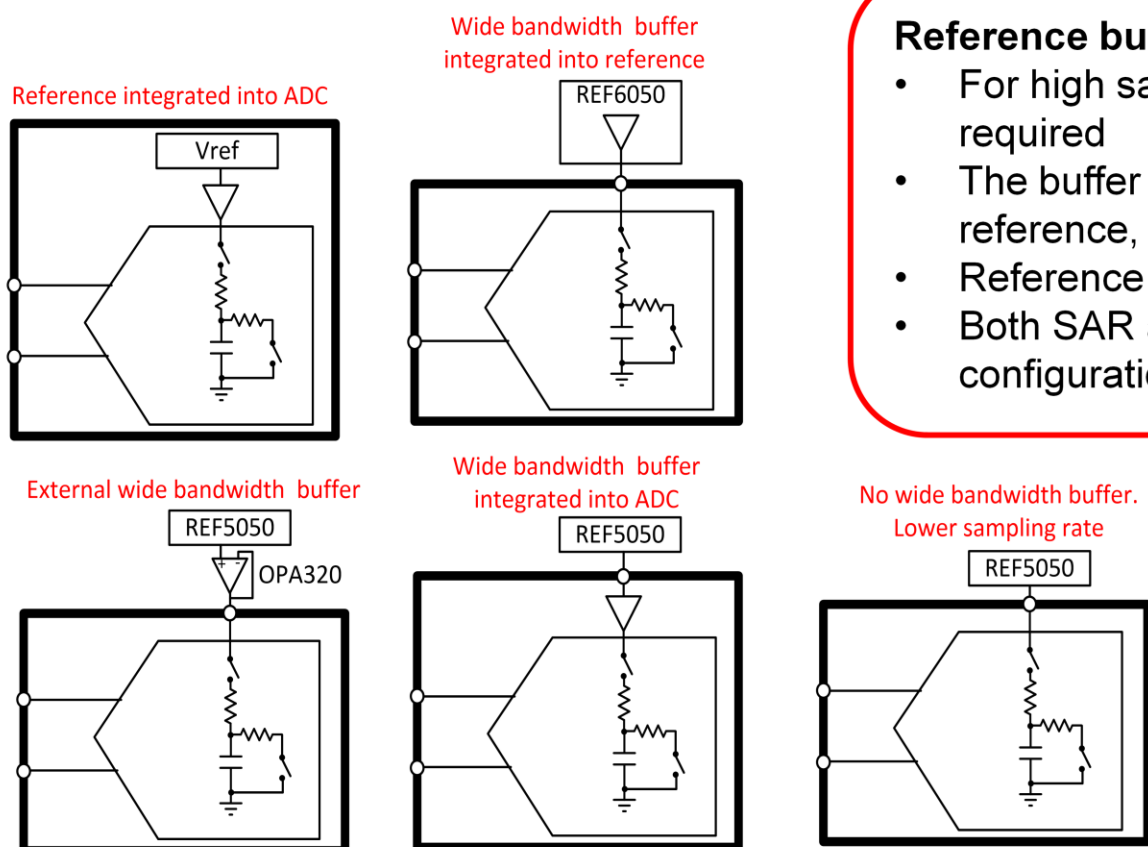
Reference integrated into ADC

Wide bandwidth buffer integrated into reference
REF6050

Reference buffer requirement
- For high sampling rates, a wide bandwidth may be required
- The buffer may be external, integrated in the reference, or integrated in the ADC.
- Reference buffer is not required for low sampling rates
- Both SAR and $\Delta\Sigma$ will both use direct drive or buffered configurations.

External wide bandwidth buffer
REF5050
OPA320

Wide bandwidth buffer integrated into ADC
REF5050

No wide bandwidth buffer. Lower sampling rate
REF5050

The last topic to discuss is the reference buffer requirement. This figure shows the different ways that an external voltage reference can be driven. For higher sampling rates, a wide bandwidth buffer is often required to drive the switch-capacitor circuit on the ADC reference input pin. This buffer may be integrated in the reference IC, like the REF6050 in the second image. However, most voltage references do not include an integrated wide bandwidth buffer.

For reference ICs without an integrated buffer, an external discrete amplifier can be used next to the ADC reference input, as shown in the bottom-left.

A third option is to use an ADC with an integrated reference buffer, as shown in the bottom-center.

For lower sampling rates, a typical low bandwidth voltage reference will work without a buffer. This reference input requirement may be important for both SAR and wide bandwidth delta-sigmas. Reviewing the applications section in the ADC data sheet will show if a wide bandwidth reference buffer is recommended for that particular device.

Thanks for your time! Please try the quiz.

That concludes this theory part of the video – thank you for your time! Keep watching to try the quiz and check your understanding of this video's content.

Questions: SAR & Delta-Sigma Introduction

1. (T/F) SAR converters commonly have digital filters that can be used to reject 60Hz noise.
   a. True
   b. **False**

2. (T/F) A simple first-order RC filter can be used for the delta-sigma anti-aliasing filter, but a more complex active filter is typically required for SAR.
   a. **True**
   b. False

TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

Question 1: True or False. SAR converters commonly have digital filters that can be used to reject 60Hz noise.

- The answer is false. SAR converters do not contain digital filters, only delta-sigma converters do.

Question 2: True or False. A simple first order RC filter can be used for the delta-sigma anti-aliasing filter, but a more complex active filter is typically required for SAR.

- The answer is true. Again – unlike a SAR converter, a delta-sigma converter has an integrated digital filter, which relaxes the antialiasing filter requirements.

Questions: SAR & Delta-Sigma Introduction

3. (T/F) Clock jitter acts as a noise source. The impact of this noise source does not depend on the input signal frequency.
   a. True
   b. False

4. (T/F) Oversampling can be used to reduce clock jitter noise.
   a. True
   b. False

Question 3: True or False. Clock jitter acts as a noise source. The impact of this noise source does not depend on the input signal frequency.

- The answer is false. The higher the input signal frequency, the larger the noise due to clock jitter will be.

Question 4: True or False. Oversampling can be used to reduce clock jitter noise.

- The answer is true. The oversampling or averaging performed by the digital filter in a delta-sigma converter can improve noise performance by a factor of 10*log(OSR).

Questions: SAR & Delta-Sigma Introduction

5. The ____ converter typically has lower noise for lower sampling rates.
   a. Delta-Sigma
   b. SAR
   c. Both Delta-Sigma and SAR have lower noise for lower sampling rates.

6. An input buffer may be required to _____.
   a. Scale the input level
   b. Match impedances
   c. Drive the input sample and hold for accurate settling
   d. All of the above
   e. Option a and b are correct

TEXAS INSTRUMENTS

Question 5: The _blank_ converter typically has lower noise for lower sampling rates. Is it

    a) Delta-Sigma
    b) SAR
    c) Both Delta-Sigma and SAR have lower noise for lower sampling rates.

The answer is a). The noise of a delta-sigma converter reduces with sampling rate, while the noise of a SAR converter remains constant due to aliasing.

Question 6: An input buffer may be required to _blank_.
    a) Scale the input level
    b) Match impedances
    c) Drive the input sample and hold for accurate settling
    d) All of the above
    e) Option a and b are correct

The answer is d). An input buffer can be used to achieve all of the above.

This slide should be leveraged for external recordings. Leave on screen for 5 seconds.