Linear Regulator Fundamentals

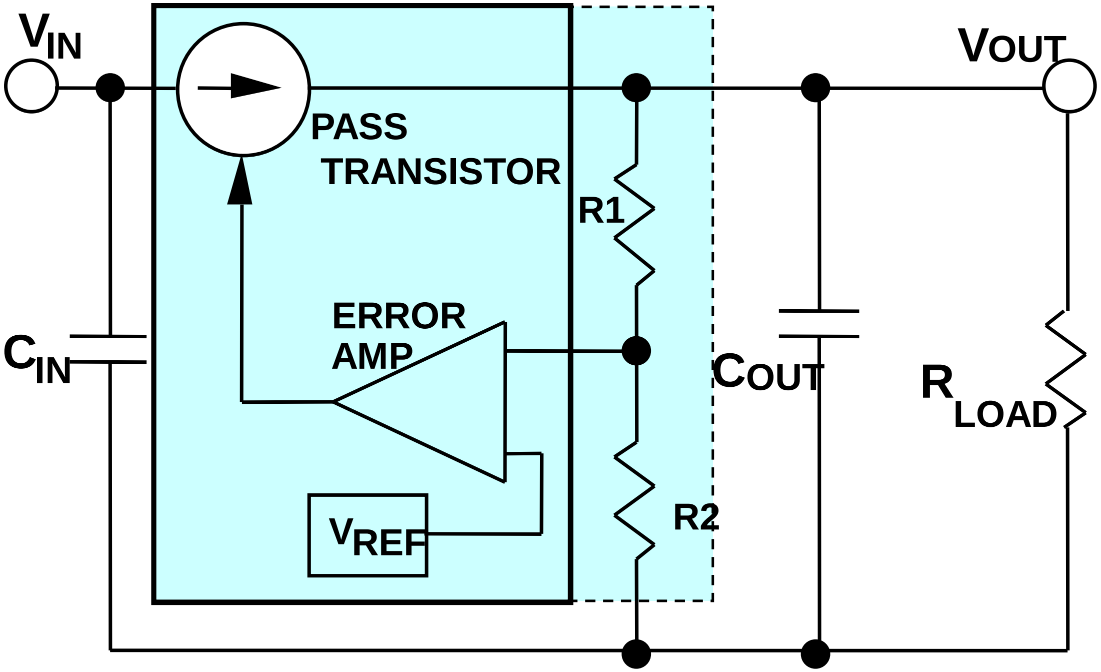
2.1 Types of Linear Regulators

What is a Linear Voltage Regulator

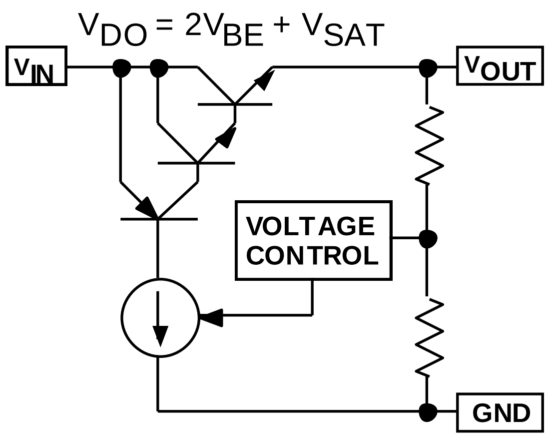
- A linear regulator operates by using a voltage-controlled current source to force a fixed voltage to appear at the regulator output terminal. The control circuitry continuously monitors (senses) the output voltage, and adjusts the current source (as required by the load) to hold the output voltage at the desired value.
- The design limit of the current source defines the maximum load current the regulator can source and still maintain regulation.
- The output voltage is controlled using a feedback loop, which requires some type of compensation to assure loop stability. Most linear regulators have built-in compensation, and are completely stable without external components.
- Some regulators (like Low-Dropout types), do require some external capacitance connected from the output lead to ground to assure regulator stability.

Linear-Regulator Operation

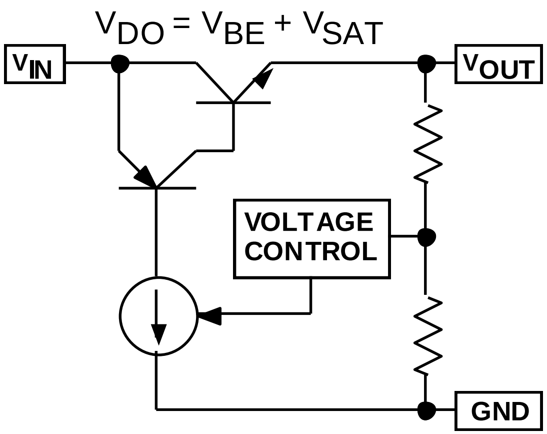
- Voltage feedback samples the output R1 and R2 may be internal or external
- Feedback controls pass transistor's current to the load



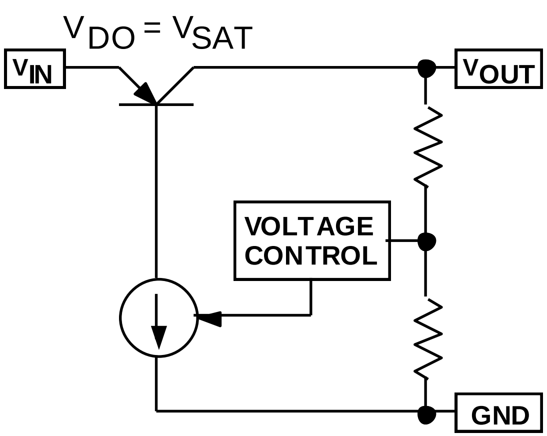
Linear-Regulator Topologies



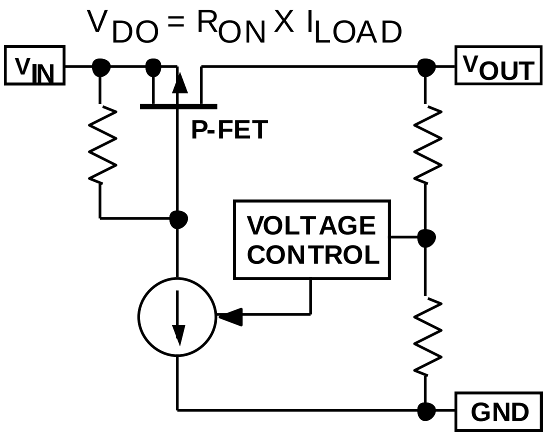
NPN DARLINGTON



NPN QUASI-LDO



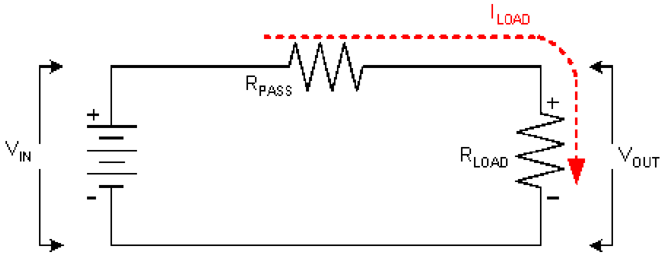
PNP LDO



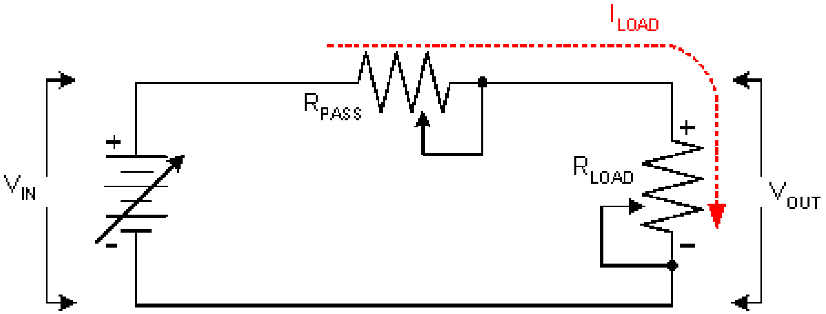
P-FET LDO

Simple Model

- A basic (first order) linear voltage regulator can be modeled with two resistors and a power supply for V_{IN}.

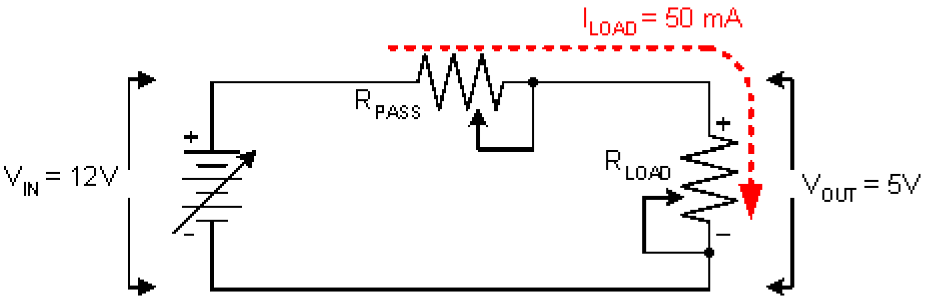


- In reality, the only constant is the output voltage, V_{OUT}. Everything else can, and will, be constantly changing.
- The input voltage may have changes due to outside influences, the load current may change due to a dynamic change in the behavior of the load.
- Changes in these variables can all happen simultaneously, and the value needed for R_{PASS} to hold V_{OUT} at a constant value will need to change as well.



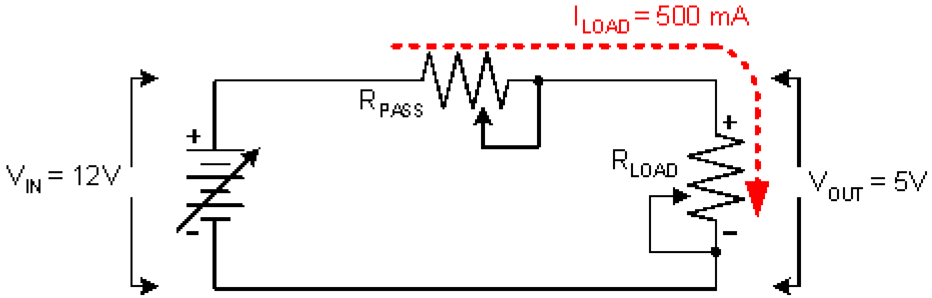
Simple Model with Values

- For the first example, we will assign typical operating values and calculate the value needed for the series pass element R_{PASS}.
  - V_{IN} = 12V
  - V_{OUT}= 5V
  - I_{LOAD} = 50 mA
- With V_{IN} = 12V and V_{OUT} = 5V, the voltage across R_{PASS} = (12V - 5V) = 7V
- With the current through R_{PASS} = I_{LOAD} = 50 mA, the needed resistance for R_{PASS} = (7V / 50mA)= 140 Ohms



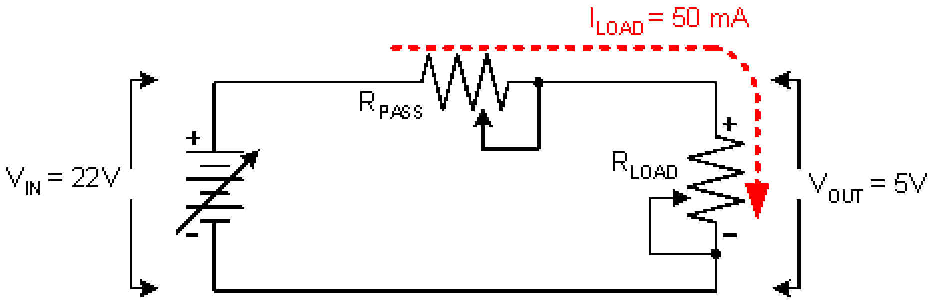
Simple Model with Change of Load Current

- For the second example, we will change the load current from 50mA to 500mA and calculate the value needed for the series pass element R_{PASS}.
  - V_{IN} = 12V
  - V_{OUT} = 5V
  - I_{LOAD} = 500 mA
- With V_{IN} = 12V and V_{OUT} = 5V, the voltage across R_{PASS} = (12V - 5V) = 7V
- With the current through R_{PASS} = I_{LOAD} = 500 mA, the needed resistance for R_{PASS} = (7V / 500mA)= 14 Ohms



Simple Model with Change in Input Voltage

- For the third example, we will change the input voltage from 12V to 22V and calculate the value needed for the series pass element R_{PASS}.
  - V_{IN} = 22V
  - V_{OUT} = 5V
  - I_{LOAD} = 50 mA
- With V_{IN} = 22V and V_{OUT} = 5V, the voltage across R_{PASS} = (22V - 5V) = 17V
- With the current through R_{PASS} = I_{LOAD} = 50 mA, the needed resistance for R_{PASS} = (17V / 50mA) = 340 Ohms



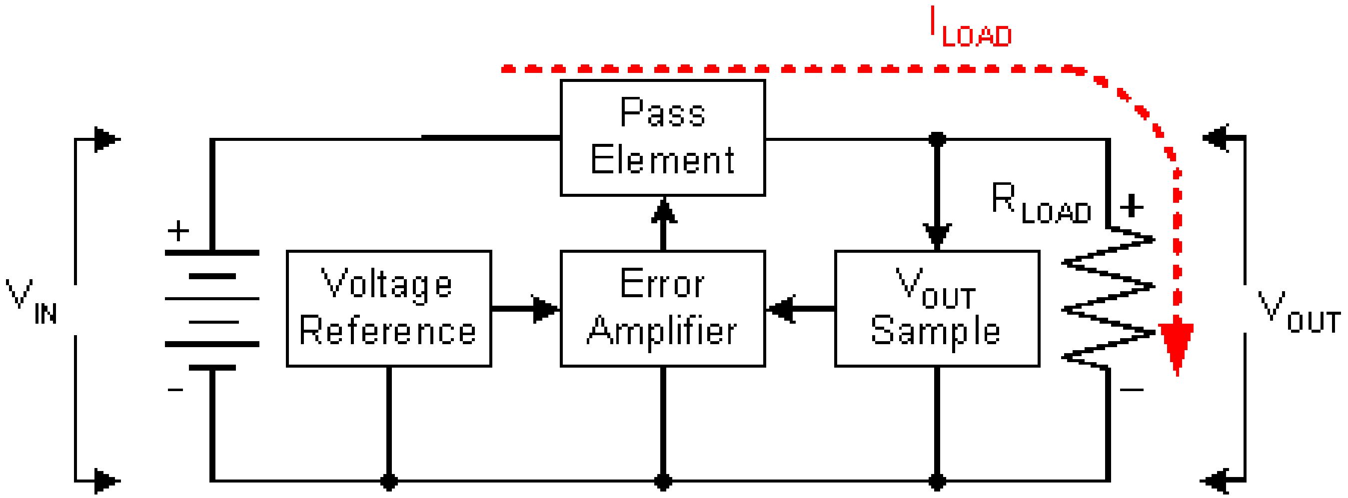
The Control Loop

- It has been shown that the resistance of series pass element, R_{PASS}, needs to change as the operating conditions change.
- This is accomplished with a control loop.
- The error amplifier monitors the sampled output voltage, compares it to a known reference voltage, and actively changes R_{PASS} to keep V_{OUT} constant.
  - A characteristic of any linear voltage regulator is that it requires a finite amount of time to "correct" the output voltage after a change in load current demand.
  - This "time lag" defines the characteristic called transient response, which is a measure of how fast the regulator returns to steady-state conditions after a load change

Simple Model, with Control Loop Blocks

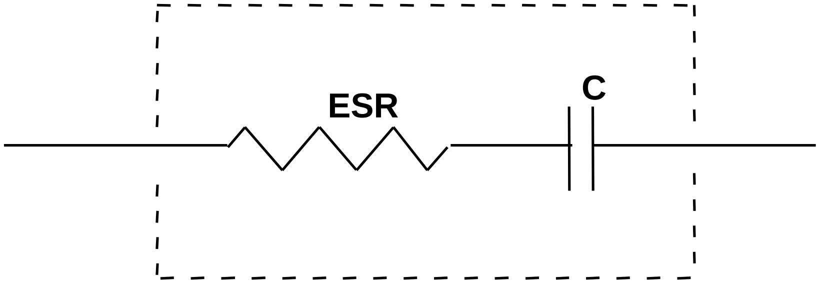
- Here 'simple' blocks have added to show the four basic divisions of any linear voltage regulator:

  1) Series Pass Element
  2) Error Amplifier
  3) VOUT Sampling Network
  4) Reference Voltage



Adding A Zero To The LDO Loop

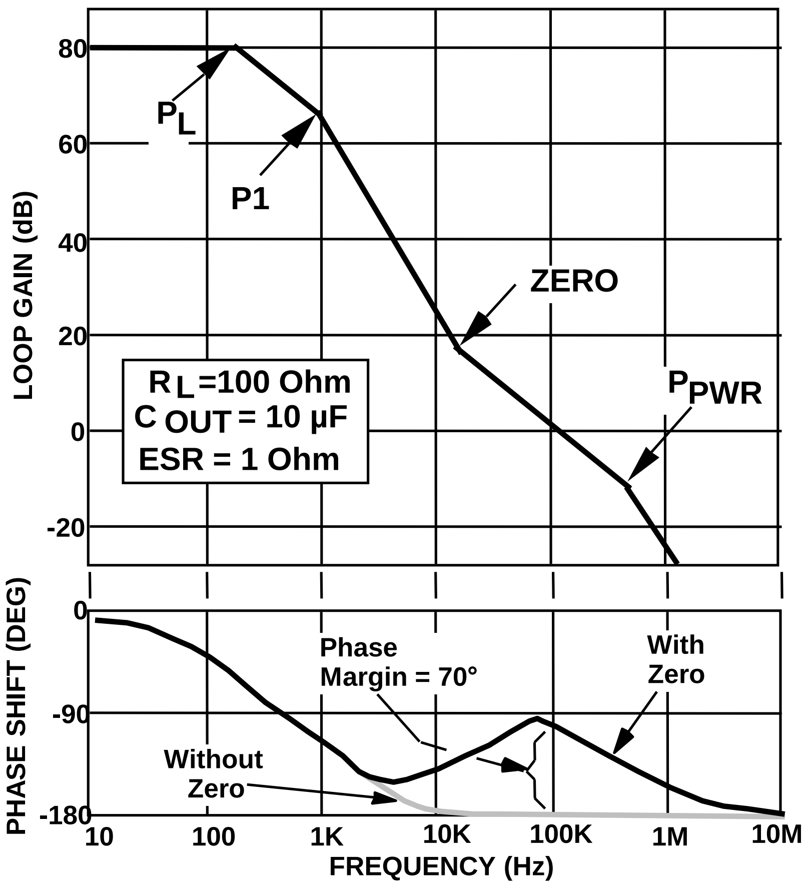
- All capacitors have an equivalent series resistance (ESR)
- The ESR adds a zero to the LDO loop whose frequency is:
  - $F_{ZERO} = 1/(2\pi \times C_{OUT} \times ESR)$
- The zero adds positive phase shift that can compensate for one of the two low-frequency poles in the LDO loop



CAPACITOR SHOWING ESR

Stabilizing the LDO Using C_{OUT} ESR

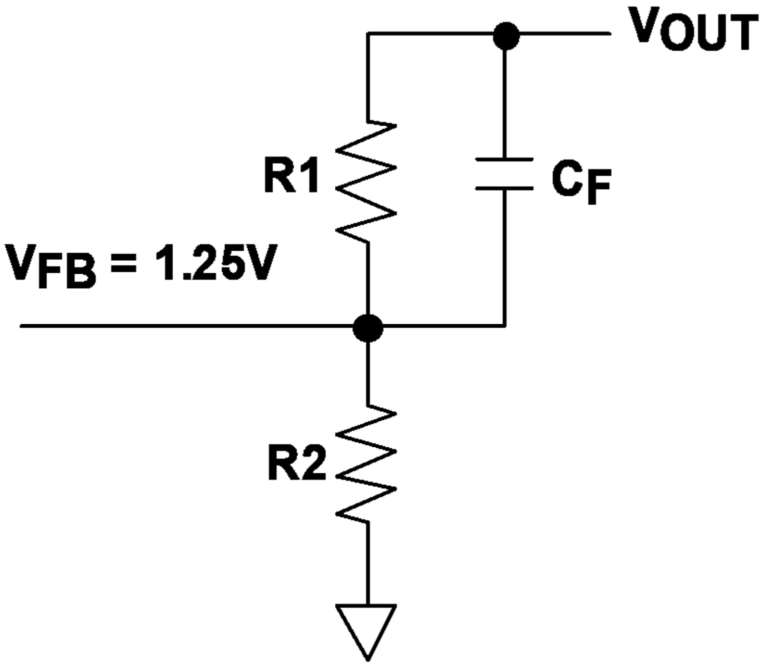
- When the output capacitor ESR is 1Ω, it adds a zero at 16 kHz
- The zero adds about +81° of positive phase shift @ 0 dB
- The zero brings the total phase shift @ 0 dB back to -110°
- The phase margin is increased to +70°, so the loop is stable



ESR ZERO STABILIZES LDO

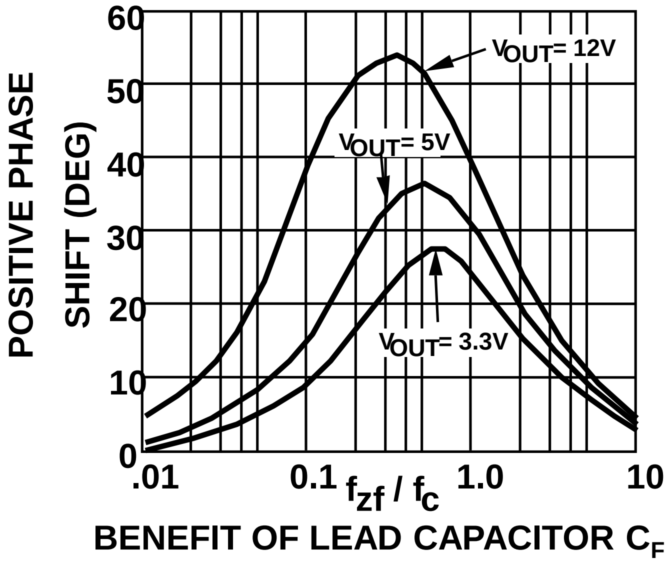
Phase Lead From Feed-Forward Capacitor

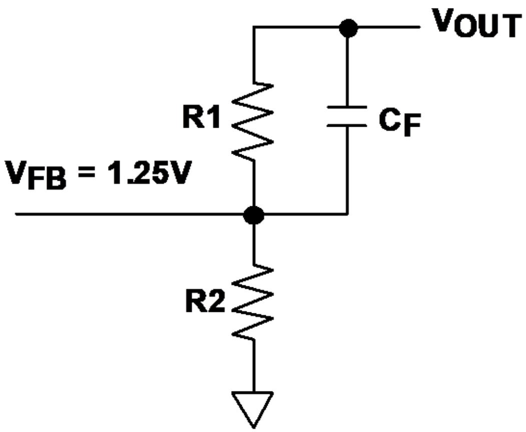
- CF and R1 form a zero:
  - $FZ = 1 / (2\pi \times R1 \times C_F)$
- Unfortunately, they also create a pole:
  - $FP = 1 / (2\pi \times R1//R2 \times C_F)$



C_F Positive-Phase Lead vs. V_{OUT}

- Maximum possible phase lead depends on:
  - V_{OUT}/V_{FB} ratio
  - Placement of zero frequency F_Z with respect to unity gain



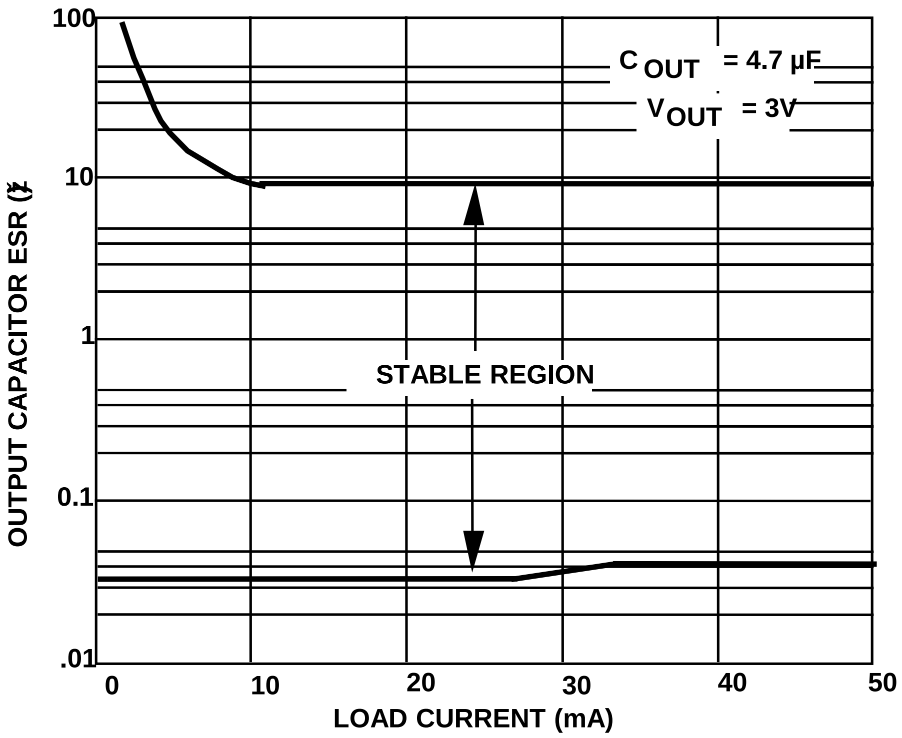


De-Stabilizing the LDO Loop: How to Build an Oscillator

- What is the most common reason why an LDO oscillates? THE OUTPUT CAPACITOR!
  - 1. ESR too high
    - Poor quality tantalum capacitors can have a high ESR
    - An aluminum electrolytic will have a high ESR at cold temperatures
  - 2. ESR too low
    - Many surface-mount ceramic capacitors have very low (<20 mW) ESRs
    - Tantalum, OSCON, SP, POSCAP, film capacitors all have low ESRs

The Stable Range for ESR

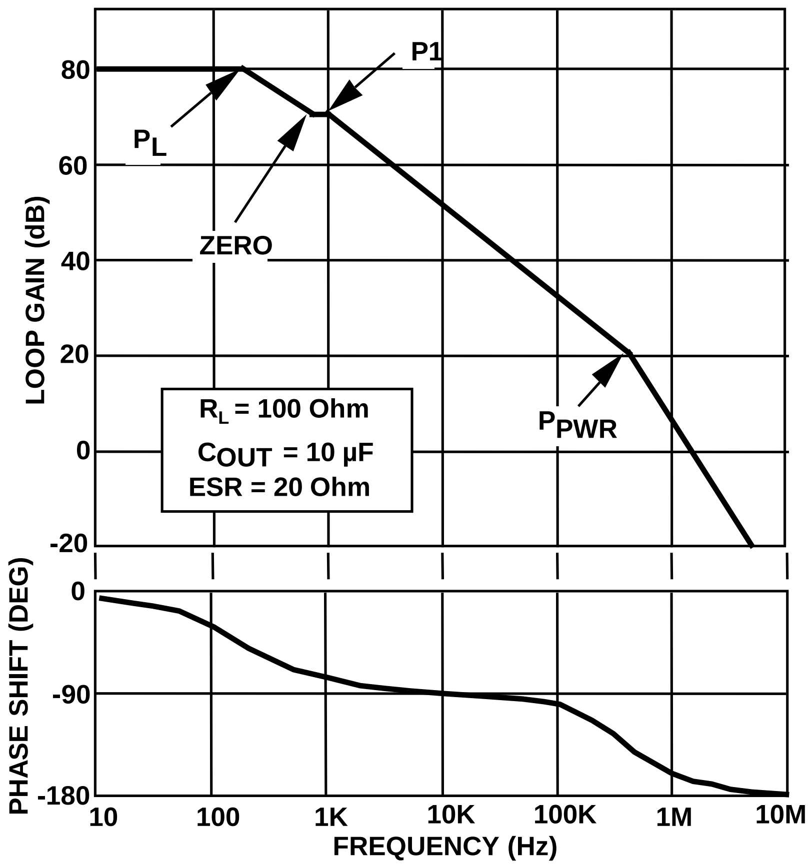
- ESR must be within the min/max range specified by the manufacturer to assure stability



ESR RANGE FOR LP2982

Why High ESR Makes an LDO Unstable

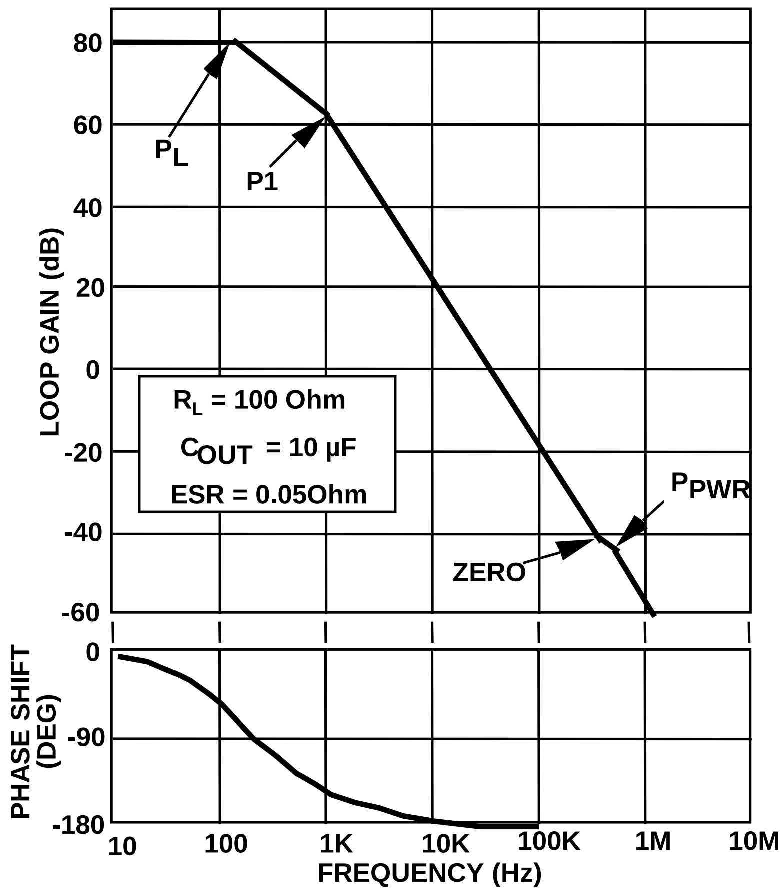
- High ESR moves the zero to a lower frequency
- This increases the loop bandwidth, allowing the pole P_{PWR} to add more phase shift before the 0 dB frequency
- Phase shift from other high frequency poles (not shown) makes ESR values >10W generally unstable



HIGH ESR CAUSES UNSTABLE LOOP

Why Low ESR Makes an LDO Unstable

- Low ESR moves the zero to a higher frequency
- The zero occurs more than a decade higher than the 0 dB frequency
- Because the zero adds no positive phase shift at 0 dB, the two low-frequency poles cause the phase shift to reach -180° (unstable)



LOW ESR CAUSES UNSTABLE LOOP

Thank you!