PCB Design for Accurate Gauging

Assuring Accuracy and Improving EMI and ESD Performance

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PCB Design for Accurate Gauging

Issue:

- Battery packs are used in many different applications and almost every environmental condition imaginable.
  - Computers
  - Handheld devices
  - Power tools
  - Transportation
  - Commercial
  - Industrial
  - Medical
  - Military
  - Hot or Cold
  - Arid or Wet
- They are also handled by untrained individuals who may not know that electronic components are susceptible to ESD damage. e.g kids and teenagers

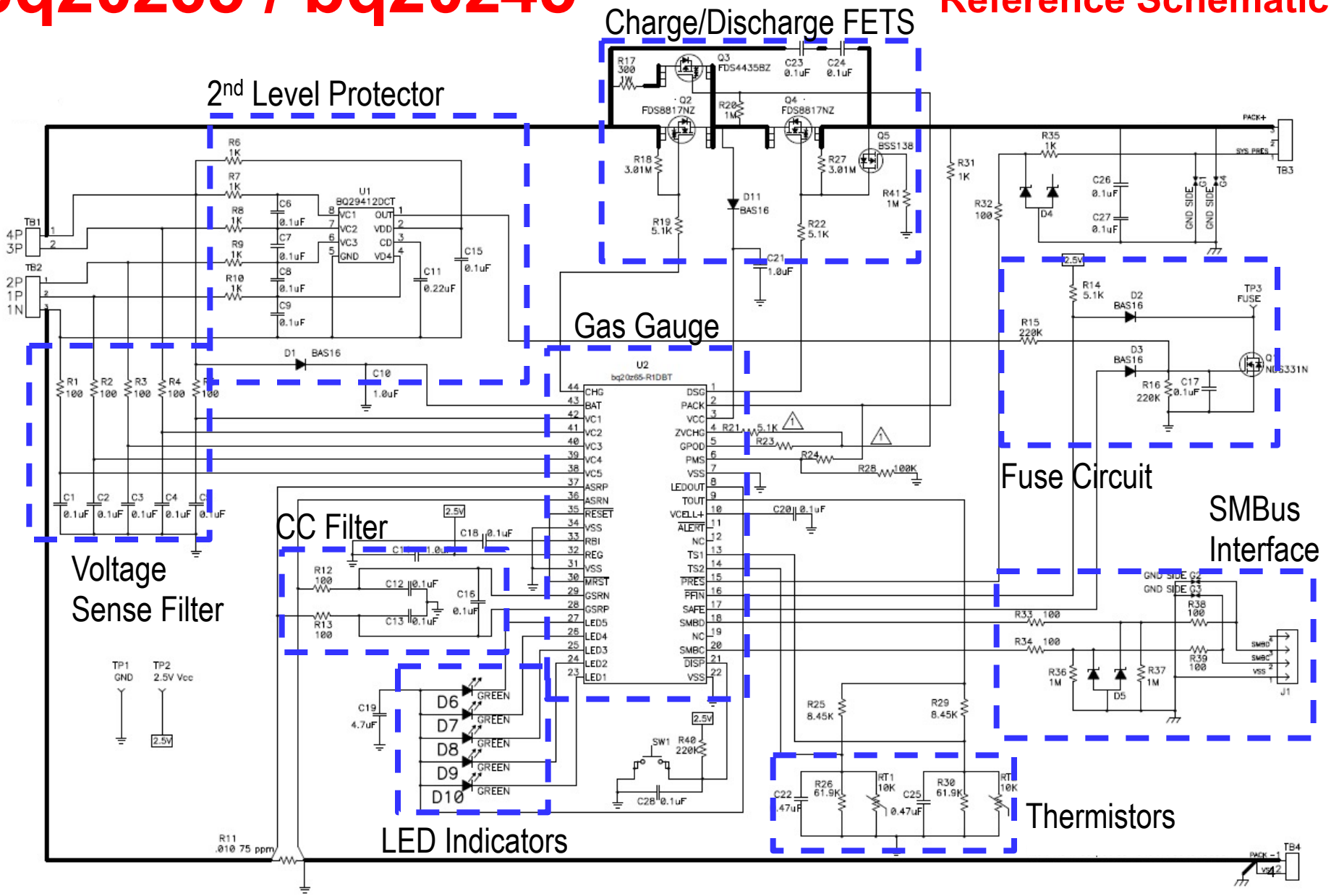
Action:

- The Gas Gauge and Cell Protection devices serve vital functions in managing the battery and protecting it from damage.
- The pack designer must take care to design the hardware to protect the pack in the conditions where it will be used.

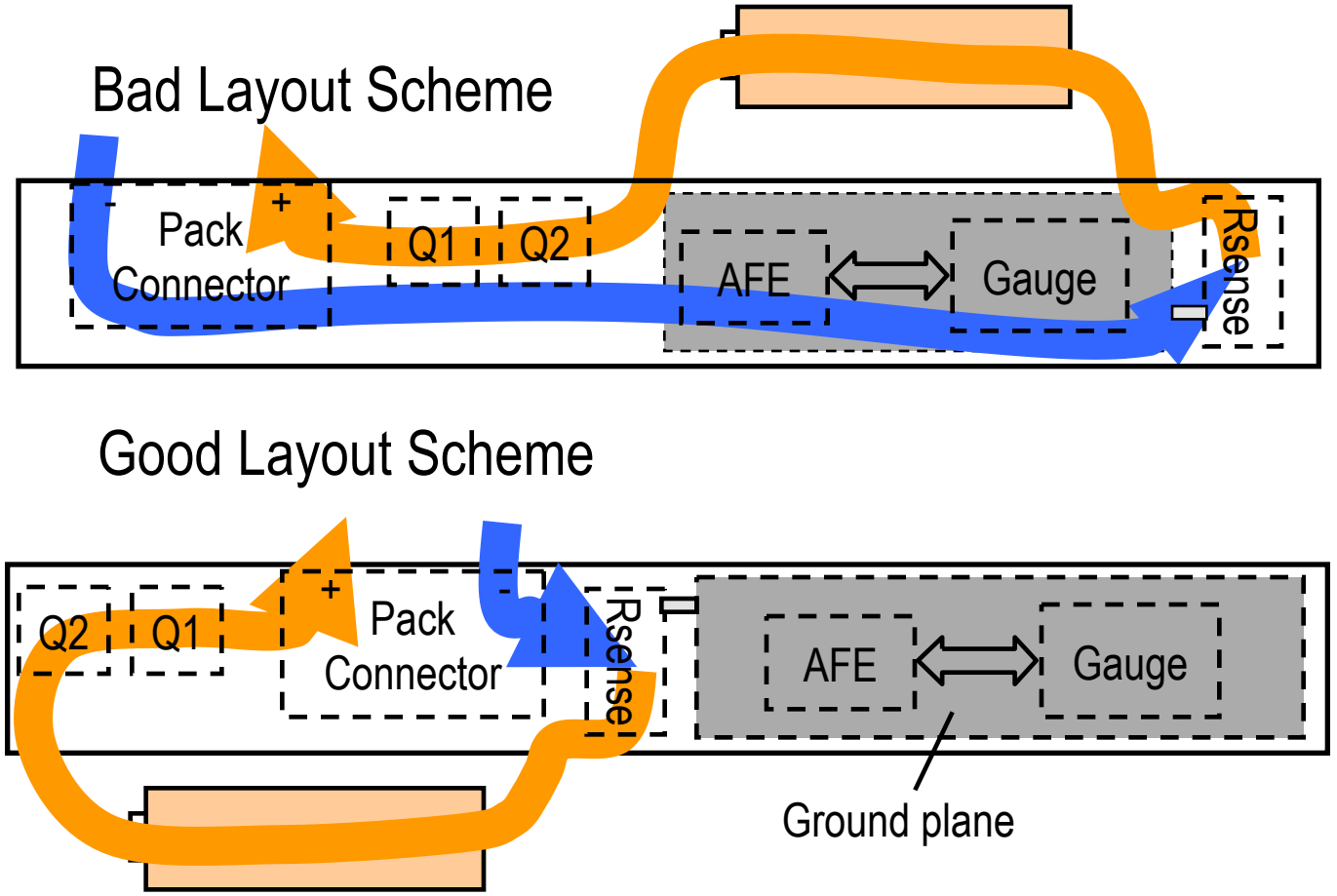
Assuring Accuracy

bq20z65 / bq20z45

Reference Schematic

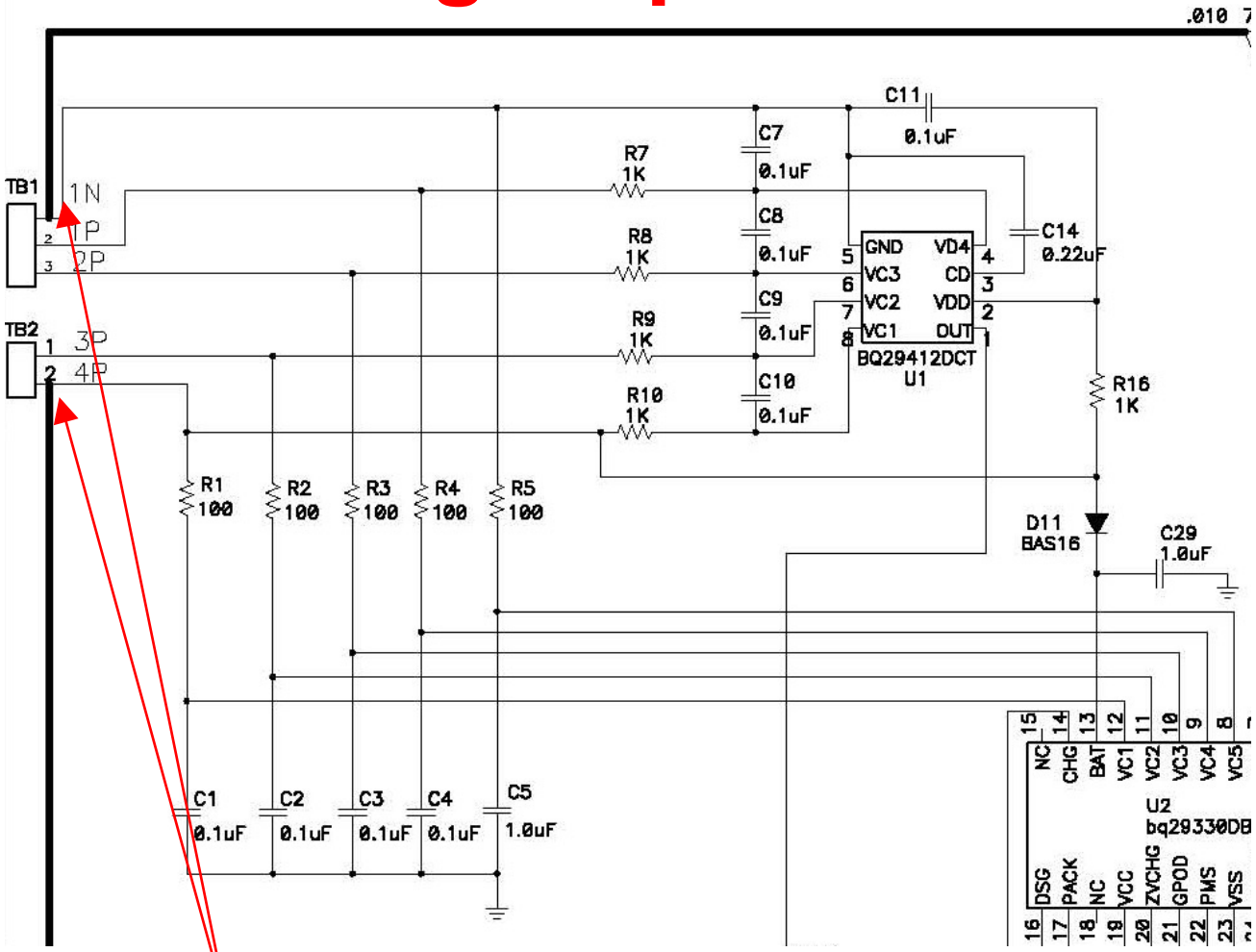


Separating High and Low Currents



- Avoid high current under the gauge and AFE ICs
- Minimize high current loop area

Cell Voltage Inputs

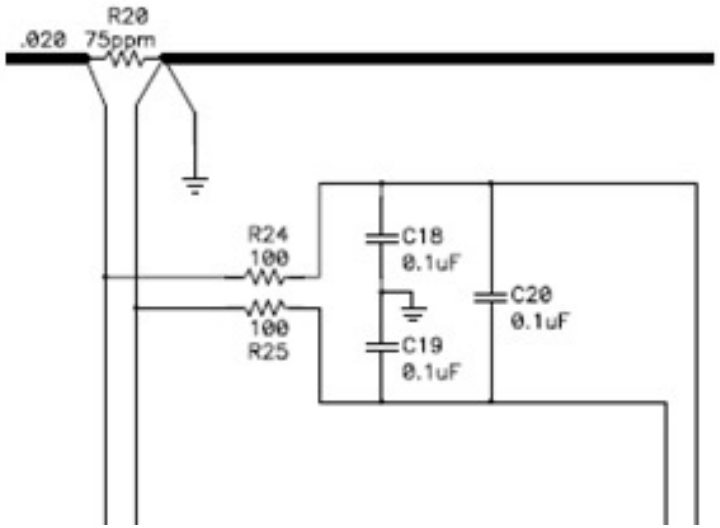


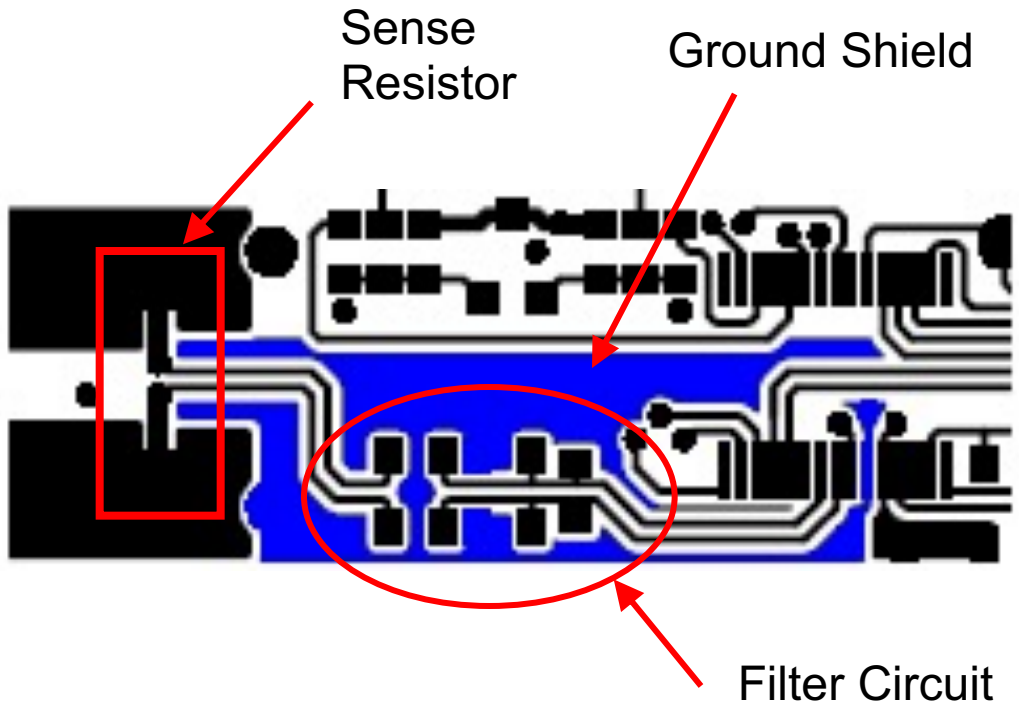
- Separate filters required for safety
- C14 sets the time delay for activation of the output after any cell exceeds the threshold voltage
- Time delay is calculated as td = 1.2V X DelayCap(uF) / 0.18uA.
- D11 and C29 stabilize IC during pack short circuit event
- R1-R5 100 ohms may be fusible type

- Insure that the top and bottom voltage sensing lines are as close to the battery terminals as possible.
  - Avoid any errors from IR drop in the high current path.

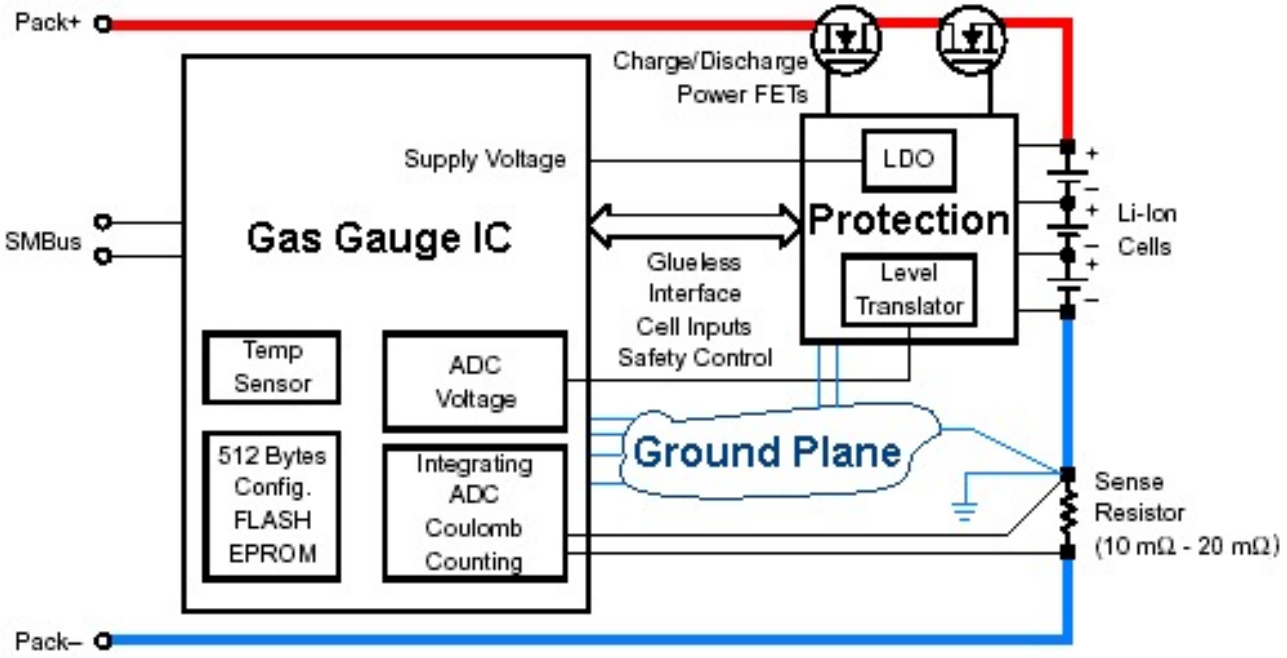
Coulomb Counter Circuit

- The circuit pattern should be symmetrical for minimum current offset and minimum noise pickup.
- Surround the differential input by ground shield.
- Connections from the sense resistor and 100 Ohm resistors should be shielded and the traces should be routed in parallel.
- The filter circuit should be placed close to the device.
- Ensure good Kelvin connections.





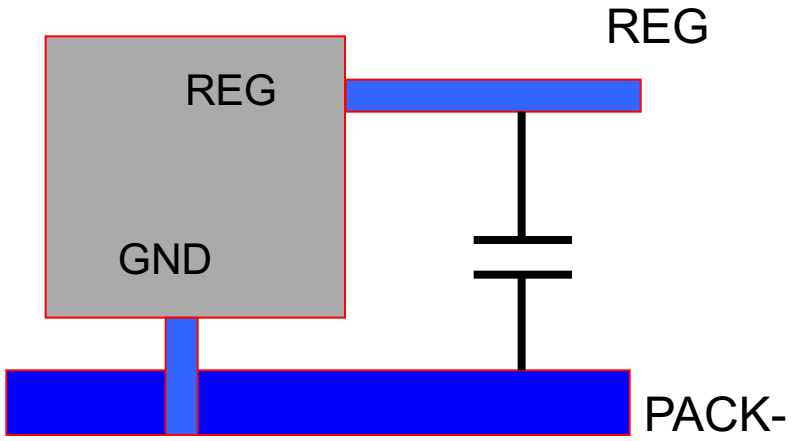
Grounding



- The thick blue wire above is high current ground. All other grounds (thin blue) are low current
- Low current ground must be separated from high current ground
- Low current ground must be connected to high current ground at one location only - at the sense resistor
- Maximize the ground pattern and reduce its inductance
- Use a ground plane if possible

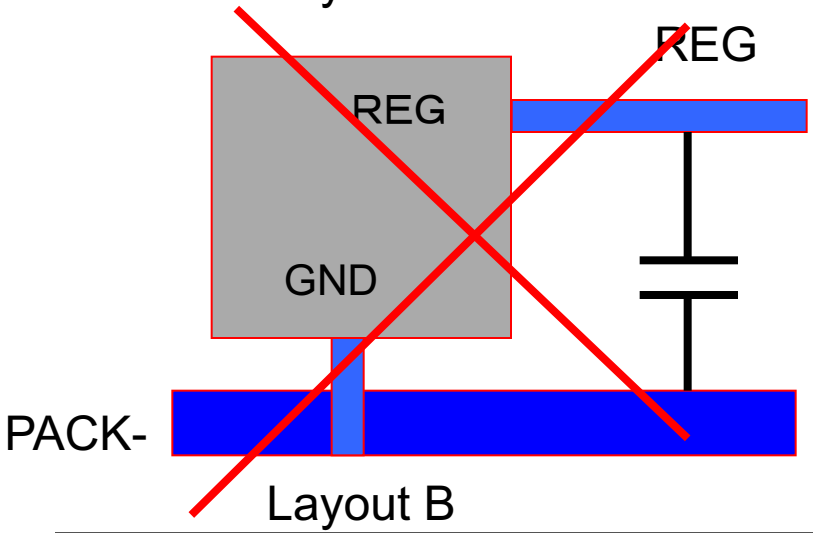
AFE Decoupling Capacitor

Wires on PCBs are not ideal connection.

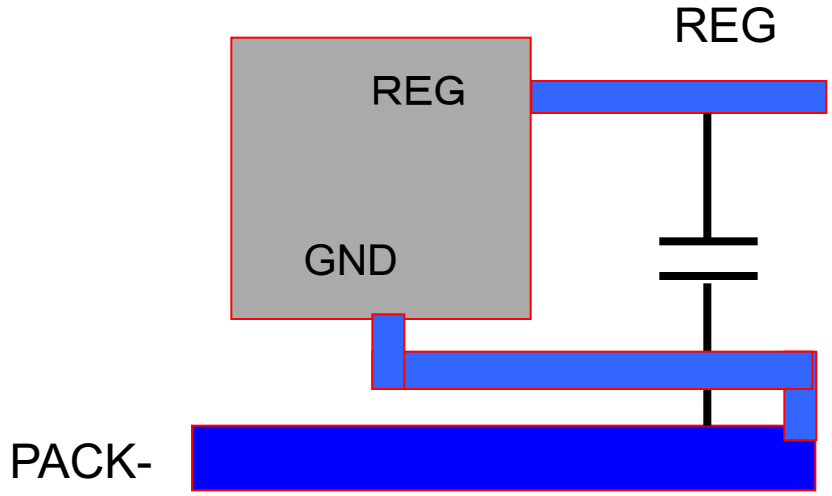


Layout A

- Layout A is ideal.
- With layout B, noise from PACK- jumps into GND before decoupling caps. NG.
- Layout C is better than layout B.



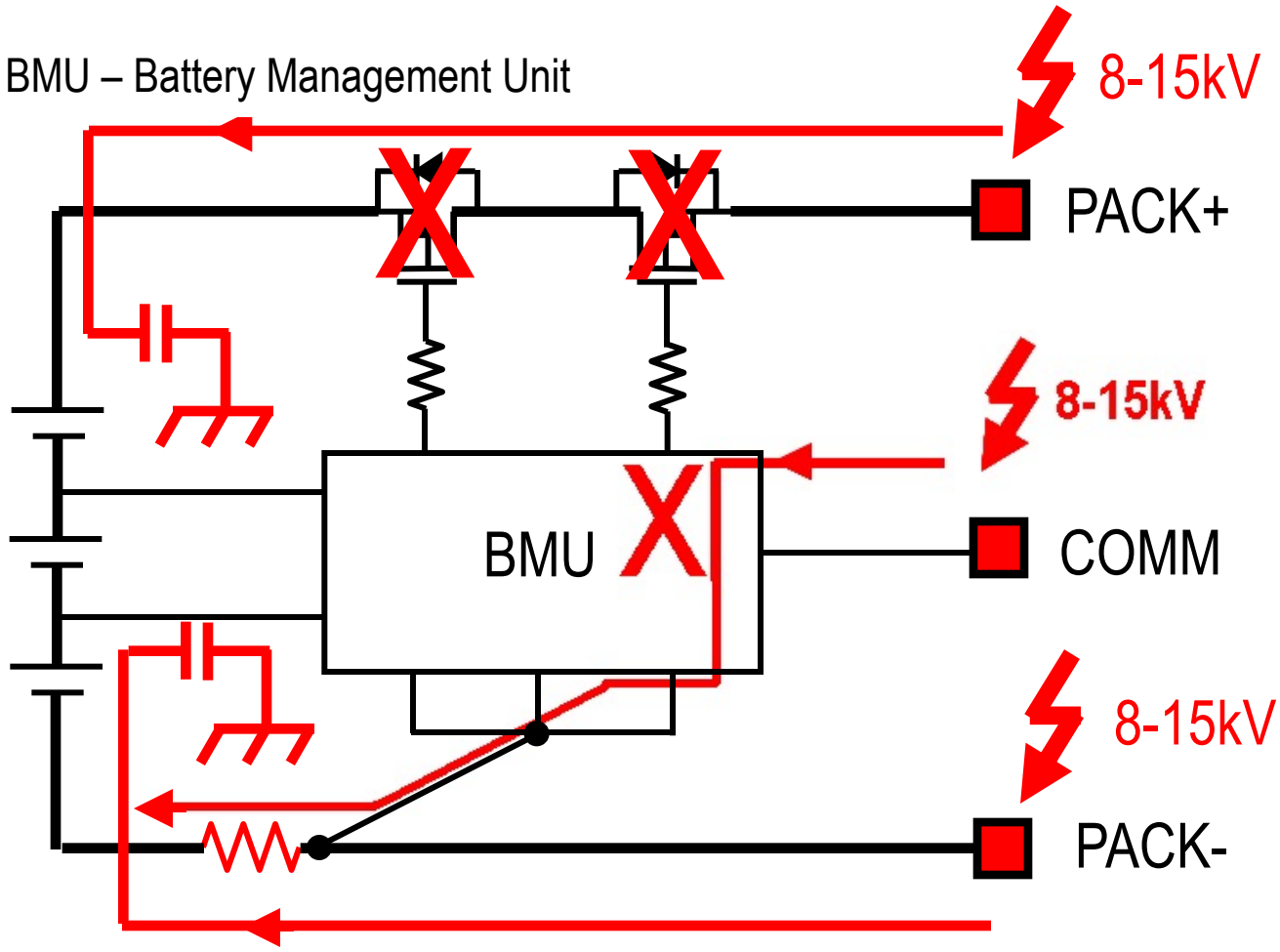
Layout B



Layout C

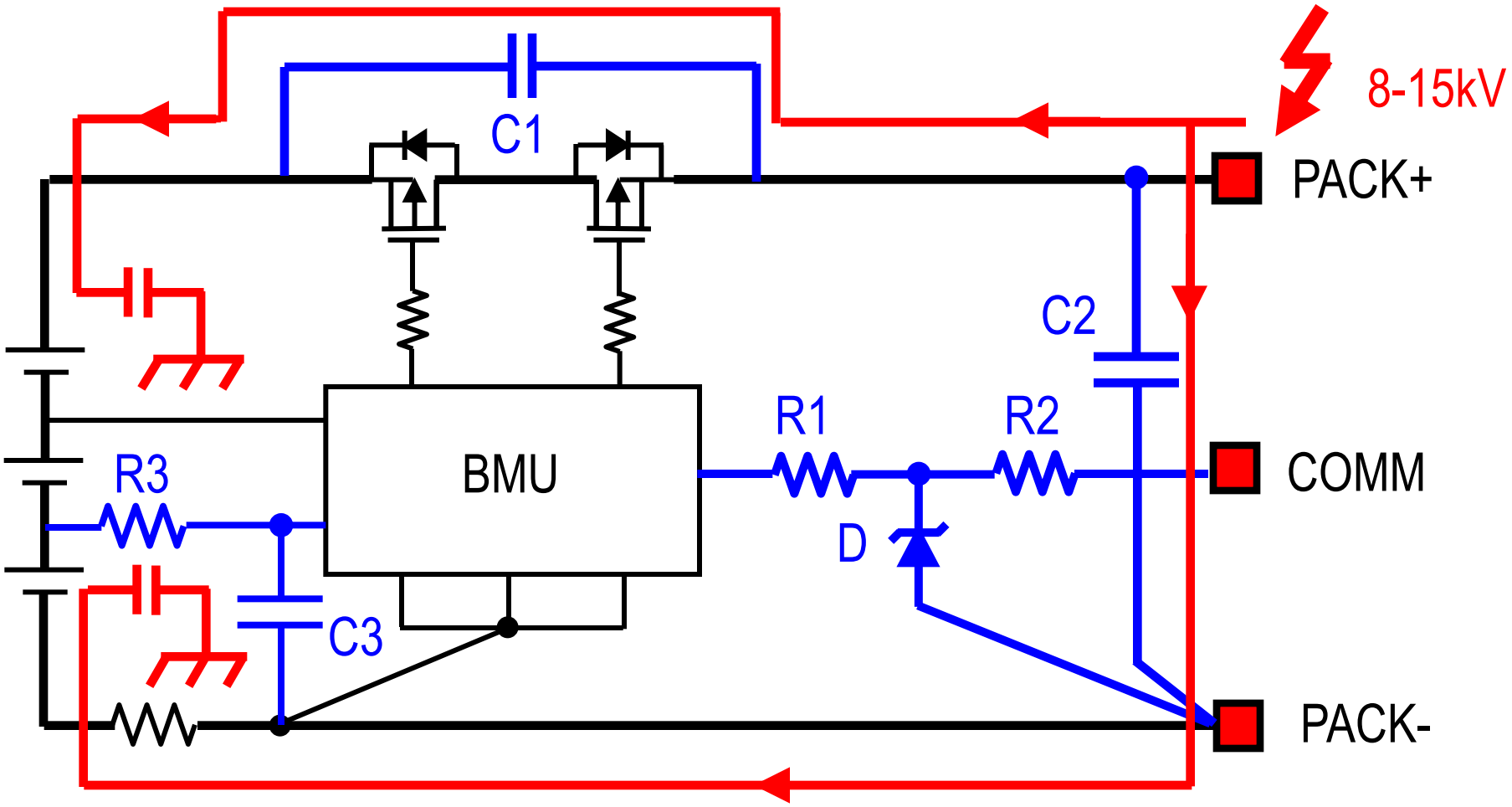
ESD Protection

Battery Pack ESD Hit



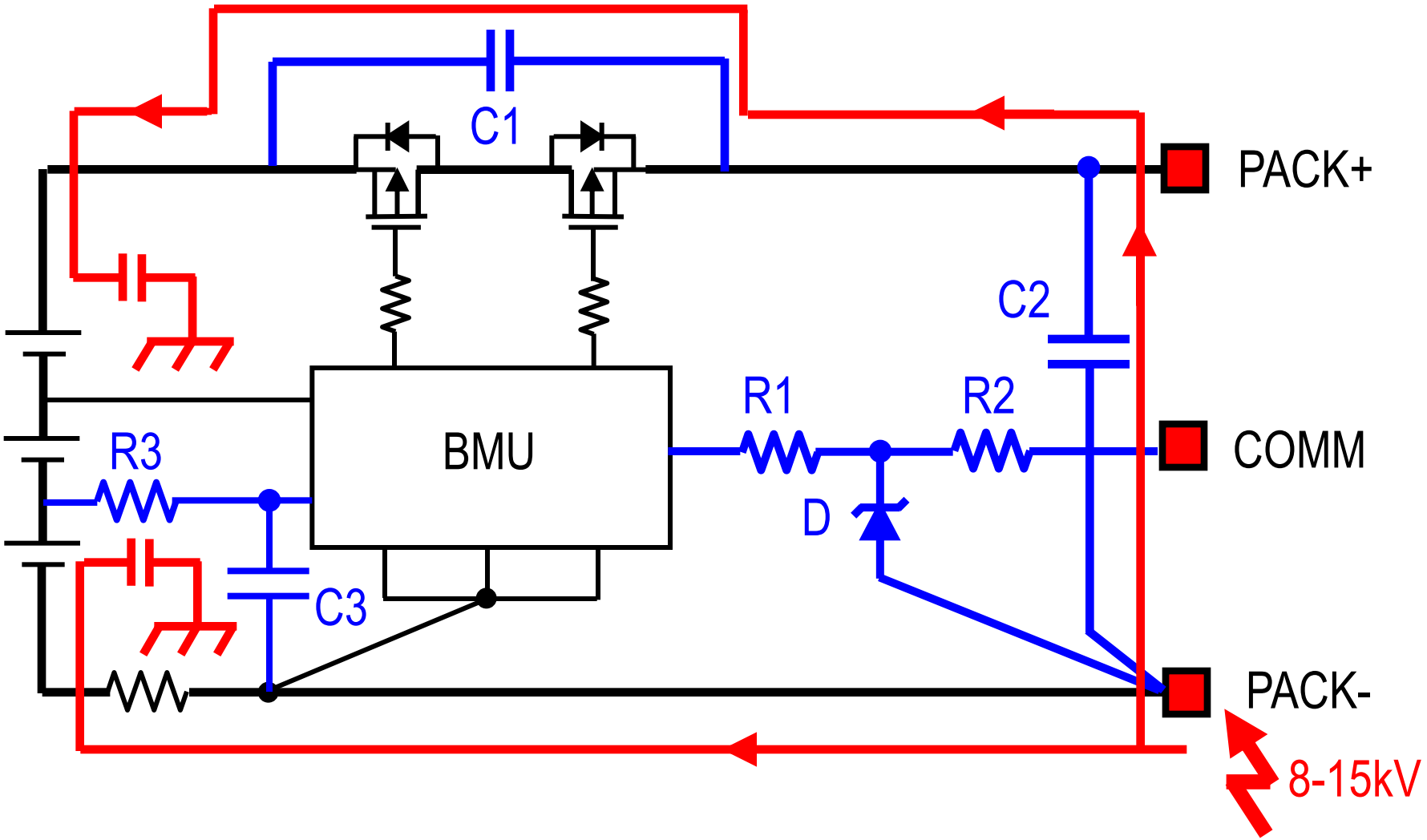
- Pin Exposure will get ESD Hit
- ESD damages Protection FETs and BMU

Battery Pack ESD Protection – PACK+



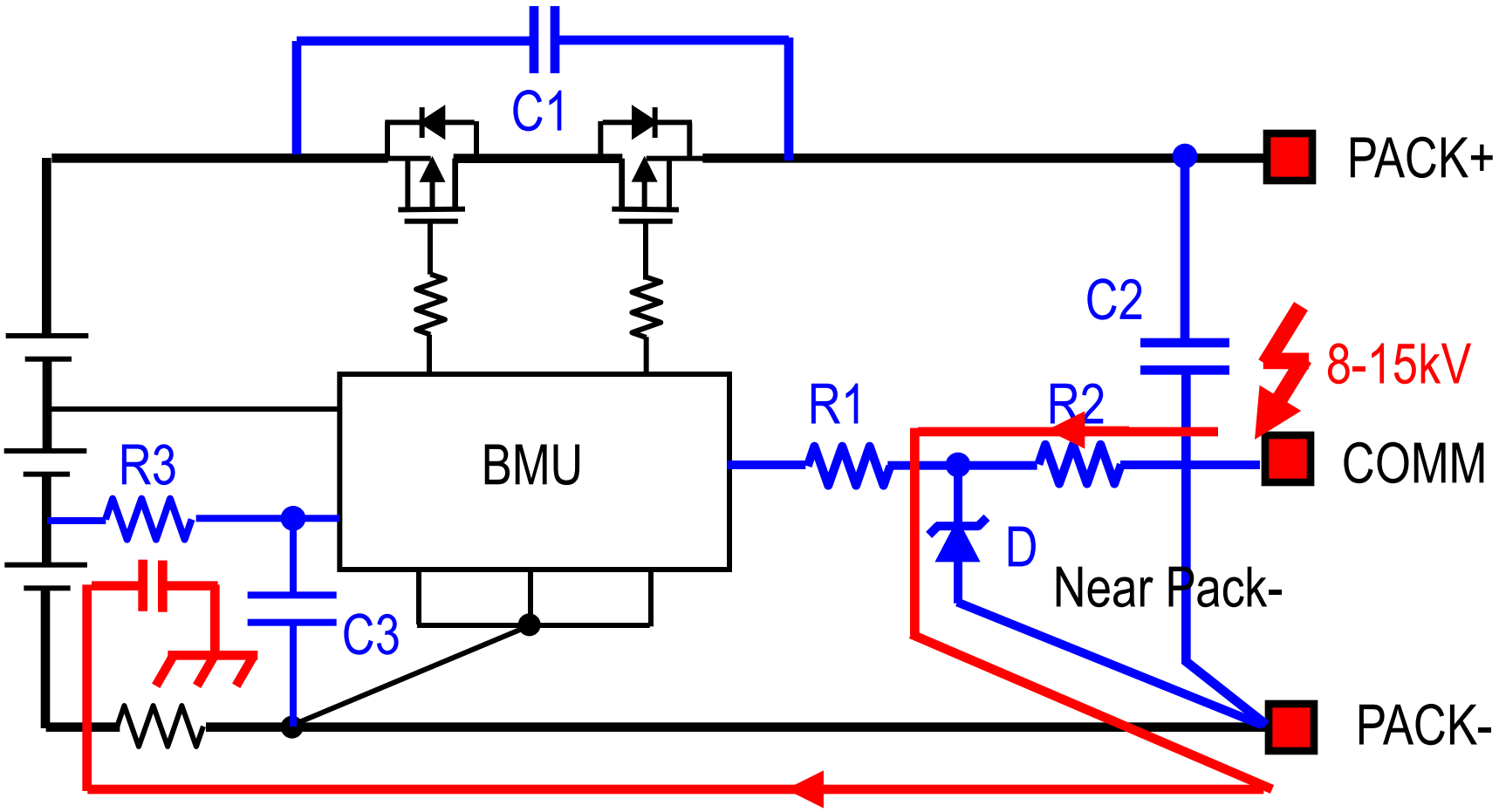
- Preferred diverting path for a ZAP to Pack +: Capacitors C1 & C2
- Ensure caps can absorb 2.5 micro coulombs

Battery Pack ESD Protection – PACK-



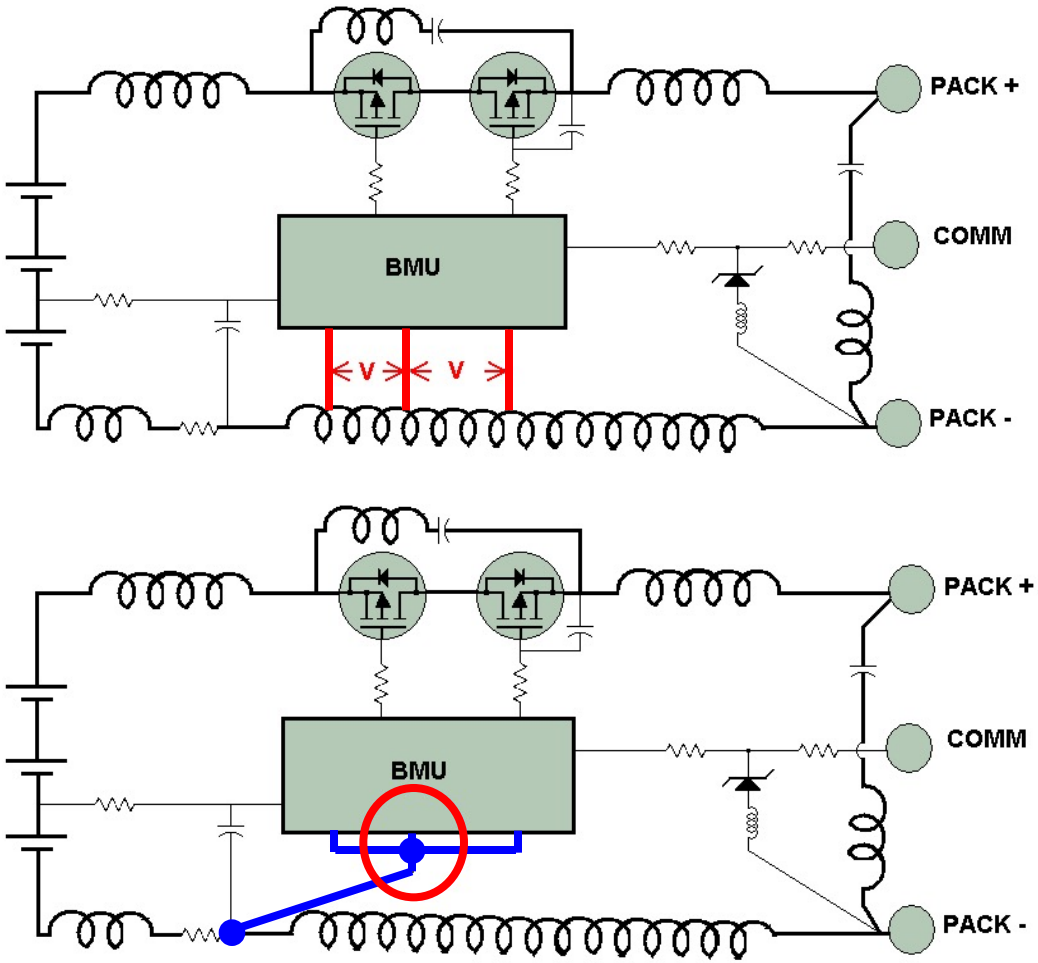
- Preferred diverting path for a ZAP to Pack-: Capacitors C1 & C2

Battery Pack ESD Protection – Other



- Preferred diverting path for a ZAP to COMM: R1, R2 and D

Use Proper Grounding



Avoid Inductive Voltage Drop

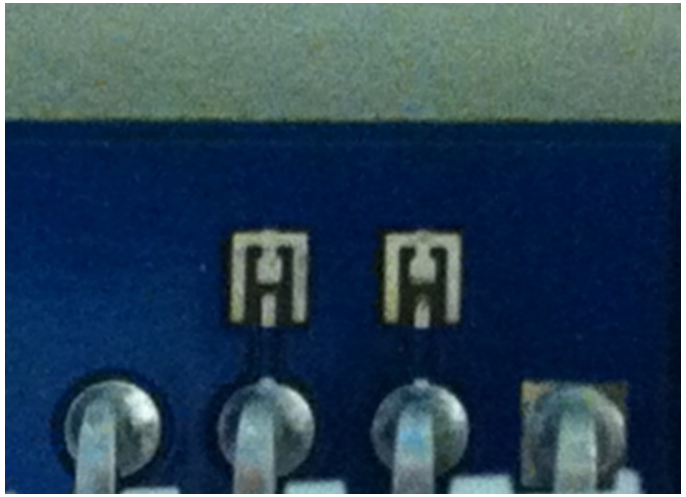
Wrong

$V = L \, di/dt$

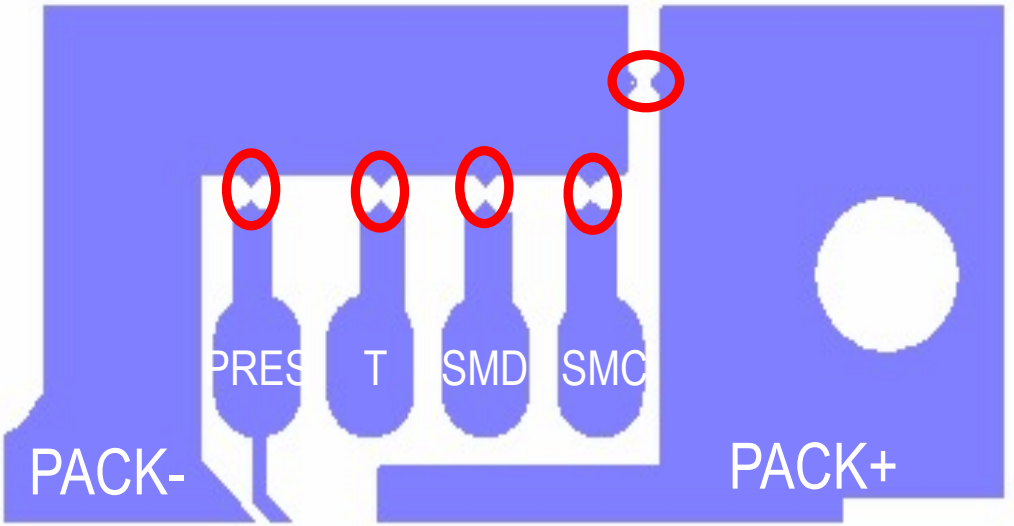
Right

Low level ground systems must connect to a single point at the sense resistor

Use Spark Gaps

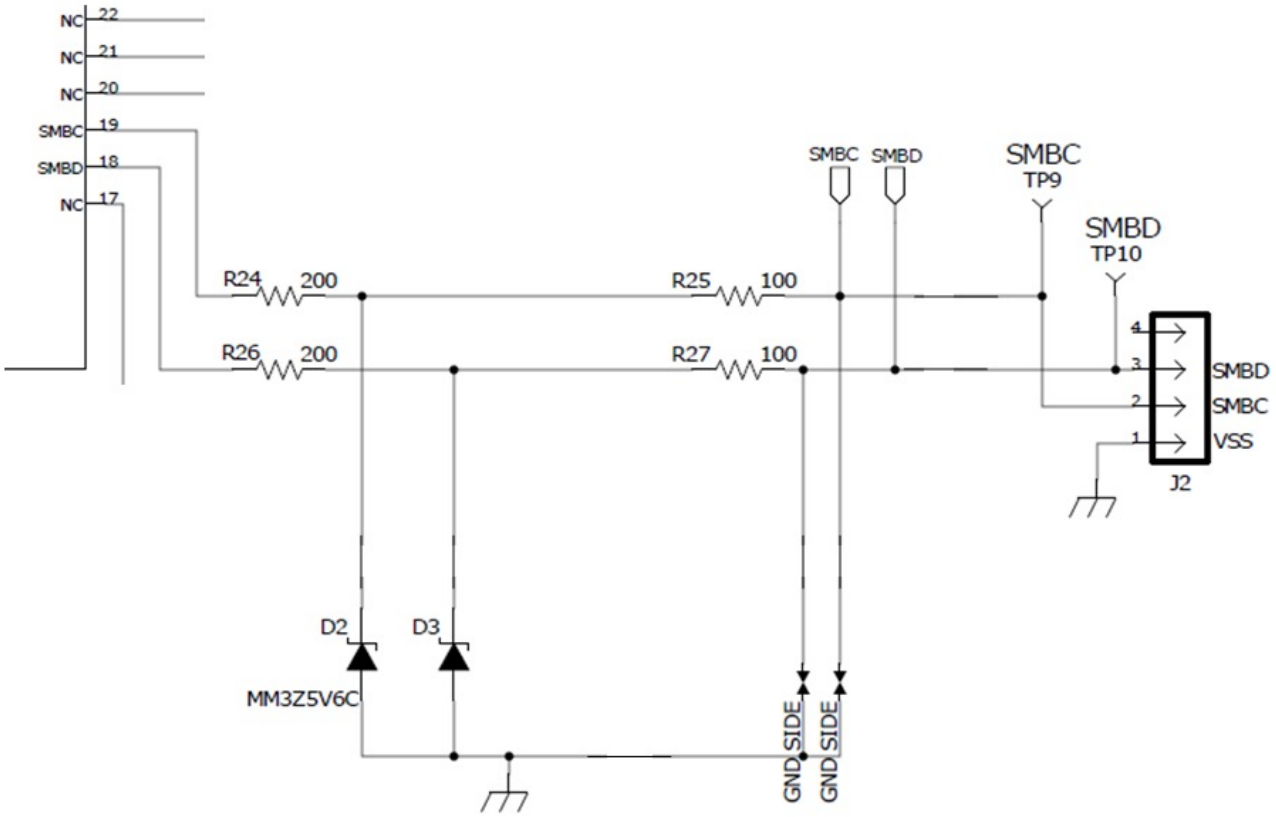


Spark gap on the right has been exposed to multiple ESD strikes.



- Use a spark gap at the pack connector
- Reduce Peak Voltage seen by the internal circuit (IC)
- Must be PCB external Layer
- Must be free of solder mask or other non-conductive coating
- A 10-mil (0.2 mm) gap has a voltage breakdown about 1500 volts

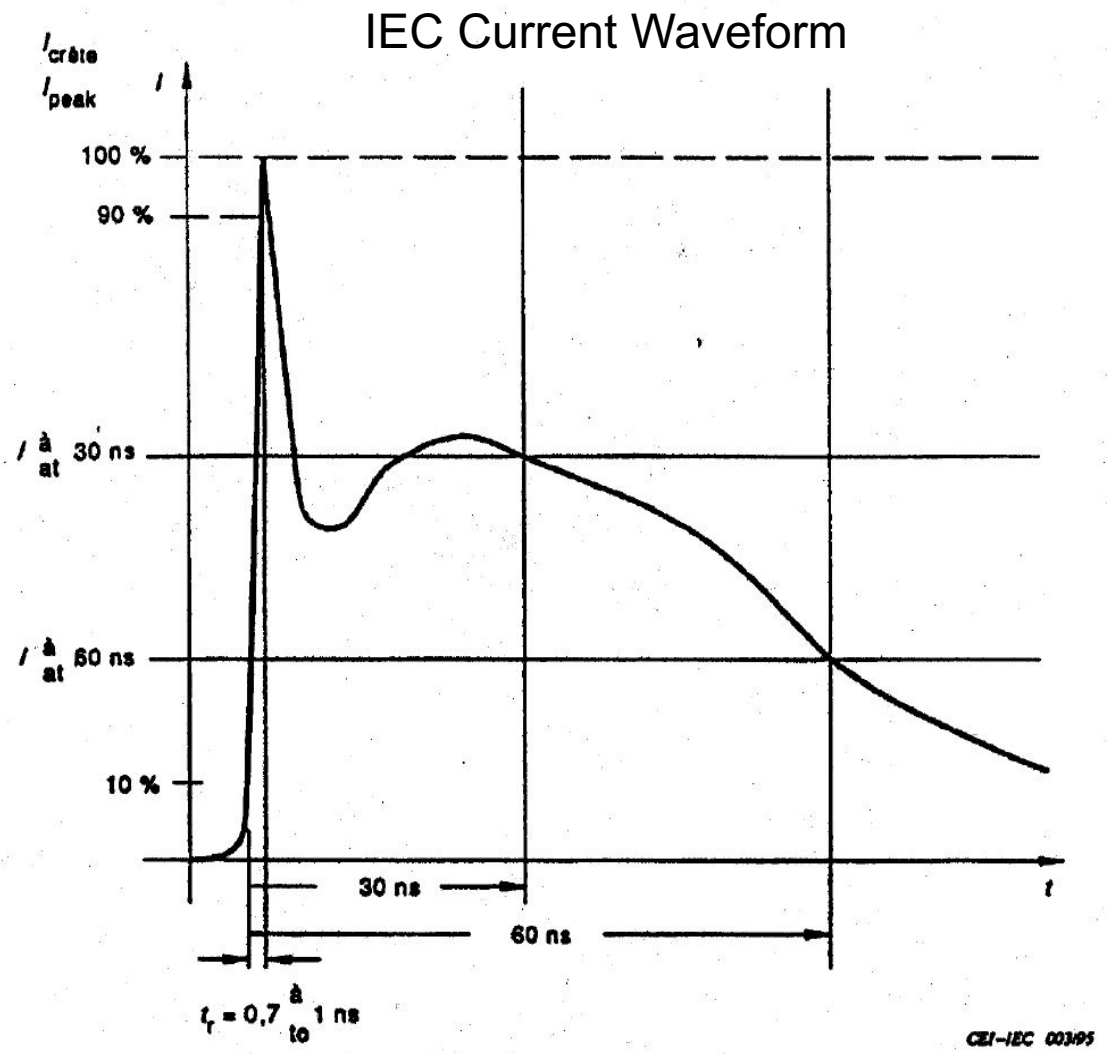
Communications Line Protection



- 100 ohms keeps signal edges sharp, but zeners may not survive continuous short
- Insure that diodes returns to Pack – not to low current ground

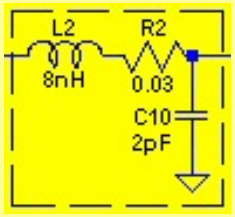
What is the Effective Frequency of ESD (IEC)?

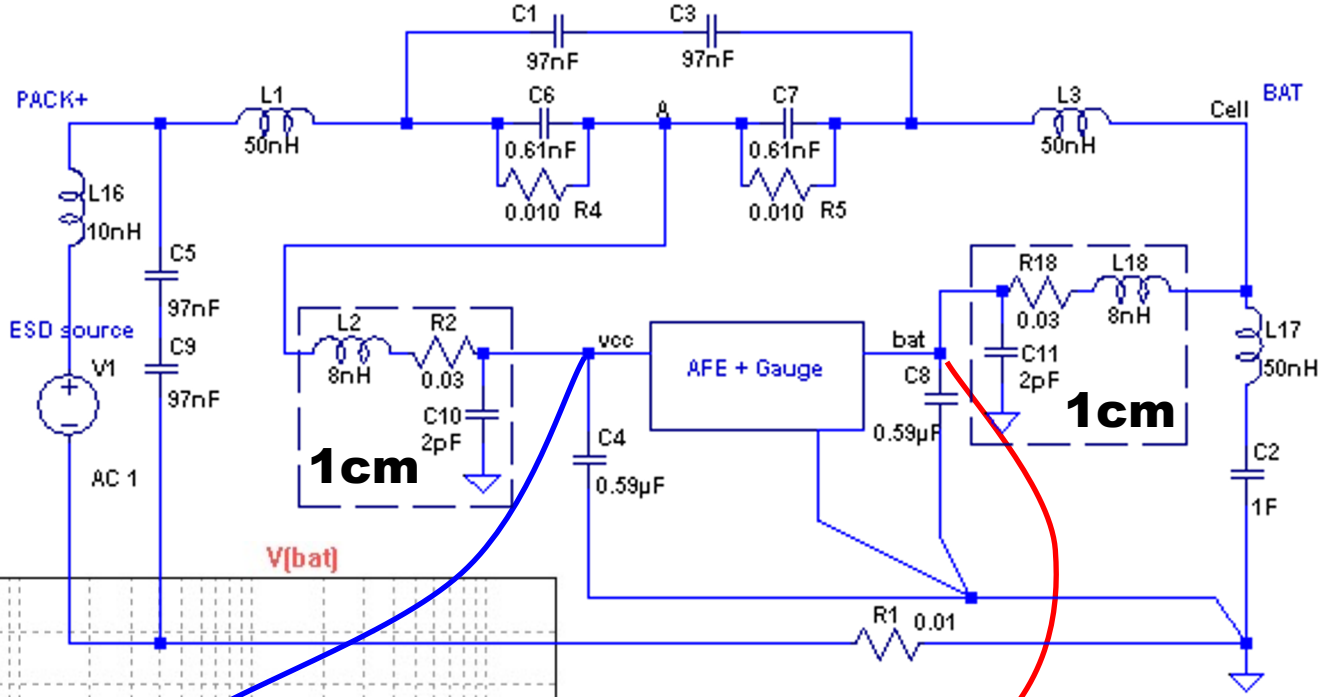
- Extremely fast current rise time, ~1nsec
- Followed by a longer, but lower-level current transient
- The initial transient is most deadly to the electronics
- Apply EFFT (Extremely Fast Fourier Transform), $1/(\pi t_r)$, where t_r is the rise time, to the IEC current waveform
- ESD event is a 300MHz phenomenon (1nsec rise time is equivalent to 318MHz)

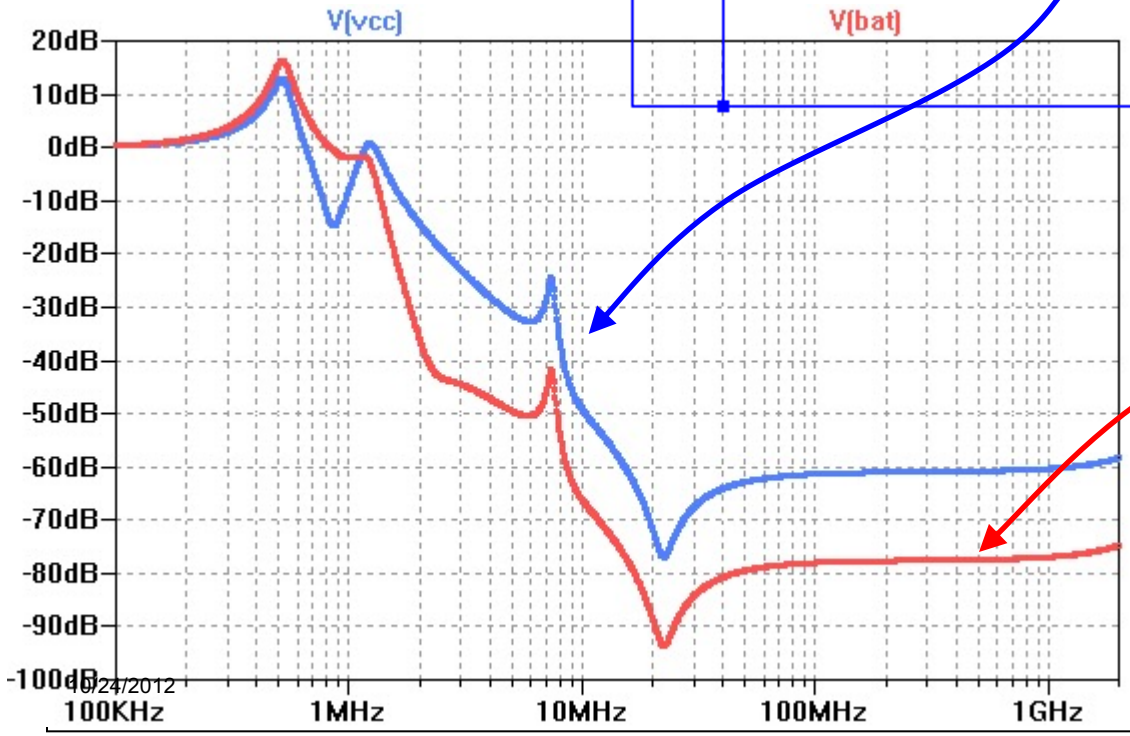


First-order Equivalent IEC Circuit

A rough model: a 10mil PCB trace of 1cm long (highly geometry-dependent!)

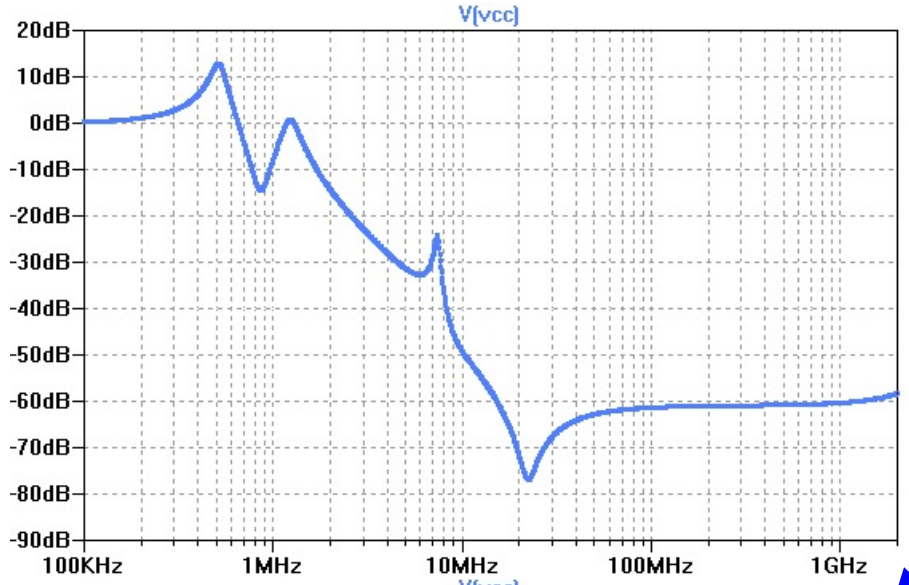






First order simulation:
VCC is worse than BAT

Effects of PCB Trace Length



Minimize trace lengths

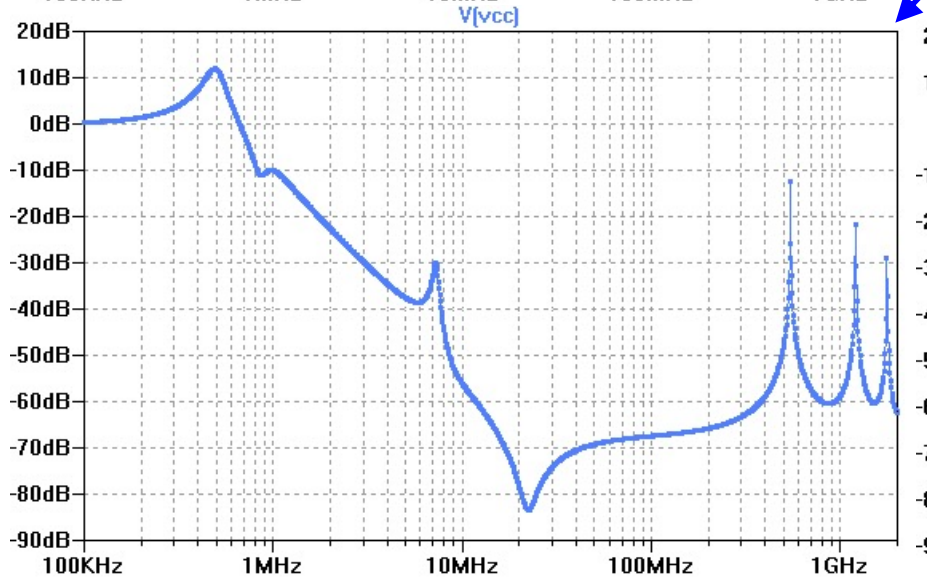
VCC Trace length:

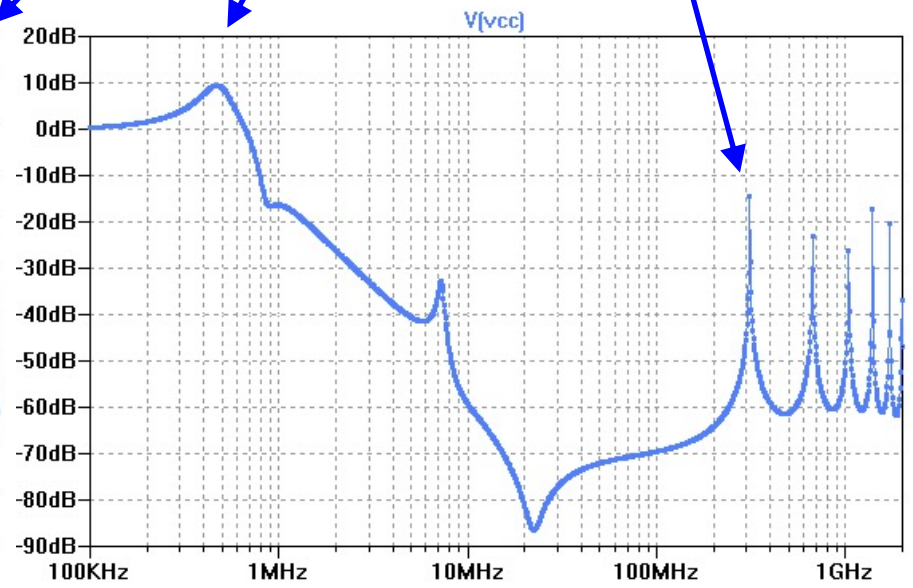
1cm

5cm

10cm

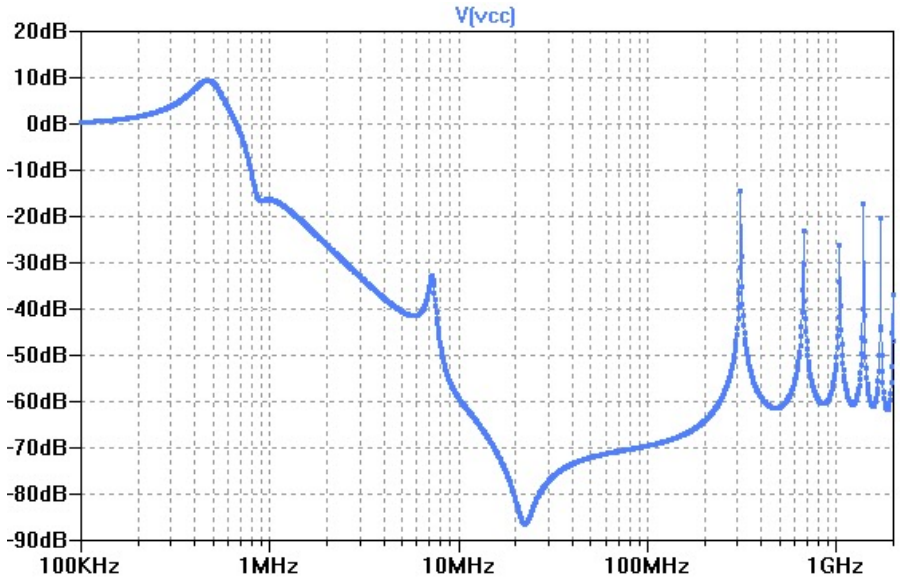
IEC frequency resonances



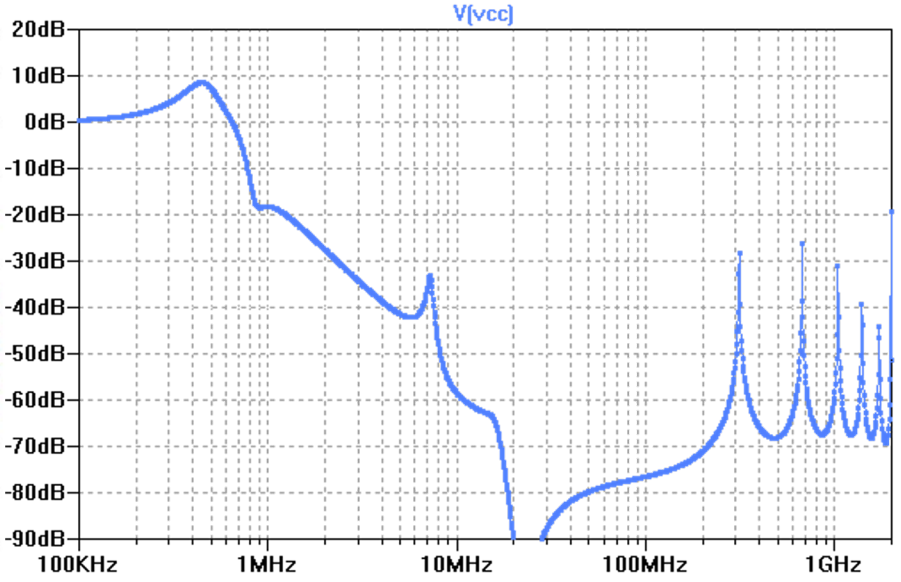


Paralleling Capacitance

- Paralleling additional small capacitors reduces high frequency gain

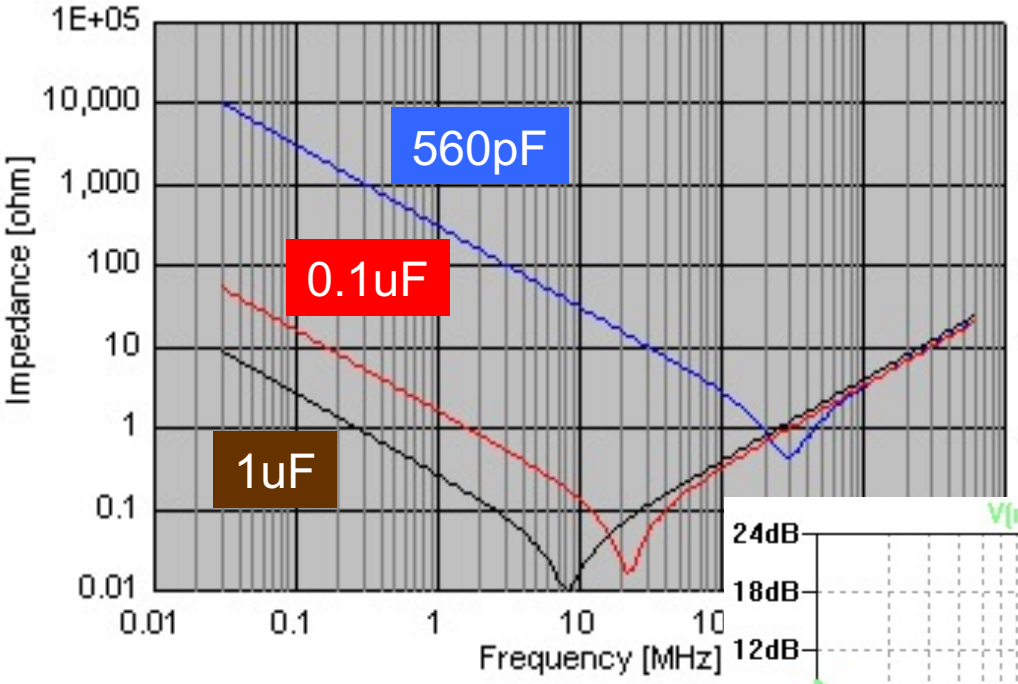


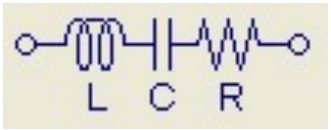
1uF

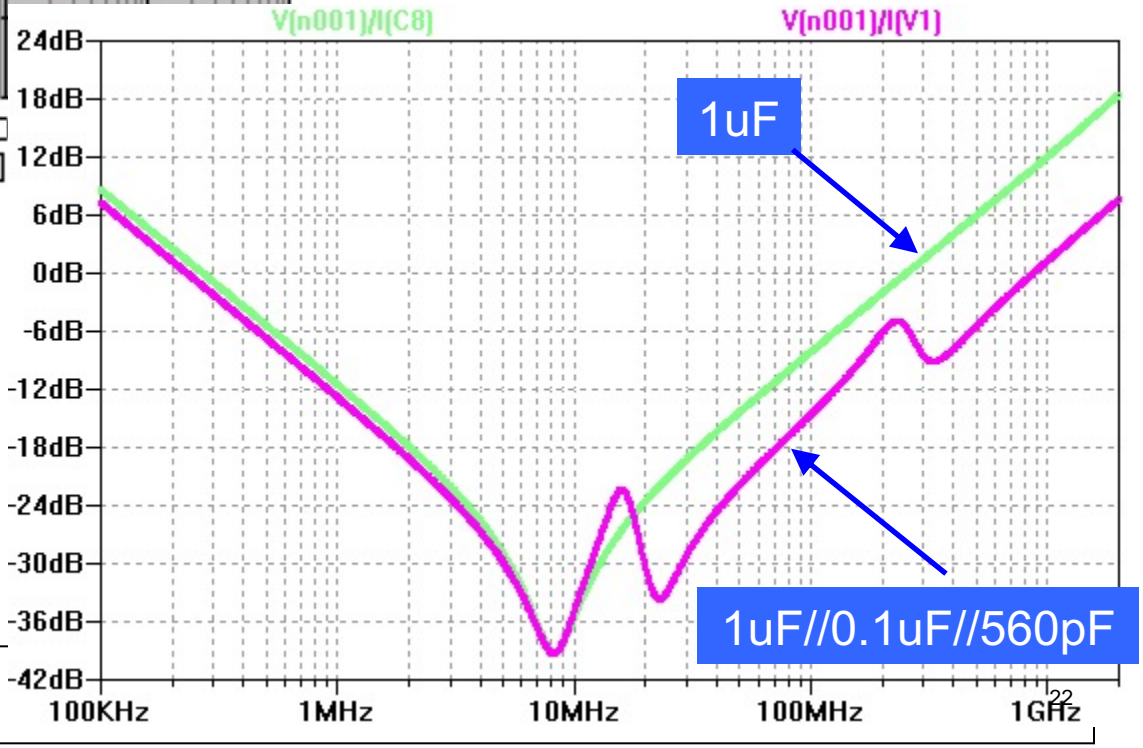


1uF//0.1uF

Will More Parallel Capacitance Help?

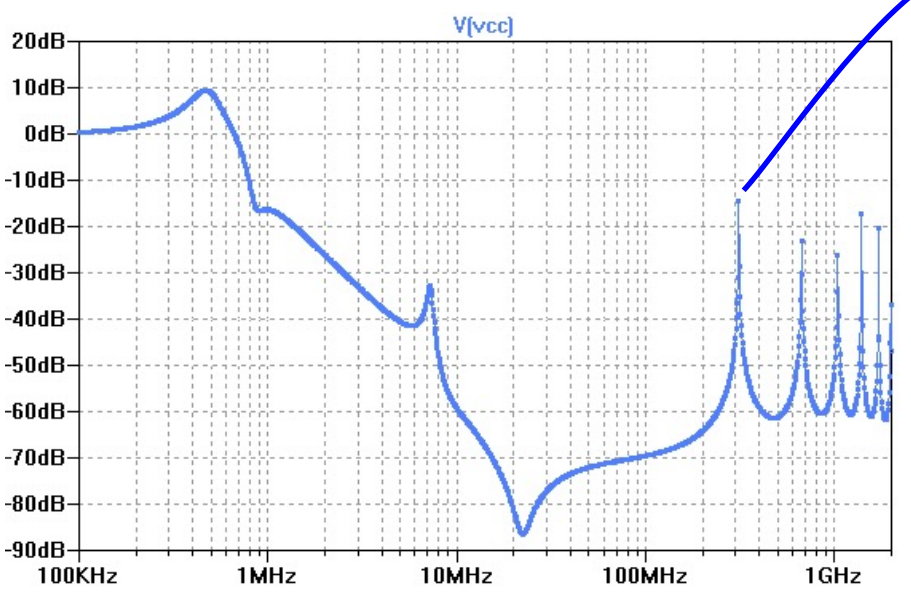




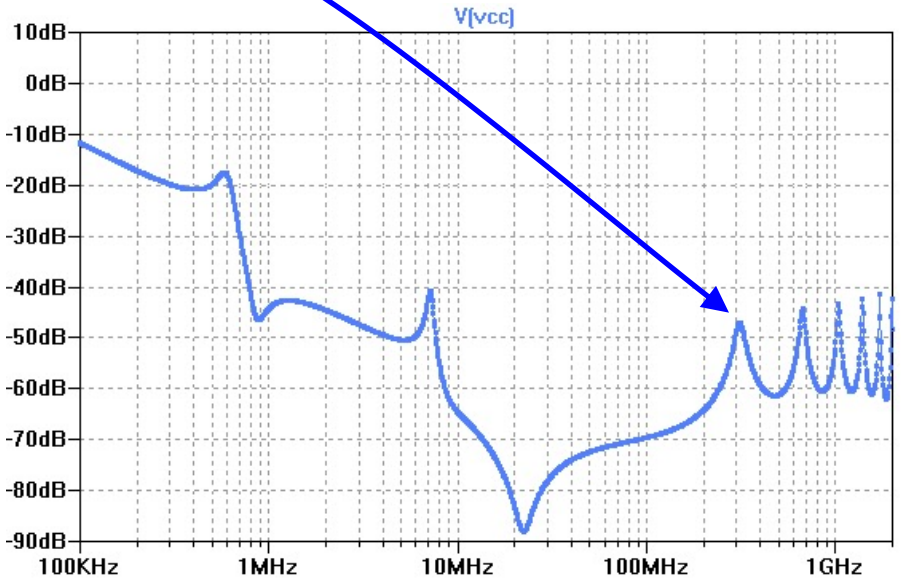


Will Adding Series Resistance Help?

- A 10 ohm resistor is added in series to the VCC
- Damps the resonance and reduces peak values



No series resistor



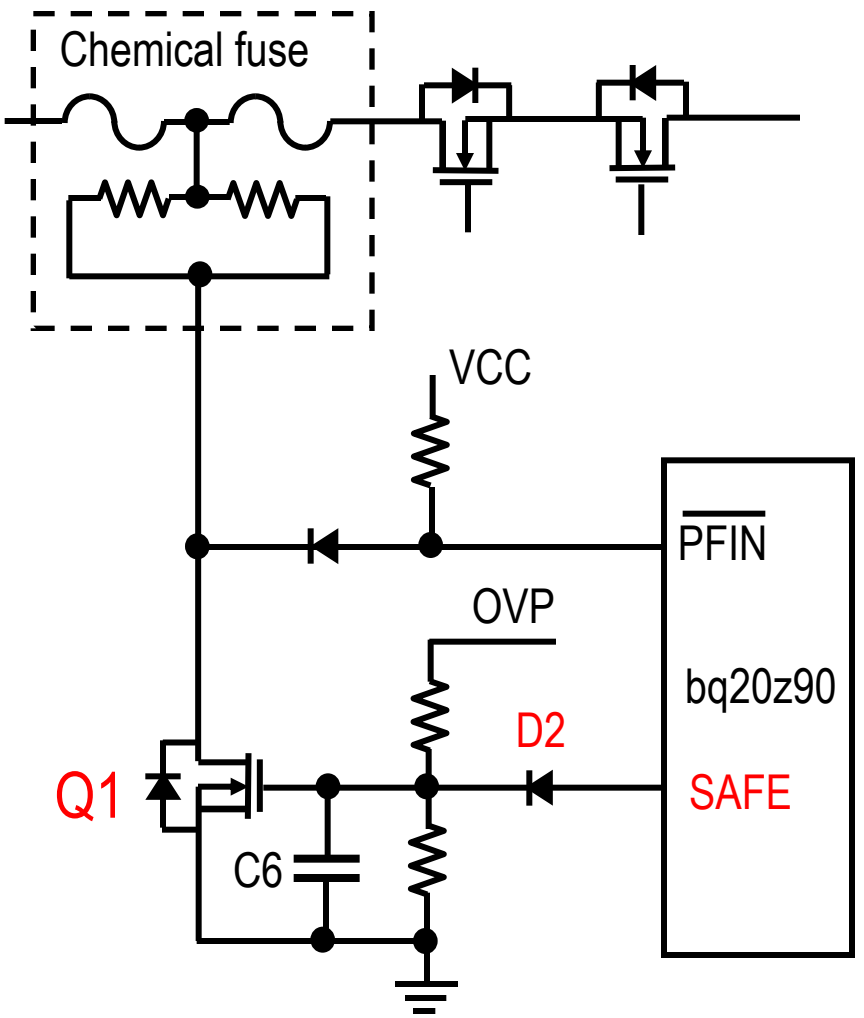
With a 10 ohm series resistor

EMI Protection

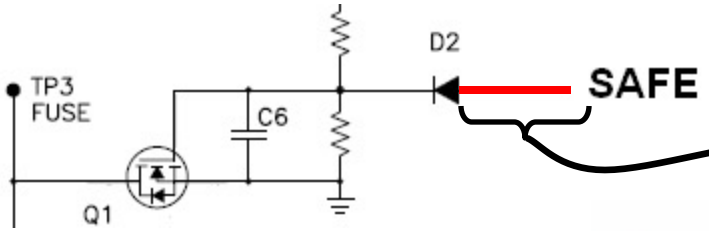
Electric Field Causing False Fuse Activation

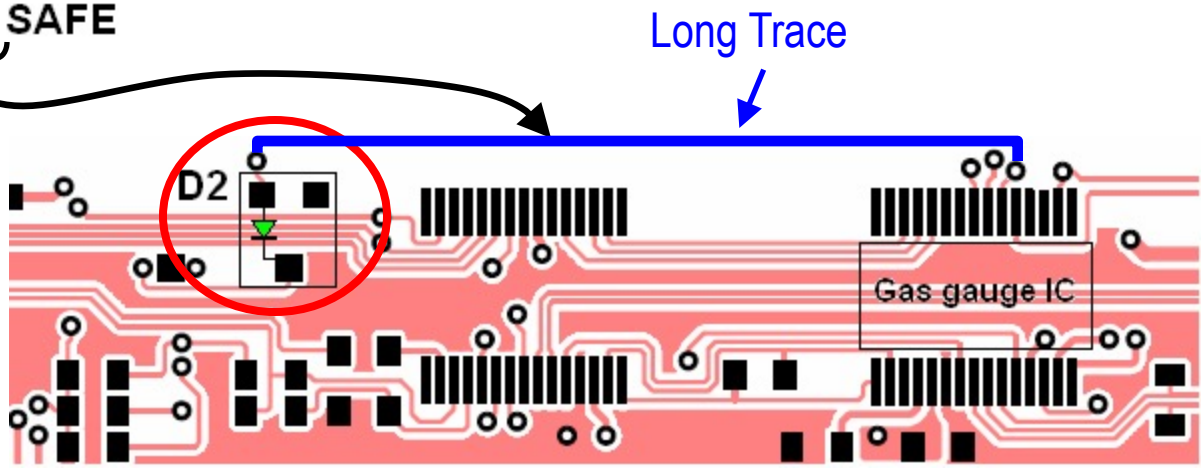
- When SAFE is not activated, D2 is reverse biased and Q1 is OFF
- Turning on a 2W walkie-talkie (SX700R) next to the circuit board can turn on Q1, falsely causing FUSE blow (462 MHz)
- What is the root cause? How can we improve?

At 462 MHz, ¼ Wavelength: 16 cm
1/20 Wavelength: 3.2 cm

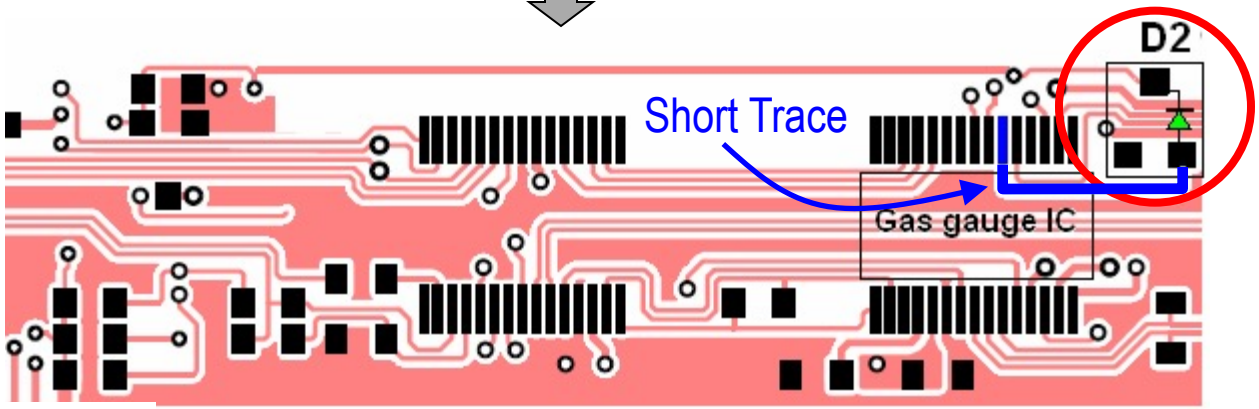


Improved Layouts: No False Fuse Blown under RF





- Old layout



- Improved layout

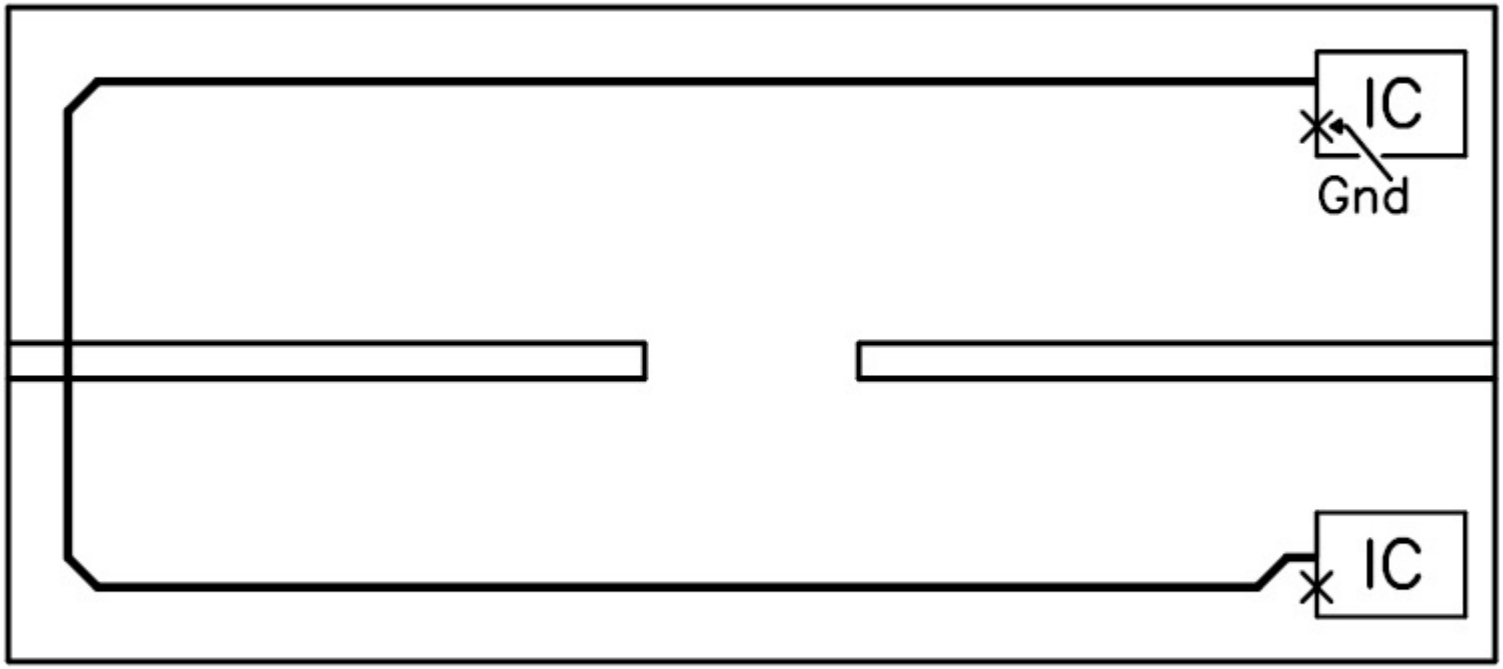
- Shorten the antenna of the receiver

Common Mode Issues

- 90% of EMI problems are caused by CM Current spreading to areas where it can couple into something which can Resonate and Radiate.
- All CM current comes from Intended Fields which are NOT properly contained!!
- “Ground” is often considered a region of zero voltage potential with zero resistance or impedance, but this is not true except at DC.

EMI Control - Routing

- What if Route Crosses Split Return Plane?



- Where does Return Current Flow in case above?

EMI Control – PCB Stackup

(A)
----Ground-----
----Sig/Pwr----
----Sig/Pwr----
----Ground-----

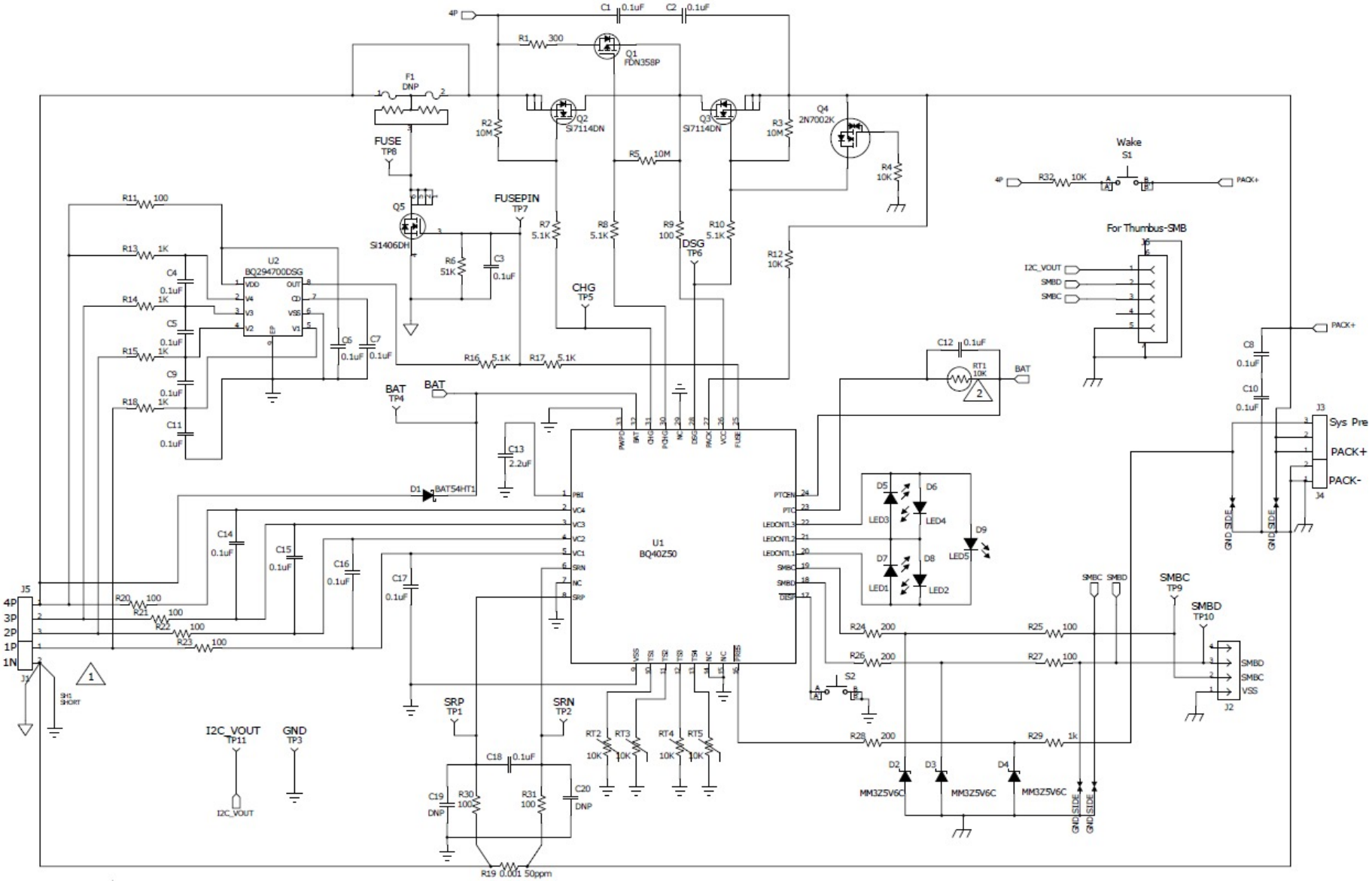
(B)
---Sig/Poured Pwr---
-------Ground---------
-------Ground---------
---Sig/Poured Pwr---

Try to provide a good ground plane.

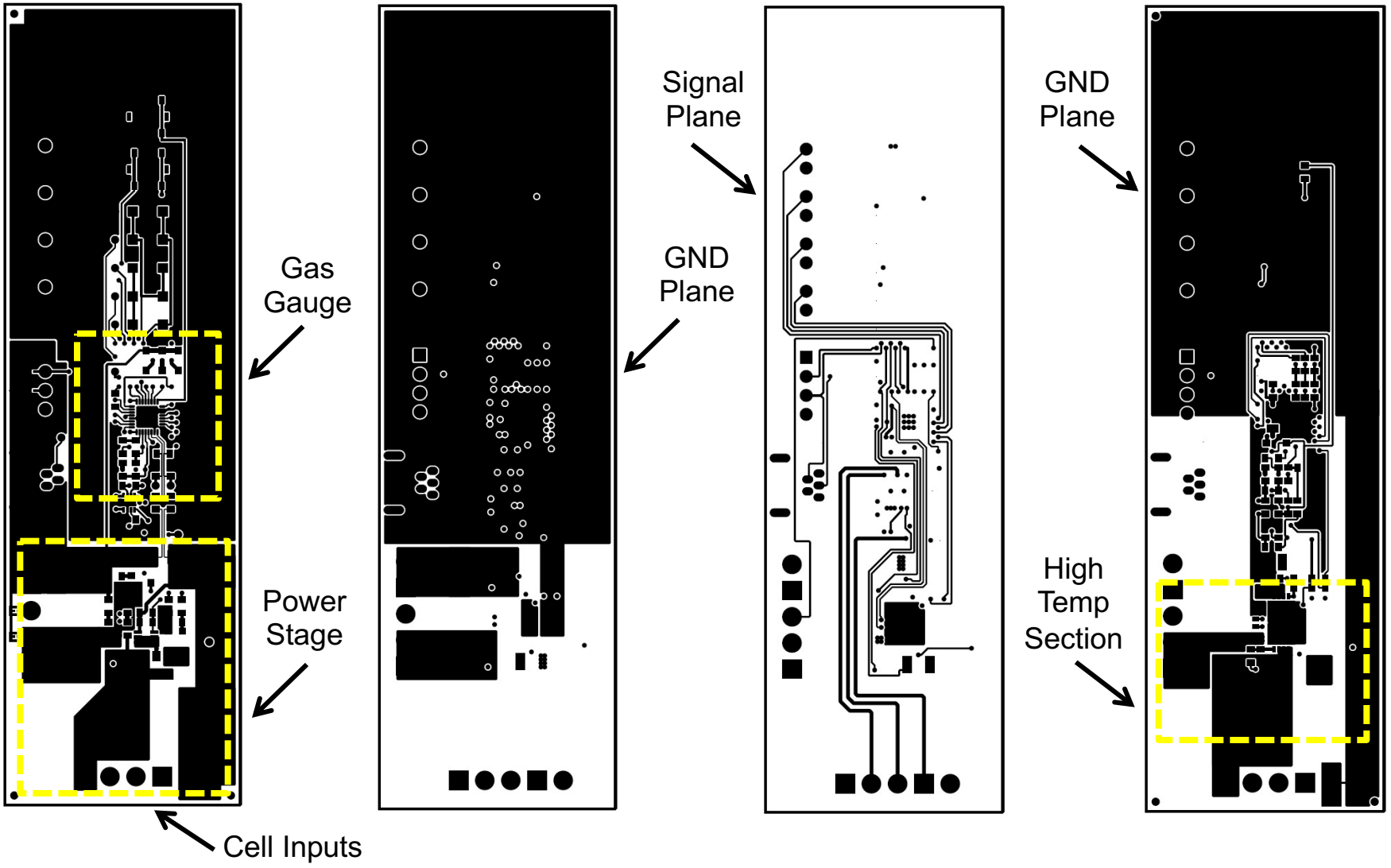
bq40z50

Next Generation IT Battery Manager

bq40z50 EVM Schematic

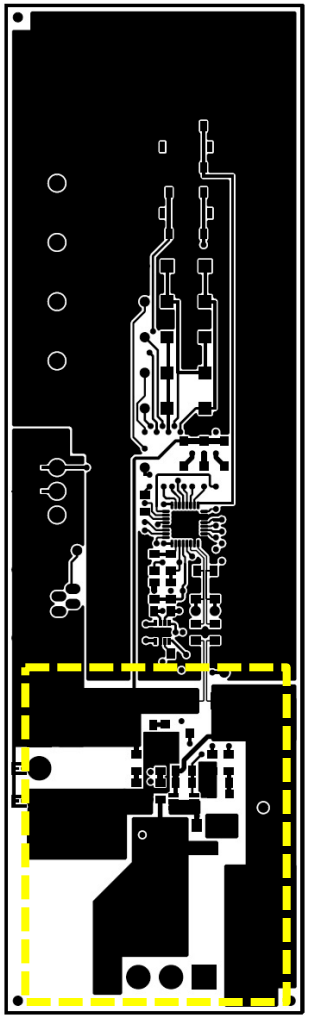


bq40z50 EVM Layout

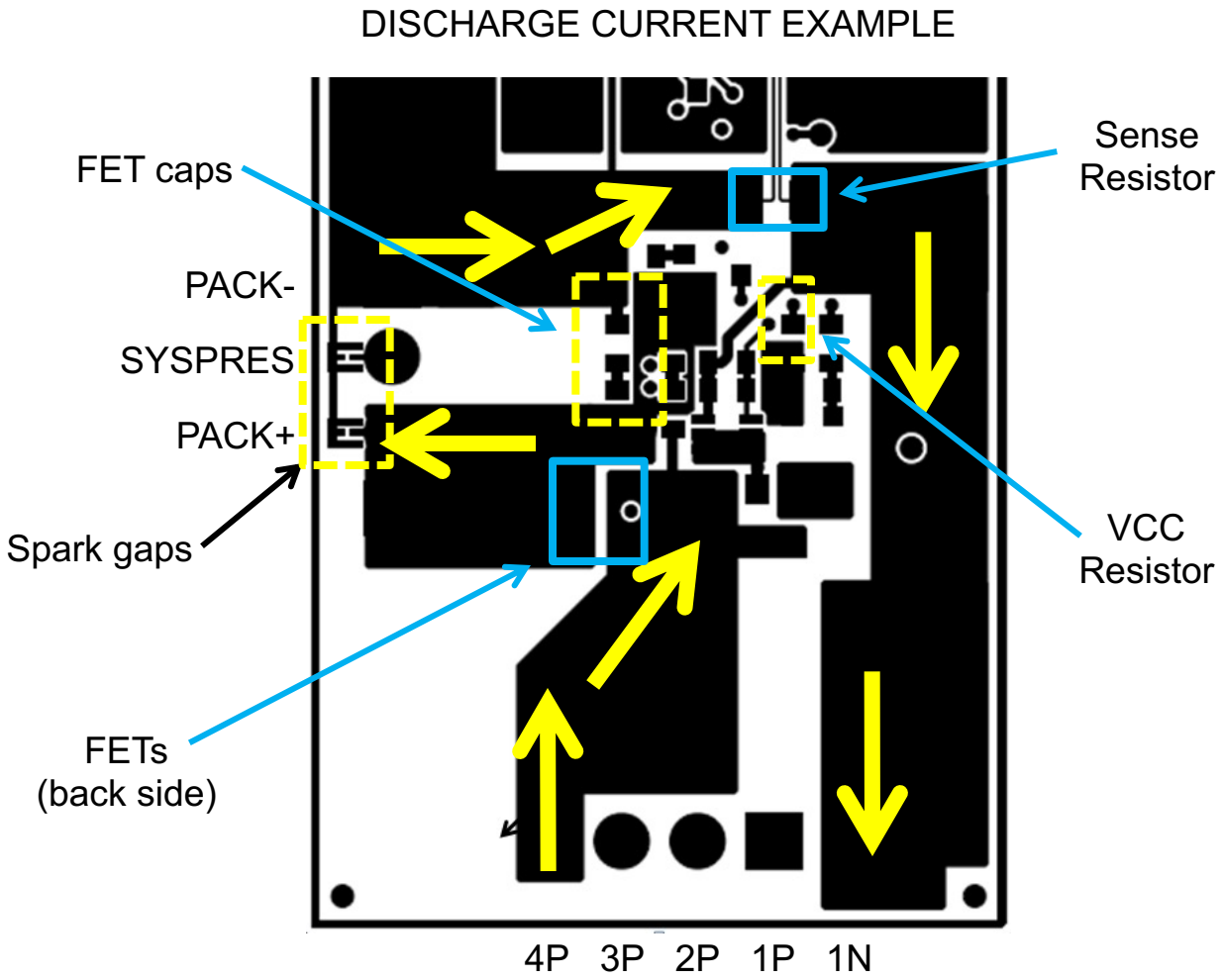


bq40z50 EVM Layout

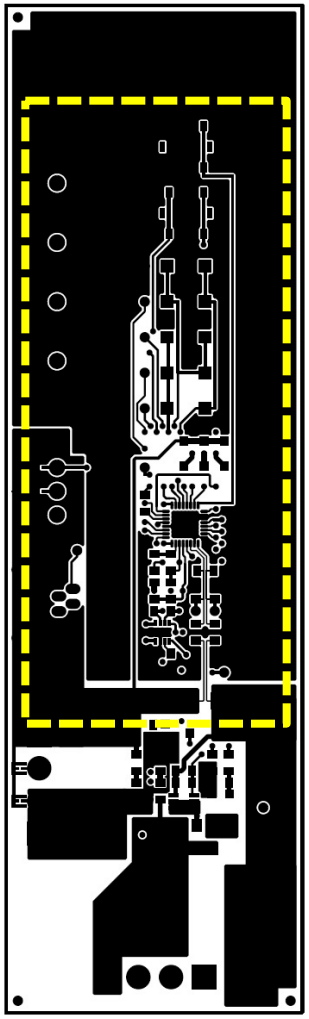
Power Stage



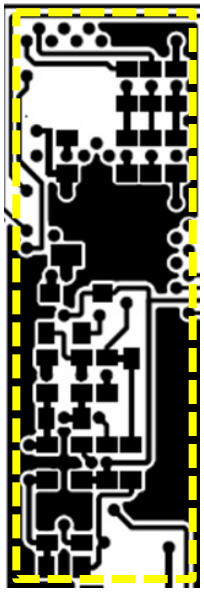
Top Layer



bq40z50 EVM Layout



Top Layer



Thermistors

LEDs
(can add heat)

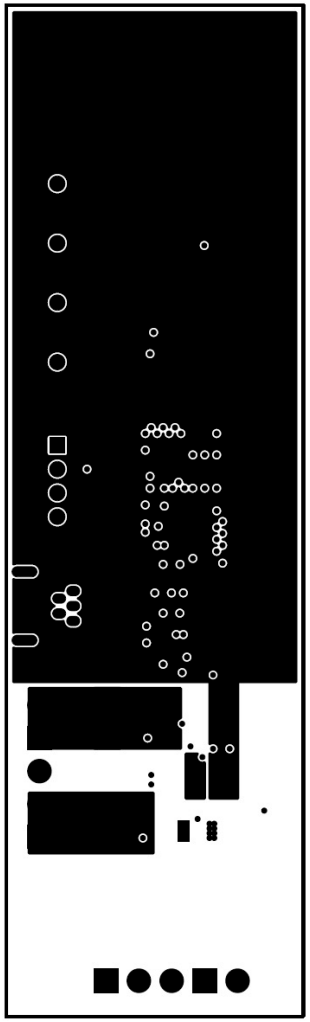
Bq40z50
Discrete components
(others on backside)

2nd Level
Protector

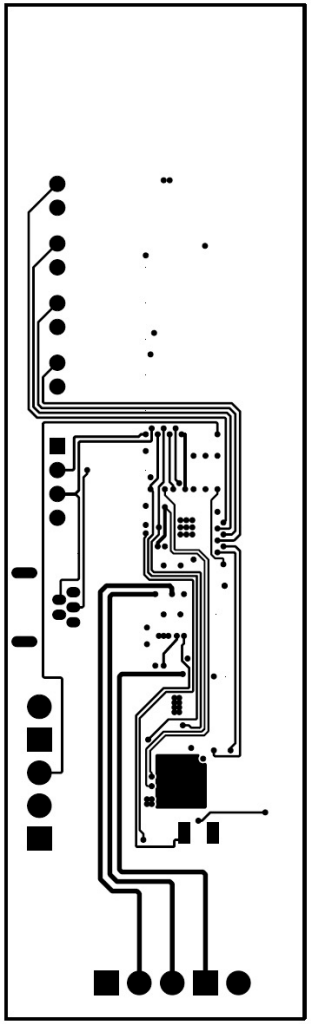
Coulomb
Counter
Filter

bq40z50 EVM Layout

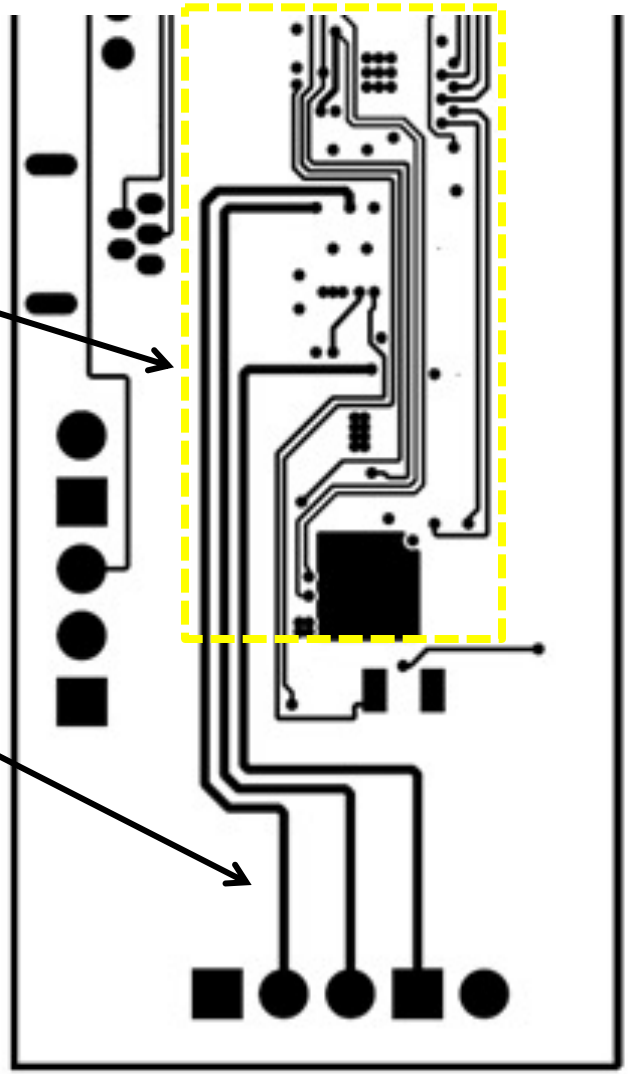
GND and Signal Planes



2nd Layer



3rd Layer



Questions