Switching Power Supply Component Selection

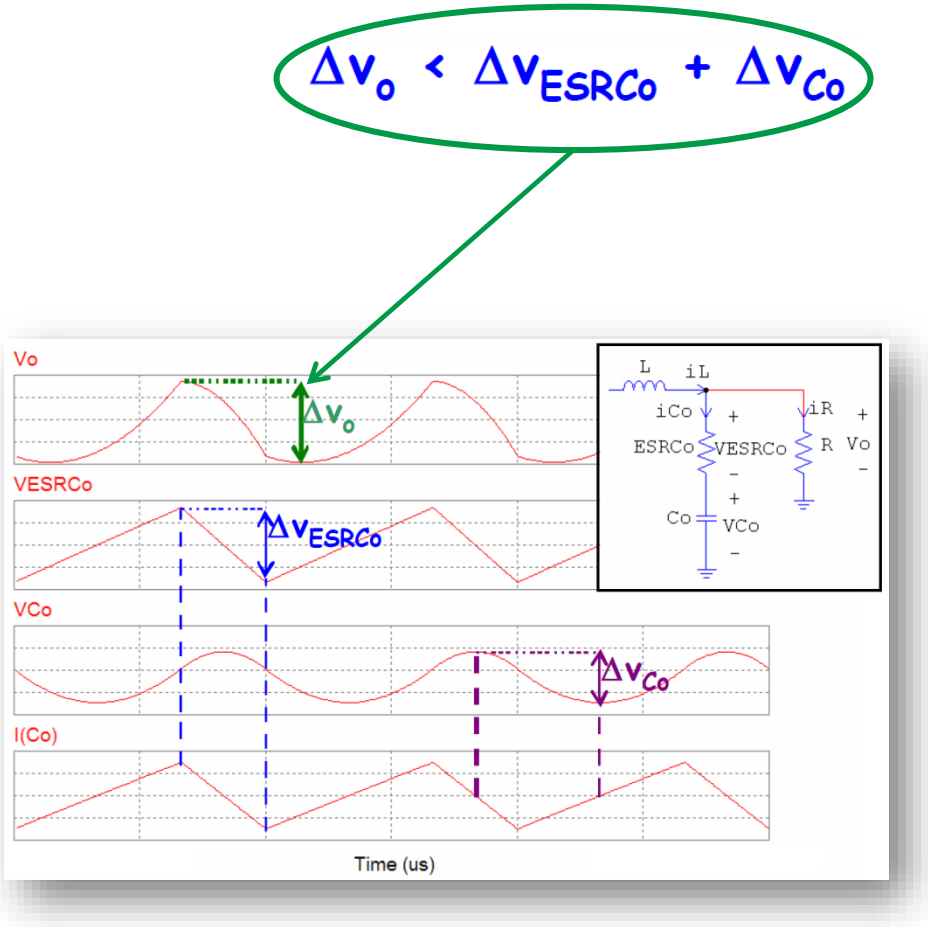
7.1c Capacitor Selection – Meeting Ripple Requirements

Output Ripple

- The output capacitor must be designed to fulfill mainly two requirements:
  - To keep the steady-state peak-to-peak output voltage ripple below the maximum allowed value ΔV_{opp}
  - To keep the output voltage waveform within the required regulation window [$V_o \pm \Delta V_{o\_reg}$] during the overshoot and undershoot caused by output current transients
- The output capacitor design of a buck converter will be discussed in this presentation

Output Ripple

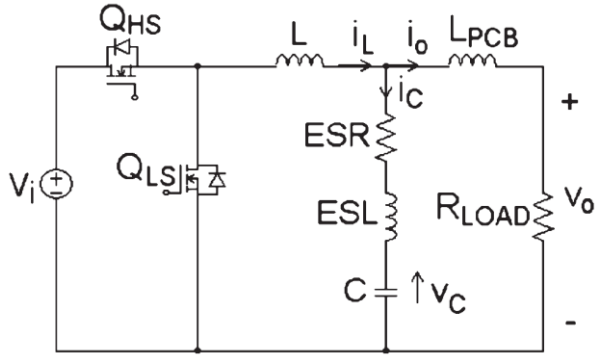
- Boundary conditions formulated separately for ESR and C of the output capacitor may lead to selection of oversized commercial components.
- Please note that there is a phase shift between the contribute of C and the contribute of ESR.
- In this presentation an approach based on Acceptability Boundary Curves which jointly considers the effect of ESR and C will be shown.

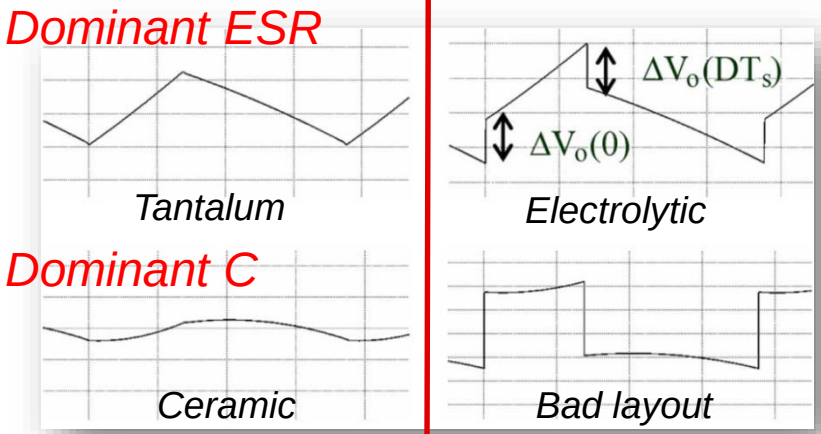


Stray Inductances in Output Ripple Analysis

- Depending on the constant ESR x C, the output voltage waveform can change from quasi-triangular to quasi-sinusoidal.
- The effect of stray inductances can be easily separated from the effect of the principal parameters ESR and C of the capacitor. In fact, stray inductances produce additive step-up and step-down effects on the output voltage, whose amplitude is given by:

$$\Delta V_o(0) = -\Delta V_o(DT_s) \cong (ESL + L_{\mathrm{PCB}})\frac{V_i}{L}$$





NO ESL

Includes ESL

Output Voltage Ripple by Chemistry

Inductor Current

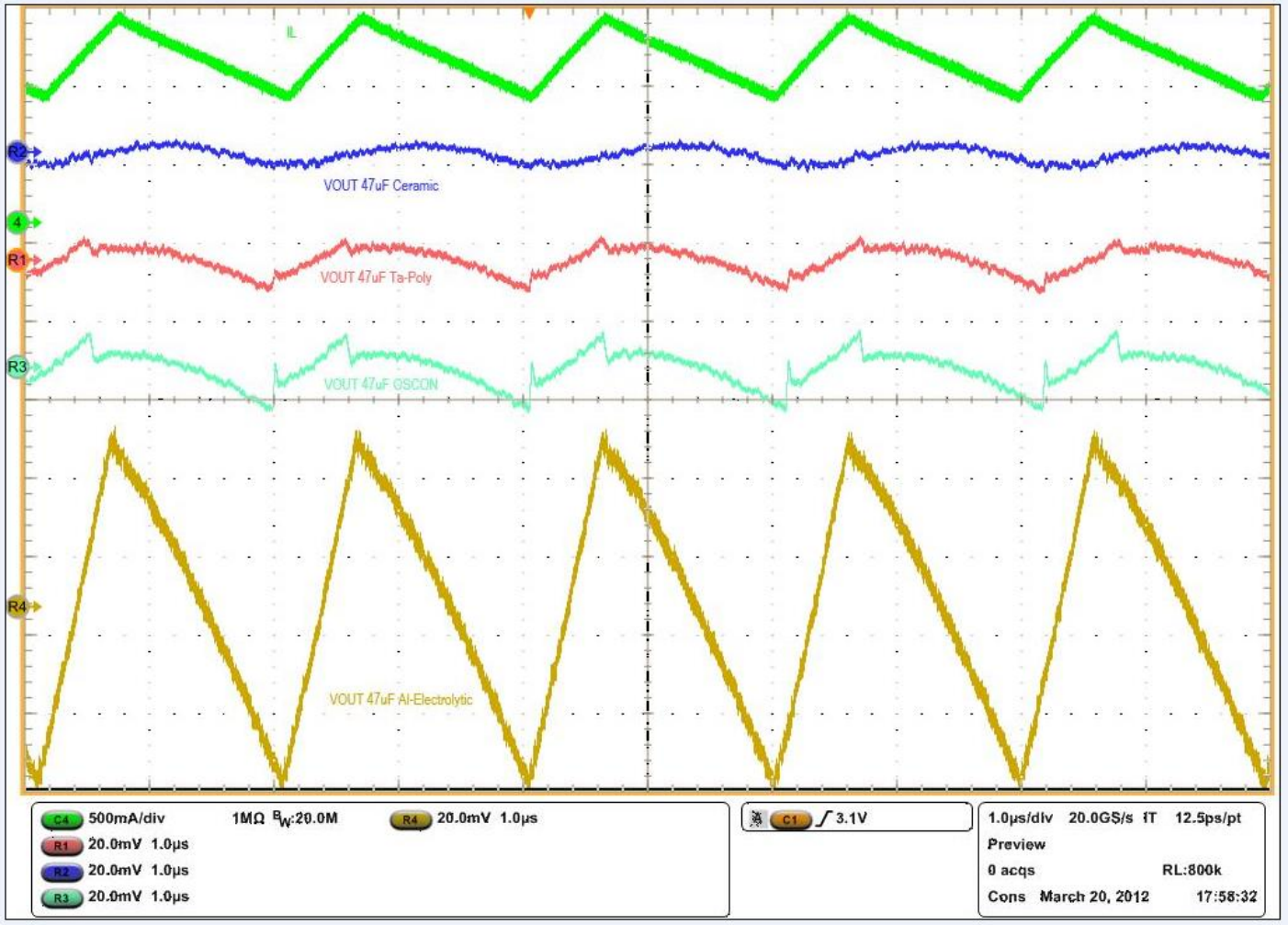
Ceramic

Tantalum Polymer

OSCON

Electrolytic

This plot shows a comparison of the output voltage ripple of a buck converter using 4 different capacitor chemistries.
All caps = 47uF.
Scale = 20mV/div



Stray Inductances in Output Ripple Analysis

- To take in account the **effect determined by the equivalent series inductance (ESL)** of the output capacitor and by the **inductance of the printed circuit board trace L_{PCB}** it is sufficient to replace the maximum allowed peak-to-peak output ripple voltage amplitude ΔV_{Opp} with the net effective peak-to-peak ripple voltage ΔV_{Oppeff} allowed to ESR and capacitance C, given by:

$$\Delta V_{\text{oppeff}} = \Delta V_{\text{opp}} - (ESL + L_{\text{PCB}})\frac{V_i}{L}$$

- If ESL and L_{PCB} are unknown, the previous formula can also be used to determine the maximum allowed ESL compatible with the ESR and capacitance C of a capacitor selected with the algorithm **not including the L_{PCB}**:

$$ESL_{\max} = \frac{L}{V_i}[\Delta V_{\text{opp}} - \Delta V_{\text{oppeff}}]$$

Output Ripple Analysis

- Current flowing into the output capacitor is given by :

$$i_C(t) = \begin{cases} -\frac{\Delta i_{Lpp}}{2} + \frac{\Delta i_{LPP}}{DT_s} t & t \in [0, DT_s] \quad \text{ON TIME} \\ \frac{\Delta i_{Lpp}}{2} - \frac{\Delta i_{LPP}}{D'T_s}(t - DT_s) & t \in [DT_s, T_s] \quad \text{OFF TIME} \end{cases}$$

- The remaining part of the peak to peak output ripple voltage can be determined by analyzing the circuit in the time intervals between switching instants and can be derived by integrating the current flowing into the output capacitor, where:

ESR contribute

Initial voltage charge

capacitance contribute

$$v_o(t) = \begin{cases} ESR\, i_C + v_C(0) + \frac{1}{C} \cdot \int_0^t i_C(\tau) d\tau & t \in [0, DT_s] \quad \text{ON TIME} \\ ESR\, i_C + v_C(DT_s) + \frac{1}{C} \cdot \int_{DT_S}^t i_C(\tau) d\tau & t \in [DT_s, T_s] \quad \text{OFF TIME} \end{cases}$$

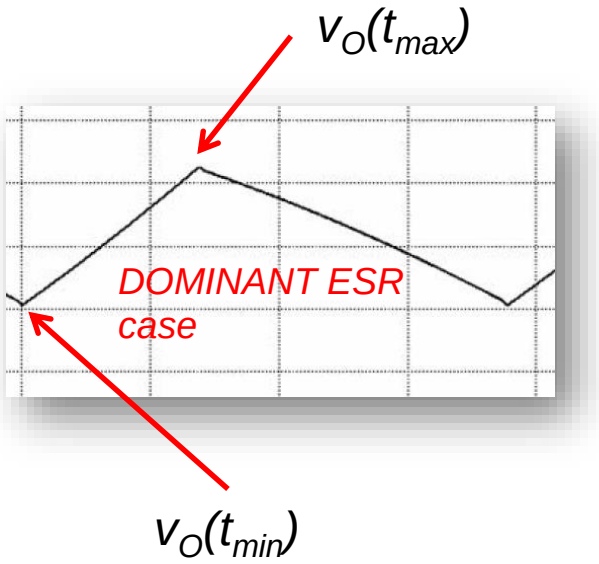
$$v_C(0) = V_o - \frac{1}{12 f_s C} \Delta i_{Lpp}(1 - 2D)$$

$$v_C(DT_s) = v_C(0) + \frac{1}{C} \int_0^{DT_s} i_C(\tau) d\tau$$

Output Ripple Analysis

- In order to determine analytical expression of output voltage ripple, maximum and minimum values of output voltage waveform must be computed.
- Instant when **minimum** occurs is given by:

$$t_{\min} = \begin{cases} -C \cdot ESR + \dfrac{D}{2 f_s} & if\ C \cdot ESR < \dfrac{D}{2 f_s} \\ 0 & if\ C \cdot ESR \geq \dfrac{D}{2 f_s} \end{cases}$$



- Instant when **maximum** occurs is given by:

$$t_{\max} = \begin{cases} -C \cdot ESR + \dfrac{D'}{2 f_s} & if\ C \cdot ESR < \dfrac{D'}{2 f_s} \\ \dfrac{D}{f_s} & if\ C \cdot ESR \geq \dfrac{D'}{2 f_s} \end{cases}$$

The analytical output ripple is given by:

$$\Delta V_{Opp} = v_O(t_{max}) - v_O(t_{min})$$

Output Ripple Analysis

- Two different **Domain Boundary Curves** (DBC) can be defined as for **D < 0.5** and **D > 0.5**
- Three different **Acceptability Boundary Curves** (ABC) can be defined for **HIGH**, **MID** and **LOW** ESR case

D<0.5	D>0.5
$R_{s-} = \frac{D'}{2Cf_s}$	$R_{s+} = \frac{D}{2Cf_s}$
$R_{i-} = \frac{D}{2Cf_s}$	$R_{i+} = \frac{D'}{2Cf_s}$

For D < 0.5 :

- ESR ≥ R_{s-} → **HIGH ESR**
- R_{i-} < ESR < R_{s-} → **MID ESR**
- ESR ≤ R_{i-} → **LOW ESR**

Please note that boundaries are duty cycle and switching frequency dependent

D<0.5		
	ΔV_{opp}	ESR
$ESR > R_{s-}$ **HIGH ESR**	$ESR\Delta i_{L\,pp}$	$ESR_H = \frac{\Delta V_{o\,pp}}{\Delta i_{L\,pp}} = R_{pp}$
$R_{i-} < ESR < R_{s-}$ **MID ESR**	$\frac{\Delta i_{L\,pp}(D'+2ESR\,f_s C)^2}{8 f_s C D'}$	$ESR_M = -\frac{1}{2 f_s C} D' + \frac{1}{f_s C}\sqrt{2 R_{pp} f_s C D'}$
$ESR < R_{i-}$ **LOW ESR**	$\frac{\Delta i_{L\,pp}(DD'+4ESR^2 f_s^2 C^2)}{8 f_s C DD'}$	$ESR_L = \frac{1}{2 f_s C}\sqrt{D(8R_{pp} f_s C - 1)D'}$

D>0.5		
	ΔV_{opp}	ESR
$ESR > R_{s+}$ **HIGH ESR**	$ESR\Delta i_{L\,pp}$	$ESR_H = \frac{\Delta V_{o\,pp}}{\Delta i_{L\,pp}} = R_{pp}$
$R_{s+} < ESR < R_{i+}$ **MID ESR**	$\frac{\Delta i_{L\,pp}(D+2ESR\,f_s C)^2}{8 f_s C D}$	$ESR_M = -\frac{1}{2 f_s C} D + \frac{1}{f_s C}\sqrt{2 R_{pp} f_s C D}$
$ESR < R_{i+}$ **LOW ESR**	$\frac{\Delta i_{L\,pp}(DD'+4ESR^2 f_s^2 C^2)}{8 f_s C DD'}$	$ESR_L = \frac{1}{2 f_s C}\sqrt{D(8R_{pp} f_s C - 1)D'}$

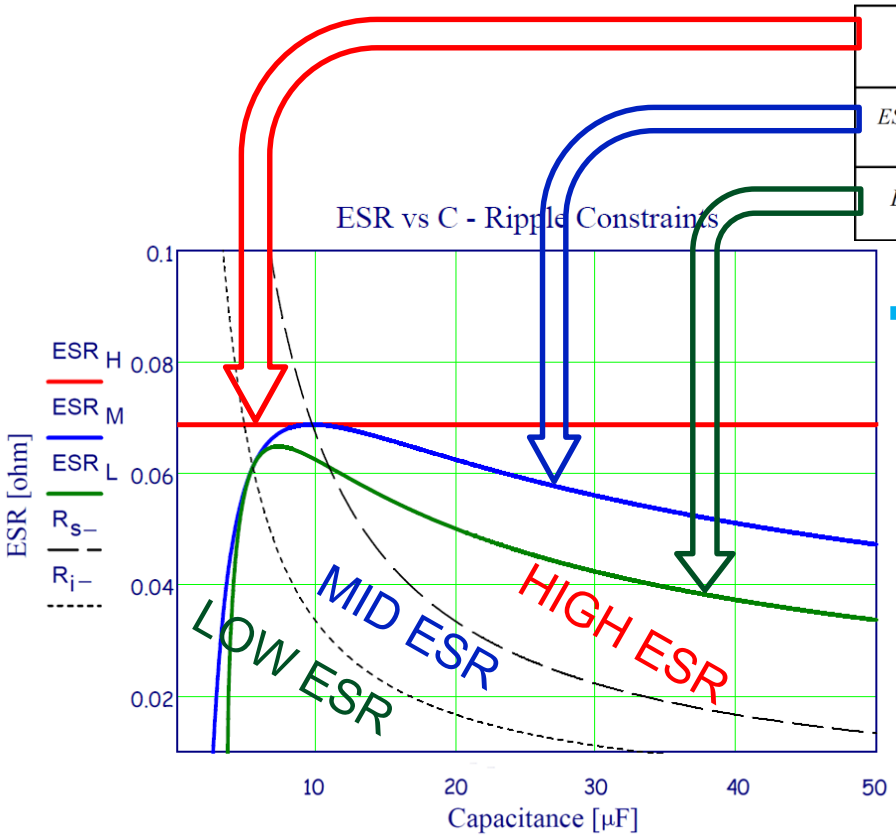
Output Ripple Analysis

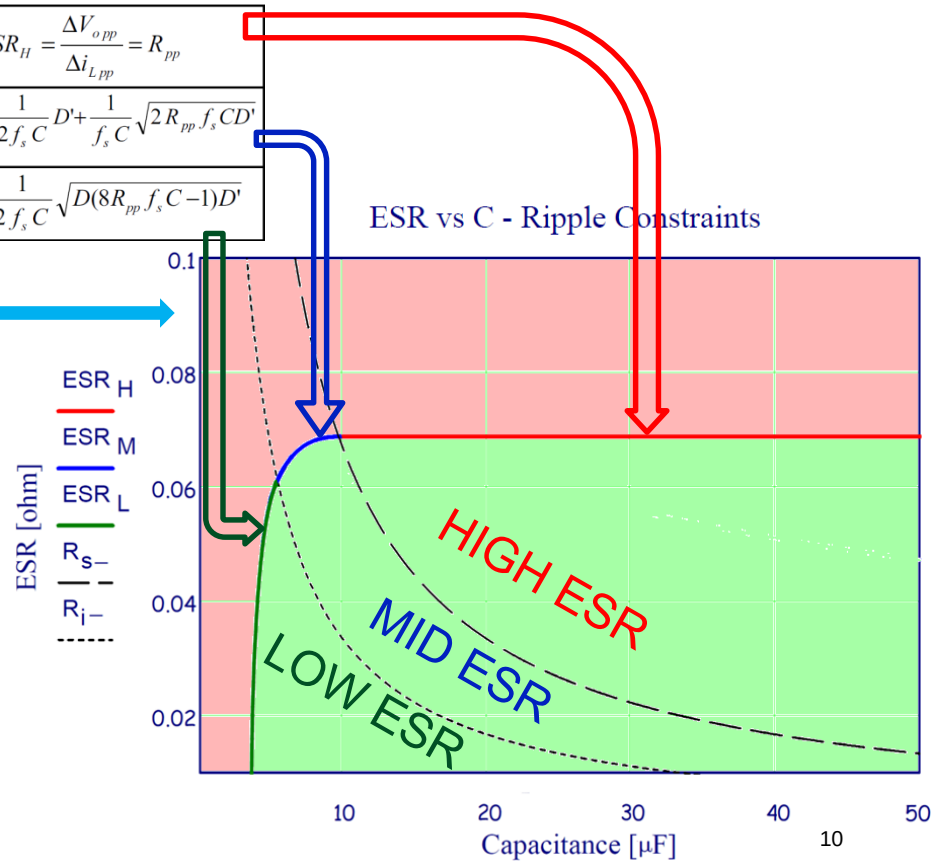
- The following figure shows Domain Boundary Curves (DBC) and the Acceptability Boundary Curves (ABC) in ESR-C plane for ***D = 33% , Δi_{Lpp} = 0.8A, ΔV_{opp_eff} = 55mV, f_S = 500kHz***. In applications where D > 0.5 the DBC are inverted.
- ABCs allow to quickly figure out real feasible capacitors representing possible design solutions **when load transient constraints are not needed**. A real capacitor whose values of ESR and C correspond to a point located below ABCs (green area) is suitable to meet ripple constraints requirements.

$$ESR_H = \frac{\Delta V_{o\,pp}}{\Delta i_{L\,pp}} = R_{pp}$$

$$ESR_M = -\frac{1}{2 f_s C} D' + \frac{1}{f_s C}\sqrt{2 R_{pp} f_s C D'}$$

$$ESR_L = \frac{1}{2 f_s C}\sqrt{D(8 R_{pp} f_s C - 1) D'}$$



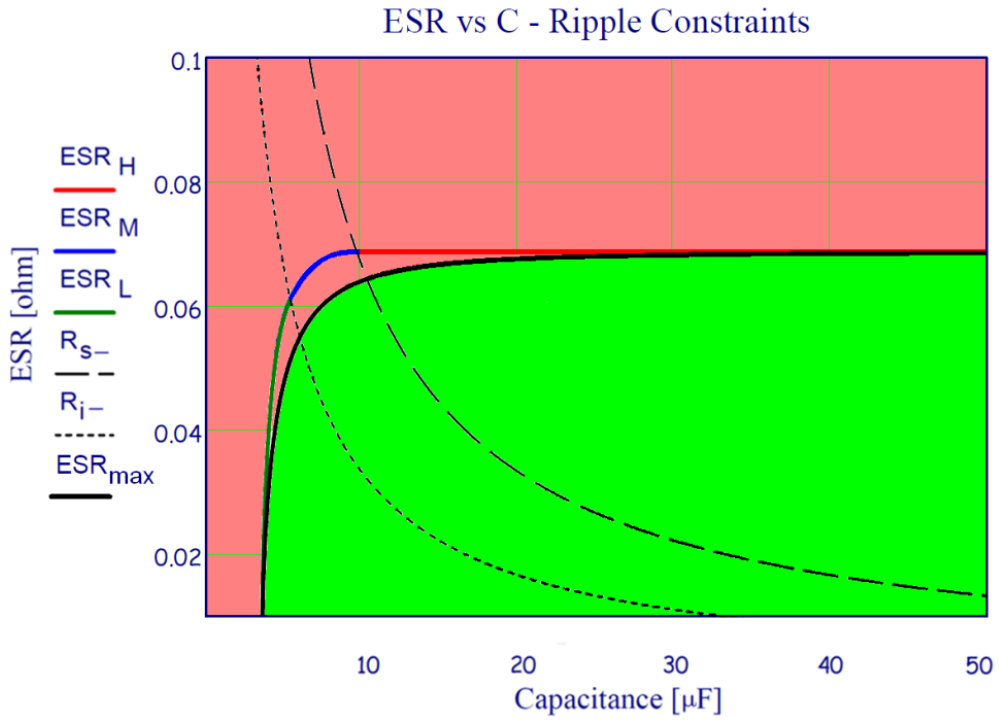


Output Ripple Analysis: Simplified Formula

- A simplified equation can be derived by calculating the fundamental component of the output ripple voltage as:

$$\Delta V_{opp} = \Delta i_{Lpp} \cdot \sqrt{ESR^2 + \left(\frac{1}{8 \cdot f_s \cdot C_o}\right)^2} \quad \Rightarrow \quad ESR_{max} = \sqrt{\left(\frac{\Delta V_{opp}}{\Delta i_{Lpp}}\right)^2 - \left(\frac{1}{8 \cdot f_s \cdot C_o}\right)^2}$$

There is an overestimation of the needed output cap nearby the MID ESR area



Thank you!