Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x

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ABSTRACT

Printed Circuit Board (PCB) layout for Switched Mode Power Supplies (SMPS) is critical to achieve proper converter operation, good thermal performance, and excellent radiated EMI performance. Optimized board layout for low radiated EMI is made very simple by the package and pin arrangement of the SIMPLE SWITCHER® Synchronous Buck Converter family LM4360x and LM4600x.

Contents

1 LM4360x and LM4600x Introduction and Layout 2
2 Buck Converter Layout Considerations 3
2.1 Identify critical paths 3
2.2 Minimize High Power High di/dt Path Loop Area 4
2.3 Minimize Area of Gate Driver Loops 5
2.4 Ground Shielding 6
2.5 Protect Sensitive Nodes 7
3 Benefits of the LM4360x and LM4600x Pin Configuration 8
4 Radiated EMI result of the LM4360x and LM4600x 9

List of Figures

1 Pin Configuration for LM4360x and LM4600x 2
2 Compact PCB Layout for LM4360x and LM4600x 2
3 Simplified Buck Converter Schematic 3
4 Buck Converter Gate Drive Circuits with Bypass Capacitors 3
5 Simplified Buck Converter Schematic Illustrating Minimized Loop Area 4
6 Large Critical Loop Area and Results 4
7 Optimized Critical Loop Area and Results 5
8 Synchronous Buck Converter Optimized Bypass Capacitor placements 5
9 Cross Section Illustration of the Two Layer Board 6
10 Cross Section Illustration of the Four Layer Board with Unbroken Ground Planes 6
11 Cross Section Illustration of the Four Layer Board with Broken Ground Planes 6
12 Radiated EMI Result from the Two Layer Board 6
13 Radiated EMI Result from the Four Layer Board with Unbroken Ground Planes 6
14 Radiated EMI Result from the Four Layer Board with Broken Ground Planes 6
15 Avoid Long Traces to the FB Node 7
16 Use Short and Thin Traces at the FB Node 7
17 Benefits of LM4360x and LM4600x Pin Configuration 8
18 LM43603 Radiated EMI Curve 9
19 LM46002 Radiated EMI Curve 9
20 LM43602 Radiated EMI Curve 9
21 LM46001 Radiated EMI Curve 9

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1 LM4360x and LM4600x Introduction and Layout

The SIMPLE SWITCHER® Synchronous Buck Converter family is an easy to use step-down DC-DC converter capable of delivering up to 3A of load current from an input of up to 60V. This family features wide input voltage range, low external component count, low quiescent current, adjustable switching frequency, synchronization, power good flag, precision enable, adjustable soft-start, tracking, PFM at light load, UVLO, over current protection and over temperature protection. It provides flexible and easy to use solutions for a wide range of applications. The devices in this family are available in an HTSSOP-16 package and are pin-to-pin compatible to each other. The pin out is designed to enable optimized PCB layout with best EMI and thermal performance. The pin configuration is shown in Figure 1 and compact layout is shown in Figure 2.

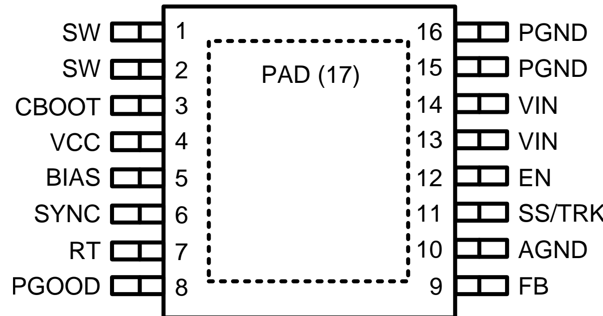

Figure 1. Pin Configuration for LM4360x and LM4600x

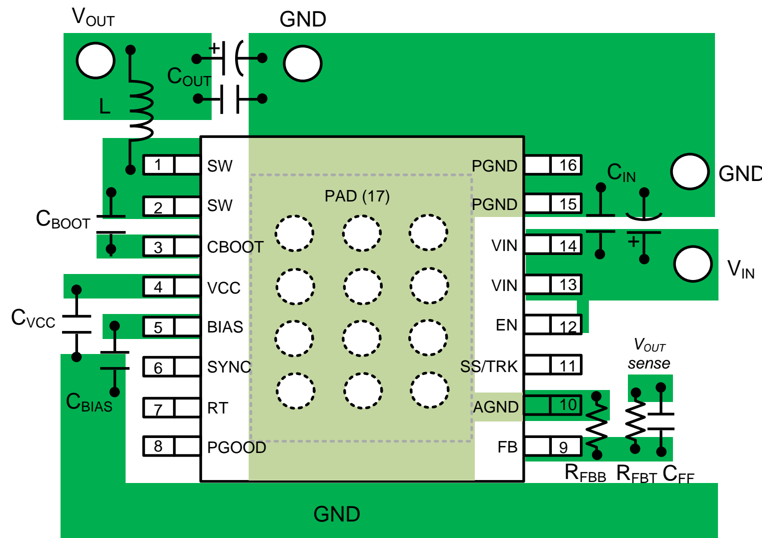

Figure 2. Compact PCB Layout for LM4360x and LM4600x

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2 Buck Converter Layout Considerations

Board layout is a critical aspect of SMPS design. The performance of an SMPS could be degraded by a poorly designed PCB. Even worse, a bad PCB layout may result in a malfunctioned converter. Due to the switching action in SMPS, large currents with fast transitions exist in the circuit. A current has to circulate through a loop and return to the source. If current transitions exist in a current loop, voltage spikes are going to be generated, v = L•(di/dt), where L is the self-inductance of the current loop and di/dt is the current transition rate. The self-inductance of a current loop is proportional to the area enclosed by it. The loops containing high di/dt current are the critical paths in SMPS PCB design. To reduce the voltage spikes and switching noises in an SMPS, the critical high di/dt paths should be identified and the area enclosed by them should be minimized.

2.1 Identify critical paths

The first step is to identify the critical paths in an SMPS.

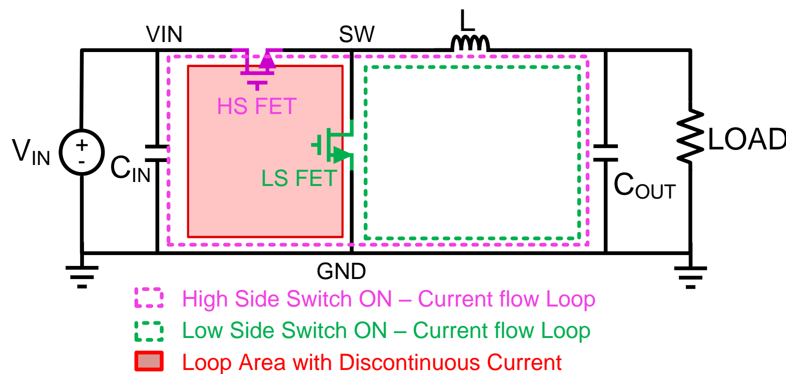

Figure 3. Simplified Buck Converter Schematic

Figure 3 shows a simplified buck converter schematic. The large current high di/dt loop in this topology is formed by the input capacitor, the high side switch and low side switches. This loop can be identified by looking at the current flow when the high side switch (HS FET) or the low side switch (LS FET) is ON. The critical path with high di/dt current is shown in solid red. The area of the red loop should be minimized by component placement and PCB layout. This is the most important high di/dt loop in a buck converter, due to large current level.

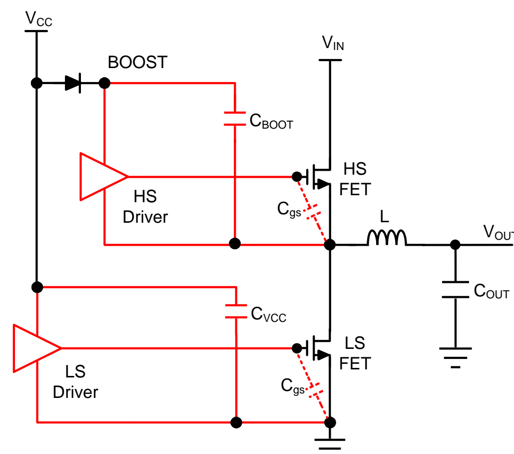

Figure 4. Buck Converter Gate Drive Circuits with Bypass Capacitors

Gate drive circuits, as shown in Figure 4, also contain high di/dt currents. They just have lower power level compared to the power stage shown in Figure 3. The gate driver loop contains the bypass capacitor (C_{BOOT} or C_{VCC}), the driver and the FET.

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2.2 Minimize High Power High di/dt Path Loop Area

Figure 5 shows, conceptually, how to minimize the critical path loop area in a buck converter.

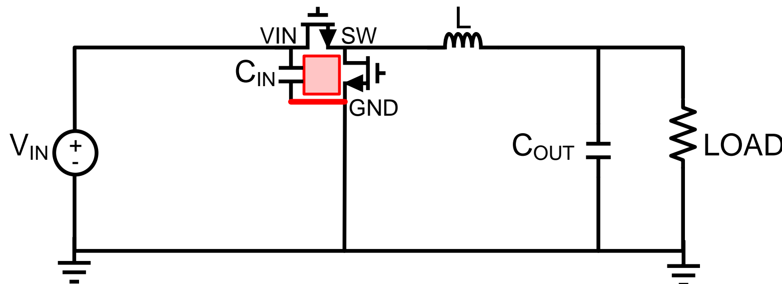

Figure 5. Simplified Buck Converter Schematic Illustrating Minimized Loop Area

The high side FET, the low side FET and the input high frequency bypass capacitor should be placed as close as possible to each other. For a synchronous buck converter, such as LM4360x and LM4600x, the high side and low side switches are integrated inside the IC. Then, the bypass capacitors should be placed as close as possible to the IC, between the VIN and GND pins.

The VIN and PGND pins of the LM4360x and LM4600x are right next to each other. This makes the placement of the input capacitor very easy and results in minimum area of the high di/dt loop.

The copper traces connecting to the bypass capacitors contain high di/dt currents. They should be short and wide traces on the same layer as the converter IC, to avoid spreading high frequency noises to other layers or planes. Avoid routing high di/dt current traces through power or ground planes.

Avoid using thin and long traces and/or vias in the connecting traces to the bypass capacitors. Parasitic inductances of the traces and vias will make the high frequency bypass ineffective. It is recommended to use short and wide traces. If vias have to be used, place multiple vias in parallel to minimize the added inductance.

Here is an example comparing the effects of two different input bypass capacitor placements on a synchronous buck converter.

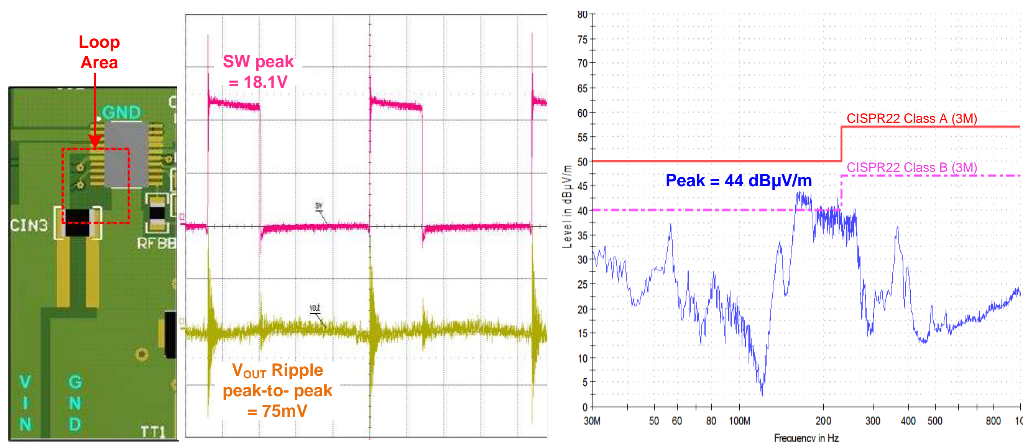

Figure 6. Large Critical Loop Area and Results

Figure 6 shows a generic synchronous buck converter PCB, waveforms measured by an oscilliscope and radiated EMI measurement data. The input capacitor is placed on the same layer as the IC, but its placement is not as close as possible to the IC pins. The high di/dt current loop area is not minimized. Because of the added loop inductance, with 12 V input the switch node rings up to 18.1 V. This ringing propagates through the parasitic parallel capacitance of the power inductor and is visible on the output. The output voltage noise is 75 mV peak-to-peak. The radiated EMI measurement shows that the class B limit is not met.

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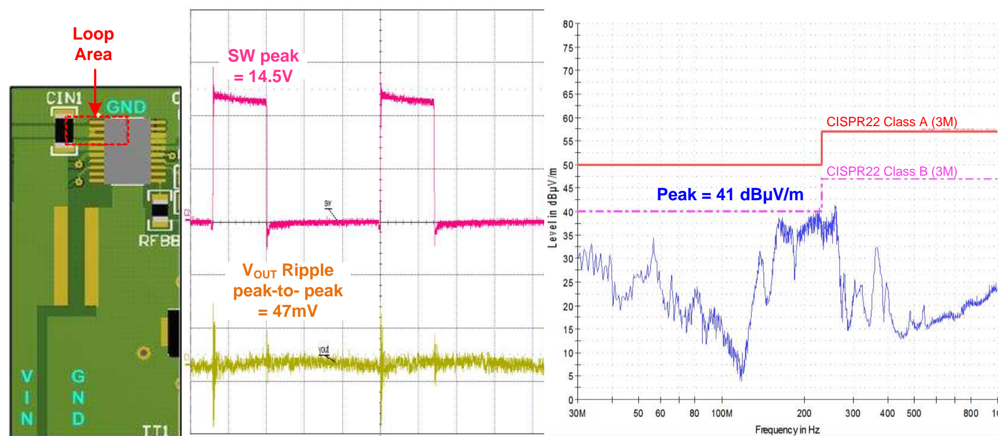

Figure 7. Optimized Critical Loop Area and Results

Figure 7 shows the same design with the input capacitor placed much closer to the pins of the IC. The area of the fast di/dt loop is minimized on this board. Under the same operation condition, the switch node ringing is reduced to 14.5 V peak (vs. 18.1 V in) and the noise on the output voltage is reduced to 47 mV peak to peak (vs 75 mV). Also, the radiated EMI is improved by 3 dBµV/m.

2.3 Minimize Area of Gate Driver Loops

In a synchronous buck converter, the high side switch gate driver connects to the C_{BOOT} through BOOT and SW pins and the low side switch gate driver connects to the C_{VCC} through VCC and GND pins. To minimize the driver loops, the bypass capacitors C_{BOOT} and C_{VCC} should be placed as close as possible to corresponding pins, as shown in Figure 8. The traces to the bypass capacitors should be short and wide.

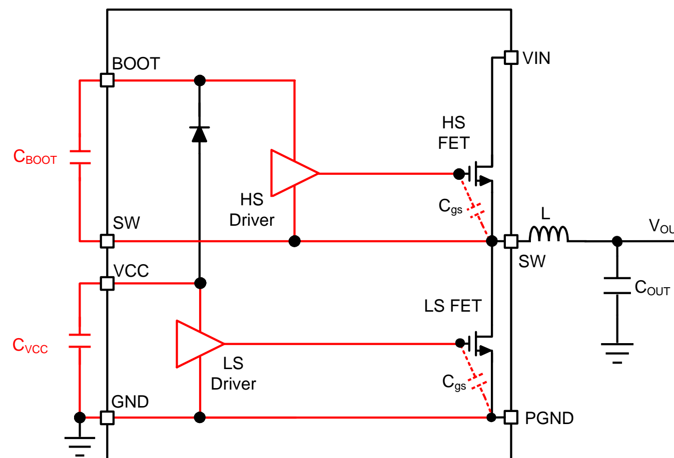

Figure 8. Synchronous Buck Converter Optimized Bypass Capacitor placements

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2.4 Ground Shielding

Better EMI results can be achieved by adding an unbroken ground plane as a middle layer in the PCB. If the IC is placed on the top layer and the high di/dt paths are routed on the top layer, the ground plane at the midlayer allows a mirror return current to be formed right underneath a top layer current. The mirror current path minimizes the current loop area and the magnetic field generated by the two opposite direction currents will be almost canceled.

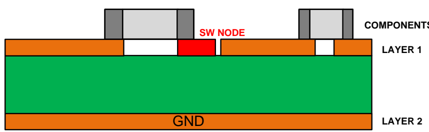

Figure 9. Cross Section Illustration of the Two Layer Board

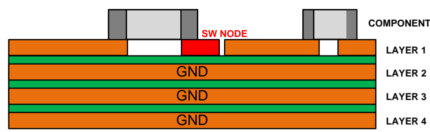

Figure 10. Cross Section Illustration of the Four Layer Board with Unbroken Ground Planes

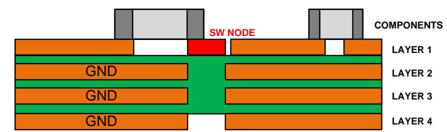

Figure 11. Cross Section Illustration of the Four Layer Board with Broken Ground Planes

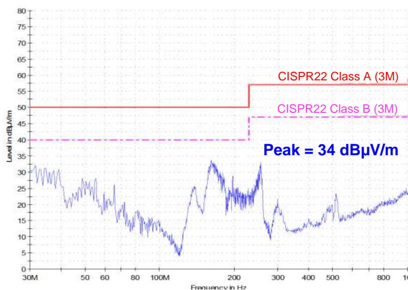

Figure 12. Radiated EMI Result from the Two Layer Board

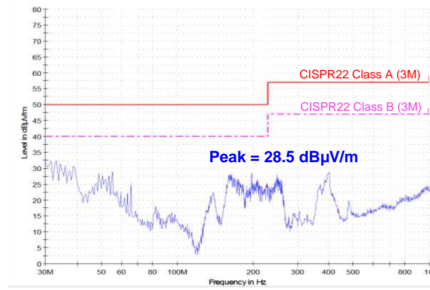

Figure 13. Radiated EMI Result from the Four Layer Board with Unbroken Ground Planes

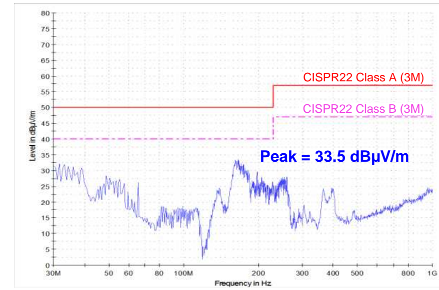

Figure 14. Radiated EMI Result from the Four Layer Board with Broken Ground Planes

A generic buck converter was used as an example to test the effectiveness of ground planes in improving EMI performance. The radiated EMI data were measured from three versions of the same boards, with identical top and bottom layer layouts, building materials, and operating condtions:

1. A two-layer board with no ground plane shielding, as illustrated in Figure 9
2. A four-layer board with two unbroken ground planes as midlayers, as illustrated in Figure 10
3. A four-layer board with two ground planes as midlayers, but each has a rectangular cut right underneath the SW node, as illustrated in Figure 11.

The corresponding EMI measurement data are shown in Figure 12, Figure 13 and Figure 14.

The four-layer board with two shielding layers in the middle achieved 5 dBµV/m in noise reduction, compared to the two-layer board. The shielding was not as effective when the plane is broken, even though it was a four-layer board, the performance was comparable to the two-layer design. It is important to avoid breaking the copper of the shielding plane, especially right underneath the noisy traces.

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2.5 Protect Sensitive Nodes

Protecting sensitive nodes is also very important for SMPS layout. One such node is the feedback (FB) pin. The FB node is a high impedance node. Avoid placing the resistor divider far away from the FB node and connecting FB node with long traces, as shown in Figure 15. To minimize the parasitic capacitance and noise pickup by the trace to FB node, the FB trace should be short and thin. As shown in Figure 16, it is recommended to place the resistor divider as close as possible to the FB pin and route a thin trace from output voltage sense away from noisy path, preferably from the other side of a shielding plane.

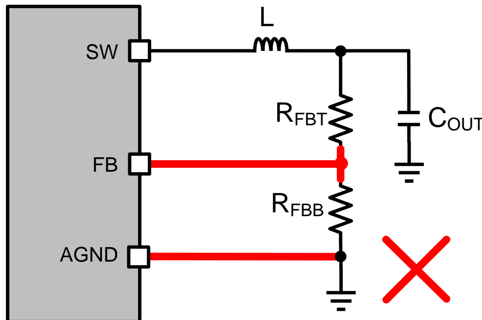

Figure 15. Avoid Long Traces to the FB Node

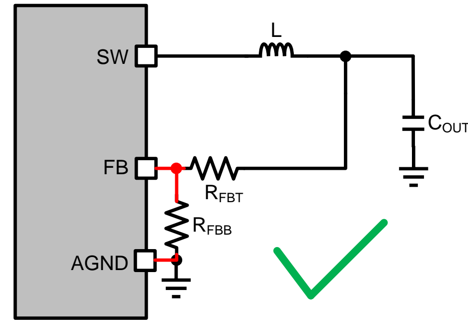

Figure 16. Use Short and Thin Traces at the FB Node

Other sensitive circuits can be the compensation network, voltage/current sensing paths, frequency setting, monitoring and protecting circuits. Sensitive circuits should be placed away from noisy paths. It is good practice to shield sensitive signal traces by ground or power planes. Circuit design and PCB design are simplified when the LM4360x and LM4600x family integrates compensation network, current sensing, monitoring and protecting circuits inside the IC.

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3 Benefits of the LM4360x and LM4600x Pin Configuration

The pin configuration of an SMPS IC should consider the PCB layout for EMI reduction and thermal performance. It should enable proper bypass capacitor placement. It should keep sensitive pins away from noisy pins, and allow large copper area for heat sinking and shielding.

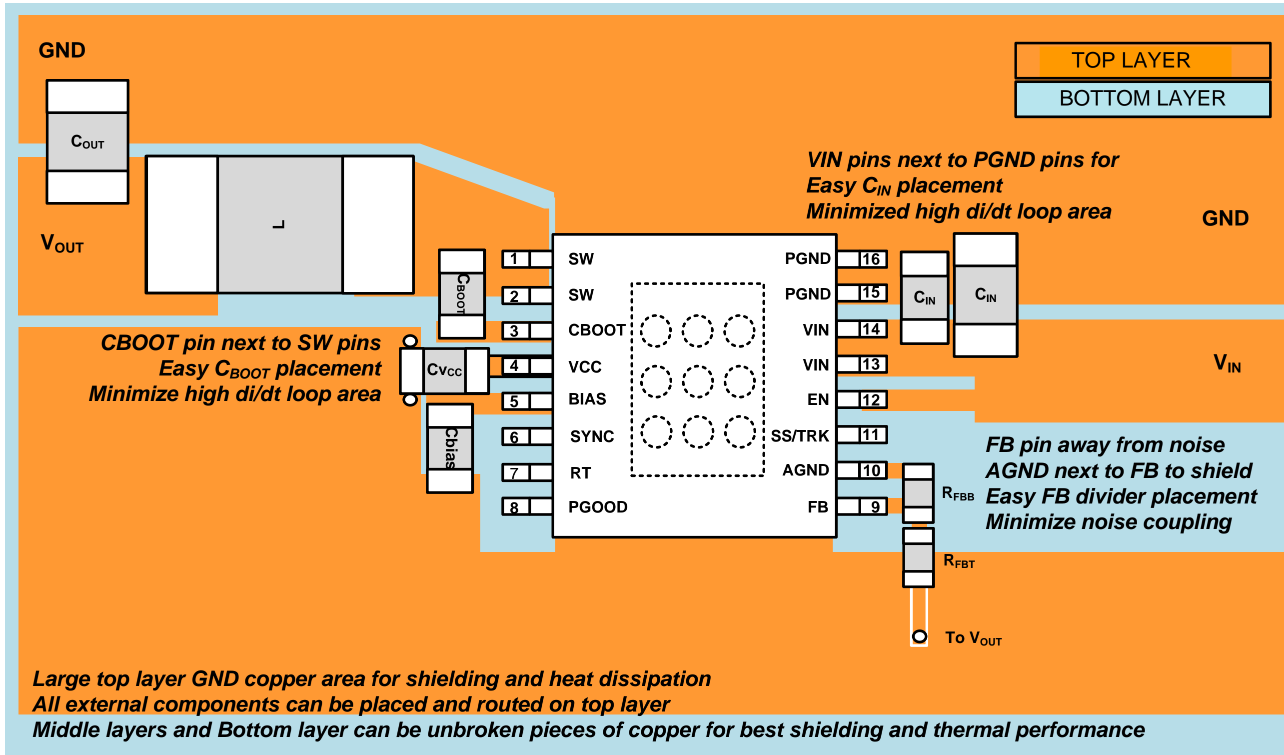

Figure 17. Benefits of LM4360x and LM4600x Pin Configuration

As shown in Figure 17, benefits of the LM4360x and LM4600x pin out include:

- All the converters in the LM4360x and LM4600x family are pin-to-pin compatible. PCB design can be easily scaled to different voltage and current levels.
- VIN and PGND pins are next to each other. The input capacitor can be placed as close as possible to the IC to minimize the high di/dt loop area. Noise generation from switching action is minimized.
- BOOT pin is next to SW pin, allowing CBOOT to be placed as close as possible to these two pins to minimize noise generated by high side FET driver.
- The SW node is on the opposite side of VIN and GND, instead of in between VIN and GND pins. Short and wide traces can be used to route VIN, GND to the input capacitor and SW to the inductor on the same layer as the IC. The SW node area, which contains high frequency noises, can be as small as possible.
- The sensitive FB pin is at the corner of the IC and far away from noisy pins. AGND pin is placed next to FB. This provides additional shielding. It also allows for resistor divider to be placed as close as possible to the FB and AGND pins, making the FB node really small and immune to noise.
- Internal compensation, current sensing, monitor and protection circuits. Circuit design and PCB layout are simplified.
- All external components can be placed and routed on the same layer as the IC. The other layers can be a full sheet of unbroken copper for the best heat dissipation and shielding.

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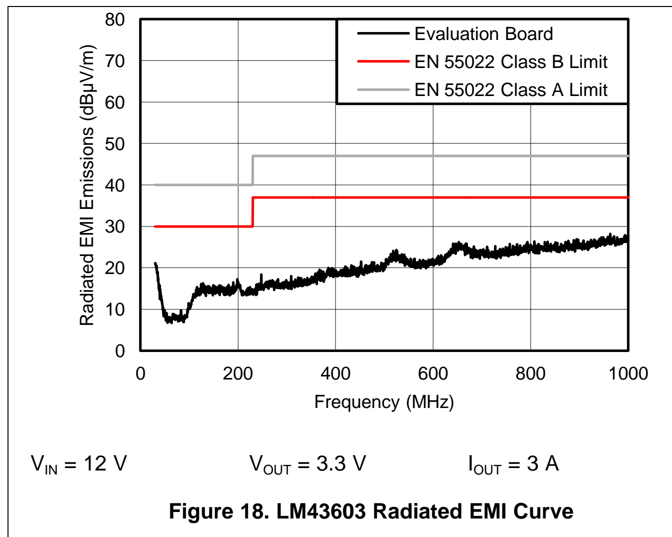
4 Radiated EMI result of the LM4360x and LM4600x

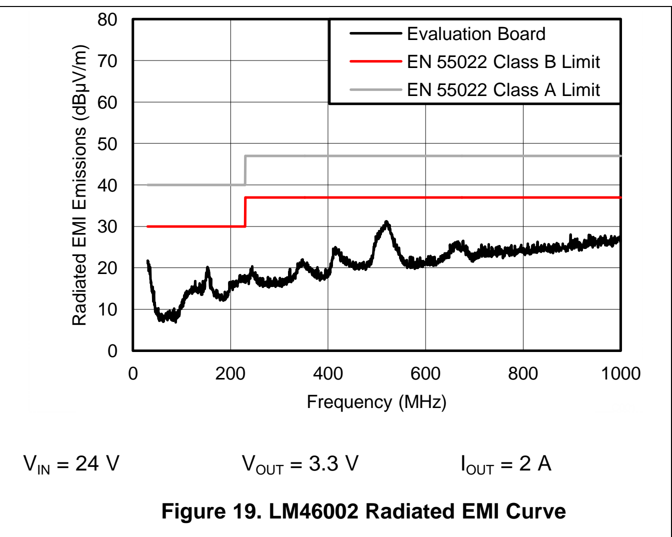
Here are the CISPR22 Radiated EMI scans performed on the LM4360x and LM4600x standard EVM, which can be ordered through ti.com. These tests were performed in a third party certified 10 meter EMI Chamber. The CISPR22 Class B limit is passed, with plenty of margin, without additional input filters.

For more plots, please see all of the family datasheets or visit simpleswitcher.com.



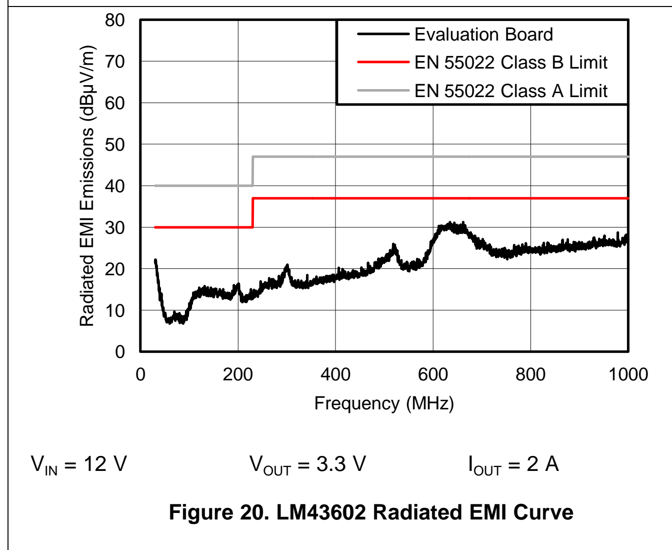
V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 3 A

Figure 18. LM43603 Radiated EMI Curve



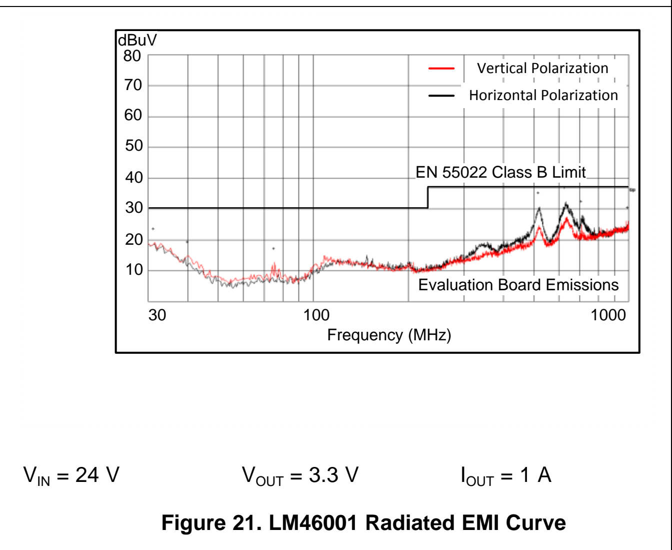
V_{IN} = 24 V V_{OUT} = 3.3 V I_{OUT} = 2 A

Figure 19. LM46002 Radiated EMI Curve



V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 2 A

Figure 20. LM43602 Radiated EMI Curve



V_{IN} = 24 V V_{OUT} = 3.3 V I_{OUT} = 1 A

Figure 21. LM46001 Radiated EMI Curve

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Revision History

Changes from Original (September 2014) to A Revision	**Page**
• Added list of figures in the TOC	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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