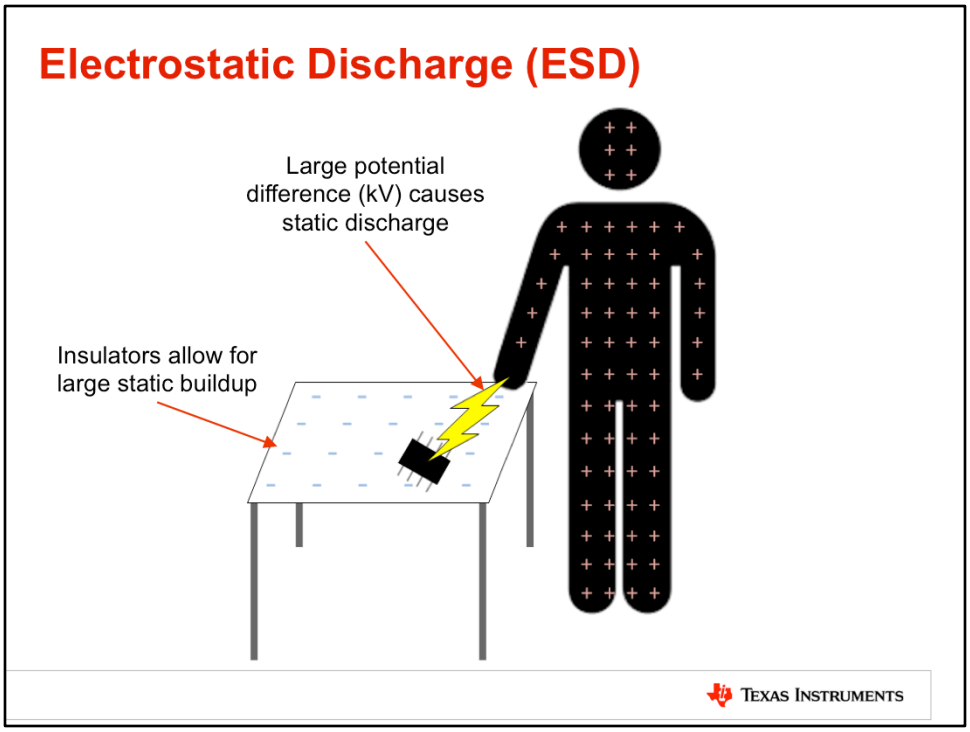
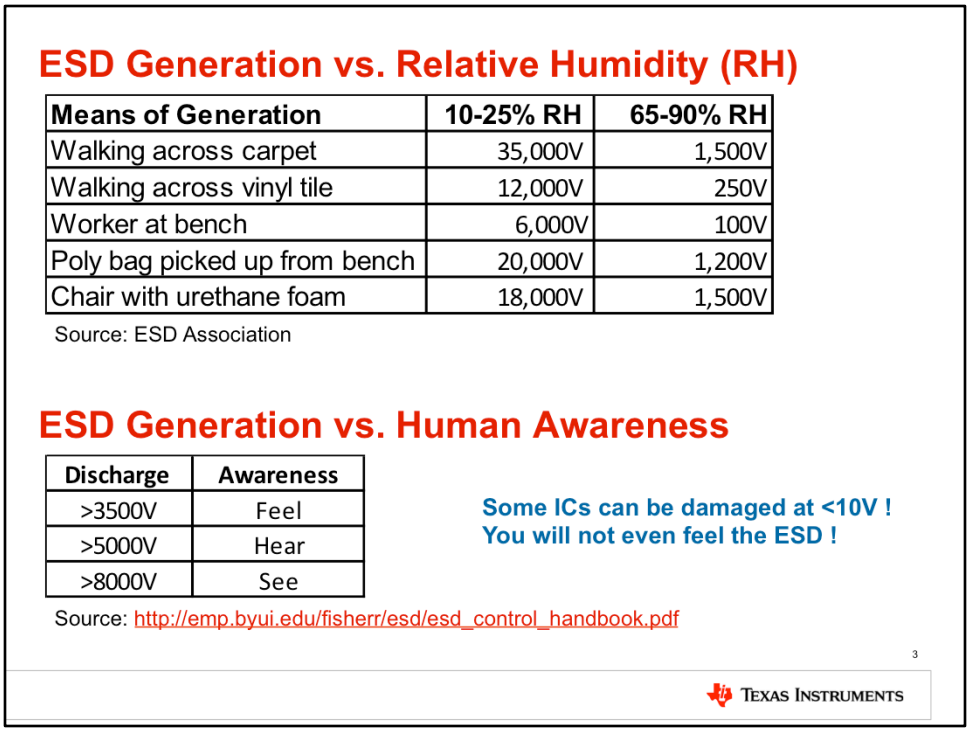
Hello, and welcome to the video for the TI Precision Lab discussing electrostatic discharge, or ESD. In this video we'll explain how ESD can damage semiconductor components. We will also give detail on internal ESD protection circuits that are included in semiconductor devices. Finally, we will explain how ESD performance is characterized so that the robustness of the device is understood.



Many common items can develop a static electrical charge. Insulators are especially prone to developing large static charges. Some materials tend to become positively charged and others become negatively charged. Whenever two items with a charge imbalance are brought in close proximity, you can have a sudden flow of electricity between the two objects, called an electrostatic discharge, ESD. ESD can show up as a visible spark and often has voltage levels in the thousands of volts. From a semiconductor perspective, ESD is the most common way that devices are damaged.



The table at the top of this slide lists some materials that generate significant static charges. Also notice that the static charge is dependent on the relative humidity. Lower relative humidity generates more static charge.

The table at the bottom of the slide shows ESD discharge voltages vs. human awareness. Notice that when you can see an ESD “spark” the voltage is very large, at 8000V or more.

Typical IC Device Sensitivity Thresholds

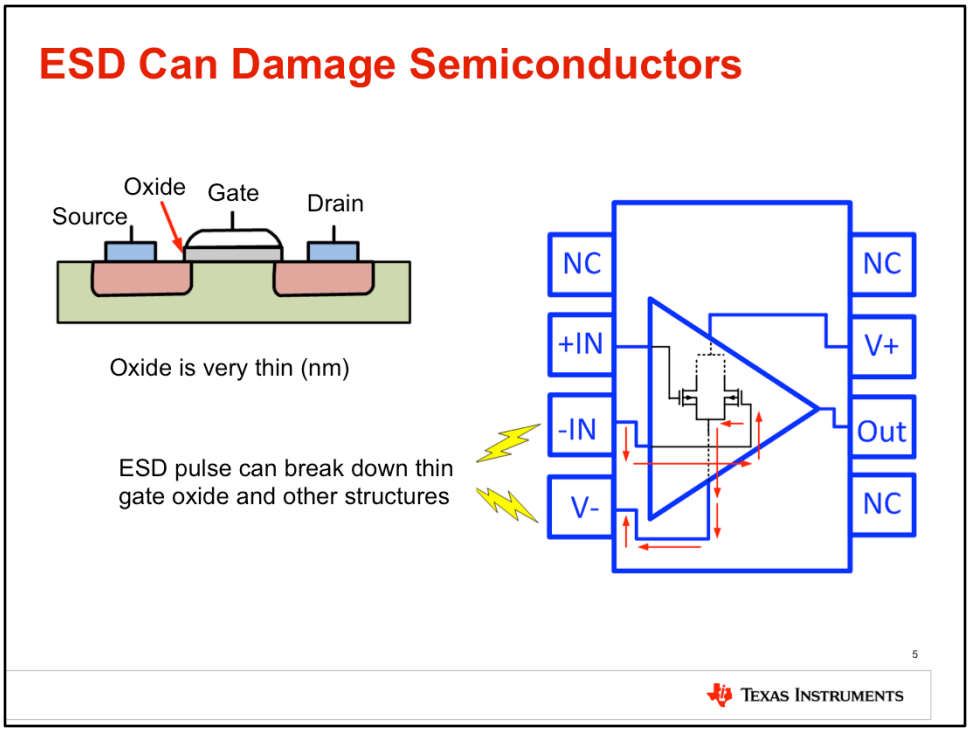
Device Type	Threshold Susceptivity (V)
MOSFET	10-100
VMOS	30-1800
NMOS	60-100
GaAsFET	60-2000
EPROM	100+
CMOS	200-3000
JFET	140-7000
SAW	150-500
Op-AMP	190-2500
Schottky Diodes	300-2500
Film Resistors	300-3000
Bipolar Resistors	300-7000
ECL	500+
SCR	500-1000
Schottky TTL	500-2500

Source: http://emp.byui.edu/fisherr/esd/esd_control_handbook.pdf

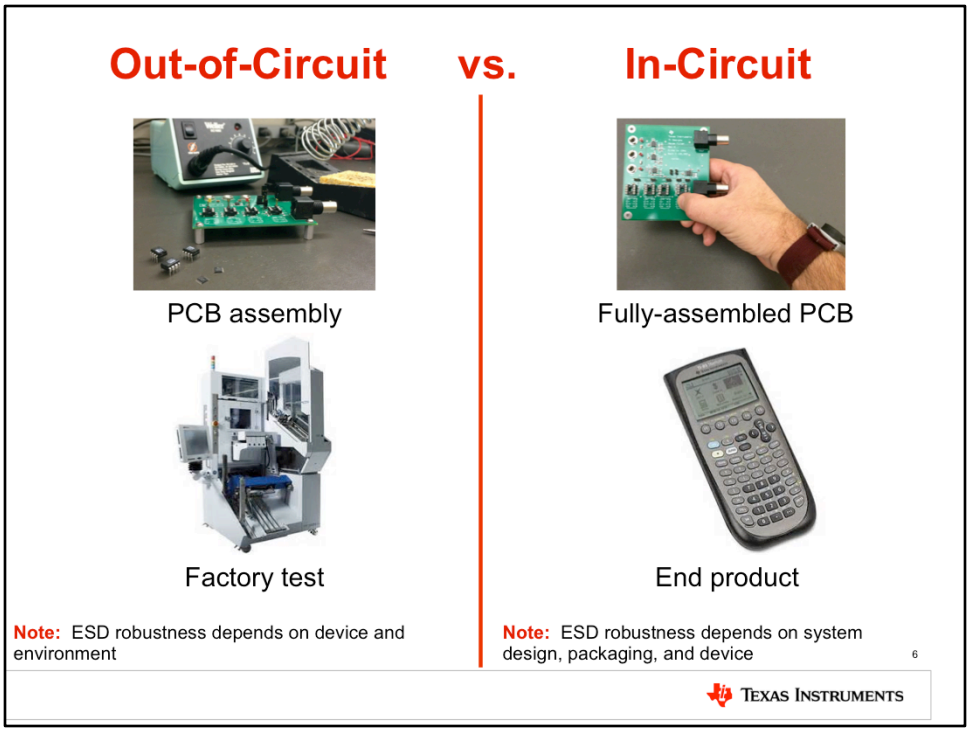
4

Texas Instruments

Different device types are susceptible to different levels of ESD voltage. Some devices, such as MOSFETs, are susceptible at very low voltages. We will see later that ESD protection circuits are used inside most semiconductor devices to enhance ESD robustness. The ESD robustness of a MOSFET can be improved from only ten volts to thousands of volts with additional ESD protection circuits.



Let's look more closely at the typical way in which semiconductor devices are damaged by ESD. Consider a large ESD potential, or voltage, which is applied between the inverting input and negative supply pin of an op amp. This places a large voltage from the gate to the source of one of the input MOSFETs, which can cause damage to the device. Keep in mind that the thickness of the MOSFET gate oxide may only be a few nanometers, making it very susceptible to this kind of damage.



There are two main categories of ESD events for semiconductor devices. An "out of circuit" ESD event can occur to a loose device; that is, a device before it is soldered to a printed circuit board. Out of circuit events can happen during manufacturing, factory test, or the assembly process. In general, factory test and manufacturing processes are designed to minimize exposure to ESD.

An "in-circuit" ESD event refers to damage caused on a fully assembled PCB, or end product. In this case the product packaging, product design, and the device's own robustness determine the ESD susceptibility of the product.

The ESD protection circuits that are included in the device are intended to protect against **out-of-circuit** events.

There are some general precautions that can be followed to minimize ESD damage to devices and assembled products. In general, these precautions use resistive materials to dissipate charge. For example, the anti-static wrist strap shown in the picture allows a controlled discharge of static electricity to ground. Typically the impedance of antistatic materials is in the mega ohms. Note that the anti-static bag, box, and work surface also contain resistive materials that are intended to slowly neutralize charge.

Characterization of Device ESD Robustness

Comprehensive test of device
- Using automated equipment
- Most specified parameters tested

Apply ESD Pulse
- Simulator generates repeatable pulses
- Different levels are applied, 1kV, 2kV…
- Different pin combinations are tested

Repeat Comprehensive Test
- Look for failures
- ESD specification set by highest pulse that doesn't damage device

ESD Simulator

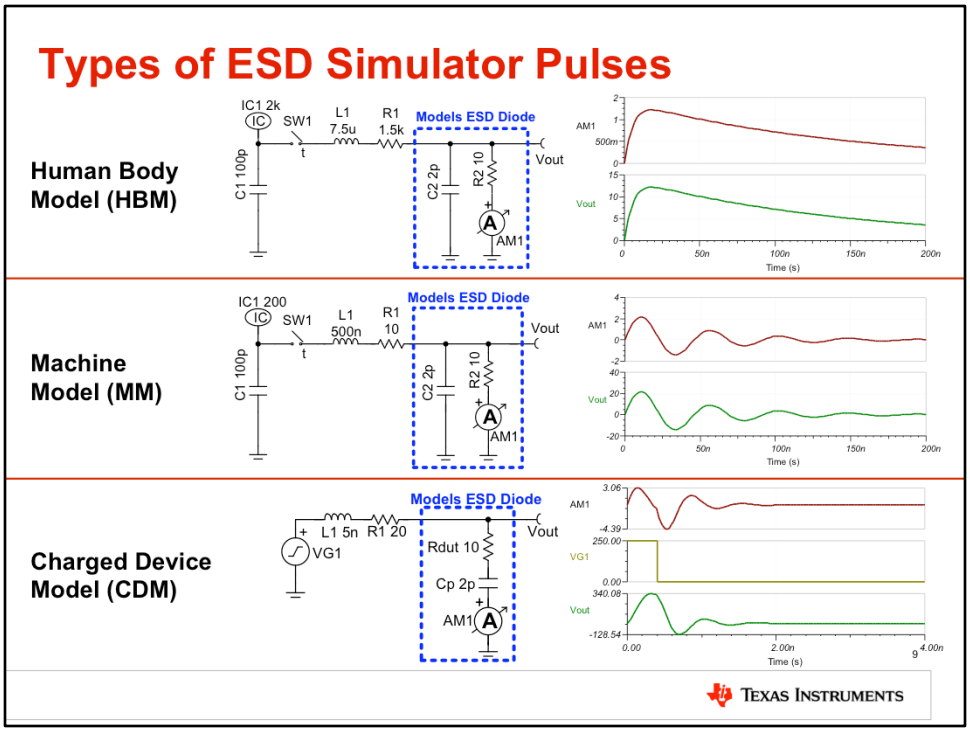
8

Texas Instruments

During the initial development of a semiconductor product the ESD robustness is characterized. First, a statistically significant sample of devices is fully tested using automatic test equipment. Generally, most of the data sheet parameters are measured during this automated test.

Second, a specialized ESD test system is used to apply a simulated ESD pulse to the device. The specific characteristics of the ESD pulse are controlled by the test hardware. For example, the amplitude and ESD model can be selected. Various ESD models will be discussed later, but in short the ESD model sets the capacitance, inductance and charge of the ESD pulse to simulate a real world ESD event. During the test the ESD pulse is applied to many different combinations of device pins for a significant sample of devices. Also, different levels of ESD pulses are applied to the device; for example, 1kV, 2kV, 3kV, and so on.

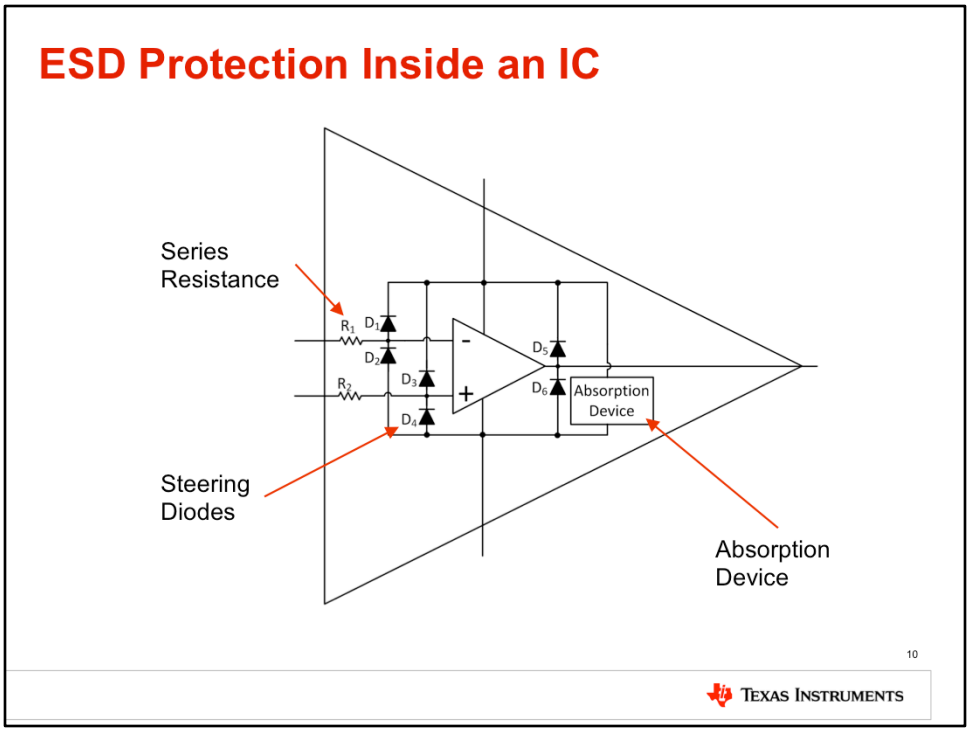
Finally, the comprehensive test is repeated on the devices. The ESD rating of the device is determined by the highest ESD level that all devices in the sample pass. This ESD rating is listed in the absolute maximum rating table of the data sheet.



3 different models are used to generate controlled ESD pulses. The "Human Body Model," or HBM, is first and the most common model developed for ESD emulation. This model attempts to emulate the ESD discharge that could occur when a human touches an microelectronic device. Typical HBM voltage levels range from 1kV to 5kV.

The "Machine Model," or MM, is also called the zero ohm model because it simulates a very low impedance discharge of static charge to ground. The MM is meant to simulate a static discharge in a metal handler or automatic assembly equipment. The Machine Model has in most cases been replaced by the Charged Device Model.

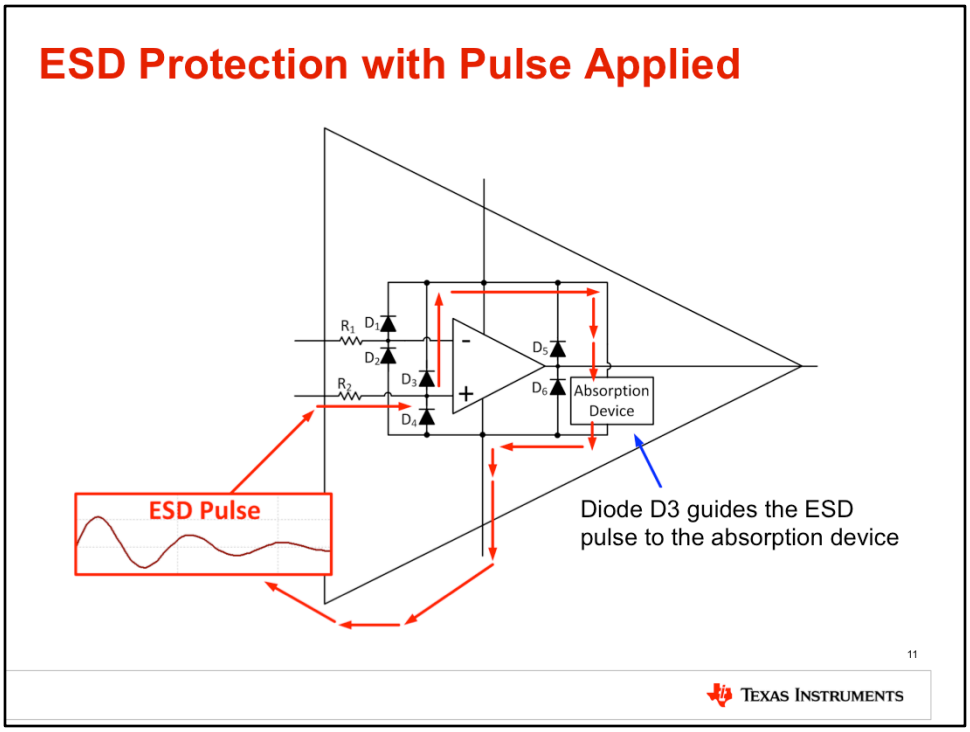
The "Charged Device Model," or CDM, is designed to accurately simulate the test and assembly environment, for example, the static charge developed when a device slides down shipping tubes. CDM voltages are typically in the hundreds to thousands of volts. CDM currents are higher than HBM currents because the current limiting resistance is much smaller.



Here we illustrate the ESD protection circuits commonly used on semiconductor devices. In this case an op-amp is shown, but similar ESD protection is used on other types of devices.

Remember that this type of ESD protection is intended to protect the device from an "out of circuit" ESD event. In other words, these structures are intended to protect the device during the test, assembly, and manufacturing process. They are also effective for ESD protection in unpowered systems, but they may actually cause issues such as latch-up in powered systems. The video series on electrical overstress will cover this topic in much more detail.

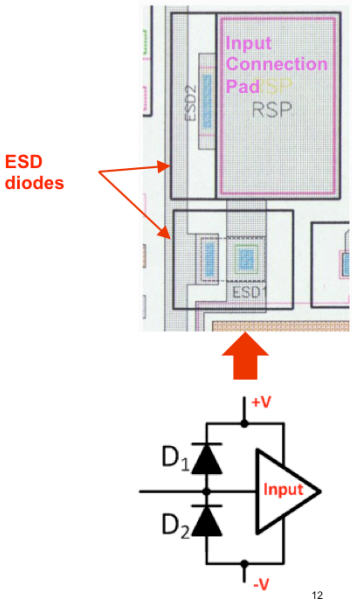
Three common structures used in ESD protection are the series resistance, steering diodes, and absorption device. The steering diodes turn on and direct the ESD pulse away from the sensitive circuit elements to the absorption device. The absorption device absorbs the energy of the ESD pulse and limits the voltage level to prevent damage. The series resistance limits the input or output current. Note that a larger series resistance offers more protection but often degrades other key parameters such as noise or maximum output current. This practical limitation on resistance may affect the ESD robustness of some devices.



Let's examine how the ESD protection structures work. In this example, an ESD pulse is applied between the non-inverting input pin and the negative power supply. In the real world this could happen by improper handling of the device; for example, assembling a PCB on a non-static safe work surface. Notice, for this example that diode D3 becomes forward biased and "steers" the ESD pulse to the absorption device. The absorption device is designed to limit the voltage and absorb the energy of the ESD pulse. Note that if the ESD pulse were applied to different pins, different diodes would turn on and steer the pulse to the absorption device. Also, notice that the input resistance R2 limits the input current from the ESD pulse. A larger value of R2 will make the circuit more robust, but may introduce errors from bias current and noise, and may also affect frequency response.

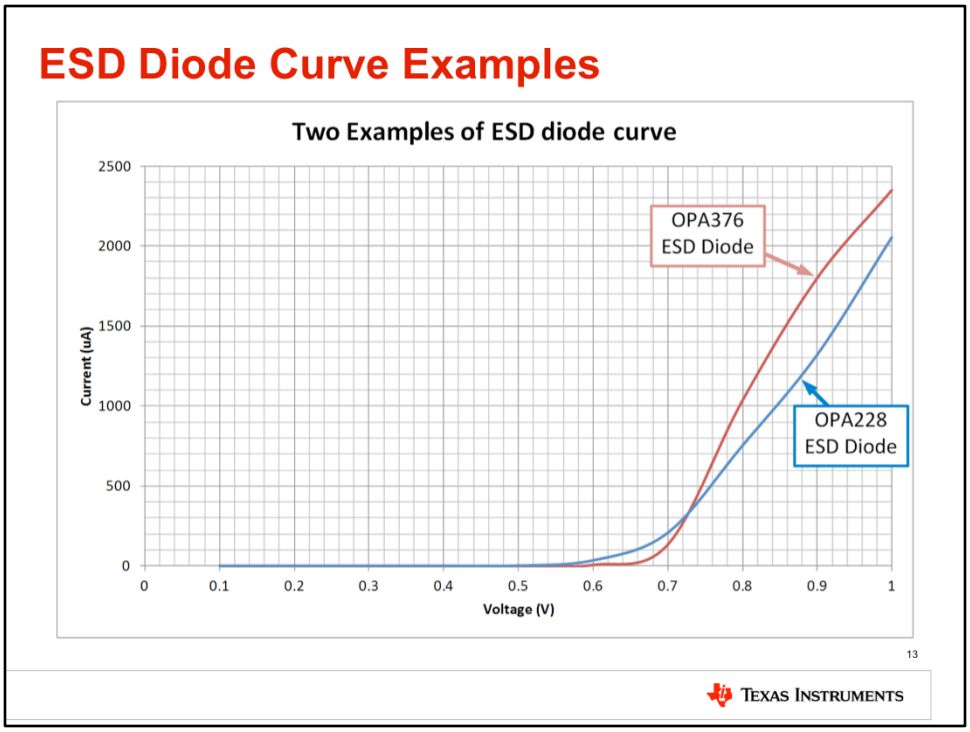
ESD Diode Specifications

Specification	Typical Value
Diode Drop (250mA)	0.7 V
Diode Drop (2A)	1 V
Pulse Current	A (for ns)
Continuous Current	10 mA
Leakage Current	0.5 nA (25°C, typical) 500 nA (125°C, typical)
Parasitic Capacitance	1 pF to 2 pF

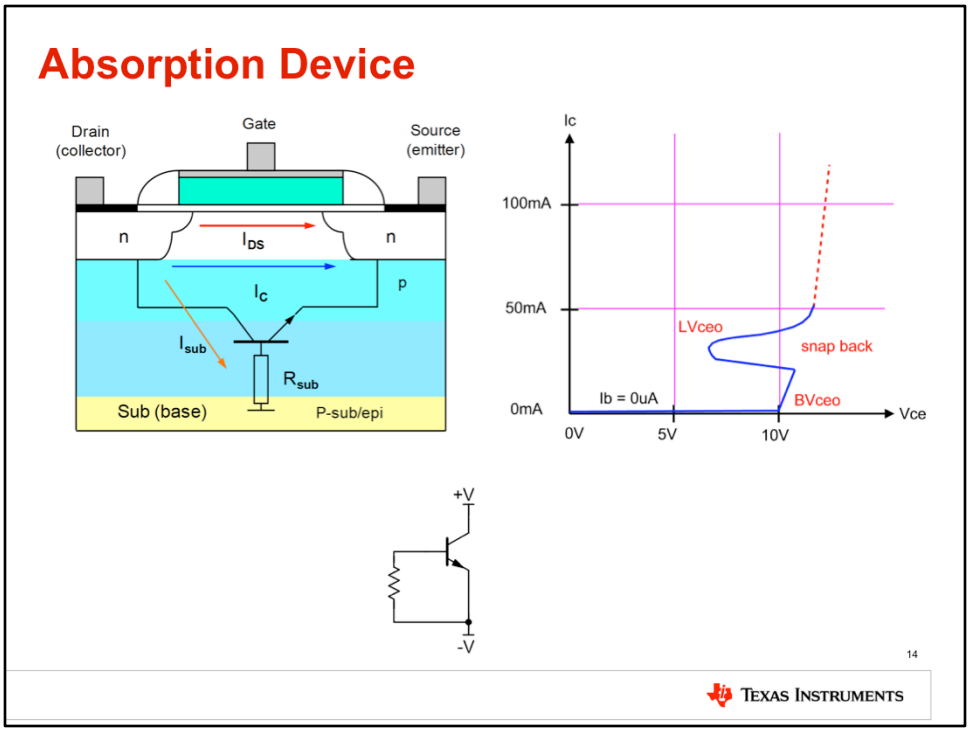


Texas Instruments

These specifications are meant to give a general idea of the ESD diode's performance. Actual diodes will very depending on the device design and the process used. One key thing to notice is that the diode drop is about 0.7V with significant current. This diode is designed to take amps of pulse currents for only a few nanoseconds, as is typical with ESD pulses. However, they are rated for only 10mA of continuous current. These diodes also have a reverse leakage current that may be less then a nano-amp at room temperature, but could be hundreds of nano-amps at high temperatures. In fact, leakage current from ESD diodes makes up the majority of the "bias current" of CMOS devices. Finally, it should be noted that the ESD diodes have parasitic capacitance in the low pico-farads.



Here we take a look at the I-V characteristic for the ESD diodes in two different op amp ICs. Notice that at low currents, the forward drop is about 0.7 V and at high current the drop increases to about 1V. Understanding the ESD diode characteristics will become useful when investigating electrical overstress issues in later videos.



We previously discussed the absorption device only in a very general sense. The absorption device is a parasitic bipolar device that is formed vertically with regards to the substrate. Normally, this device is reverse biased so that no base current flows. As the voltage across the device increases, the Collector-to-Emitter reverse breakdown is approached. Increasing the voltage beyond the breakdown level causes a rapid increase in current. Collector current will increase until a point where a "snap back" takes place. Beyond the snap region, current again begins to rapidly increase. If there isn't another source of resistance in the transistor's path to limit the current, it can increase to the point where the thermal generation results in excessively high temperatures and transistor melt down. Usually the emitter ends up spiking through the base and shorting to the collector forming a permanent short circuit.

The absorption device is designed to clamp the supply voltage during an **out-of-circuit** ESD event to prevent damage. Once the event ends, typically after a few nano-seconds, the absorption device turns off since there is no power supply connected to the device. On the other hand, if the absorption device turns on for an **in-circuit** event, it will remain on and in a low impedance state until power is removed from the circuit. Thus, it is imperative that the absorption device is not allowed to turn on during in-circuit electrical overstress events. This topic is the focus of the next video series.

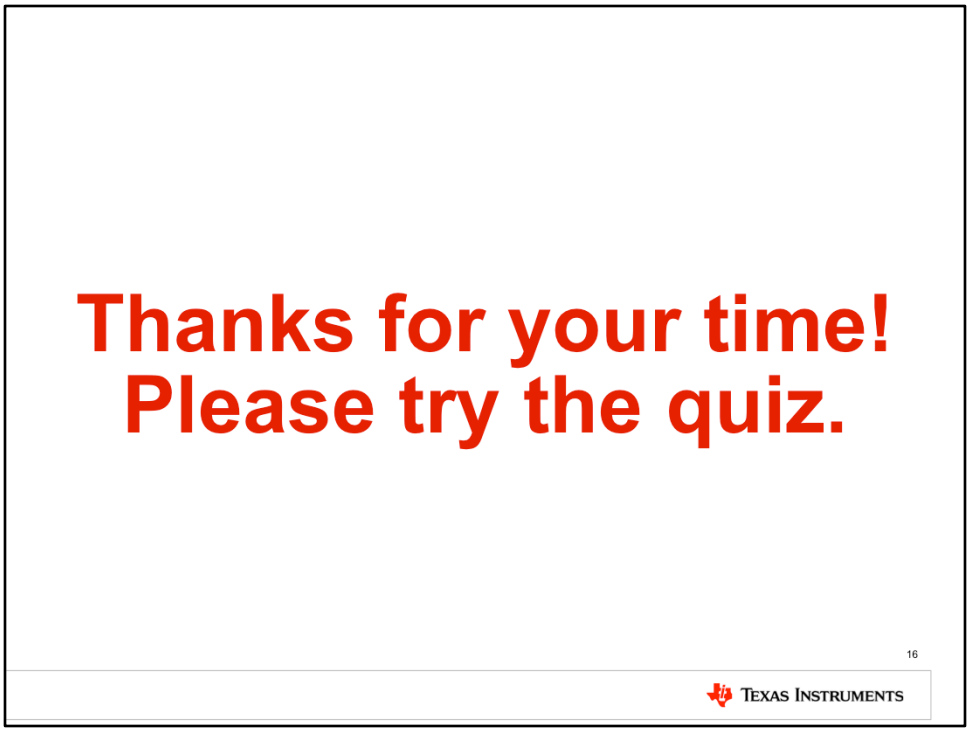
Absolute Maximum Ratings

			VALUE	UNIT
Supply voltage			±20 (+40, single supply)	V
Signal input terminals	Voltage	Common-mode	(V-) - 0.5 to (V+) + 0.5	V
		Differential	(V+) - (V-) + 0.2	V
	Current		±10	mA
Output short circuit			Continuous	mA
Operating temperature			-55 to +150	°C
Storage temperature			-55 to +150	°C
Junction temperature			+150	°C
Electrostatic discharge (ESD) ratings	Human Body Model (HBM)		4	kV
	Charged device model (CDM)		1	kV

15

Texas Instruments

The absolute maximum ratings given in a device data sheet describe the worst case conditions that can be applied to a device before damage occurs. Maximum supply voltage, input voltage, input current, and temperature are given. Notice that the maximum input current is given as ±10mA. This is the limit for most devices and is based on the maximum continuous current that the ESD diodes can sustain. Also notice that the ESD ratings for the device are given in the maximum ratings table. In this example, the rating is 4kV for human body model and 1kV for charged device model. Different devices will achieve different ratings based on their performance during characterization.

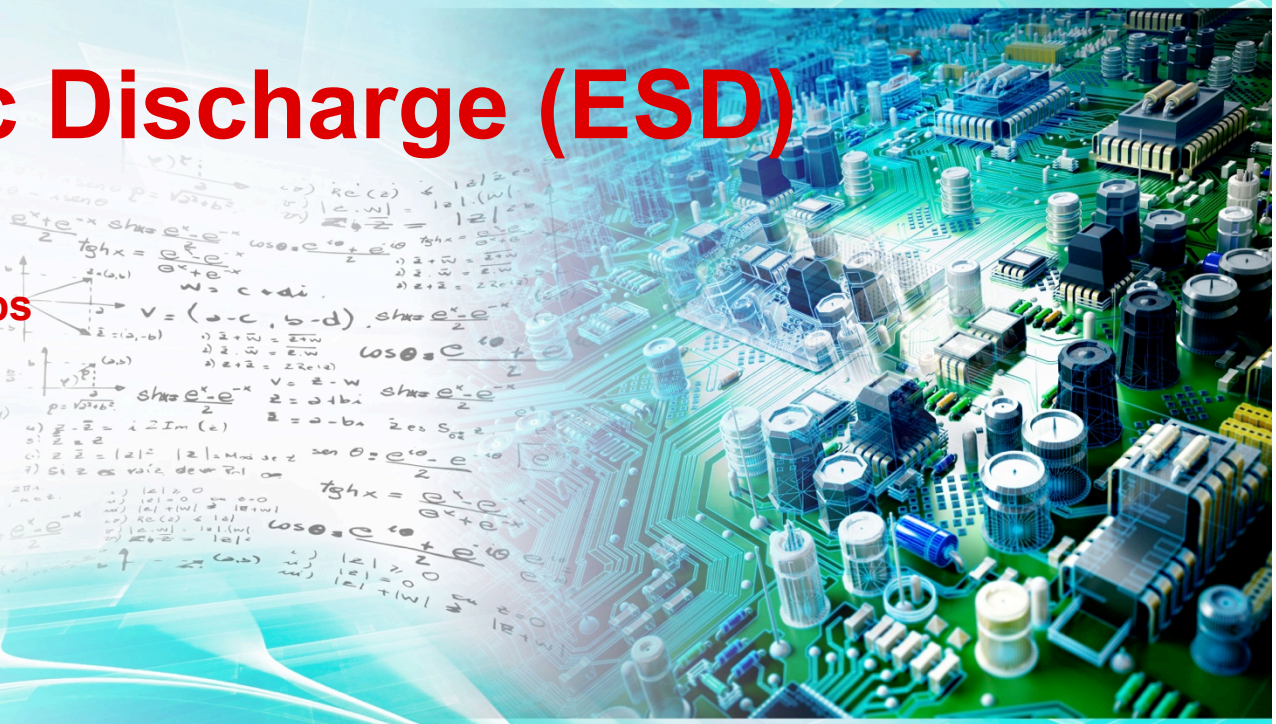


That concludes this video – thank you for watching! Please try the quiz to check your understanding of the video's content.

Electrostatic Discharge (ESD)

Multiple Choice Quiz

TI Precision Labs – Op Amps



Quiz: Electrostatic Discharge (ESD)

1. ESD voltage as low as _____can cause damage to some semiconductor devices.

a. 10V
b. 50V
c. 100V
d. 1000V

2. Humans can feel ESD at_____.

a. 3500V
b. 2000V
c. 1000V
d. 100V

3. (T/F) The absolute maximum input current is determined by the ESD diodes and is generally set to 10mA.

a. True
b. False

Quiz: Electrostatic Discharge (ESD)

4. Exceeding the _____ will cause damage to the device.

a. Specified power supply range
b. Absolute maximum power supply range
c. Pulsed power specification
d. Over-current protection specification

5. Internal Op Amp ESD cells are designed to_____.

a. Protect against all EOS events once assembled in a PCB
b. Provide latch-up-free operation under all EOS events
c. Prevent ESD damage from out-of-circuit events
d. Discharge any nearby lightning strikes

6. (T/F) ESD protective devices such as an ESD work surface or ESD wrist straps use very low resistance (0Ω) to quickly discharge ESD charge to ground.

a. True
b. False

Quiz: Electrostatic Discharge (ESD)

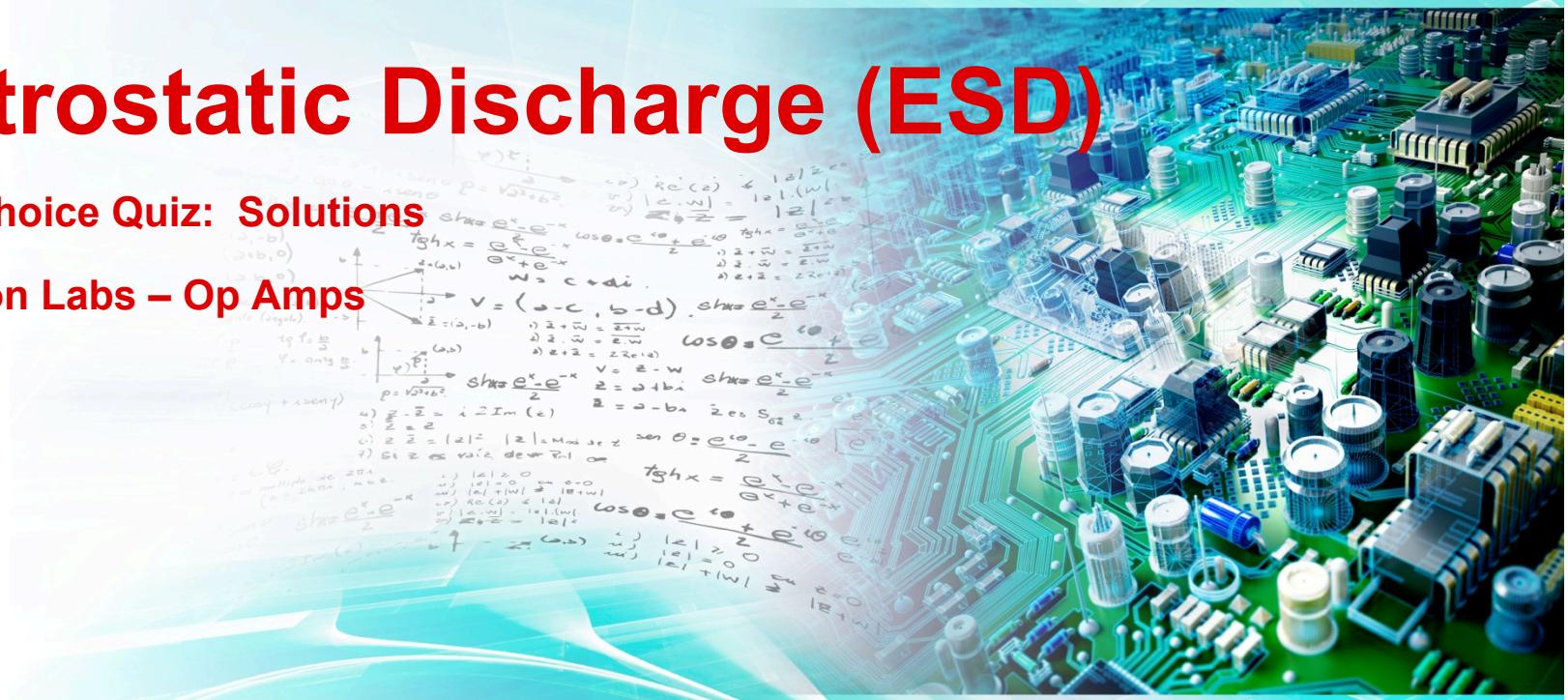
7. The absorption device is designed to _____.

a. Turn on and limit the supply voltage during an electrical overstress event
b. Turn on and limit the supply voltage during an ESD event
c. Turn on and limit the input current during an ESD event.
d. Turn on and limit the supply current during an ESD event.

Electrostatic Discharge (ESD)

Multiple Choice Quiz: Solutions

TI Precision Labs – Op Amps



Quiz: Electrostatic Discharge (ESD)

1. ESD voltage as low as _____can cause damage to some semiconductor devices.

a. 10V
b. 50V
c. 100V
d. 1000V

2. Humans can feel ESD at_____.

a. 3500V
b. 2000V
c. 1000V
d. 100V

3. (T/F) The absolute maximum input current is determined by the ESD diodes and is generally set to 10mA.

a. True
b. False

Quiz: Electrostatic Discharge (ESD)

4. Exceeding the _____ will cause damage to the device.

a. Specified power supply range
b. Absolute maximum power supply range
c. Pulsed power specification
d. Over-current protection specification

5. Internal Op Amp ESD cells are designed to_____.

a. Protect against all EOS events once assembled in a PCB
b. Provide latch-up-free operation under all EOS events
c. Prevent ESD damage from out-of-circuit events
d. Discharge any nearby lightning strikes

6. (T/F) ESD protective devices such as an ESD work surface or ESD wrist straps use very low resistance (0Ω) to quickly discharge ESD charge to ground.

a. True
b. False

Quiz: Electrostatic Discharge (ESD)

7. The absorption device is designed to _____.

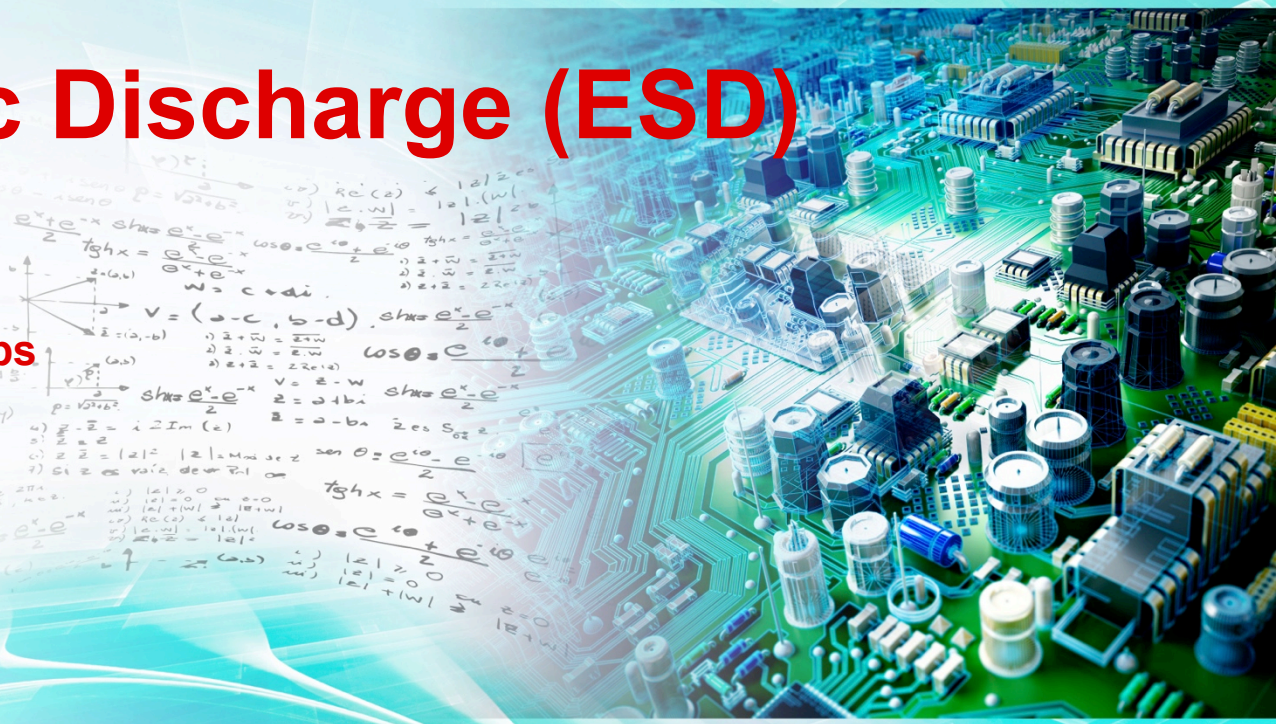
a. Turn on and limit the supply voltage during an electrical overstress event
b. Turn on and limit the supply voltage during an ESD event
c. Turn on and limit the input current during an ESD event.
d. Turn on and limit the supply current during an ESD event.

Electrostatic Discharge (ESD)

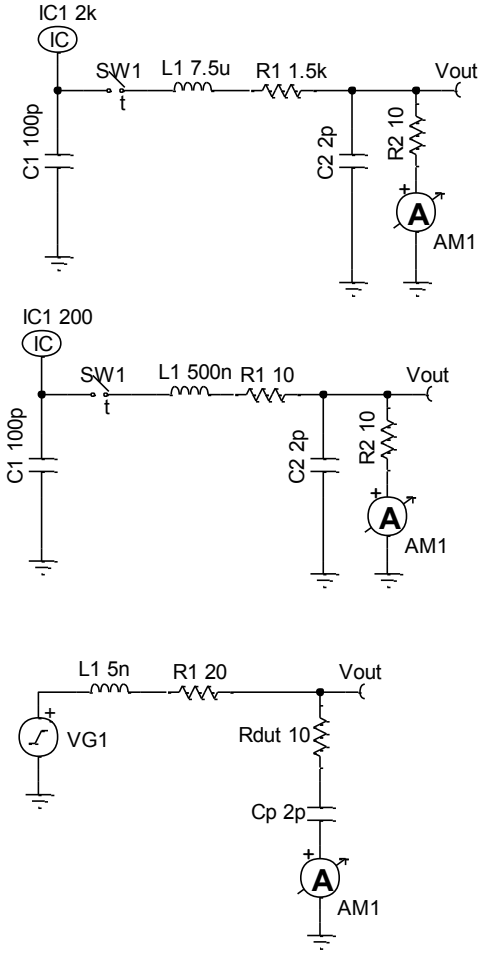
TIPL 1401

Exercises

TI Precision Labs – Op Amps



1. Simulate the a) Human Body Model, b)Machine Model, and c) Charge Device Model.

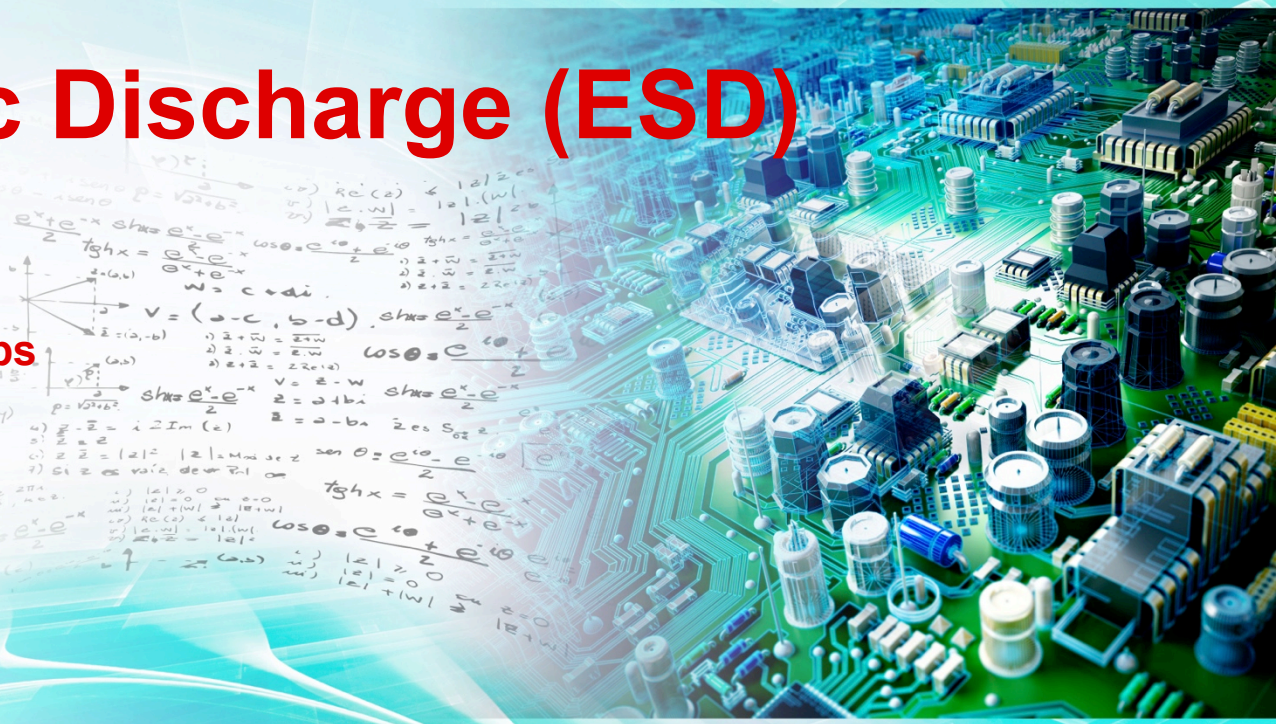


Electrostatic Discharge (ESD)

TIPL 1401

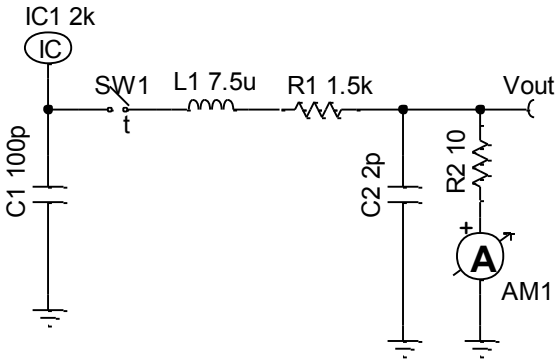
Solutions

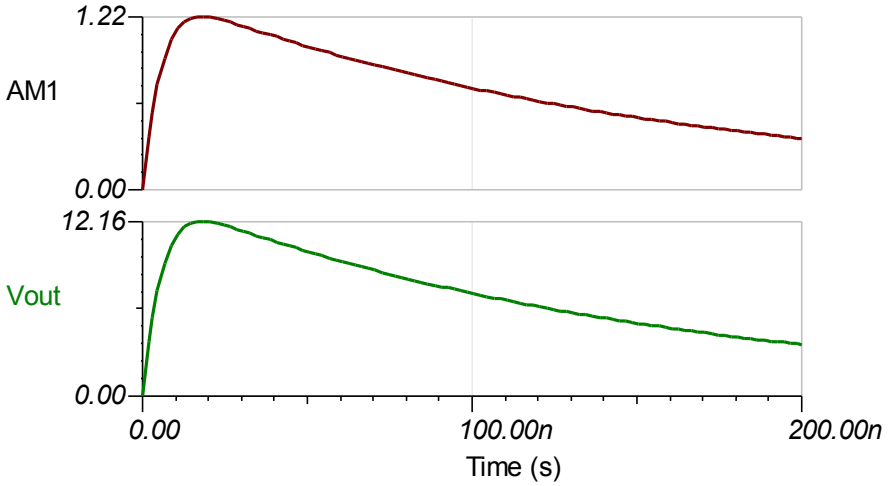
TI Precision Labs – Op Amps



1. **Simulate the a) Human Body Model, b) Machine Model, and c) Charge Device Model.**

HBM shown below:

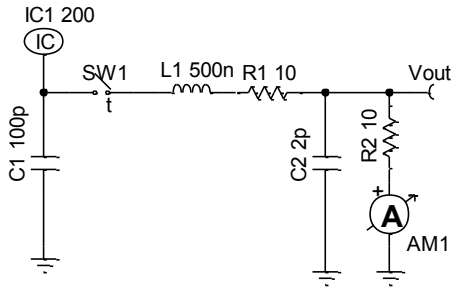


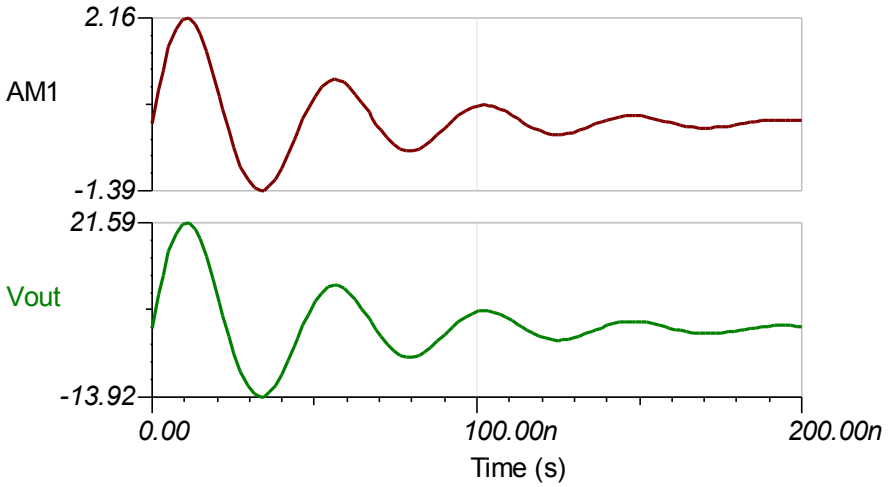


1401 - ESD - Exercise 1a.TSC

1. **Simulate the a) Human Body Model, b) Machine Model, and c) Charge Device Model.**

MM shown below:

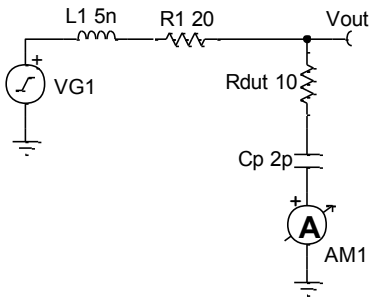


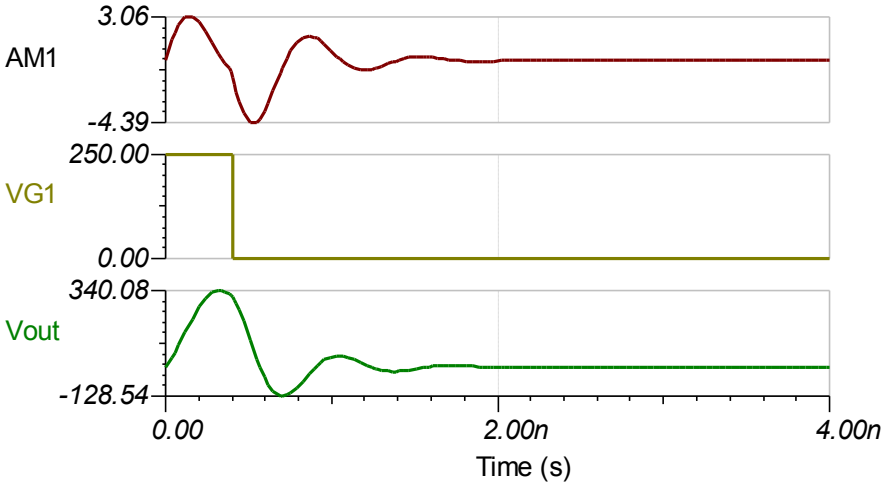


1401 - ESD - Exercise 1b.TSC

1. Simulate the a) Human Body Model, b) Machine Model, and c) Charge Device Model

CDM shown below:





1401 - ESD - Exercise 1c.TSC