Low Distortion Design – 4

TIPL 1324
TI Precision Labs – Op Amps

Presented by Collin Wells

Prepared by John Caldwell

Prerequisites: Noise 1 – 3
(TIPL1311 – TIPL1313)

TEXAS INSTRUMENTS

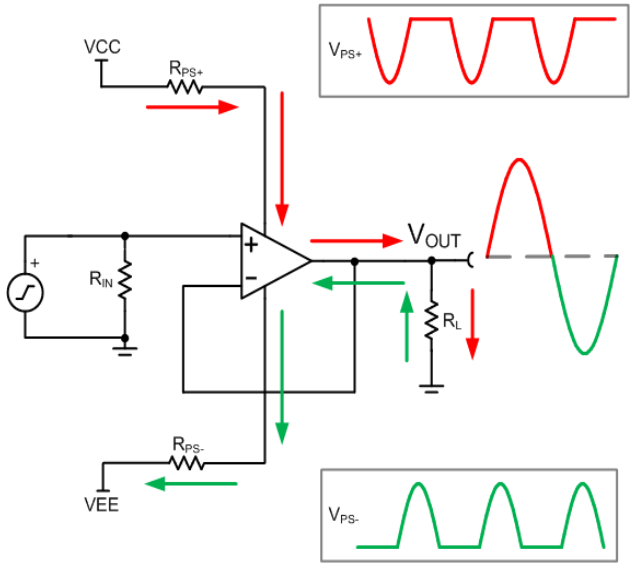
Hello, and welcome to part 4 of the TI Precision Labs series on designing low distortion op amp circuitry. This video focuses on external sources of distortion. Specifically we will consider how discrete components like resistors and capacitors impact distortion. We will also see how power supply impedance can impact distortion.

Distortion from Power Supplies

- Power supplies can contribute distortion as well as noise
- Power supplies have non-zero Zout
  - Output impedance of an LDO or switching converter
- Op amp supply drops for a half-cycle of the output waveform
  - Half-wave rectified sine waves have even harmonics:

Half wave rectified sine wave: $\omega_0 = \frac{2\pi}{T}$

$$f(t) = \frac{A}{\pi} + \frac{A}{2}\sin\omega_0 t - \frac{2A}{\pi}\sum_{n=1}^{\infty}\frac{\cos(2n\omega_0 t)}{4n^2 - 1}$$



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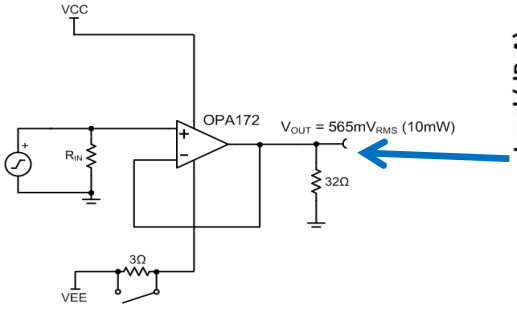
The first external source of distortion we will discuss is distortion introduced by the power supply. Power supplies can contribute distortion as well as noise. To understand how this happens, lets look at this circuit with a gain of one. This op amp sources current out of the positive supply into the load resistor for positive half cycles of the sine wave, and it sinks current out of the negative supply during the negative half cycles of the sine wave.

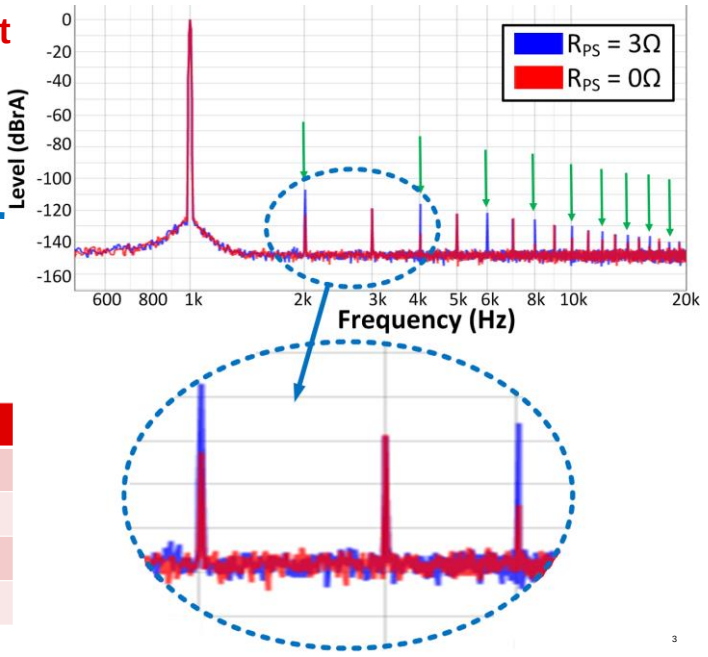
Power supplies all have some non-zero output impedance, represented in this schematic as R_{PS+} and R_{PS-}. That means as the op amp sources current from the positive supply to the load, a voltage drop occurs across the output impedance of the power supply. If we measured the voltage at the op amp positive power supply pin, we would see little dips in the power supply voltage when the op amp conducts current from the positive supply. Likewise, if we were to look at the op amp negative supply pin, we would see little humps in the supply voltage when the op amp conducts current from the negative supply.

The voltage on the op amp's supply pins looks just like a half wave rectified sine wave. If we perform a Fourier expansion on a half wave rectified sine wave as shown here, the factor of 2 time n in the cosine function will generate only even harmonics. Note that the even harmonics are attenuated by the power supply rejection of the op amp, but this is finite and so some of these harmonics will

show up in the output signal.

Demonstration – FFT of Output





Harmonic	0 Ohms	3 Ohms
2nd	-122dB	-107dB
4th	-134dB	-116dB
6th	-147dB	-121dB
8th	-140dB	-125dB

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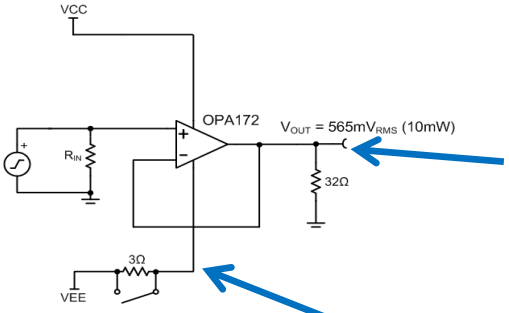
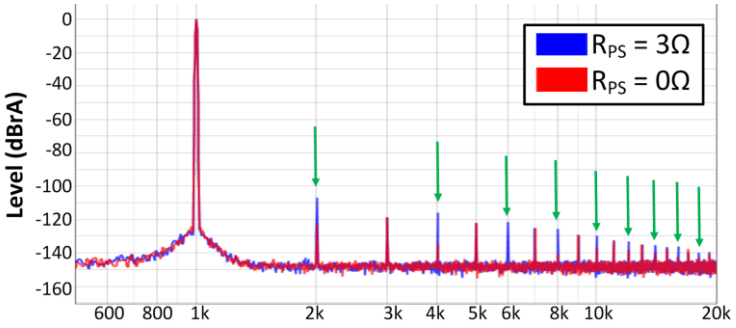
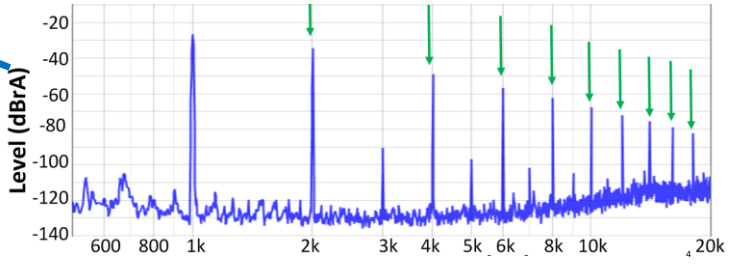
To demonstrate this let's look at an OPA172 with a 32Ω load. The load was intentionally selected to be a low value so that the current the op amp sources and sinks from the power supplies would be significant. We also added a 3Ω source impedance to the supply, with a switch across it so that the source impedance could be shorted to zero ohms. That way we can compare the ideal case where the supply impedance is zero to the case where the supply impedance is 3Ω. The FFT result for both cases is shown here where the 3Ω case is shown in blue and the 0Ω case is shown in red. We see that the even harmonics, are substantially larger in the case where the source impedance is 3Ω than in the case where it is 0Ω. The table lists the specific levels for the even harmonics for the 0Ω and 3Ω cases.

Demonstration – FFT of Power Supply







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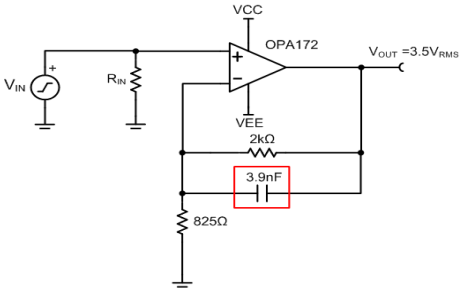
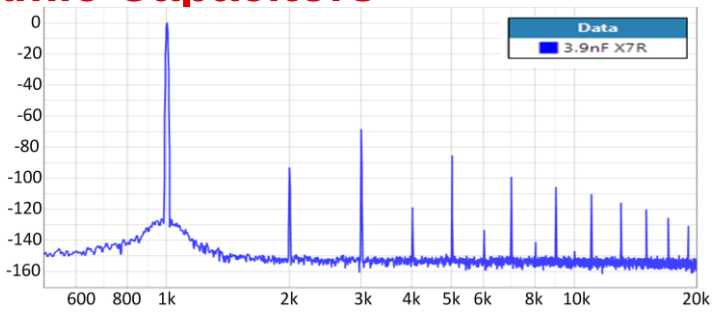
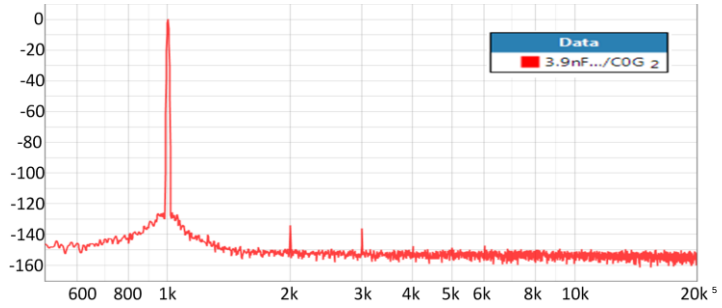
Continuing with the same circuit, this slide shows the FFT of the supply voltage of the device. As we would expect from the Fourier expansion results for the half-wave rectified sine wave, the supply has a lot of even harmonic content. As mentioned previously, these harmonics are attenuated by the power supply rejection of the op amp and then appear at the output.

Distortion from Ceramic Capacitors







- Non-inverting amplifier circuit
  - Gain: 3.42
  - Output voltage 3.5Vrms
- 3.9nF Feedback Capacitor
  - 50V Rated
  - Voltage Drop: 2.48Vrms
- THD:
  - X7R → -68dB (Blue)
  - NP0/C0G: -135dB (Red)

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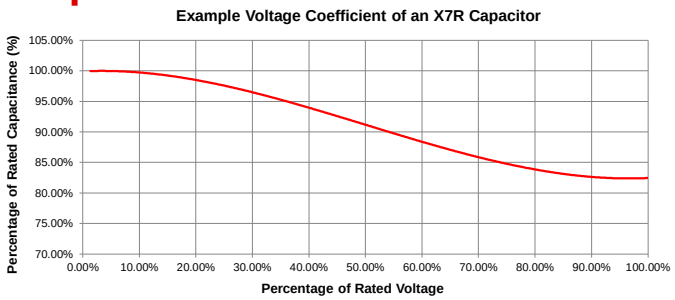
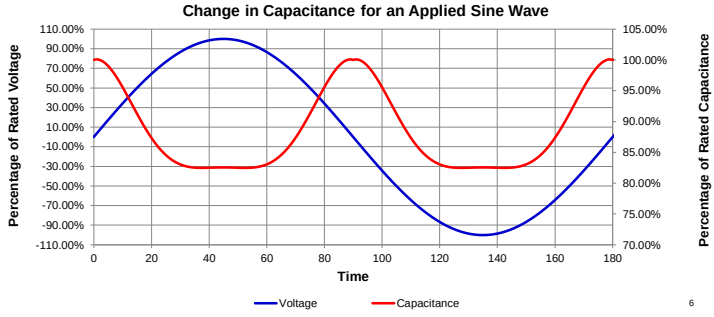
Probably the most common external source of distortion that engineers face is related to ceramic capacitors. Most often Y5V, X7R or other high K dielectric type capacitors are the problem. To demonstrate this, let's compare the results when using the OPA172 with an X7R feedback capacitor and then a C0G or NP0 feedback capacitor. The C0G capacitor has a low voltage coefficient whereas the X7R capacitor has a high voltage coefficient. In this circuit the output signal is 3.5Vrms, and the voltage across the capacitor is 2.48Vrms. Because the X7R capacitor has a high voltage coefficient, its capacitance changes as the voltage across it changes, and it will therefore draw a non-linear current. If the voltage across the capacitor is really small it may not contribute significant distortion, but in this particular location there is a significant voltage across it. Notice that if you compare the blue X7R measured results to the red C0G results, the C0G circuit has substantially less distortion. In fact the harmonics are at -135dB for the C0G circuit whereas they are at -68dB for the X7R circuit.

Distortion From Ceramic Capacitors

- Capacitance of Class II & III ceramics will vary greatly with the applied voltage
  - This is known as the “voltage coefficient of capacitance” or VCC
- Causes:
  - Dielectric constant changes with the intensity of an applied electric field
  - Capacitor dimensions change with an applied electric field
    - Reverse piezoelectric effect (ceramic capacitors)
    - Electrostatic force (Polyester film capacitors)
- The top graph shows a typical voltage coefficient curve from a manufacturer’s datasheet
- The bottom graph shows how the value of the capacitor will change in real time for an applied sine wave





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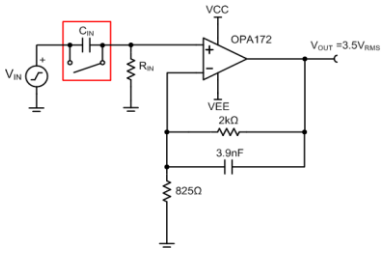
Let's look a little closer at the distortion caused by ceramic capacitors. First, the capacitance of Class II & III ceramics will vary greatly with the applied voltage, examples of these are X7R and Y5V capacitors. The change in capacitance versus applied voltage is called the “voltage coefficient of the capacitance”, or VCC. This effect is caused by changes in the capacitor dielectric constant with the intensity of an applied electric field. The change in electrical field also causes changes to the dimensions of the capacitor. This will cause a reverse piezoelectric effect in ceramic capacitors making the capacitance decrease with applied voltage. In the case of film caps the opposite occurs; that is, the electrostatic force will actually cause the plates to squeeze closer together which causes an increase in the total capacitance. In either case, the key point is that the changing

capacitance will introduce distortion.

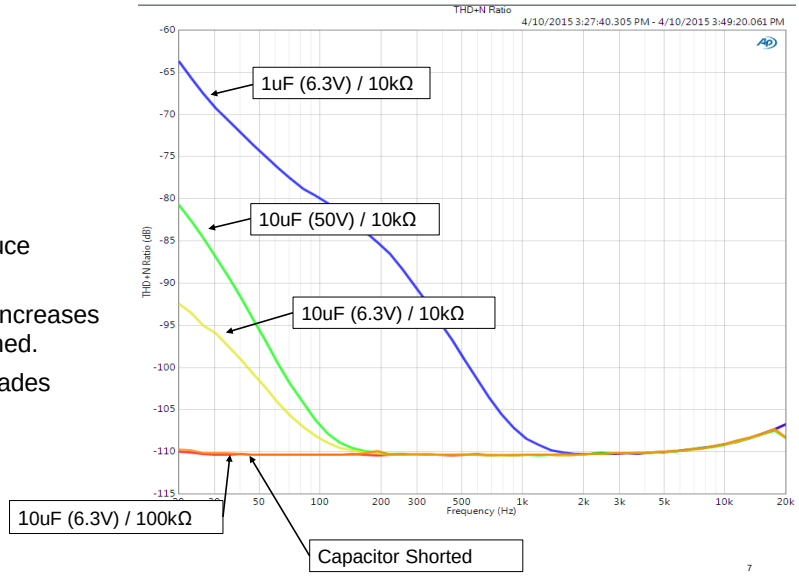
The top plot on the right was taken from an X7R manufacturer datasheet, and shows how X7R capacitance changes as a percentage of rated voltage. The graph on the bottom shows how the value of a capacitor will change in real time for an applied sine wave.

What About AC Coupling Capacitors?



- AC coupling capacitors may also produce distortion
- Voltage across the coupling capacitor increases as the low frequency cutoff is approached.
- Place the low frequency corner >2 decades below desired passband.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}}$$



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Input ac coupling capacitors can also produce distortion. Many engineers believe that because the input coupling capacitor is so large, that the voltage across should be low enough that it won't contribute significant distortion, but this is not the case. The graph at the right shows the THD+N for several different combinations of input coupling capacitors and input resistors, C_{IN} and R_{IN}. First, the red curve at the bottom shows the results with the ac coupling capacitor completely shorted. This is the distortion floor for the system.

Next the blue curve is from a 1uF, 6.3V rated input coupling capacitor with a 10kOhm resistor. The distortion from that combination starts fairly high in frequency at about 2kHz.

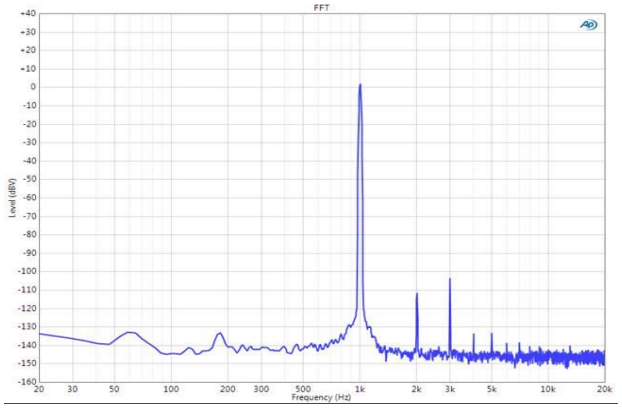
Increasing the coupling capacitor value pushes the ac coupling corner lower in frequency and helps to reduce the distortion because the voltage drop across the capacitor is reduced. The green and yellow curves are both for 10uF coupling capacitors with 10kOhm resistors. The difference is that the green curve is for a 50V cap, and the yellow curve is for a 6.3V capacitor. We did not mix these two curves up, and the 50V capacitor actually measured worse than the 6.3V capacitor. Ceramic capacitor dielectric types only specify the behavior over temperature and there isn't a standard that defines the behavior versus applied voltage.

So, the voltage coefficient of two capacitors can be drastically different regardless of the voltage rating. Of course, you shouldn't draw the conclusion

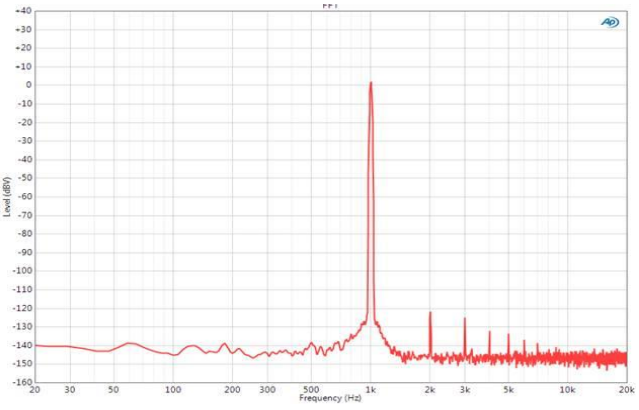
that the 6.3V rated capacitor will always be better, as it's just as likely to be worse in some cases depending on the manufacturer and other factors. Finally, the orange curve at the bottom uses a 10uF coupling capacitor and 100kΩ input resistor. In this case the input impedance was increased by a factor of 10 to reduce the cutoff frequency. We adjusted the input impedance in this case because a 100uF coupling capacitor may not be practical in some applications. For this case we see that the distortion is very near the distortion floor. The conclusion is that if we need to use non-linear input coupling capacitors types, it is best to set the high pass corner frequency two decades below the desired corner frequency. For example, if we want the corner frequency at 20Hz, we need to set the corner frequency to 0.2Hz.

Distortion from Surface Mount Resistors

- Thick film resistors may produce distortion
  - Voltage coefficient of the resistive element
    - Usually only seen for large signal voltages (>3V_{RMS})
  - Effect is worst for small package sizes and high resistance values



Thick Film, 0603



Thin Film, 0603

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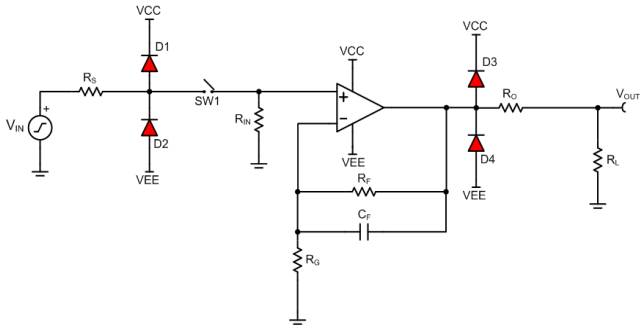
Surface mount resistors also have a voltage coefficient. This is especially a problem with small package types, such as 0201, 0402, and 0603. The problem mainly happens with thick film resistors types. Also, this issue usually is only seen at large signal voltages such as 3Vrms and greater. This behavior occurs because with smaller package types, the end caps of the resistor are closer together, and consequently the electric field across the resistor is higher and the resistivity changes as a function of the electric field across it. These two plots compare the same circuit tested with thick film and thin film resistors. Clearly, the thick film resistors significantly increase the distortion. Of course, thin film resistors cost more than thin film resistors, but if you are using an expensive low distortion op amp and you need to use small resistors packages, then they need to be thin film to maintain good performance.

Distortion from External ESD Protection



- The capacitance of ESD diodes varies according to the equation:

$$C_D \approx \frac{C_{DO}}{\sqrt{1+\frac{V_R}{0.7}}}$$

- The signal across the ESD diode causes its capacitance to change
  - Draws a non-linear current
  - Converted to a non-linear voltage by source impedance
- Chose diodes with the lowest junction capacitance possible!
- Place them at low impedance nodes
  - Non-linear current drawn does not produce a non-linear voltage

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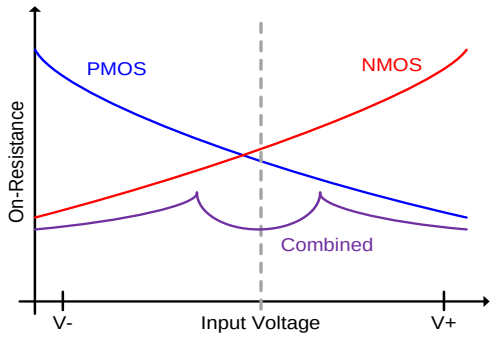
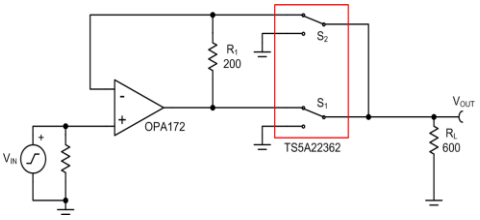
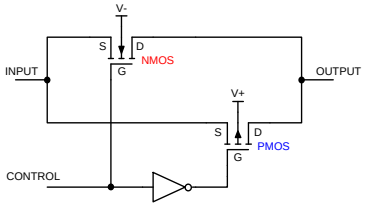
Distortion from ESD protection is caused by the same effects that we discussed for op amp input stage distortion. That is, the reverse biased junction capacitance will vary with applied voltage. As the signal applied to the ESD protection diodes changes their capacitance will change. This causes them to draw a non-linear current which is converted to a non-linear voltage by the source impedance. If we examine the circuit above there are ESD protection diodes on the input and output. The interesting thing is that the input ESD diodes introduce distortion while the output diodes will not. The input ESD diodes draw a non-linear current through the source impedance which may be fairly large. The ESD diodes draw a non-linear current as well, but because the op amp output impedance is very low the translation of non-linear currents to voltage is minimized. So, the general recommendation is to first, choose diodes with the lowest junction capacitance possible, and second place the diodes at low impedance nodes if possible.

CMOS Switch Impedance

- CMOS Switches are composed of NMOS and PMOS devices in parallel
  - Allows them to conduct current in both directions
- Control voltage (V_G) is typically constant
- Signal voltage (V_S) is variable
- Changing V_{GS} modulates the on-resistance of the FETs
- Varying impedance creates distortion
  - Worst for high load currents / low load impedances
- Increase load impedance
- Close feedback loop around the switch







"Reducing Distortion from CMOS Analog Switches" Caldwell, 1Q2015 AAJ

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CMOS switches will normally have an NMOS switch and a PMOS switch in parallel - with their sources and drains connected together. The control logic, connects directly to the gate of the NMOS switch and is inverted and then connects to the gate of a PMOS switch. As the switch input voltage gets more positive, the voltage drop between the gate and source of the NMOS is decreasing and the voltage drop between the gate and source of the PMOS is increasing. This has the effect of decreasing the PMOS resistance and increasing the NMOS resistance. For positive voltage the current flows through the PMOS and conversely, for negative voltages the current flows back through the NMOS. The two transistors are in parallel and so their resistances are in parallel. Combining the two parallel impedances produces the combined on-resistance curve shown in purple. A constant theme in low distortion design is that anytime an impedance in the signal path changes with voltage it will produce distortion.

So, if a switch is placed in series with the load the switch will often produce distortion. This is especially true if the load resistance is low in value. For high impedance loads, where the current through the switch is minimal, variations in the switch on resistance may be inconsequential. The op amp circuit illustrates one possible solution to this problem using two switches. Switch S1 is in the forward pathway, and switch S2 is in the feedback path. The current through S2 is essentially zero since it connects to the inverting input of the amplifier. Since no current is flowing through switch S2, it does not introduce any additional distortion. Switch S2 provides feedback from the output node and allows

feedback to cancel the distortion introduced by switch S1. Resistor R1 provides a feedback path when switch S1 and S2 are in the ground position and the amplifier is disconnected from the load. Further details on this circuits operation is given in “Reducing Distortion from CMOS Analog Switches” Caldwell, published in the 1Q2015 AAJ”.

Reducing Distortion From External Sources

- Minimizing distortion from power supplies
  - Chose op amps with high PSRR in the desired passband
  - Design power supplies to limit their output impedance
    - Bulk decoupling capacitors, linear regulators, short PCB traces
- Capacitors
  - Use NP0/C0G ceramic or Polypropylene film capacitors in the signal path
  - For AC coupling capacitors set f_c >2 decades below the passband
- Resistors
  - Use thin film surface mount resistors (Larger packages are better)
  - Through-hole metal film resistors are also very good
- ESD Protection
- CMOS Switches

In summary, there are several guidelines for reducing distortion from external sources. First, minimize the distortion from power supplies by choosing amplifiers that have high PSRR in the desired signal passband. Also, use large bulk decoupling capacitors near the voltage regulator to decrease the ac impedance, and also try to minimize the PCB trace length.

Use low distortion NP0/C0G or Polypropylene film capacitors in the signal path. For AC coupling capacitors place the corner frequency greater than two decades below the pass band.

Use thin film surface mount resistors when small package sizes are required.

Larger packages such as 1206 are possible, then thick film are also ok. For the absolute best results, use through-hole metal film resistors.

When adding external ESD protection, select the protection devices with the lowest junction capacitance available. Also, place the ESD protection at low impedance nodes to minimize the distortion contribution. Finally, in the case of CMOS switches, minimize the current through the switch by using it with high impedance loads. Another option is to close the switch inside the feedback loop of the amplifier allowing feedback to minimize distortion.

Thanks for your time! Please try the quiz.

In summary, we explained the external sources of distortion in op amp circuitry We also learned methods for minimizing this distortion.

This concludes the series on designing low distortion op amp circuitry.

Thank you for time! Please try the quiz to check your understanding of this video's content.