UCD3138 Digital Power Peripherals Programmer's Manual

SLUU995A
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Scope of this Document

The following topics are covered in the UCD3138 Digital Power Peripheral Programmer's Manual

- **Digital Pulse Width Modulator (DPWM)**
  - **Modes of Operation (Normal/Multi/Phase-shift/Resonant etc)**
  - **Automatic Mode Switching**
  - **DPWMC, Edge Generation & Intra-Mux**
- **Front End**
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  - **Oscillator Failure Detection**
- **Register Map for all of the above peripherals in UCD3138**

Other topics related to UCD3138 are covered in the additional documents listed below:

UCD3138 ARM and Digital System Programmer's Manual

- Boot ROM & Boot Flash
  - BootROM Function
  - Memory Read/Write Functions
  - Checksum Functions
  - Flash Functions
  - Avoiding Program Flash Lock-Up
- ARM7 Architecture
  - Modes of Operation
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  - Instruction Set
  - Dual State Inter-working (Thumb 16-bit Mode/ARM 32-bit Mode)
- Memory & System Module
  - Address Decoder, DEC (Memory Mapping)
  - Memory Controller (MMC)
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- Register Map for all of the above peripherals in UCD3138

UCD3138 Monitoring and Communications Programmer's Manual

- ADC12
  - Control, Conversion, Sequencing & Averaging
  - Digital Comparators
  - Temperature Sensor
  - PMBUS Addressing
  - Dual Sample & Hold

- Miscellaneous Analog Controls (Current Sharing, Brown-Out, Clock-Gating)
- PMBUS Interface
- General Purpose Input Output (GPIO)
- Timer Modules
- PMBus
- Register Map for all of the above peripherals in UCD3138

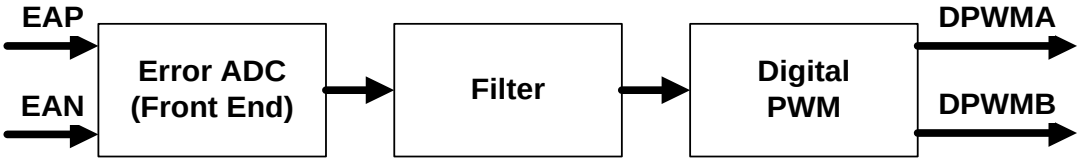
For the most up to date product specifications please consult the UCD3138 Device datasheet (Lit # SLUSAP2) available at www.ti.com.

1 Introduction

UCD3138 is a digital power supply controller from Texas Instruments offering superior levels of integration and performance in a single chip solution targeting high-performance isolated power supply applications. At its core are the digital control loop peripherals, also known as Digital Power Peripherals (DPP) that are used for controlling the high-speed voltage/current loops in the power supply and an ARM7TDMI-S microcontroller/processor that performs real-time monitoring, configures peripherals and manages communications. The device also contains a 12-bit, 265ksps general purpose ADC with up to 14 channels, timers, interrupt control, JTAG debug and PMBus and UART communications ports. In terms of memory, UCD3138 offers 32kB of program flash, 2kB of data flash, 4kB RAM and 4kB of ROM.

The Digital Power Peripherals (DPPs) are elemental blocks in the UCD3138 controller which are specifically architected for digital power supply control. They are designed to replace the analog compensation network and PWM generation system that are employed in power supplies based on analog power management controller ICs, and add enhanced digital features to the system. In many cases, after initialization by firmware, the DPPs can control a power supply completely autonomously, with no firmware intervention. This leaves processor resources for improved monitoring, communication, and other functions.

The simplest configuration of the Digital Power Peripherals highlighting the key blocks involved in loop control is shown below:



The Error ADC (in the Front End) accepts a differential voltage signal as an input. It measures the difference between this input and a digitally controlled reference voltage and generates a digital error output. It passes this digital error information to the Filter. The Error ADC (or EADC) is a specialized high speed, high resolution ADC with a small dynamic range, optimized for power supply error measurement.

The Filter takes the error signal and passes it through a PID based digital filter which compensates for the characteristics of the external loop. This filter can be dynamically reprogrammed for changing power load source, and circuit characteristics. It also offers non-linear response capability for better handling of transients.

The output of the compensator is passed to a Digital PWM (DPWM) generator. The DPWM has two outputs, which can be used in many different ways. There are modes for synchronous rectification, multiple phases, various bridge topologies, and LLC configurations. In addition to the 2 DPWM outputs, the DPWM has other signals which are used externally and internally. These include:

- Frame start – start of a switching cycle
- Sample Trigger – signals Front end to take a sample
- Sync out – signals another DPWM to start a frame
- Sync in – a signal to this DPWM to start a frame
- Fault signals – signal the DPWM to take various fault actions

These signals will be covered in much more detail in the DPWM section of this document.

The peripherals can be run tied together as shown above, or they can be used in different groupings and interconnections, not shown in the picture above. For example, the DPWM can be used to trigger the Error ADC, which will trigger the Filter at the end of its conversion.

The UCD3138 device supports multiple sets of the Digital Power Peripherals affording the ability to control upto 3 feedback loops (voltage or current) and drive 8 outputs simultaneously. To inter-connect all the DPPs, there is a large module called the Loop Mux. This permits a high degree of flexibility in DPP

configuration. Any Front End can be connected to any Filter, and any Filter output can be connected to any DPWM. Additionally, information can be passed between the peripherals. For example, the output of one Filter (eg. controlling a slow Voltage loop), can contribute to the reference of another Front End (eg. monitoring a fast current loop) and enable implementation of nested loops (such as in Average Current mode control).

In addition, the DPPs in UCD3138 provide other modules and functions for power supply and control. These include:
- Fault Handling
- Cycle by Cycle Current Limit
- Constant Power/Constant Current
- Ramp up/Ramp Down
- Peak Current Mode control

and so on.

There is also a module called Fault Mux which connects fault detection circuitry outputs to control inputs, primarily on the DPWMs, to customize fault handling and recovery.

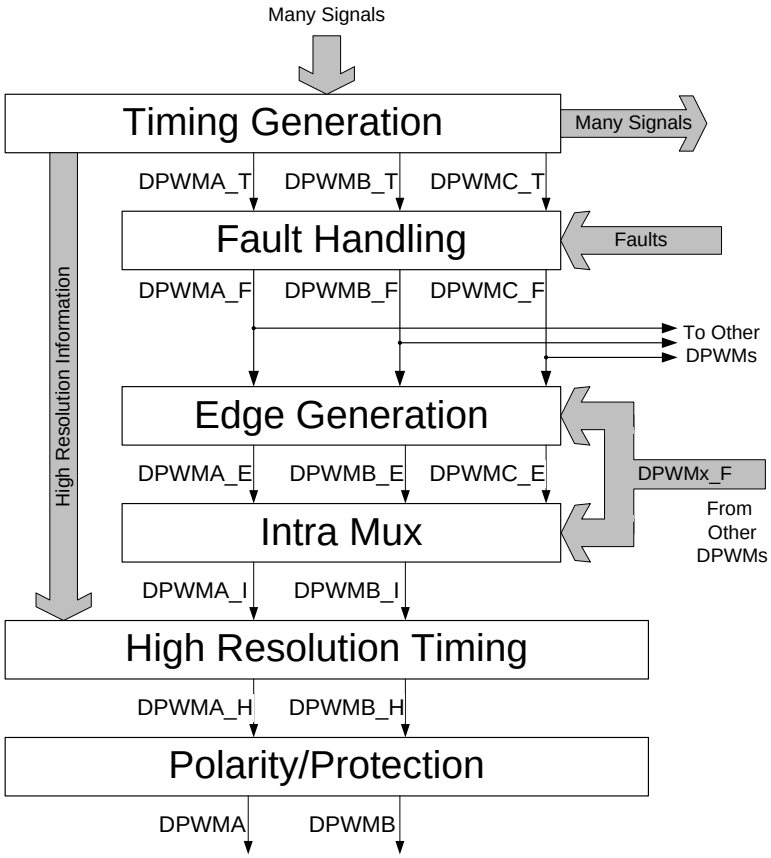
This documentation provides information about the DPP modules in UCD3138, starting with a detailed description, continuing with some configuration examples, and ending with a reference section which lists each bit field in each DPP module.

2 Digital Pulse Width Modulator (DPWM)

The DPWM Module is probably the most complex and central of the DPPs. It takes the output of the Filter and converts it into the correct PWM output for many power supply topologies. Each DPWM module has two output pins – DPWMxA and DPWMxB (x=0, 1, 2 & 3). The DPWM provides for programmable dead times and cycle adjustments for current balancing between phases. It controls the triggering of the EADC. It can synchronize to other DPWMs or to external sources. Alternately, it can provide synchronization information to other DPWMs or to external recipients. The DPWM can also be synchronized to external devices using the SYNC pin as either an input or an output. In addition, it interfaces to several fault detection circuits. The response to these faults is part of the DPWM function.

2.1 DPWM Block Diagram

The picture below illustrates an overall view of a single DPWM block, which is composed of many different individual modules, through which the signals propagate:



Block Diagram of a DPWM module

- The Timing Generation Module outputs 3 DPWM signals (DPWMx_T, x=A, B, C), as well as many other signals for other modules. It is the section where the filter output is translated into pulse widths and sometimes into the period.

- The Fault Handling Module is next. It shuts off the DPWM signals if a fault occurs. After the DPWM signals come from the Fault Module (DPWMx_F, x=A, B, C), they are sent to other DPWM Modules.

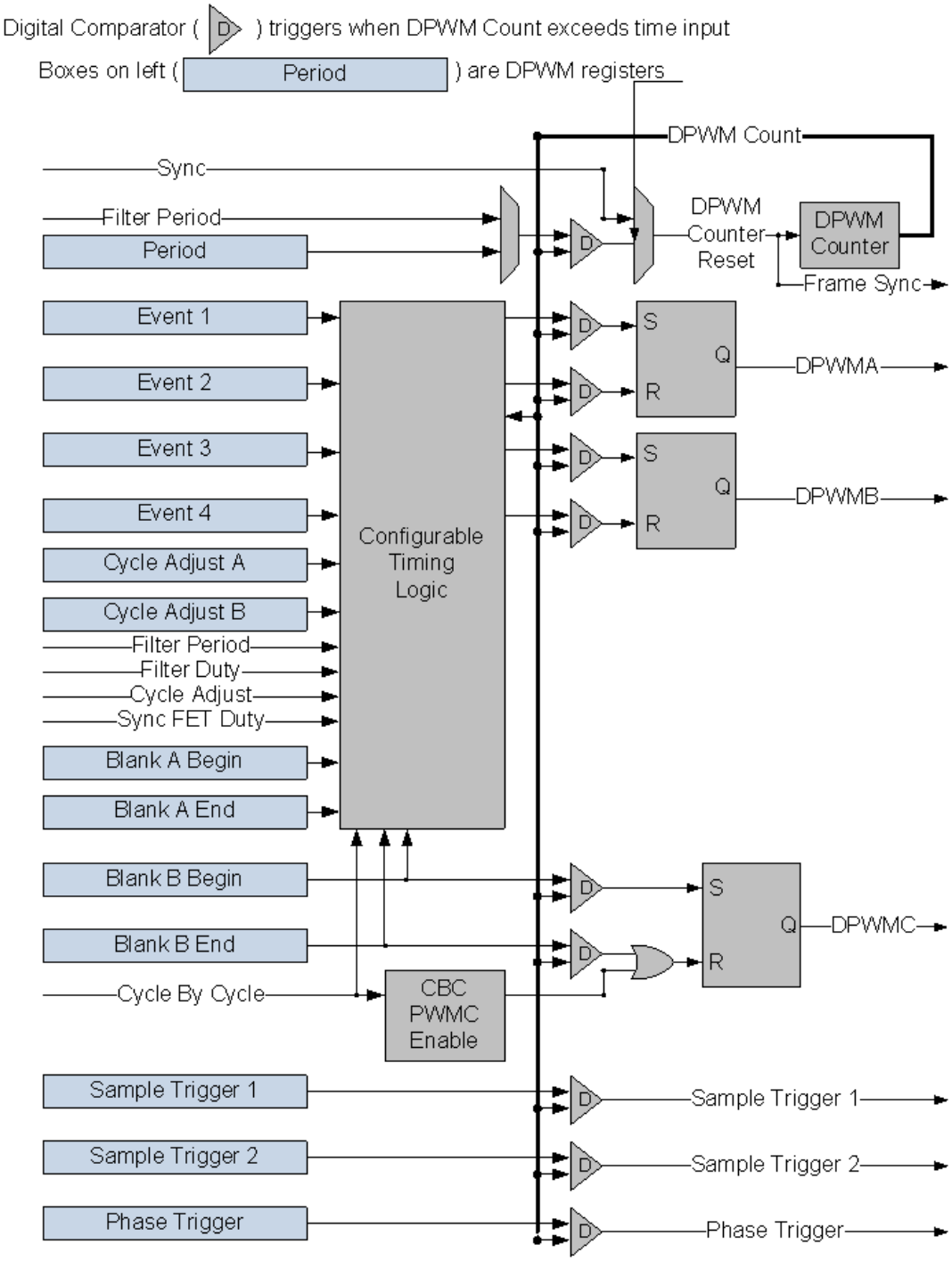
- The Edge Generation and Intra Mux modules can combine signals from several DPWMs to generate new signals (DWMx_E, DPWMx_I, x=A, B, C).

The notation of DPWMx_T, DPWMx_F (where x=A, B, C) etc is very useful here to understand the origin and relationship between the signals. For example DPWM2A_F may have no relationship at all to DPWM2A_I.

Many topologies use neither the DPWMC signal nor Edge Generation and Intra Mux modules. The default is for these modules to just pass signals through unchanged. However certain topologies such as Phase Shifted Full Bridge (PSFB) use both modules as well as DPWMC signal.

These diagrams merely illustrate the signal propagation through the various modules in the DPWM and do not show the configuration logic which controls how each module works and which can dynamically reconfigure the DPWM between switching cycles.

The next figure shows a block diagram of just the Timing Module illustrating the data, signals and main elements involved (once again, the real logic of the Timing Module is not illustrated here).



Block Diagram of Timing Module in the DPWM module

2.2 Introduction to DPWM (DPWM Multi-Mode, Open Loop)

The DPWM is based on a DPWM counter, which counts up from 0 to a period value, and then is reset and starts over again. The counter can also be reset by a sync signal, either from the SYNC pin, or from another DPWM.

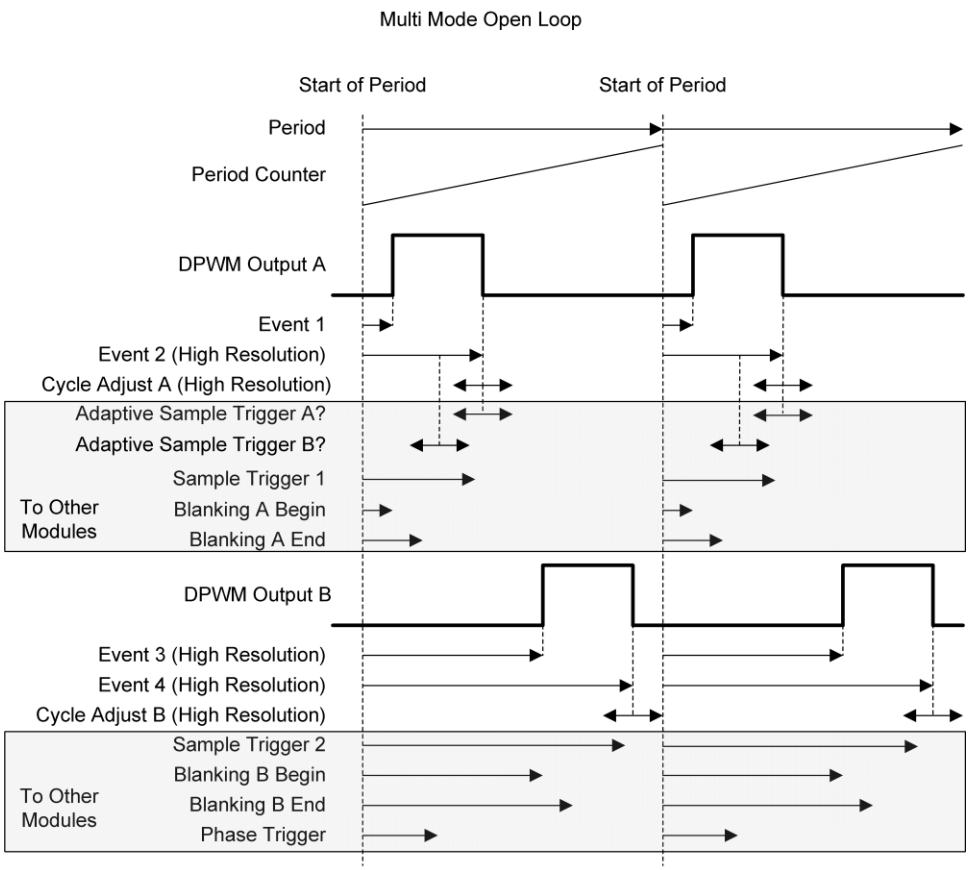
The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal. In the Timing Module block diagram shown above, this is functionality is represented by a digital comparator.

The DPWM has a basic 250 MHz clock, giving a resolution of 4 nanoseconds. 15 other 250 MHz clocks are generated spaced 250 picoseconds apart. Output pulse widths and pulse spacing are controlled by these clocks, giving a resolution of 250 picoseconds. The edges generated by these clocks are hence referred to as "High Resolution" in the illustrations throughout this section.

Most of the signals out of the DPWM are fairly simple. The only complex signals are DPWMA and DPWMB. These vary depending upon the power supply topology and are the most important signals coming out of the DPWM.

The DPWM has many modes to support different topologies. These are selected by a mode bit field in a DPWM control register. The "Multi mode, Open loop" mode is used to introduce the DPWM here, while the other DPWM modes are described in subsequent sections.

The following figure illustrates most of the signals involved in the DPWM in a mode known as "Multi mode, Open loop". Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed. This mode is used for introducing the DPWM because there is a very simple correlation between DPWM register values and signal timing.



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 2 + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 3
DPWM B Falling Edge = Event 4 + Cycle Adjust B
Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

DPWM Mode - Multi-mode, Open Loop

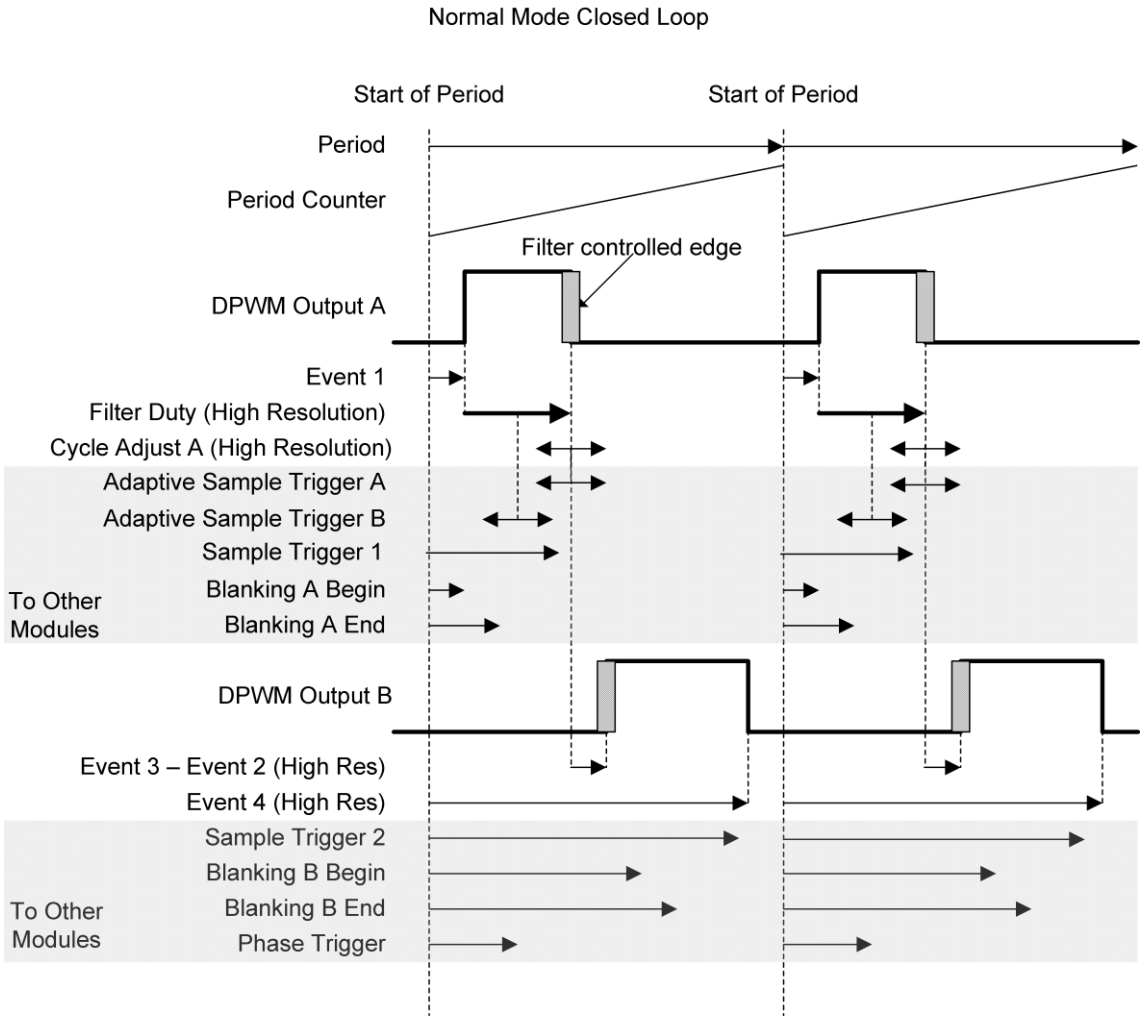
The Sample Trigger signals are used to trigger the Front End to sample input signals. The Blanking signals are used to blank fault measurements during noisy events, such as FET turn on and turn off. This prevents false detection of faults caused by noise. They only affect the Cycle By Cycle (CBC) module. Other faults are not blanked.

Note that Sample Trigger 1 and 2, Blanking A and B, and Phase Trigger are shown at logical locations for this specific mode, but they can be placed anywhere within the period.

2.3 DPWM Normal Mode

In Normal mode, the Filter output determines the pulse width on DPWM A. DPWM B fits into the rest of the switching period, with a dead time separating it from the DPWM A on-time. It is useful in topologies

that use D and 1-D type waveforms. For example, buck and boost derived topologies can be driven using Normal mode. Here is a drawing of the Normal Mode waveform:



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 1 + Filter Duty + Cycle Adjust A + (Event 3 – Event 2)
DPWM B Falling Edge = Event 4
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

DPWM - Normal Mode

Cycle Adjust A can be used to adjust pulse widths on individual phases of a multi-phase system. This can be used if current balancing is necessary, for example. The Adaptive Sample Triggers can be used to sample in the middle of the on-time (Adaptive Sample Trigger B - for an average output during on-

time), or at the end of the on-time (Adaptive Sample Trigger A - to minimize phase delay). The Adaptive Sample Register provides an offset from the center or end of the on-time for DPWM signal from the chip. This can compensate for external delays, such as FET and gate driver turn-on times.

The Blanking signals are used to disable the CBC fault signal during noise. Generally the noise is caused by DPWM edges. The Blanking registers hold fixed values, so they are easiest to use with fixed edges, rather than with edges that change dynamically. So in this case, the rising edge of DPWM A and the falling edge of DPWM B are easy to provide blanking for. In this mode, both blanking times act on the falling edge of A, since this is what the Cycle By Cycle logic works on.

Cycle Adjust B has no effect in Normal Mode.

CAUTION – In Normal Mode, the DPWM calculated rising edge of DPWMB must not be permitted to exceed DPWM Event 4. This can be done either with a clamp on the filter output, or by using an appropriate KCOMP value in the filter output multiply operation. If this is not done, the DPWMB on time may overlap the DPWMA on time, causing shoot through.

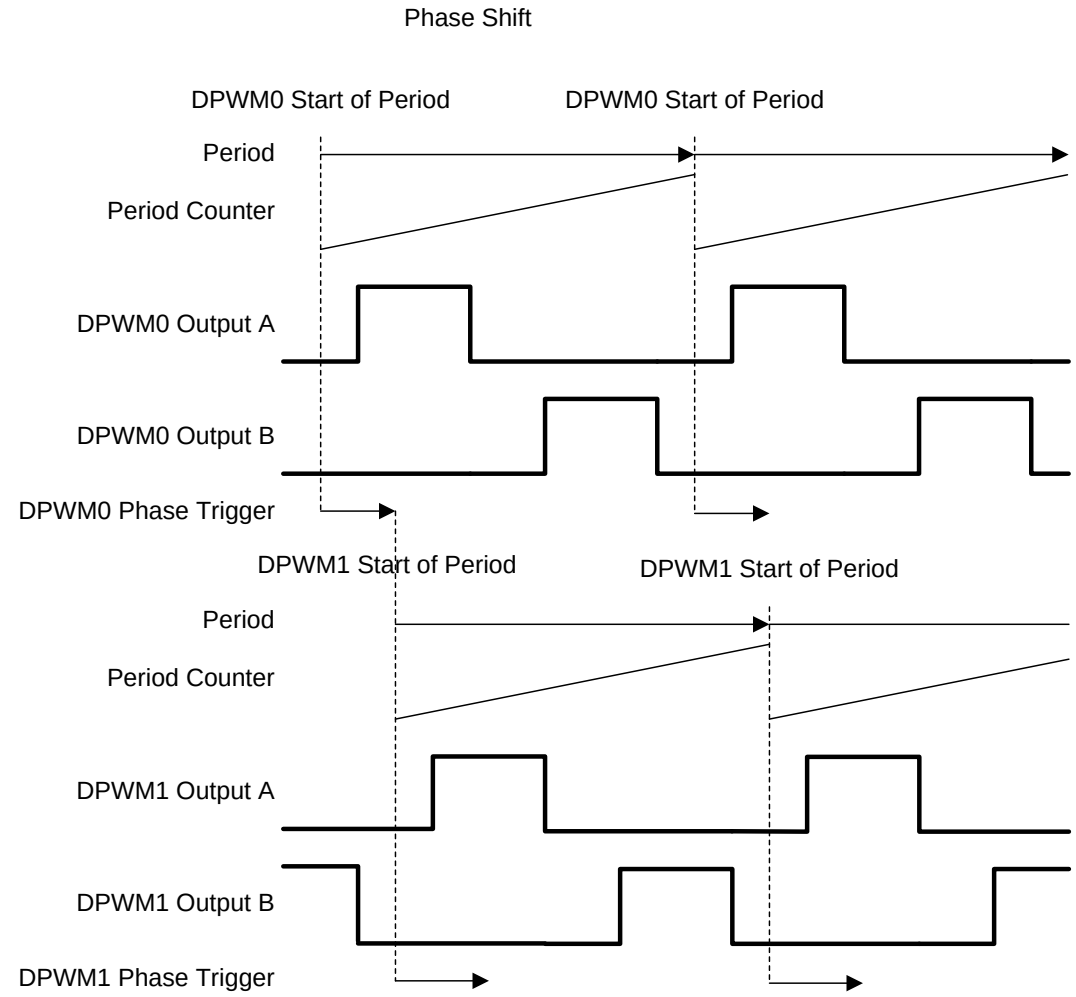
2.4 DPWM Phase Shift Mode

In most modes, it is possible to synchronize multiple DPWM modules using the phase shift signal. The phase shift signal has two possible sources. It can come from the Phase Shift Register or from the Filter Duty value.

The Phase Shift Register provides a fixed value, which is useful in simple multiphase systems such as interleaved PFC.

When the Filter Duty is the source, the changes in the filter output cause changes in the phase relationship of two DPWM modules. This is useful for phase shifted full bridge topologies if voltage mode control is desired rather than peak current mode.

The following figure shows the mechanism of phase shift:



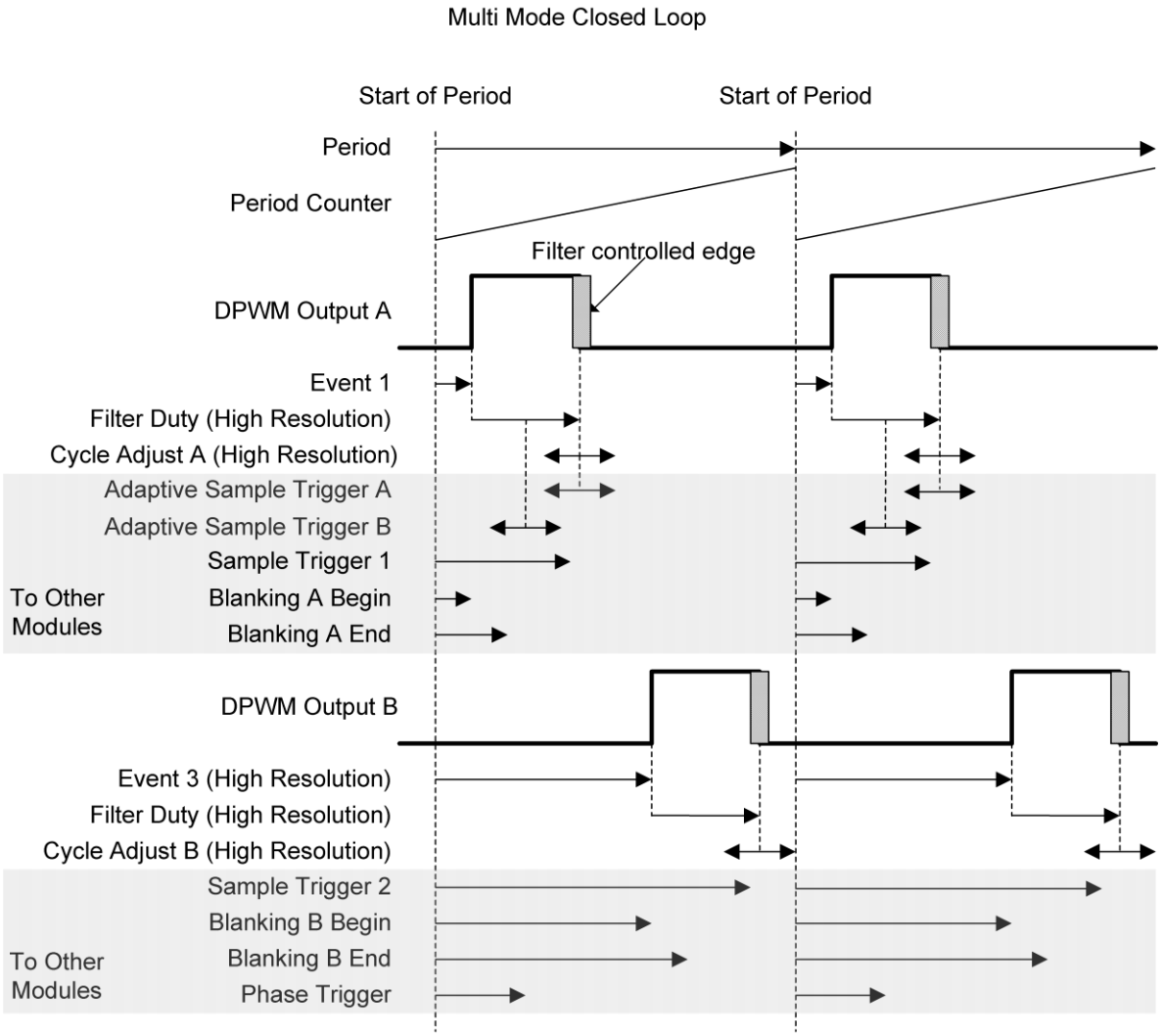
Phase Trigger = Phase Trigger Register value or Filter Duty

DPWM - Phase Shift Mode

2.5 DPWM Multiple Output Mode (Multi Mode)

Multi Mode is used for systems where each phase has only one driver signal requirement. In this mode, each DPWM peripheral can drive two phases with the same pulse width, but with a time offset between the phases, and with different cycle adjusts for each phase.

Here is a diagram for Multi mode:



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 3
DPWM B Falling Edge = Event 3 + Filter Duty + Cycle Adjust B
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

DPWM – Multiple Output Mode (Multi Mode)

Event 2 and Event 4 are not relevant in Multi mode.

As shown in the illustration, DPWMA is designed to turn on close to the start of the period. It can turn off any time until the end of the period, achieving essentially 100% on-time. DPWMB is designed to start later in the period to support a multi-phase system. Therefore DPWMB is designed to cross over the

period boundary safely, so long as it does not ever move into or out of an event update window. This makes 100% pulse width operation possible for DPWMB as well.

Since the rising edge on DPWMB is also fixed, Blanking B Begin and End can be used for blanking this rising edge. In this mode, Blanking A works only on the falling edge of A, and Blanking B works only on the falling edge of B.

And, of course, Cycle Adjust B is usable on DPWM B.

There is no restriction preventing the two signals from overlapping each other. The diagram shows the two signals 180 degrees out of phase, but this is not required. They could be 90 degrees, 60 degrees or whatever offset is desired.

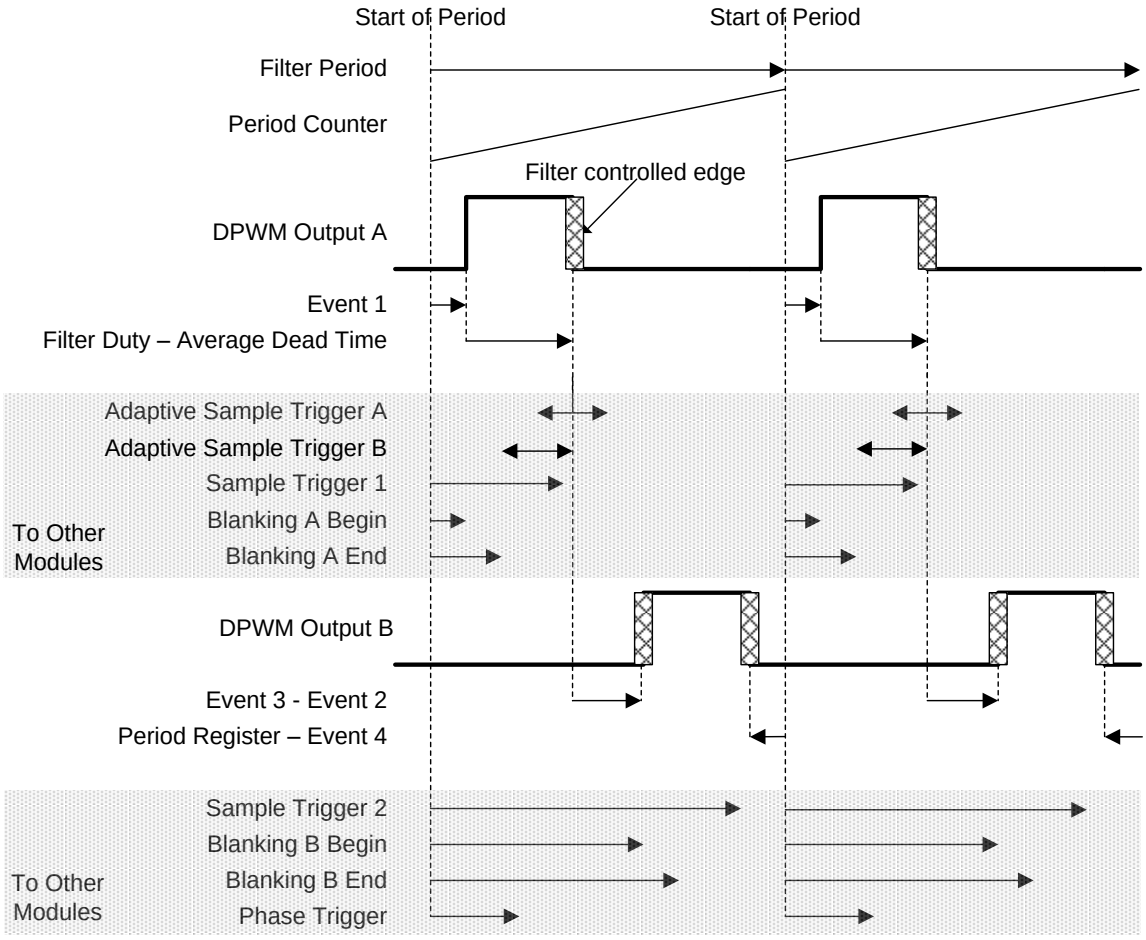
2.6 DPWM Resonant Mode

The resonant mode operation depends on the status of the RESON_DEADTIME_COMP_EN bit. Setting the RESON_DEADTIME_COMP_EN bit provides for a symmetrical waveform where DPWMA and DPWMB have the same pulse width. As the switching frequency changes, the dead times between the pulses remain the same. This mode is ideal for the LLC topology.

Clearing the RESON_DEADTIME_COMP_EN bit provides a mode where the pulse widths are the same and the duty cycle percentage is constant as the period changes. This means that as the frequency increases, the dead times shrink proportionally.

The equations for this mode are designed for a smooth transition from PWM mode to Resonant mode, as described in Section 2.10.1 Resonant LLC Example on page 27. Here is a diagram of this mode:

Resonant Symmetrical Closed Loop



Events which change with DPWM mode:

Dead Time 1 = Event 3 – Event 2
Dead Time 2 = Event 1 + Period Register – Event 4)
Average Dead Time = (Dead Time 1 + Dead Time 2)/2

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty – Average Dead Time
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 1 + Filter Duty – Average Dead Time + (Event 3 – Event 2)
DPWM B Falling Edge = Filter Period – (Period Register – Event 4)
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

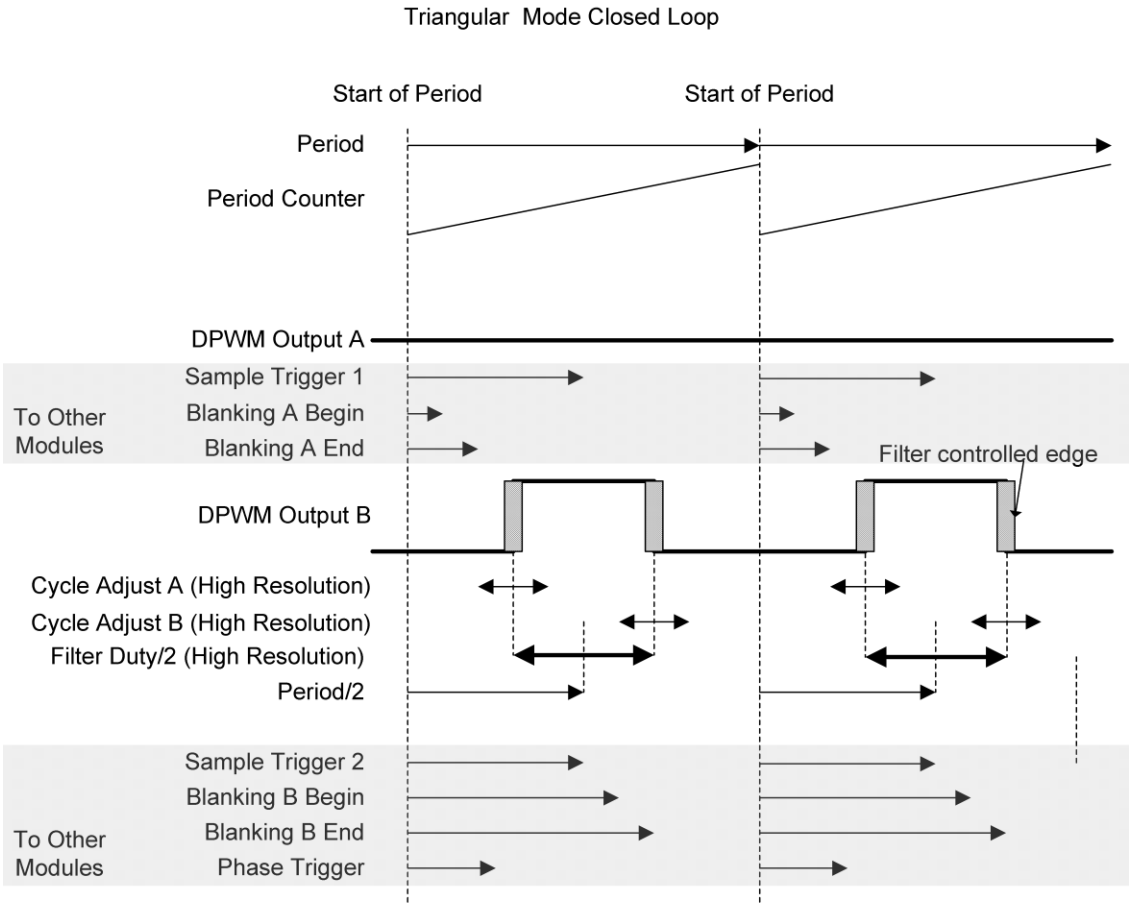
DPWM – Resonant Mode

As seen later, the Filter module has two outputs, Filter Duty and Filter Period. In the Resonant mode, the Filter is configured so that the Filter Period is twice the Filter Duty. With zero dead times, each DPWM pin would be On for half of the period. For dead time handling, the average of the two dead times is

subtracted from the Filter Duty for both DPWM pins. Therefore both pins will have the same on-time, and the dead times will be fixed regardless of the period. The only edge which is fixed relative to the start of the period is the rising edge of DPWM A. Blanking A and Blanking B both work only on DPWMA.

2.7 Triangular Mode

Triangular mode provides a very stable phase shift in interleaved PFC and similar topologies. In this case, the PWM pulse is centered in the middle of the period, rather than starting at one end or the other. In Triangular Mode, only DPWM B is available. Here is a diagram for Triangular Mode:



Events which change with DPWM mode:

DPWM A Rising Edge = None
DPWM A Falling Edge = None
Adaptive Sample Trigger = None?
DPWM B Rising Edge = Period/2 - Filter Duty/2 + Cycle Adjust A
DPWM B Falling Edge = Period/2 + Filter Duty/2 + Cycle Adjust B
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

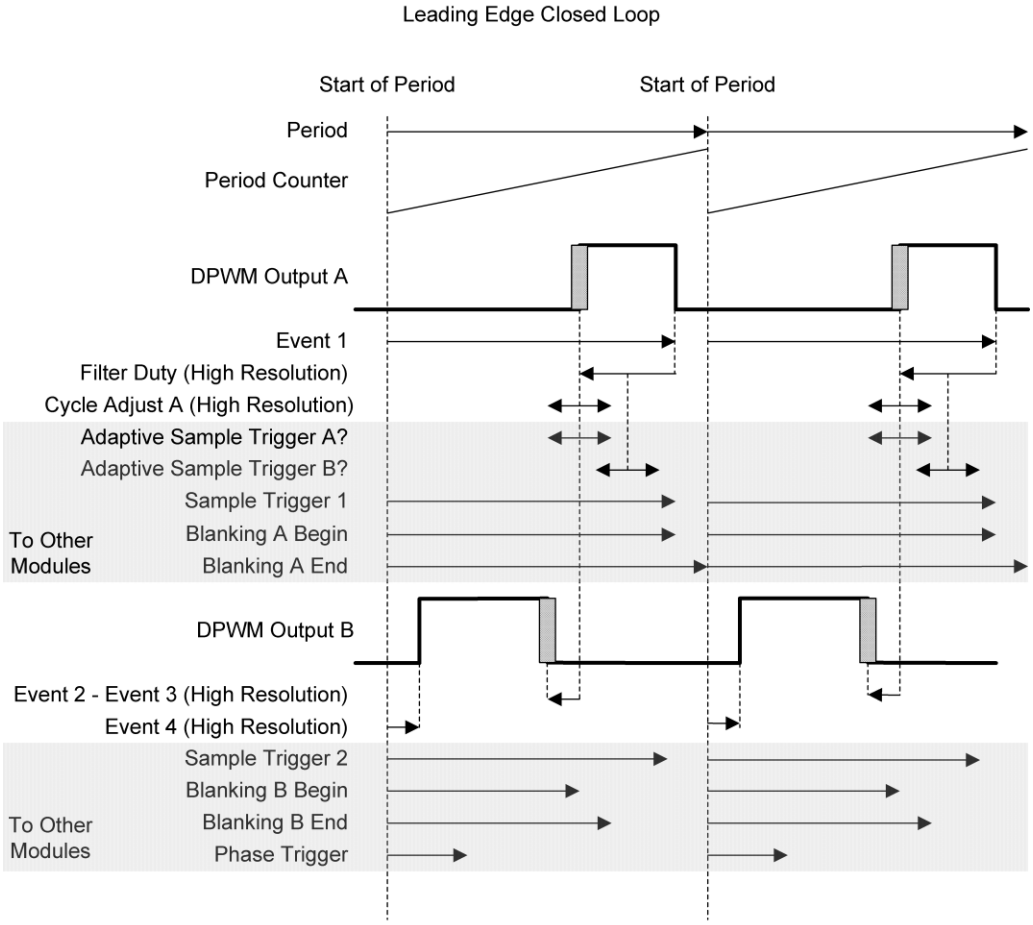
Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

DPWM – Triangular Mode

All edges are dynamic in triangular mode, so fixed blanking is not that useful. The adaptive sample trigger is not needed. It is very easy to put a fixed sample trigger exactly in the center of the On-time, because the center of the on-time does not move in this mode. Both Blanking A and Blanking B are applied to DPWMB.

2.8 DPWM Leading Edge Mode

Leading edge mode is very similar to Normal mode, reversed in time. The DPWM A falling edge is fixed, and the rising edge moves to the left, or backwards in time, as the filter output increases. The DPWMB falling edge stays ahead of the DPWMA rising edge by a fixed dead time. Here is a diagram of the Leading Edge Mode:



Events which change with DPWM mode:

DPWM A Falling Edge = Event 1
DPWM A Rising Edge = Event 1 - Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 - Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 - Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 4
DPWM B Falling Edge = Event 1 - Filter Duty + Cycle Adjust A -(Event 2 – Event 3)
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

DPWM – Leading Edge Mode

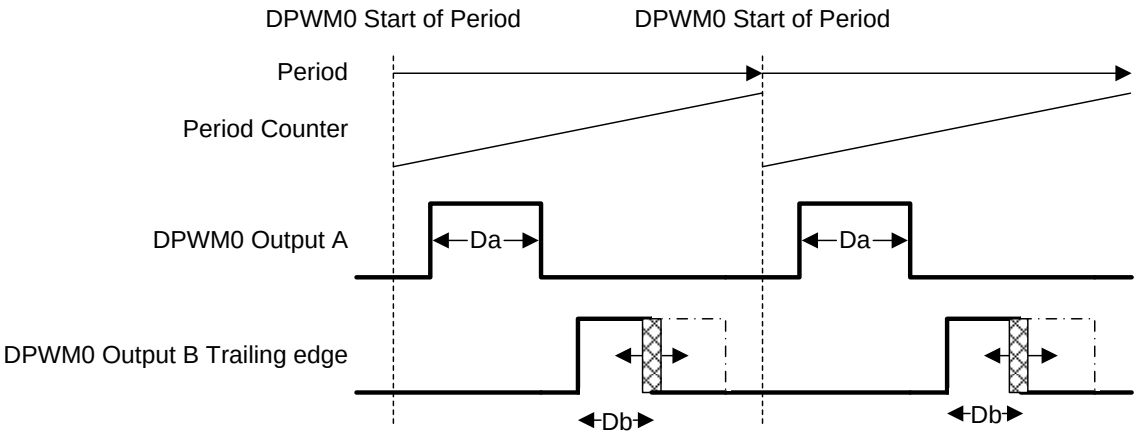
As in the Normal mode, the two edges in the middle of the period are dynamic, so the fixed blanking intervals are mainly useful for the edges at the beginning and end of the period.

2.9 Sync FET Ramp and IDE Calculation

For many topologies, it is useful to replace diodes with synchronous rectification (SR), a concept also known as Ideal Diode Emulation (IDE). In continuous conduction mode, the SR FET control is simple, because it can be turned on for the entire off time of the primary FET, minus a dead time. This is handled perfectly by Normal mode. The Sync FET Ramp and IDE calculation are only available in Normal mode. They are not compatible with the Cycle by Cycle Fault module.

However, in discontinuous mode, the SR FET needs to be turned off before the end of the period. The UCD3138 hardware provides an automatic function to make this easier. In this case, the falling edge of DPWMB is adjusted, as shown below:

Normal Mode with Sync FET IDE and/or Ramp



Sync FET edge on DPWM B controlled by Ramp logic and/or Integrated Diode equation
Stays within dead time limits for Normal Mode

SyncFET IDE (Normal Mode)

The digital hardware implements the equation $D_b = D_a * K_d$. The firmware measures Vin and Vout and calculates Kd. For example, for a Buck topology, $K_d = (V_{in} - V_{out})/V_{out}$, where D_a is duty cycle of the control FET, D_b is duty cycle of SR FET, V_{in} is input voltage and V_{out} is output voltage. The firmware periodically measures the slowly changing V_{in} and V_{out}, and puts the calculated result into the Kd register. The DPWM hardware adjusts D_b every switching cycle, maintaining proper IDE even during transients which cause rapid changes in D_a.

When starting up in prebias mode i.e. with a voltage already present on the outputs, it is difficult to accomplish precise diode emulation (IDE). One solution to this issue is to ramp the voltage up to the target without synchronous rectification (SR), and then to activate SR after the voltage is regulated. When activating or de-activating SR, in order to avoid glitches in the regulated voltage, it is best to gradually increase/decrease the Sync FET on-time. The UCD3138 provides what is termed as Sync FET Soft-On/Soft-Off (ramp) logic to accomplish this. This is documented in Section 3.3.8 **Sync FET Soft On/Off using Ramp Module**. The Ramp module in the Front End is used for this function. It will ramp up to either the limits imposed by normal mode, or to the limits imposed by the IDE logic.

With digital IDE enabled, as the system transitions from discontinuous mode into continuous conduction Mode (sync FET is on until end of the period) the IDE will stop reducing the Sync FET pulse width. This

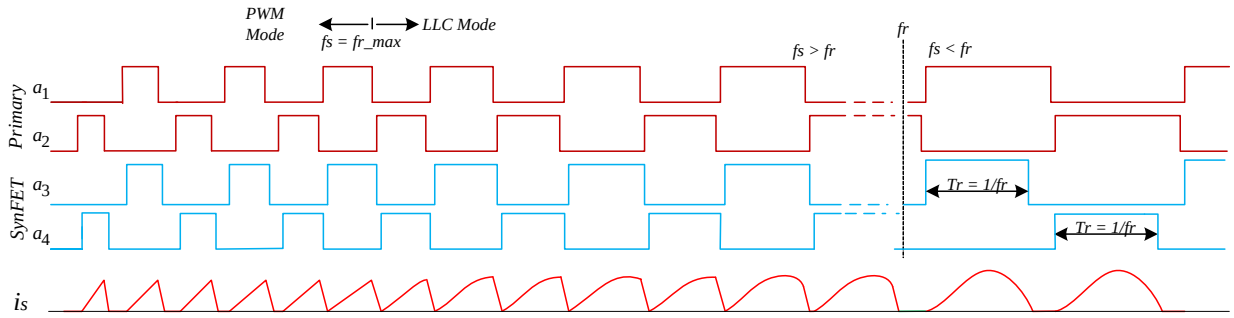
is because the reverse conduction through the Sync FET will keep Da and Db the same. It is necessary to detect DCM (Discontinuous Conduction Mode) current levels in the IDE approach. Once these levels are detected, the Sync FET should be ramped down, and then ramped back up with IDE enabled.

2.10 Automatic Mode Switching

Automatic Mode switching enables the DPWM module to switch between modes automatically, with no firmware intervention. This is useful to increase efficiency and power range and also to achieve smooth system performance (such as monotonic start-up) in certain topologies. An example of mode switching in LLC topology is provided next.

2.10.1 Resonant LLC Example

In Resonant LLC topology, three modes are used. At the lowest power, a pulse width modulated mode (Multi Mode) is used. As power increases and frequency decreases, Resonant mode is used. As the frequency gets still lower, resonant mode is still used, however the Sync FET driver changes so that the on-time is fixed and does not increase (SR Pulse Width is clamped). Here are the waveforms for the LLC:

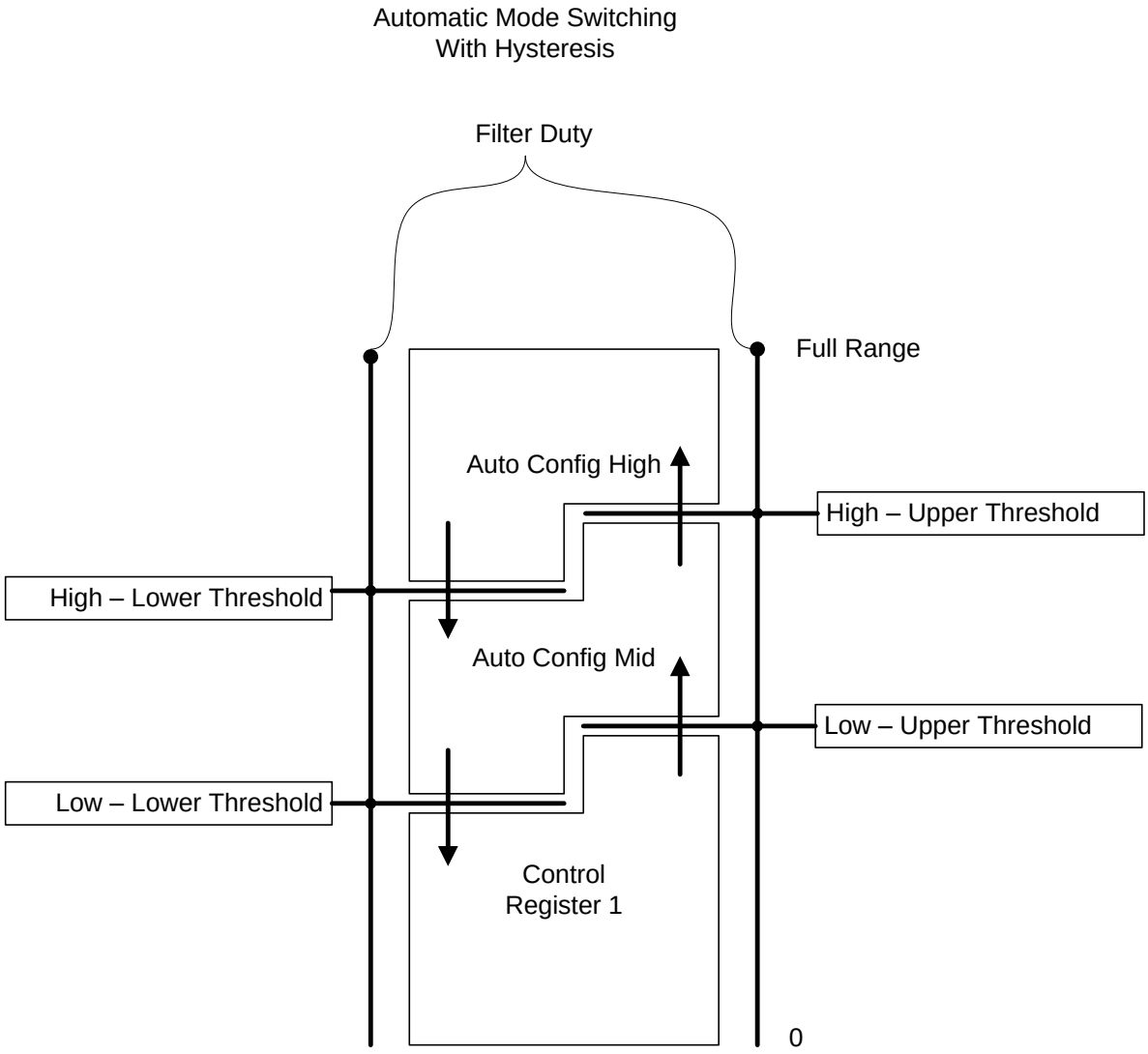


Resonant LLC implementation in UCD3138 with Automatic Mode Switching

2.10.2 Mechanism for Automatic Mode Switching

Many of the configuration parameters for the DPWM, including the mode, are in DPWM Control Register 1. For automatic mode switching, some of these parameters are duplicated in the Auto Config Mid and Auto Config High registers.

If automatic mode switching is enabled, the Filter Duty signal is used to select which of these three registers is used. There are 4 registers which are used to select the points at which the mode switching takes place. They are used as shown below:



Mechanism for Automatic Mode Switching in UCD3138

As shown, the registers are used in pairs for hysteresis. The transition from Control Register 1 to Auto Config Mid only takes place when the Filter Duty goes above the Low Upper threshold. It does not go back to Control Register 1 until the Low Lower Threshold is passed. This prevents oscillation between modes if the filter duty is close to a mode switching point. In some applications it is necessary to make the values the same, disabling hysteresis. This has to be done to make the DPWM signals from the two modes match properly at the mode switching point.

2.11 DPWMC, Edge Generation, IntraMux

The UCD3138 has sophisticated hardware for generating complex waveforms beyond the simple DPWMA and DPWMB waveforms already discussed. The DPWMC, the Edge Generation Module, and the IntraMux play a key role in delivering this capability

DPWMC is a signal inside the DPWM logic. It goes high at the Blanking B begin time, and low at the Blanking B end time.

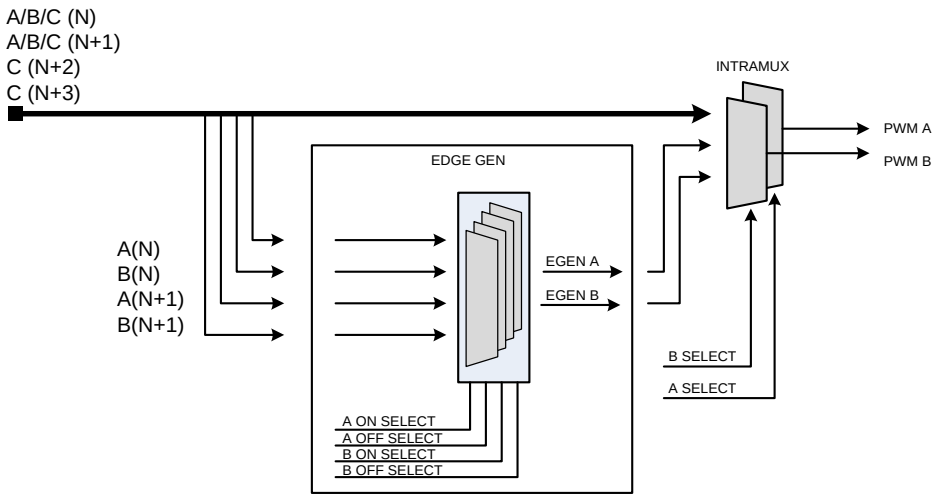
The Edge Gen module takes DPWMA and DPWMB from its own DPWM module, and the next one, and uses them to generate edges for two outputs. For DPWM3, the DPWM0 is considered to be the next DPWM. Each edge (rising and falling for DPWMA and DPWMB) has 8 options which can cause it.
The options are:

0 = DPWM(n) A Rising edge
1 = DPWM(n) A Falling edge
2 = DPWM(n) B Rising edge
3 = DPWM(n) B Falling edge
4 = DPWM(n+1) A Rising edge
5 = DPWM(n+1) A Falling edge
6 = DPWM(n+1) B Rising edge
7 = DPWM(n+1) B Falling edge

The Edge Gen is controlled by the DPWMEDGEGEN register. It also has an enable/disable bit.

The IntraMux is controlled by the Auto Config registers. The IntraMux takes signals from multiple DPWMs and from the Edge Gen. It can be programmed to route these signals to the DPWMA and DPWMB outputs. This is useful for complex topologies like Phase Shifted Full Bridge, especially when they are controlled with automatic mode switching. It is disabled by setting the Intramux to Pass Through mode for each of the DPWM signals, A and B. If the Intra Mux is enabled, high resolution must be disabled.

Here is a drawing of the Edge Gen/Intra Mux:



UCD3138 Edge-Gen & Intra-Mux

Here is a list of the IntraMux modes for DPWMA:

0 = DPWMA(n) pass through (default)
1 = Edge-gen output, DPWMA(n)
2 = DPWNC(n)
3 = DPWMB(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

Here is a list of the IntraMux modes for DPWMB:

0 = DPWMB(n) pass through (default)
1 = Edge-gen output, DPWMB(n)
2 = DPWNC(n)
3 = DPWMA(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

The DPWM number wraps around just like the Edge Gen unit. For DPWM4, DPWM(n+1) is DPWM0, DPWM(n+2) is DPWM1, and so on.

Note that the Fault logic affects the Fault module, which is before the Edge Gen and IntraMux units (refer to DPWM Block diagram in section 2.1). The effect of a fault must be calculated taking into account the impact of the Edge Gen and IntraMux units.

2.12 Time Resolution of Various DPWM registers

Different registers in the DPWM block have different time resolutions. Pulse widths are generally adjustable in nominal 250 picosecond steps, while period and phase shift are adjustable in 4 nanosecond steps. The sample trigger is adjustable in 16 nanosecond steps.

Register	Resolution	Number of bits	Bit Alignment
Phase Trigger, Period, Event1, Blanking A and B Begin Blanking A and B End Minimum Duty Cycle Low Minimum Duty Cycle High Counter Preset	4 ns.	14	Standard
Sample Trigger 1 and 2	16 ns	12	Standard
Event2,3,4	250 ps	18	Standard
Cycle Adjust A and B	250 ps	16 (signed)	Standard
Adaptive Sample	16 ns	12 (signed)	16 ns LSbit
Resonant Duty	4 ns.	16 (signed) or 14 (unsigned)	4 ns LSbit

DPWM Register Time Resolutions in UCD3138

On the UCD3138, all these registers are aligned so that their bit fields match the scaling, except for the Resonant Duty and Adaptive Sample register. All the registers are unsigned, except for the 2 adjust registers, Resonant Duty and Adaptive Sample register, which are signed to permit positive or negative adjustment.

The Resonant Duty register is used in the UCD3138 LLC reference firmware (implemented in UCD3138LLCEVM-028 EVM) as a 14 bit unsigned register. It can also be used as a 16 bit signed register. See Section 2.21 Resonant Duty Register, page 44.

This means that the Phase Trigger, Period, and Event1 registers ignore the 4 least significant bits, as shown below:

DPWM Period Register (DPWMPRD) – All other 4 ns registers with standard alignment are the same.

Bit Number	17:4	3:0
Bit Name	PRD	RESERVED
Access	R/W	-
Default	00_0011_0100_0001	0000

The Sample Trigger registers ignore the 6 least significant bits, as shown here:

DPWM Sample Trigger 1 Register (DPWMSAMPTRIG1)

Bit Number	17:6	5:0
Bit Name	SAMPLE_TRIGGER	RESERVED
Access	R/W	-
Default	0000_0010_0000	00_0000

Only the Event 2, 3, and 4 registers use all 18 bits of the field, as shown below.

DPWM Event 2 Register (DPWMEV2) – Event 3 and 4 are the same, Cycle Adjust registers only go to bit 15.

Bit Number	17:0
Bit Name	EVENT2
Access	R/W
Default	00_0000_0001_0110_0011

This means that in all these registers, each bit has the same weight in terms of time. This makes configuration simpler, since all register loads can use the same time base.

To use this feature, use the .all extension on the register structure. The bit fields do not include the ignored bits.

All of these C statements put 100 microseconds into the respective registers. Note that the "Low" resolution clock is at 4 nanoseconds, and "High" resolution is at 250 picoseconds So the corresponding numbers for the registers are 2,500 and 40,000 respectively.

```
Dpwm0Regs.DPWMPRD.all = 40000; //includes 4 unused least significant bits
Dpwm0Regs.DPWMPRD.bit.PRD = 2500;  //only puts in PRD bit field = 40000/16
Dpwm0Regs.DPWMEV1.all = 40000; //includes 4 unused bits
Dpwm0Regs.DPWMEV1.bit.EVENT1 = 2500; //EV1 is the only low resolution event register
Dpwm0Regs.DPWMEV2.all = 40000; //EV2 is high resolution, so
Dpwm0Regs.DPWMEV2.bit.EVENT2 = 40000; //both forms are the same
Dpwm0Regs.DPWMSAMPTRIG1.all = 40000; //includes 6 unused lsbs
Dpwm0Regs.DPWMSAMPTRIG1.bit.SAMPLE_TRIGGER = 625;
 //needs to be divided by 64 for 6 bits
```

The adaptive sample and resonant duty registers do not follow the standard bit alignment. Their least significant bits are worth 16 nanoseconds and 4 nanoseconds respectively.

2.13 PWM Counter and Clocks

The PWM counter is the center of the DPWM logic. There is no register that can be read to give the value of the PWM counter, but most events are triggered by it. In all modes it is allowed to count up to the period value, and then restarted at zero. Since it restarts at zero, the period is technically equal to PERIOD + 1. So in the example above, the number should really be 2499. Generally the error is unimportant. In all modes but the resonant modes, the period is a fixed value. In the resonant modes, the period comes from the output of a Filter.

The PWM counter is also restarted by the receipt of a sync signal (if sync is enabled), as shown above in Section 2.4, DPWM Phase Shift Mode on page 19.

Sync signals received exactly at the end of the period run very smoothly. Sync signals received at other times during the period will restart the counter and the period. The effects of this should be taken into consideration for each application.

Even though the period register has only 14 bits, the PWM counter effectively has 18 bits. Each 4 nanosecond period is subdivided into 16 intervals, nominally 250 picoseconds long. The extra 4 bits representing these intervals are called "high resolution bits".

2.14 DPWM Registers - Overview

This section discusses each DPWM register, with examples of their use where appropriate. In addition, it interacts with many other peripherals, parts of which are also described below.

2.15 DPWM Control Register 0 (DPWMCTRL0)

The DPWM Control Register 0 is one of 3 DPWM control registers which configure the DPWM. All 3 registers control a variety of DPWM functions. It is not possible to draw a clear dividing line between the 3 registers.

2.15.1 DPWM Auto Config Mid and Max Registers

There are two other registers – DPWMAUTOMAX and DPWMAUTOMID, which have many of the same bits as control register 0.

These two Auto Mode Switching (AMS) registers are used in topologies where the DPWM mode changes automatically as the filter output changes, such as resonant and phase shifted full bridge. See the section 2.10.2Mechanism for Automatic Mode Switching in page 27 on the auto switch level registers for more information on mode switching.

Not all bits in DPWMCTRL0 are duplicated in the auto registers. The bits that occur only in DPWMCTRL0 are used for all modes. Bits were selected based on mode switching needs for LLC and PSFB topologies. The following bitfield descriptions tell whether each field occurs in the auto mode switching registers.

2.15.2 Intra Mux

The Intra Mux bit fields, PWM_A_INTRA_MUX, and PWM_B_INTRA_MUX, enable signals from different sources to be multiplexed into the 2 DPWM outputs, A and B. This functionality is used in full and half bridge topologies. The default value for this bit field, 0, causes normal functionality, with the standard DPWM waveforms as described in the mode descriptions above section to appear on the DPWMA and DPWMB pins. For details of the Intra Mux, see section 2.11 DPWMC, Edge Generation, IntraMux, page 28.

These fields also occur in the AMS registers.

2.15.3 Cycle by Cycle Current Limit Enable

There are several enable bits related to cycle by cycle current limit:

DPWMCTRL0 contains:

CBC_PWM_C_EN
CBC_PWM_AB_EN
CBC_ADV_CNT_EN
CBC_SYNC_CUR_LIMIT_EN
CBC_BSIDE_ACTIVE_EN

All of these bits, except for CBC_BSIDE_ACTIVE_EN also occur in the AMS registers.

The first two, CBC_PWM_C_EN and CBC_PWM_AB_EN simply enable cycle by cycle current limit for their respective signals. In all modes, CBC_PWM_EN has an independent effect on DPWMC. The other bits have no effect on DPWMC

The other three bits have different effects in different modes. Here are the effects:

Normal Mode

In normal mode, a CBC event will cause DPWMA to go low before the time dictated by the CLA. The dead time for DPWMB will be preserved, so the rising edge of DPWMB will be moved forward by the same amount as the falling edge of DPWMA.

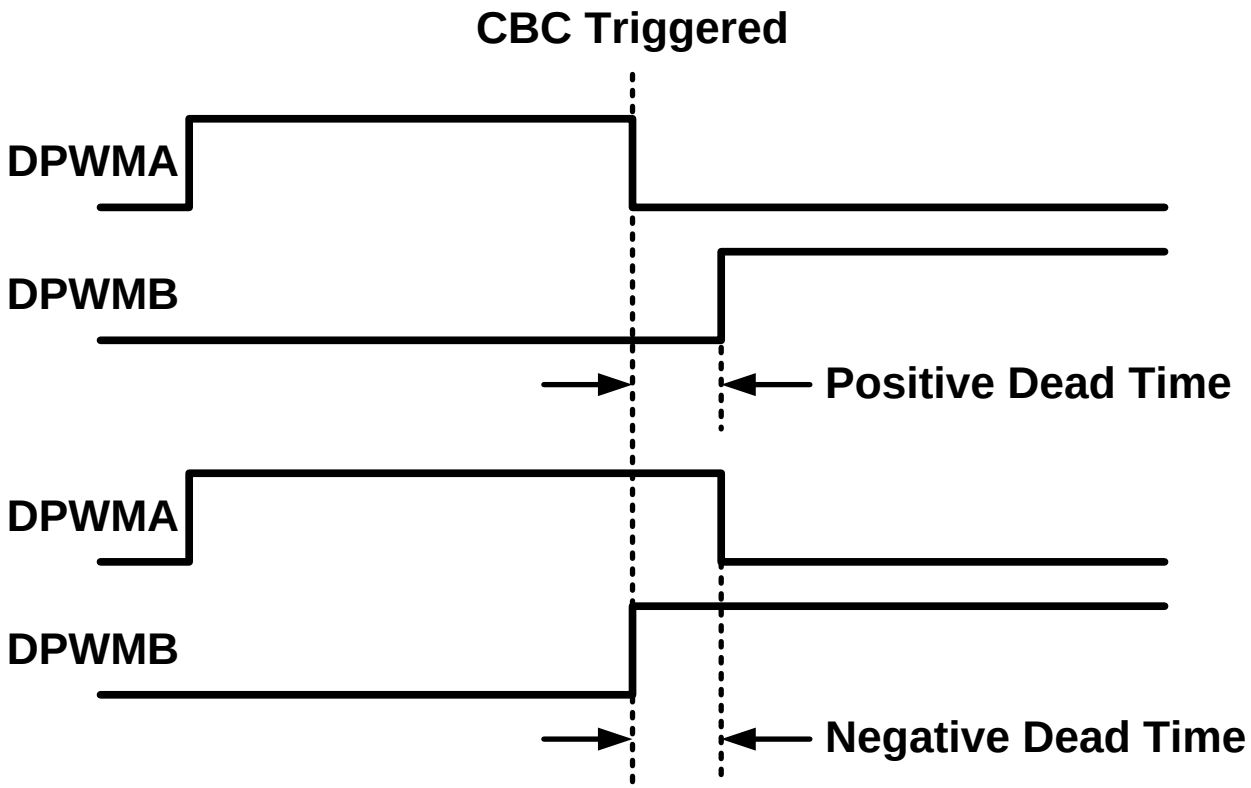
There are only two options for setting the CBC bits in normal mode:

1. All cleared, no CBC.

2. Set both CBC_PWM_AB_EN and CBC_ADV_CNT_EN to get CBC.

CBC_BSIDE_ACTIVE_EN has no effect. Normal mode has some support for negative dead times, as does the CBC logic. Even negative dead times will be preserved. As seen in the figure below, if there is a negative dead time, the minimum pulse width on DPWMA will be equivalent to the dead time. To preserve a negative dead time, the CBC will trigger a rising edge on DPWMB. After the dead time is expired, then DPWMA will fall.

With a positive dead time, of course, DPWMA will fall with the CBC event, and DPWMB will rise after the dead time:



Even if DPWMB is being used as a GPIO, it is important to program Event 3 for dead times with CBC.

Resonant/multi Mode

In resonant/multi mode, the systems are often symmetrical. In this case, DPWMB may need to be controlled by the Cycle by Cycle Fault logic as well. Sometimes a shortened on time on one DPWM pin needs to be followed by an equal length on time on the other DPWM pin to prevent an offset from building up in a capacitor or inductor. In this case, it is possible to enable *duty cycle matching* in these two modes. If DPWMA or DPWMB is cut short by a CBC event, the next pulse, on the other DPWM pin, will also be shortened to the same length.

Here are the states for resonant and multi modes:

- All cleared - no CBC
- Only CBC_PWM_AB_EN set - CBC on A only, no duty cycle matching
- CBC_PWM_AB_EN and CBC_BSIDE_ACTIVE_EN only set - CBC on A and B, no duty matching
- All three set - CBC on A and B, duty cycle matching
- CBC_PWM_AB_EN and CBC_ADV_CNT_EN set, CBC_BSIDE_ACTIVE_EN not set - CBC on A only and B duty cycle matches to A

Truth table:

CBC_PWM_AB_EN	CBC_ADV_CNT_EN	CBC_BSIDE_ACTIVE_EN	CBC A	CBC B	duty match
0	x	x	0	0	0
1	0	0	1	0	0

1	1	0	1	0	B matches A
1	1	1	1	1	1

CBC_SYNC_CUR_LIM_EN is used to control the slave sync. If this bit is set, the slave sync is advanced during current limit. This is not used in any topology configuration at this time. If this bit is set, the sync out pulse from the DPWM will occur if the CBC fault occurs. If the CBC fault does not occur during a period, the sync pulse will occur according to the normal setting of the sync control bit fields.

For more information on cycle by cycle current limit, refer to the section 6 Fault Mux in page 81.

2.15.4 Multi Mode on/off

The MULTI_MODE_CLA_A_OFF and MULTI_MODE_CLA_B_OFF bits dictate which calculation is used for each DPWM pin in multi mode only. In other modes they should not be set. If the bit is cleared, the on-time of the DPWM pin is controlled by the Filter output. If the bit is set, then the on-time is controlled by the Event registers.

The AMS registers only have MULTI_MODE_CLA_B_OFF, they do not have MULTI_MODE_CLA_A_OFF.

2.15.5 Minimum Duty Mode

The MIN_DUTY_MODE bits select how the DPWM handles minimum duty cycle limits.

- 0 Default - Filter output is passed directly through to the DPWM
- 1 – Filter value passed through if above minimum. If below minimum, no pulse from DPWM
- 2 - Filter value passed through if above minimum. If below minimum, DPWM pulse width = minimum value

There are two registers setting minimum duty and hysteresis:

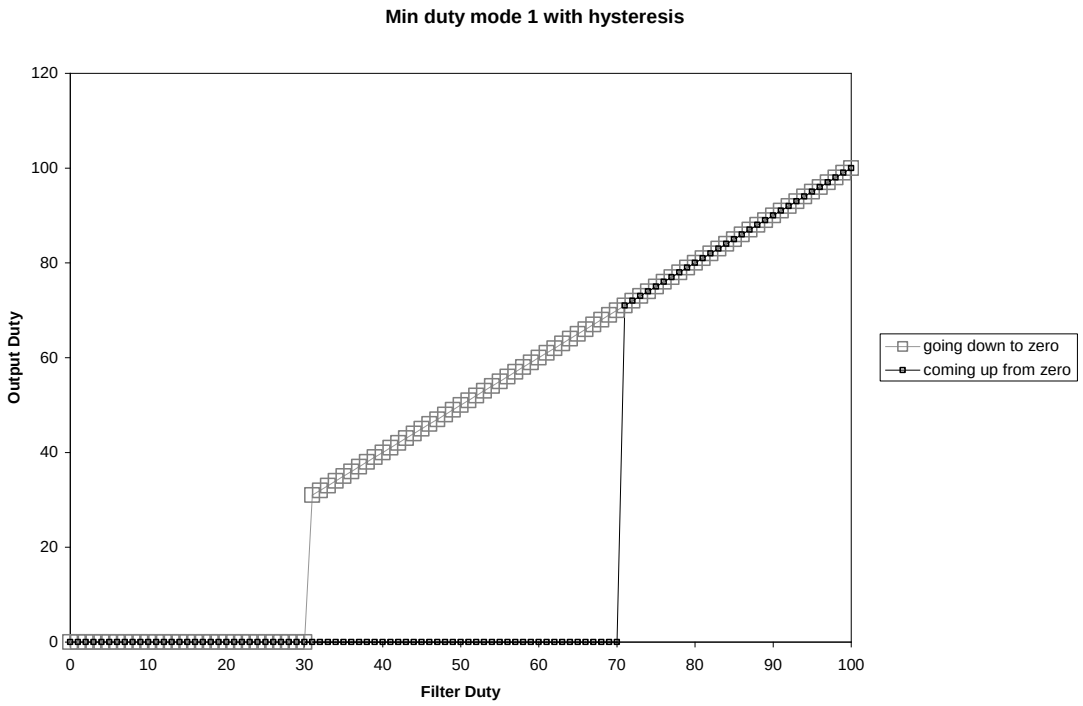
DPWMMINDUTYLOW
DPWMMINDUTYHI

The Low register sets the point at which the minimum duty mode will take effect as the duty drops. In mode 2, it also sets the minimum duty.

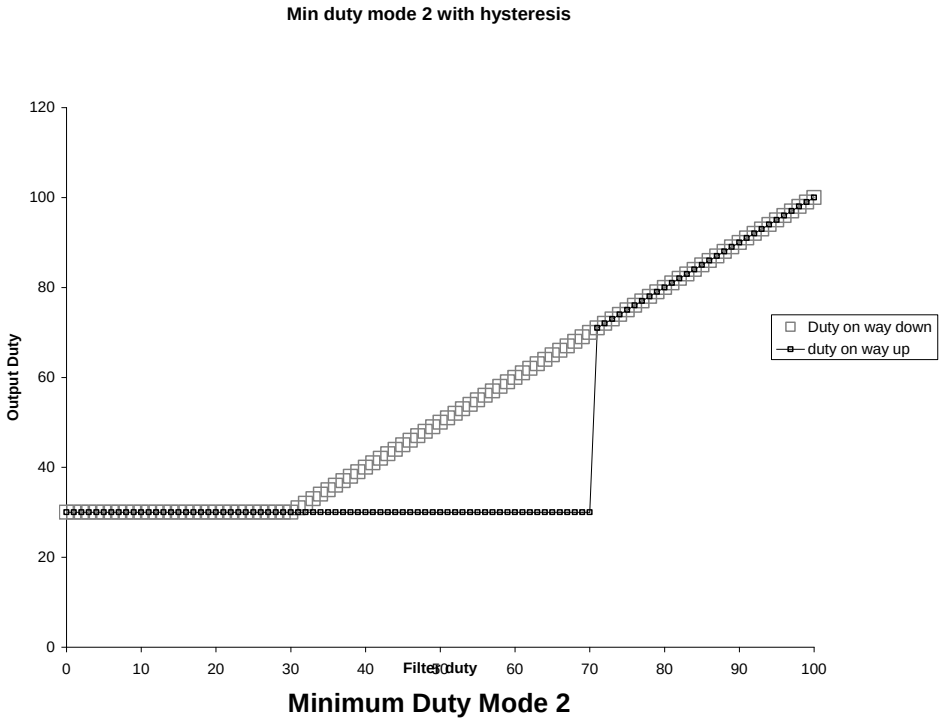
The High register sets the point at which minimum duty mode is exited as the duty goes up.

These bits are not duplicated in the AMS registers.

These two graphs show modes 1 and 2 with PMMINDUTYLOW at 30, and DPWMMINDUTYHI at 70.



Minimum Duty Mode 1



Minimum Duty Mode 2

2.15.6 Master Sync Control Select

The MASTER_SYNC_CNTL_SEL bit selects where the sync output of the DPWM channel comes from.

The default value, 0, causes the sync delay to come from the Phase Trigger register. This is useful for systems that have fixed intervals between phases, such as interleaved PFC and hard switching full bridge. See Section 2.4, DPWM Phase Shift Mode, on page 19.

Putting a 1 into this bit causes the master sync output to be controlled by the Filter output.

This bit is duplicated in the AMS registers.

2.15.7 Master Sync Slave Enable

Setting the MSYNC_SLAVE_EN bit enables the DPWM channel to be slaved to the sync output of another DPWM channel. This bit works together with the DPWMx_SYNC_SEL bits in the DPWMMUX register in the Loop Mux section. The sample code below makes DPWM1 a slave to DPWM0:

```
LoopMuxRegs.DPWMMUX.bit.DPWM1_SYNC_SEL = 0; //DPWM1 is slave to DPWM0
Dpwm1Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; //enable slave mode for DPWM1
```

This bit is not duplicated in the AMS registers.

2.15.8 D Enable

Normally, the Filter Duty (D) is used to set the on-time of DPWM pins directly. In other words, OnTime = D. The D_ENABLE bit can be used to make the OnTime = 1-D instead.

A default value (0) causes the output of the Filter to be used directly for DPWM output calculations. So in multi mode, for example, the DPWMA and B on-times would increase as the Filter Duty increases.

If the D_ENABLE bit is set, however, the Filter Duty is subtracted from the period register. In this case, as the Filter Duty increases from zero to full range, the on-time will decrease from 100% of the period to 0% of the period.

This bit is not duplicated in the AMS registers.

2.15.9 Resonant Mode Fixed Duty Enable

The RESON_MODE_FIXED_DUTY_EN bit only controls the duty cycle width in the resonant modes. With the default (0) value, the duty cycle comes from the filter directly. This is for use above the lower resonant frequency, Fmin, and provides a duty cycle that fills half the period minus a fixed dead time.

Setting this bit causes the pulse width to be derived from the Auto Switch High Upper Threshold Register.

This bit is generally only set for LLC for the Sync FETs in the mode where the output frequency is below the lowest resonant frequency of the circuit. At this point any increases in pulse width are not beneficial, so they are stopped. There is also a waveform showing the modes in Section 2.10.1, Resonant LLC Example on page 27.

This bit is duplicated in the AMS registers.

2.15.10 DPWM A and B Fault Polarity

The PWM_A_FLT_POL and PWM_B_FLT_POL bits increase the flexibility of the DPWM by permitting arbitrary output states for the DPWM pins in case of a fault. The values in these bits will also appear on these pins when the DPWM is disabled. These values actually appear on the output of the Fault Module in the DPWM. Therefore, if the IntraMux or Edge Generation units are used, the same value may not appear on the output of the DPWM.

These bits do not affect the DPWM status after device reset. After reset, all DPWM pins are configured as outputs and actively driven low.

These bits are not duplicated in the AMS registers.

2.15.11 Blank Enable

The BLANK_A_EN and BLANK_B_EN bits are used for fault detection. They work with the blanking registers – See Section 2.26 Blanking Registers on page 46 – to enable blanking for current limit detection. Without blanking, noise may cause false Cycle By Cycle (CBC) fault detection.

These bits are not duplicated in the AMS registers.

2.15.12 DPWM Mode

The PWM_MODE bits select the mode for the DPWM. See the DPWM reference section for the mode numbers, and sections above for the descriptions of the various modes.

These bits are duplicated in the AMS registers.

2.15.13 DPWM Invert

The PWM_A_INV and PWM_B_INV bits invert the output of the DPWMA and DPWMB pins.

These bits do not affect the DPWM status after device reset however. After reset, all DPWM pins configured as outputs which are actively driving low.

These bits are not duplicated in the AMS registers.

2.15.14 Filter Enable (CLA_EN)

In the past, the filter was called a Control Law Accelerator, so for historical reasons, the Filter Enable bit is called CLA_EN. This bit, when set, causes the DPWM to take its input from a Filter. Otherwise, the DPWM output comes from the DPWM registers only.

This bit is duplicated in the AMS registers.

The filter which controls each DPWM is selected by the DPWMx_FILTER_SEL bit in the DPWMMUX register in the Loop Mux.

2.15.15 DPWM Enable

The PWM_EN bit, when set enables the DPWM channel. If it is 0 (default), the DPWM outputs are set to the value in the DPWM Fault Polarity bits (Section 2.15.10 DPWM A and B Fault Polarity on page 37.

This bit occurs only in the Control 0 register, not in the AMS registers.

2.16 DPWM Control Register 1

Like DPWMCRTL0, the DPWMCTRL1 register contains a wide assortment of control bits for the DPWM.

2.16.1 Period Counter Preset Enable

The PRESET_EN bit adds flexibility for systems with multiple DPWM modules that have different period starting times. It can be used to start up all DPWMs simultaneously, even if their periods do not start at the same times. It can also be used for synchronizing these DPWMs.

Normally, the period counter is reset to zero by three events

1. DPWM ENABLE
2. Sync Received (slave mode enabled)
3. Counter reaches Period Register value

If PRESET_EN is enabled, this changes:

1. DPWM_ENABLE – Period Counter set to preset value
2. Sync Received (slave mode enabled) – Period Counter set to preset value
3. Counter reaches Period Register value – Period counter set to zero

2.16.2 Sync FET Ramp Enable

The SYNC_FET_EN bit enables the Sync FET Ramp logic to take control of DPWM B. For more on the Ramp logic, see Section 3.3.8 Sync FET Soft On/Off using Ramp, on page 59. The Front End which provides the Ramp data is selected in the DPWMMUX register in the Loop Mux. The following code enables Sync FET Ramp for DPWM0, and sets up Front End 0's Ramp Engine to provide the ramp source.

```
LoopMuxRegs.DPWMMUX.bit.DPWM0_SYNC_FET_SEL = 0;
        //use ramp engine on Front End 0
Dpwm0Regs.DPWMCTRL1.bit.SYNC_FET_EN = 1;  //enable sync FET ramp
```

The Sync FET Ramp logic ramps the pulse width of DPWMB up from a starting point to a width controlled by Normal mode, or by the IDE function, if enabled. It only works in Normal mode.

2.16.3 Burst Mode Enable

Setting the BURST_EN bit enables burst (light load) mode for this DPWM. For more information on Light load mode, see the light load section.

2.16.4 Current/Flux Balancing Duty Adjust

Setting the CLA_DUTY_ADJ_EN bit enables the Current Balancing logic to modify the input to the DPWM so that current controlled by this DPWM can be balanced with the current controlled by another DPWM in the same UCD3138. For more information, see the Current Balancing section.

2.16.5 Sync Out Divisor Selection

The SYNC_OUT_DIV_SEL bit field selects a divisor generating the sync out pulse on the external sync out pin. It is only effective on the sync out, not on internal chip sync signals sent to other DPWMs.

The divisor has 4 bits, and a range from 1 to 16 for the divisor. The divisor = SYNC_OUT_DIV_SEL + 1.

So 0 in the bit field would give a divisor of 1, 1 gives a divisor of 2, and so on.

2.16.6 Filter Scale

The CLA_SCALE bits control shifting of the Filter Duty output before it is used by the DPWM. Shifts available range from a 3 bit right shift to a 3 bit left shift. The Filter Period is not scaled by these bits.

The default value, 0, causes no shift. For the shift table, see the DPWM reference section 8.2, DPWM Control Register 1 (DPWMCTRL1)on page 95.

This can be used in complex topologies where the same filter output is needed for different circuits at different frequencies. It can also be used to change the overall gain of the Filter.

2.16.7 External Sync Enable

Setting the EXT_SYNC_EN bit causes the DPWM to use the Sync In pin as a source for Sync.

2.16.8 Cycle By Cycle B Side Active Enable

For more on the CBC_BSIDE_ACTIVE_EN bit, see Section 2.15.3 above Cycle by Cycle Current Limit Enable on page 33.

2.16.9 Auto Mode Switching Enable

The AUTO_MODE_SEL bit, when set, enables auto mode switching.

2.16.10 Event Update Select

The EVENT_UP_SEL enables 4 different modes of DPWM Event Updating. The DPWM needs a period of 72 nanoseconds (nominal) to update its timing for the next period. During this period, it takes the latest Filter outputs and any firmware changes to register values and recalculates the timing of the DPWM signals. **The time selected for update should NOT have any DPWM edges moving in or out of the window.**

CAUTION: *If DPWM edges move in or out of the Event Update Window, those transitions may be missed, leading to DPWM pulses longer or shorter than expected.*

The modes are:

- 0 – As soon as Filter calculation is done
- 1 – At end of period (starts at end of period, and extends 72 nsec into start of new period)
- 2 - At time set by sample trigger 2
- 3 – At both End of Period and at time set by sample trigger 2

Note that all modes except for mode 1 make the Event Update timing dependent on the position of the sample trigger. For most topologies, mode 1 is used, and dead times or minimum pulse widths are used to keep moving edges out of the first 72nsec of the DPWM period. Please refer to the reference firmware code provided with UCD3138 EVMs for specific guidance regarding each topology.

2.16.11 Check Override

The CHECK_OVERRIDE bit, when set, overrides the internal DPWM checking. The DPWM checking will prevent invalid placement of Event settings/period settings or invalid configurations.

Setting this bit may be necessary for some topologies.

2.16.12 Global Period Enable

The GLOBAL_PERIOD_EN bit, if set, enables the use of the Global Period register to provide the period for this DPWM. It is intended for use with systems which use multiple DPWMs and have need for frequency dithering. This makes it possible to change the frequency of multiple DPWMs at one location.

For more information, see 5.8 PWM Global Period Register (PWMGLBPRD), page 79.

2.16.13 Using DPWM Pins as General Purpose I/O

There are 6 bits in DPWMCTRL1 which can be used to make the DPWM pins into general purpose I/O pins:

These bits take effect immediately.

- PWM_A_OE – 0 makes DPWMA into an output if enabled as a GPIO, 1 makes it an input
- PWM_B_OE – 0 makes DPWMB into an output if enabled as a GPIO, 1 makes it an input
- GPIO_A_VAL – Value put on DPWMA if it is an output
- GPIO_B_VAL – Value put on DPWMA if it is an output

GPIO_A_EN – 1 enables DPWMA as a GPIO
GPIO_B_EN – 1 enables DPWMB as a GPIO

In addition, there are 2 bits in the DPWMOVERFLOW register which are also used for GPIO:

- GPIO_A_IN – reports level on DPWM_A pin if used as input
- GPIO_B_IN – reports level on DPWM_B pin if used as input

2.16.14 High Resolution enable/disable

There are 5 bits which all enable/disable High Resolution Mode in some way or another

- PWM_HR_MULT_OUT_EN – Set only for multi mode
- HIRES_SCALE (2 bits) – Sets resolution of DPWM high res block
- ALL_PHASE_CLK_ENA – enables all phases or only needed phases
- HIRES_DIS – disables high res logic

As a general rule, all can be disabled when high resolution is not possible, and all should be enabled when high resolution is possible and required.

2.16.15 Asynchronous Protection Disable

The PWM_A_PROT_DIS and PWM_B_PROT_DIS bits disable asynchronous protection on their respective pins. Please consult to the reference firmware code provided with UCD3138 EVMs for specific guidance on whether to set these bits or not in the desired topology.

2.16.16 Single Frame Enable

The SFRAME_EN bit enables a single frame to be output from the DPWM. It is useful for putting out a single pulse on the DPWM, and triggering a single Front End and Filter cycle. It can be used, for example, when measuring input voltage on an isolated supply. To use Single Frame enable, first initialize the DPWM module and set the SFRAME_EN bit, and enable the DPWM globally. To actually start the single frame, set the PWM_EN bit. This will trigger a single frame.

2.17 DPWM Control Register 2

The DPWMCTRL2 register, like the other 2 control registers, has a wide selection of bit fields.

2.17.1 External Synchronization Input Divide Ratio

The SYNC_IN_DIV_RATIO bit field has 4 bits, which are initialized to zero at reset. They set the divide ratio for the synchronization both from the outside and from another DPWM. The divide ratio is the bit field value plus 1. So 0 is divide by 1, 1 divide by 2, and so on.

2.17.2 Resonant Deadtime Compensation Enable

Setting the RESON_DEADTIME_COMP_EN bit enables a dead time adjustment to the CLA Duty signal from the Filter. This compensation, which only has an effect in resonant mode, makes it possible to have constant, fixed, symmetrical dead time in resonant mode for the full range of frequencies. Generally this is the best configuration for LLC. If the bit is not set, the CLA Duty Signal is used without adjustment. This leads to DPWMA putting out 50% Duty + Cycle Adjust A, and DPWMB putting 50% - dead time + Cycle Adjust B, which cannot be made to yield a symmetrical signal on A and B over the frequency range for LLC.

2.17.3 Filter Duty Select

The FILTER_DUTY_SEL bit field has 2 bits, selecting from 3 modes. These modes select what value is sent to the Resonant Duty input of the Filter Duty multiplicand multiplexer. For example, if LoopMux.FILTERMUX.FILTER0_PER_SEL is set to 0, and the OUTPUT_MULT_SEL bits for Filter 0 are

set to 3, then the FILTER_DUTY_SEL will select the Filter Duty multiplicand. This value will be multiplied by the output of the filter to scale it appropriately for the DPWM.

Bit Value	Multiplier for Filter Value	Result
0	DPWM Period	Maximum Filter output gives 100% duty cycle
1	Event 2	Maximum Filter output gives Event 2 duty cycle
2	Resonant Duty Register	Maximum Filter output gives value of Resonant Duty Register
3	Not applicable	

Mode 2 is used for LLC with Resonant Mode.

2.17.4 Ideal Diode Emulation (IDE) Enable for PWMB

Setting the IDE_DUTY_B_EN bit enables the digital IDE logic to take control of DPWM B. The IDE logic is used to make sync FETs turn off at the perfect times, emulating an ideal diode (one with lower voltage drop). See Section 2.9, Sync FET Ramp and IDE Calculation on page 26 for more details.

2.17.5 Sample Trigger 1 Oversampling

As mentioned earlier, the DPWM module generates signals to generate a sample trigger in the Error ADC in the Front End. The DPWMs can also provide oversampling function in co-ordination with the sample triggers. The SAMP_TRIG1_OVERSAMPLE bit field permits oversampling of 2, 4, and 8 samples in the Front End. The samples are equally distributed in time, starting at the start of the period, and with the last sample at the Sample Trigger 1 point.

The values are:

- 0 – 1 sample at the sample trigger time.
- 1 – 1 sample at ½ of the sample trigger time, and one at the sample trigger time
- 2 – 4 samples at ¼, ½, ¾, and full sample trigger time
- 3 – 8 samples at 1/8, ¼, 3/8, ½, 5/8, ¾, 7/8 and full sample trigger

Sample trigger 1 can be used either to trigger a complete cycle with Front End and Filter, or it can be used for spatial averaging. See the Front End section, especially Section 3.1.5 EADC Averaging, page 52.

2.17.6 Sample Trigger 1 Mode

In addition to oversampling, Sample Trigger 1 offers several modes of calculation. The SAMPLE_TRIG1_MODE bit field selects from 4 of these:

- 0 - Sample Trigger is set using Sample Trigger register (DPWMSAMPTRIG1)
- 1 – Sample Trigger = Event 1 + (DUTY/2) + Adaptive Offset where Duty is most recent Filter Duty
- 2 – Sample Trigger = Event 1 + (DUTY/2) + Adaptive Offset where Duty is Filter Duty from last cycle
- 3– Sample Trigger = Event 1 + DUTY + Adaptive Offset + Fixed Offset where Filter Duty is from last cycle

On the diagrams earlier in this chapter, option 1 is called Adaptive Sample Trigger B, and option 3 is called Adaptive Sample Trigger A

The Adaptive Offset comes from the DPWMADAPTIVE register, which is an 11 bit signed register. Without the Adaptive Offset, the sample trigger will be in the middle of the on-time for DPWMA in Normal and Multi Modes. The Adaptive Offset is used to correct for system delays in gate drivers, FET turn-on

times and voltage and current sensing circuits. Using the Adaptive Offset properly can put the sample trigger in the middle of the voltage or current on-time. The adaptive offset register has the same resolution as the Sample Trigger Register – 16 nanoseconds. The adaptive register, though is not mapped the same. Bit 0 is the first usable bit. See the DPWM Reference section for more information

Note that using adaptive offset will cause the phase delay of the control loop to change somewhat as the duty cycle changes.

The Fixed Offset in mode 3 is a value of 4. This is added to the DPWMADAPTIVE Register and to the Event 1 and Duty Terms

2.17.7 Sample Trigger Enable bits

Sample Trigger 2 is only driven by the Sample Trigger 2 Register - DPWMSAMPTRIG2. Setting the SAMPLE_TRIG_2_EN bit enables it.

SAMPLE_TRIG_1_EN enables Sample Trigger 1.

2.18 Period and Event Registers

The period and event registers DPWMPRD, DPWMEV1, DPWMEV2, DPWMEV3, and DPWMEV4 have different effects in different modes. See DPWM Modes below for more information about each mode. Generally the registers work somewhat as described above in Section 2.2 Introduction to DPWM, page 15. Often, the pulse widths are controlled by the filter, and the differences between Event Registers are used as dead times.

2.19 Phase Trigger Register

The DPWMPHASETRIG register is a low resolution (4 ns.) register. It dictates the number of 4 ns. steps between the start of the period and the output of a sync pulse for synchronizing a slave DPWM. See Section 2.4 DPWM Phase Shift Mode, page 19.

2.20 Cycle Adjust Registers

DPWMCYCADJA and DPWMCYCADJB are registers that are added to the Filter Duty before the DPWM pulse width is calculated. They have different effects in different modes, see the DPWM Mode sections above. They are signed high resolution registers so that the duty can be increased or decreased from the Filter value. They only have 16 bits, so they cannot adjust the full 18 bit range of the DPWM. But their range is still +-8 milliseconds, which is typically more than a whole switching period.

High resolution is 250 picosec, and the range of a signed 16 bit value is $\pm 2^{15}$. So

$$2^{15} \times 250\ psec = 8.192\ msec$$

2.21 Resonant Duty Register

This register is used in LLC topologies to produce the correct Filter Duty output. The Filter output is multiplied by this register to calculate Filter Duty. In the LLC reference firmware (UCD3138LLCEVM-028)

it is set to ½ of the maximum desired period. In this case, bits 13-0 are used as an unsigned number. To enable this mode, the DPWM must be in Resonant Mode, and the FILTER_DUTY_SEL field in DPWMCTRL2 must be set to a 2.

If FILTER_DUTY_SEL is set to 0 or 1 and the DPWM is in resonant mode, the 16 bit signed contents of the register are added to the Filter Period value, and the result is used for the DPWM Period. This is another option for adjusting the resonant mode timing to match other modes across a mode shift. This mode is not currently used in any topologies.

2.22 DPWM Fault Control Register

See the Fault Mux section for information on the DPWMFLTCTRL register.

2.23 DPWM Overflow Register

The DPWMOVERFLOW register has, as already mentioned, 2 bits which give the input status of the DPWM pins when they are used as general purpose I/O.

It also has 6 bits which indicate that the protection logic for the DPWM has detected overflows.

2.24 DPWM Interrupt Register

The DPWMINT register has interrupt enable bits, interrupt flags, one interrupt flag clear bit, and one interrupt scale register.

For more information on the enable bits and flags related to faults, see the Fault Mux Reference section.

2.24.1 DPWM Period Interrupt Bits

There are three bit fields related to the Period interrupt.

PRD is the flag which indicates that there is a period interrupt occurring. It is only a strobed signal, so it is very unlikely that it will ever be read as set. If the interrupt bit is set, and no other bits are set, this means it is the period bit which has set it.

PRD_INT_EN enables the period interrupt.

PRD_INT_SCALE programs a divider for the period interrupt. The selections range from an interrupt every period to an interrupt every 256 periods. See the DPWM Reference section for the table.

Note that if the DPWM is disabled, under most circumstances, it will generate a period interrupt continuously, if the interrupt is enabled.

2.24.2 Mode Switching Interrupt Bits.

There are three bit fields related to the Mode Switching Interrupt.

See Section 2.29 DPWM Auto Switch Registers, page 47 for more detail on Mode Switching.

MODE_SWITCH goes high when the DPWM has switched modes.

MODE_SWITCH_INT_EN enables this interrupt.

A rising edge on MODE_SWITCH_FLAG_CLR clears the MODE_SWITCH bit. This bit is not auto cleared, so it will be necessary to clear it with firmware before the next rising edge.

2.24.3 INT bit

The INT bit shows that one or more of the interrupt flags is set and enabled, and the DPWM is sending an interrupt to the Central Interrupt Module (CIM). When the interrupt bits are cleared, so is the INT bit.

2.25 DPWM Counter Preset Register

If enabled, the DPWMCNTPRE register is loaded into the Period Counter at DPWM startup or on a rising sync edge. This is used for applications requiring complex synchronization and phase shifting between DPWMs. See 2.16.1 Period Counter Preset Enable, page 39 for more information.

2.26 Blanking Registers

There are 4 Blanking Registers in each DPWM:

DPWMBLKABEG
DPWMBLKBBEG
DPWMBLKAEND
DPWMBLKBEND

There are two blanking periods, A and B, which both have a beginning and an end, measured in 4 nanosecond steps of the period counter.

These registers are used to blank out CBC signals during noisy times of the signal, for example around hard switching. See the Fault Mux section for more information. They can also be used to align current limit response times between multiple DPWMs with different dead times.

The Blank B values are also used to generate the DPWMC signal for the IntraMux for complex topologies. See Section 2.15.2, Intra Mux on page 33.

2.27 DPWM Adaptive Sample Register

The DPWMADAPTIVE register is used in adaptive sample trigger modes. See Section 2.17.6 Sample Trigger 1 Mode on page 43 for more information.

2.28 DPWM Fault Status Register

The DPWMFLTSTAT Register has bits which indicate faults, IDE detection, and Burst mode detection.

See the Fault section for Faults, the IDE section for IDE, and the Light Load mode section for Burst mode.

2.29 DPWM Auto Switch Registers

For an overview of what these registers do, see Section 2.10, Automatic Mode Switching on page 27. There are 4 Auto Switch threshold registers:

DPWMAUTOSWIHIUPTHRESH
DPWMAUTOSWIHILOWTHRESH
DPWMAUTOSWILOUPTHRESH
DPWMAUTOSWILOLOWTHRESH

These registers are used in topologies which dynamically switch from one DPWM mode to another, such as Phase Shifted Full Bridge and LLC. They control which one of three registers sets many of the DPWM control bits. There are 4 registers so that each of the 2 dividing lines can have hysteresis.

The three registers are:

DPWMCTRL0
AUTOCONFIGMID
AUTOCONFIGMAX

If the Filter input to the DPWM goes above DLWMAUTOSWIHIUPTHRESH, then the AUTOCONFIGMAX register is used until the Filter input goes below the DPWMAUTOSWIHILOWTHRESH register value.

Below this value the AUTOCINFIGMID control bits are used, until the Filter value goes below DPWMAUTOSWILOLOWTHRESH. Below this value, DPWMCTRL0 is used.

Mode switching is enabled by setting the AUTO_MODE_SEL bit in DPWMCTRL1. Making the waveforms transition smoothly across the mode switching boundary can be complex.

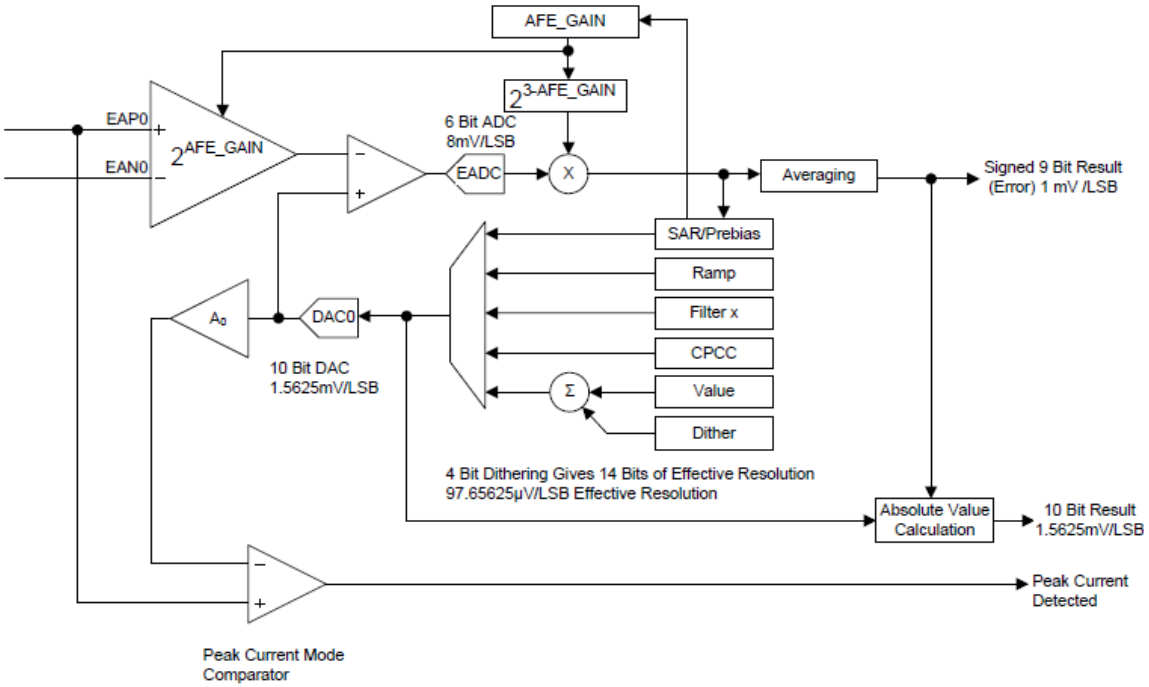
2.30 DPWM Edge PWM Generation Register

DPWMEDGEGEN is used for complex systems like phase shifted full bridge, in conjunction with the IntraMux. It enables each edge to be generated from a wide selection of sources in a very flexible manner. The options are described in Section 2.11 DPWMC, Edge Generation, IntraMux, page 28.
The DPWM Reference section shows the specific bit assignments.

High Resolution should also be disabled if the Edge Generator is enabled.

3 Front End

There are 3 Front-End modules available in UCD3138 (Front End 0,1,2). Here is a simplified block diagram of the Front End showing an accurate representation of the block's overall functionality:



Simplified Block Diagram of Front End in UCD3138 (Front End 2 recommended for Peak Current Mode Control)

The input to the Front End is a differential signal on 2 input pins (EANx, EAPx, x=0, 1, 2) of the UCD3138 device. A differential amplifier resolves this to a single ended signal, representing the difference between the two pins. Typically this signal represents voltage or current in the power supply, or some other value to be regulated via a feedback loop and/or measured.

This signal is fed into another differential amplifier. The other input to this differential amplifier comes from a Digital to Analog Converter (DAC) which has an effective range of 0 to 1.6 volts. This DAC output typically represents a target for a regulated value (reference).

There is a gain programmable differential amplifier which outputs the difference between the DAC output and the Front End input. This analog signal typically represents the error between the regulated value and the target value. This signal is turned into a digital value by the Error Analog to Digital Converter (EADC). This digital value is typically fed to the input of one or more filters, although it can be used in other ways.

Other blocks in the UCD3138 Front End aid implementing typical power supply functions. The Successive Approximation Control turns the Front end from a high speed, limited range error ADC to a 1.6 volt range, slower, successive approximation ADC.

The Ramp Control ramps the EADC DAC value up or down at a programmable rate for simple soft start and soft stop functionality. The Ramp engine can also be used for other ramps as well.

The Pre-Bias Control adds pre-bias handling support.

There is also a single ended comparator connected between EAP pin and the DAC which is used for Peak Current Mode control, such as in Phase Shift Full Bridge topology. Front End 2 is recommended for Peak Current mode control.

All of these are described in more detail in later sections of this chapter.

3.1 Error ADC and Front End Gain

The Error ADC (EADC) is a high speed 6 bit ADC converter.

3.1.1 Front End Gain

The Front End gain (the gain before the EADC) can be adjusted to 1X, 2X, 4X, and 8X. This gives an EADC resolution of 8mV, 4mV, 2mV, and 1mV respectively.

To set a fixed front end gain, the gain value is written to the AFE_GAIN bits in the EADC Control register.

FeCtrl0Regs.EADCCTRL.bit.AFE_GAIN = 2; //set AFE gain to 4X

In addition, there are 2 automatic gain setting modes, available only on Front End 0. They are enabled by setting the AUTO_GAIN_SHIFT_ENABLE bit in the EADC control register.

FeCtrl0Regs.EADCCTRL.bit.AUTO_GAIN_SHIFT_EN = 1; //enable auto gain shift mode.

In the simpler mode, the gain is shifted to the next lower mode whenever the EADC over or underflows. The gain is increased if the EADC output is less that +-1/4 of its range at the current gain.

By setting the AUTO_GAIN_SHIFT_MODE bit in the EADCCTRL register, the second auto gain mode can be enabled. In this mode, the shift points are set by the Filter nonlinear mode thresholds. These thresholds are described in section 4.3.6 Nonlinear Mode on page 68. There are 4 Filters with non linear thresholds. The FECTRLxMUX register in the Loop Mux section selects which set of nonlinear thresholds are used with each Front End.

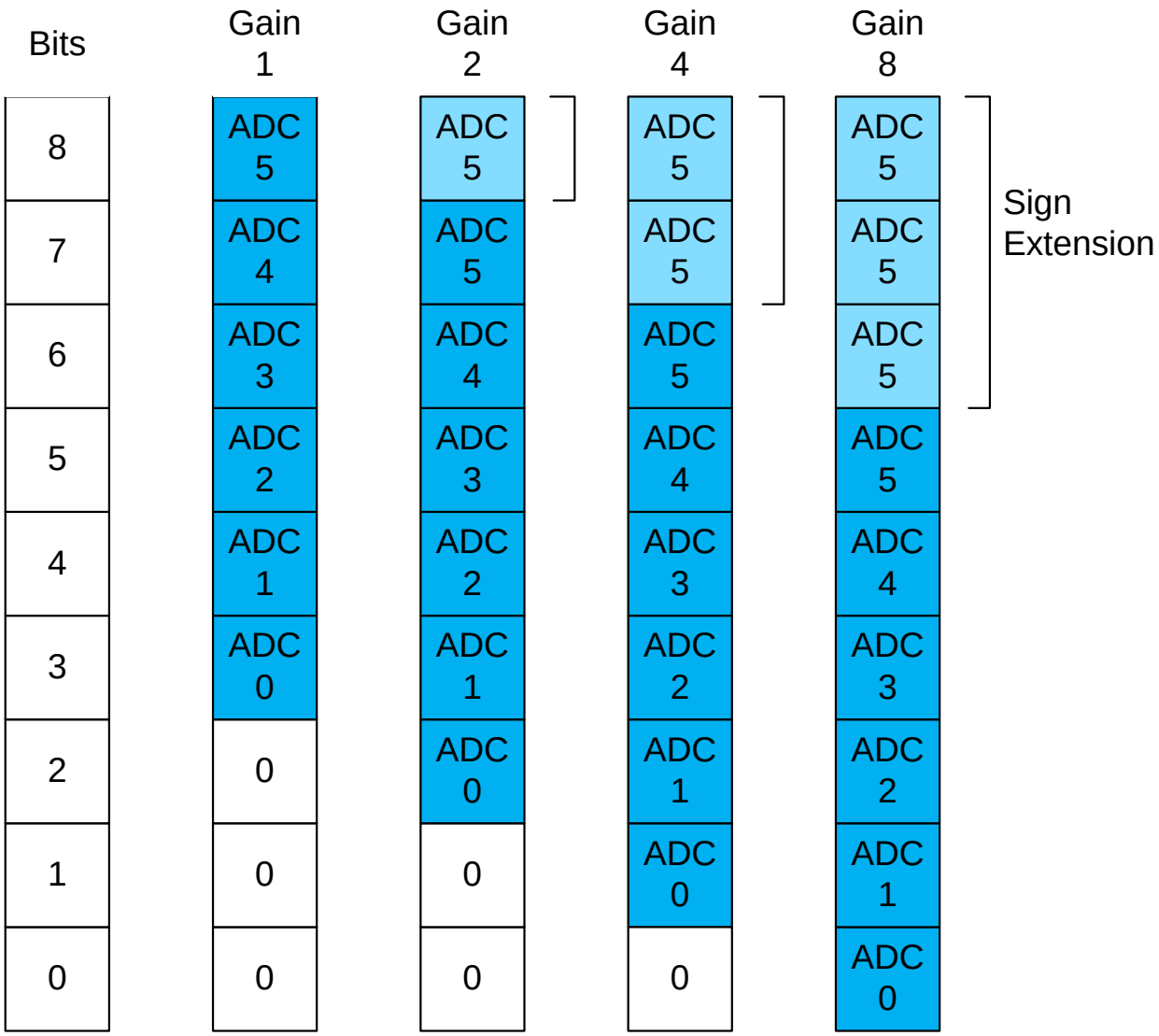
3.1.2 EADC Error Output

The internal EADC output is a 6 bit two's complement number. Depending on AFE gain, the least significant EADC bit can have a value of 1 to 8 mV. To simplify automatic AFE gain changes, this EADC output is shifted depending on the AFE gain, giving a 9 bit output to the filter.

This way, regardless of the AFE gain, the least significant bit will always have a resolution of 1mV. Depending on AFE gain, the bits and range of the output actually used will change:

Analog Gain	AFE_GAIN bits	Input Range (mV)	Bits used	Left Shift	Measurement Resolution (mV)
1	0	+248 to -256	3 - 8	3	8
2	1	+124 to -128	2 – 7	2	4
4	2	+62 to -64	1 – 6	1	2
8	3	+31 to -32	0 – 5	0	1

Here is a graphical representation of the EADC output:



The EADC error output as described above can be read from the EADC raw value register:

eadc_error = FeCtrl0Regs.EADCRAWVALUE.bit.RAW_ERROR_VALUE;

It is also sent to the Filter, and is one of the values which can be used by the digital comparators controlled by the Fault Mux.

3.1.3 EADC Triggering, EADC Output to Filter

The EADC is generally triggered by a sample trigger signal from a DPWM module. After this trigger, if averaging is enabled, additional triggers may come from the averaging module. The EADC can also be triggered by the Successive Approximation (SAR) module. Multiple DPWMS can be used to trigger a single EADC at different times in the same period.

Each DPWM module has 2 sample trigger registers to set sample trigger timing. The DPWMs can also provide oversampling of 2, 4, or 8 samples in coordination with 1 of the 2 sample triggers. See the Section 2.17.5 Sample Trigger 1 Oversampling, page 43 for more information.

The Sample Trigger Control register in the Loop Mux module controls the routing of sample trigger signals from the DPWMs to the EADCs. There is a bit in that register for every possible DPWM/Front End combination. If that bit is set, then the sample trigger from that specific DPWM will be routed to that specific front end. For example, to use DPWM3 to trigger Front End 2, this is the code:

```
LoopMuxRegs.SAMPTRIGCTRL.bit.FE2_TRIG_DPWM3_EN = 1;
```

See the Loop Mux Reference section of this document for more information.

If the EADC is driving a filter, that filter will compute its output at the conclusion of the EADC conversion. The Filter Mux register in the Loop Mux selects which front ends send data to which filters. For instance to send the output from Front End 2 to Filter 1:

```
LoopMuxRegs.FILTERMUX.bit.FILTER1_FE_SEL = 2; //use Front end 2 for filter 1.
```

See the Loop Mux Reference section for more information.

Sample triggers can also be divided so that the EADC only fires every 1 to 16 sample triggers:

```
FeCtrl0Regs.EADCCTRL.bit.SAMP_TRIG_SCALE = 4; //trigger every 5 sample triggers.
```

3.1.4 EADC Timing

The EADC takes either 16 or 32 cycles of the 250 MHz high speed clock to complete an analog to digital conversion. The timing logic runs continuously, producing samples every 64 or 128 ns. This gives maximum sample rates of 16 MHz and 8 MHz respectively. The sample trigger, when it occurs, takes the latest sample. It does not trigger the start of a conversion.

To set the EADC speed, use the Switched Cap Front End (SCFE) Divide by 2 (SCFE_DIV_2) bit in the EADC Control register:

```
FeCtrl0Regs.EADCCTRL.bit.SCFE_CLK_DIV_2 = 0; //clear for 16X clock divide.
```

By default the EADC switched cap filter runs continuously at a fixed rate. If the period is not an integer multiple of this rate, the sample time could shift around within a 64 nanosecond window.

To avoid this, set the Frame Sync Enable bit:

```
FeCtrl0Regs.EADCCTRL.bit.FRAME_SYNC_EN = 1;
      //resync EADC sampling to frame boundary at start of each frame.
```

The frame start signal comes from 1 or more DPWMs. DPWM selection is done in the Front End Control Mux Registers in the Loop Mux. Each Front end has a Front End Control Mux register which controls many inputs to the Front End, including the frame sync for the EADC sampling reset.

For example, to use DPWM3 frame sync for Front End 2:

```
LoopMuxRegs.FECTRL2MUX.bit.DPWM3_FRAME_SYNC_EN = 1;
```

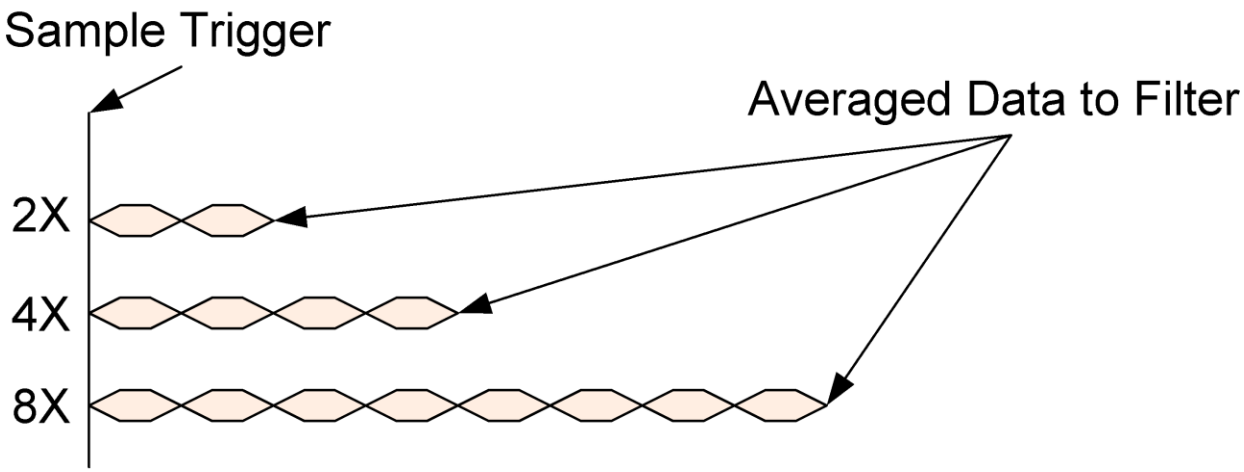
There is a bit which initializes the state machine counter for the front end to a non-zero value. This should be left at 0, however. Other numbers will cause unexpected results.

```
FeCtrl0Regs.EADCCTRL.bit.SCFE_CNT_INIT = 0; //leave at 0.
```

3.1.5 EADC Averaging

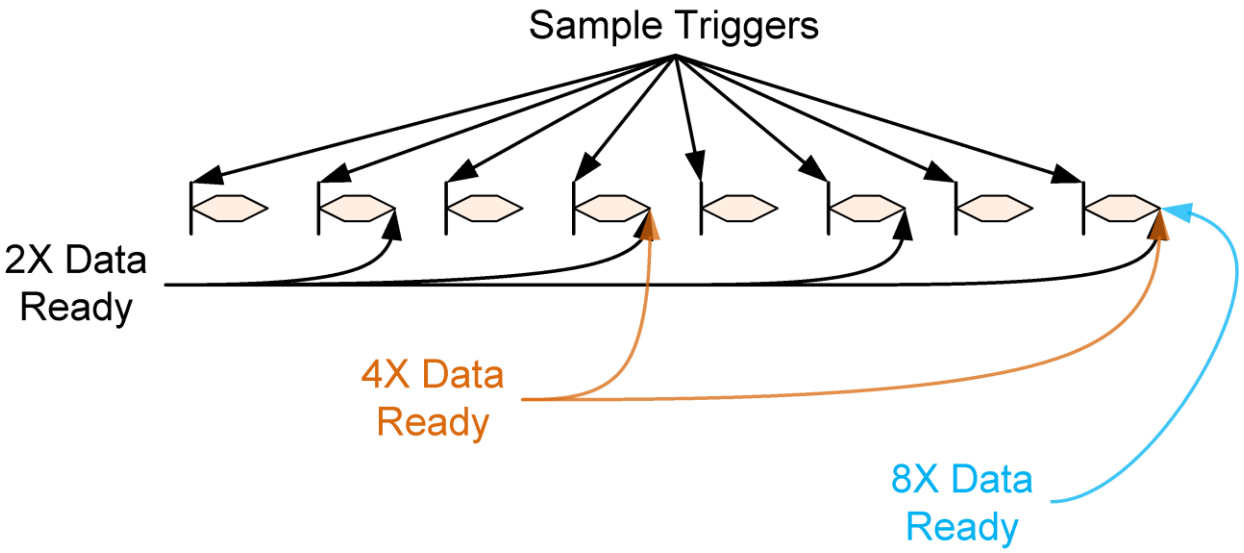
It is possible to average 2, 4, and 8 EADC samples. There are two modes of EADC Averaging – consecutive and spatial. It is true averaging – the samples are added and then divided by the number of samples. There is also a weighted average available.

Consecutive mode takes the specified number of samples immediately after the sample trigger, at the EADC sample rate of 16 or 8 MHz. It then triggers the Filter and provides the average of the samples as the filter input.



Consecutive Mode of Averaging by EADC

Spatial mode takes one sample for each sample trigger, and sends averaged data to the filter after the specified number of sample triggers.



Spatial Mode of Averaging by EADC

The average error value can also be read from the EADC Value register:

eadc_error = FeCtrl0Regs.EADCVALUE.bit.ERROR_VALUE;

This value will reflect the averaging value if averaging is enabled. Otherwise it will be the same as the raw EADC value mentioned earlier.

Averaging is controlled with the EADC control register. To select Averaging mode, write a 1 into the EADC_MODE bits:

FeCtrl0Regs.EADCCTRL.bit.EADC_MODE = 1; //averaging mode

There are 3 bits, giving a total of 8 modes, all of which will be discussed later in this section.

The simplest mode is mode 0 – 1 sample, no averaging.

To select spatial mode, write a 1 to the AVG_SPATIAL_EN bit:

FeCtrl0Regs.EADCCTRL.bit.AVG_SPATIAL_EN = 1; //spatial averaging mode

A 0 in this bit will select continuous mode.

To select which number of samples to average, use the AVG_MODE_SEL bits. They work as follows:

0 = 2x Averaging (Default)
1 = 4x Averaging
2 = 8x Averaging

FeCtrl0Regs.EADCCTRL.bit.AVG_MODE_SEL = 2; //select 8X averaging

There is also a weighted average control bit available, which gives more weight to the most recent samples. See the Front End reference section in this document for details.

3.1.6 Enabling the EADC and Front End.

There are several bits which must all be set to enable the EADC and the entire front end. Most of them are enabled by default. To save power and reduce noise, the default bits can be cleared if the EADC is not being used.

The enable bits for EADC 0 are:

FeCtrl0Regs.EADCCTRL.bit.EADC_ENA = 1; //1 is default
FeCtrl0Regs.EADCCTRL.bit.SCFE_ENA = 1; //1 is default

Some modules in the Front End can be used without enabling the EADC.

There is also a bit in the Loop Mux which must be set for the Front End 0 to start.

LoopMuxRegs.GLBEN.bit.FE_CTRL0_EN = 1; //0 is default

The GLBEN register is a special register, with enables for all front ends and all DPWMs in the same register. It is designed to allow simultaneous start up of all front ends and DPWMs, by writing to the whole register at once. This is very useful for complex topologies where all FET control waveforms need to start up simultaneously to prevent malfunction.

```
union GLBEN_REG glben_temp; //make a temp variable to accumulate
                            desired configuration

glben_temp.bit.FE_CTRL0_EN = 1;
glben_temp.bit.FE_CTRL2_EN = 1;
glben_temp.bit.DPWM0_EN = 1;
```

```
glben_temp.bit.DPWM1_EN = 1;

LoopMuxRegs.GLBEN = glben_temp; //enable FE0, FE2, DPWM0, DPWM1
```

The code above makes a temporary variable called glben_temp, initializes it, and then writes it all to the GLBEN register at once. It is also possible to do this:

```
LoopMuxRegs.GLBEN.all = 0x53; //enable FE0, FE2, DPWM0, DPWM1
```

This is a bit more efficient, but not nearly as readable. The best way would be:

```
#define FE_CTRL0_EN_BIT 0x100
#define FE_CTRL2_EN_BIT 0x400
#define DPWM0_EN_BIT    1
#define DPWM1_EN_BIT    2

LoopMuxRegs.GLBEN.all = FECTRL0_EN_BIT + FE+CTRL2_EN_BIT + DPWM0_EN_BIT +
      DPWM1_EN_BIT;
```

Of course, writing to each bit of the register directly would not accomplish a simultaneous start up. This could cause a power supply malfunction. For both DPWM and Front End, both local bits and global bits must be set to enable these peripherals. For a simultaneous startup, it is necessary to set the local bits before writing to the global register.

3.2 Front End DAC

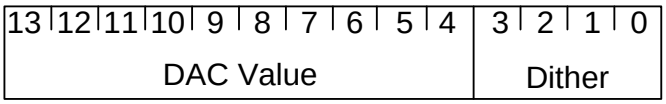
The reference voltage for the Front End is set by the DAC, sometimes called the EADC DAC. This is a 10 bit analog to digital converter, with a nominal step size of 1.5625 millivolts per bit. The DAC input is a unsigned 10 bit number, giving a range from 0 to 1.6 Volts.

In the simplest configuration, the DAC is set by writing to the EADCDAC register:

```
FeCtrl0Regs.EADCDAC.bit.DAC_VALUE = 100 * 16;//set 10 bit DAC to 100 (.15625 Volts)
```

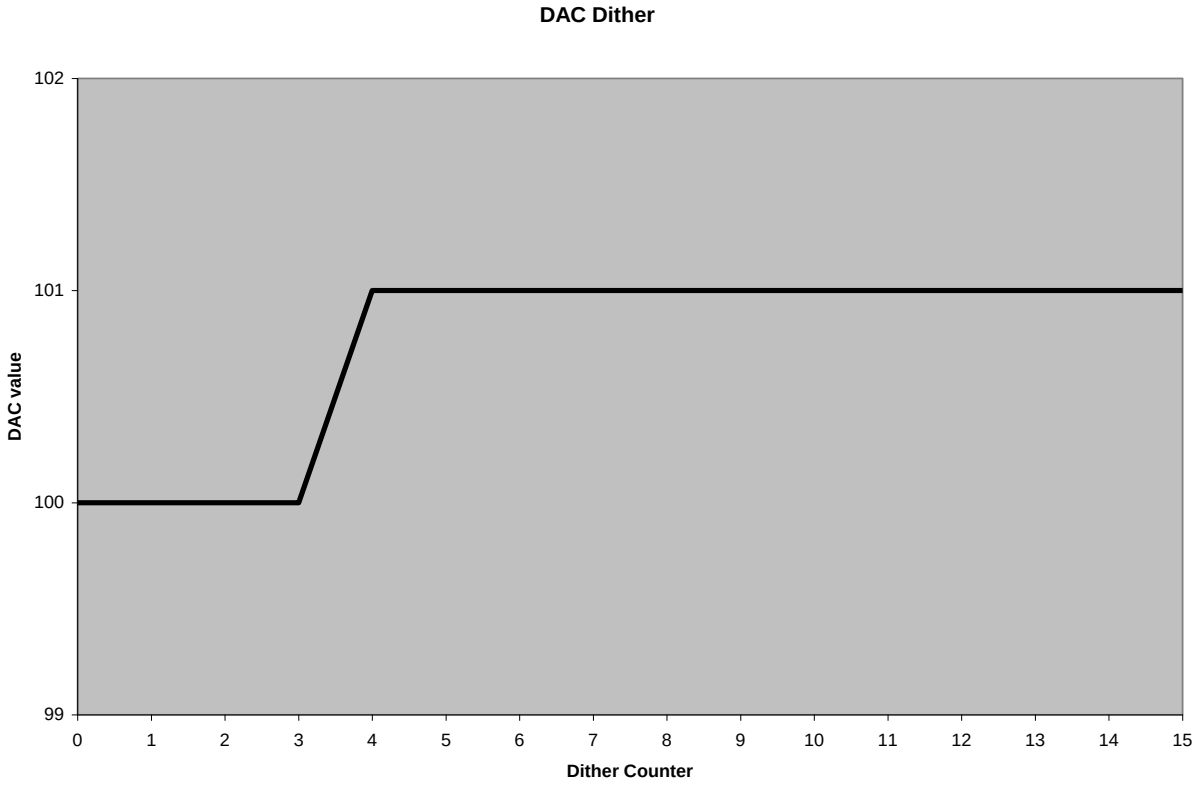
The 16X multiply is necessary because the DAC logic also supports a 4 bit dither capability.

The DAC_VALUE bit has 14 total bits - 10 actual DAC bits, and 4 bits that are used for dither:



This dither has a 4 bit counter driven by a selected DWPM signal, which will switch back and forth between 2 DAC values. For example, if the DAC value is set to 100.75 *16, there will be a 1100 in the 10 DAC bits, and a 4 in the dither bits.

The dither logic will put out a 100 for 4 counts and 101 for 12 counts. This will give an average of 100.75. Here is the waveform:



The dither counter will increment at the start of a pulse on DPWMA and/or DPWMB. The specific DPWM pins used are selected in the FECTRLxMUX registers in the Loop Mux.

For example, to set the rising edge of DPWM3B to trigger DAC dither on Front End 2:

```
LoopMuxRegs.FECTRL2MUX.bit.DPWM3_B_TRIG_EN = 1;
    //set DPWM3B up to trigger dither.
```

Note that if the DPWM pin is not active, because of anything from a zero filter output to a fault, the dither counter will not be incremented.

To enable dither, the DAC_DITHER_EN bit must be set:

```
FeCtrl0Regs.EADCDAC.bit.DAC_VALUE = (int)(100.25 * 16);
    //set 10 bit DAC to 100.25 (0.156640625 Volts)

FeCtrl0Regs.EADCDAC.bit.DAC_DITHER_EN = 1;//enable dither
```

The DAC can also be controlled by other DACs, by the output of filters, or by the constant power module.

The External DAC Control register in the Loop Mux can be used to select which DAC source is used.

There are several options:

0 = DAC 0 Setpoint Selected
1 = DAC 1 Setpoint Selected
2 = DAC 2 Setpoint Selected
3 = Output of Constant Power Module Selected

4 = Filter 0 Output Selected
5 = Filter 1 Output Selected
6 = Filter 2 Output Selected

LoopMuxRegs.EXTDACCTRL.bit.DAC0_SEL = 5; //control DAC 0 with Filter 1

To enable external DAC Control, it is also necessary to set the enable bit for the specific DAC:

LoopMuxRegs.EXTDACCTRL.bit.EXT_DAC0_EN = 1; //enable external DAC for DAC 0

Filter output is used to control the DAC when two filters are used together, typically in average current mode control, where the voltage error goes to a voltage loop filter, and the output of the voltage loop filter controls the DAC for a current loop filter.

The actual value being used for the DAC at any given time can be read from the DAC Status register – DACSTAT.

dac_value = FeCtrl0Regs.DACSTAT.bit.DAC_VALUE;

3.3 Ramp Module

The Ramp Module is used to control the EADCDAC for ramp up and ramp down of current and voltage. It is also used to ramp up and down the pulse width of Synchronous Rectifier FET pulses to avoid glitches when enabling and disabling synchronous rectification. Portions of the Ramp Module are also used for Prebias handling. The Ramp module is also used for the ramp compensation in peak current mode. The Ramp module can be used for only one purpose at a time. There are three Ramp modules, one for each front end, so it is possible to have 3 ramp functions running simultaneously

3.3.1 DAC Ramp Overview

The Front End Control Module in UCD3138 provides the capability to generate an automated ramp of the DAC set point through hardware. Firmware has the capability to configure the following parameters of the ramp:

1. Configurable DAC end value at completion of soft-start or soft-stop ramp
2. Configurable DAC step (8.10 format with 10 fractional bits)
3. Firmware can program number of switching cycles per DAC step (Configurable from 1-128)
4. Configurable number of delay cycles prior to start of ramp (Configurable from 0-65535)
5. Ramp can be initiated by one of the following events: firmware start bit, PMBus Control pin, Ramp Delay Completion pulse from another Front End Control Module or Ramp Completion pulse from another Front End Control Module
6. Firmware can configure the DAC Saturation Step Size (if EADC is in saturation at time of DAC update, hardware will increment/decrement DAC Value by DAC Saturation Step Size).

3.3.2 DAC Ramp Start and End points

The DAC Ramp start point is taken from the EADC DAC Value Register:

FeCtrl0Regs.EADCDAC.bit.DAC_VALUE = 0; //start ramp at 0

The DAC Ramp end point is taken from the Ramp DAC Ending Value register

FeCtrl0Regs.RAMPDACEND.bit.RAMP_DAC_VALUE = 100 * 16;

//set 10 bit DAC to 100 (.15625 Volts)

These two values above will lead to a ramp down. Both of these registers are 14 bits, so a dithering value is supported at the beginning and end of the ramp.

The DAC will stay at the end value until something else is asked for. Before another ramp is done, though, this end value should be written to the DAC_VALUE register so that the ramp will start from the same place.

3.3.3 DAC Ramp steps

The DAC Ramp steps are controlled by two bit fields, the Switch Cycles per Step field and the DAC Step register.

The Switch Cycles per Step bits determine how many DPWM inputs are required before 1 step occurs. It has 7 bits, so the register can hold values from 0 to 127, corresponding to 1 to 128 cycles.

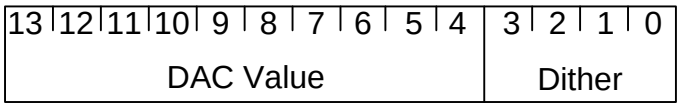
The Switch Cycle signal is a DPWM output. The DPWM output used for the Ramp module is the same as the one for dither above:

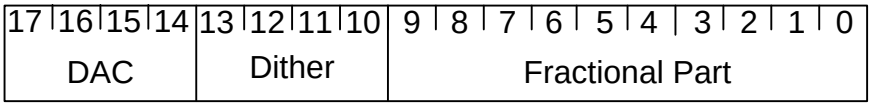
LoopMuxRegs.FECTRL2MUX.bit.DPWM3_B_TRIG_EN = 1;
//set DPWM3B up to trigger dither and ramp modules.

The step size is an unsigned value. The Ramp module logic checks the start and end values. If the start value is lower than the end value, the step size is added to the DAC value. If the start value is higher than the end value, the step size is subtracted from the DAC value.

The step size has a 10 bit fractional part, allowing very precise and also very slow ramps. There are 10 fractional bits, below the dither portion of the DAC. There are 8 bits matching the DAC value, including dither.

DAC_VALUE





DAC_STEP

There is a register, not visible to the programmer, which retains the sum of the fractional bits between steps.

For instance, suppose that bit 8 was the only bit set in the DAC Step register:

FeCtrl0Regs.DACSTEP.bit.DAC_STEP = 0x100; //set bit 8 in DAC_STEP

Every step, 0x100 would be added to the step register. The sequence would look like this:

Hidden step register	DAC register
0x000100	0x0000
0x000200	0x0000
0x000300	0x0000
0x000400	0x0001
0x000500	0x0001
0x000600	0x0001
0x000700	0x0001
0x000800	0x0002
0x000900	0x0002
0x000A00	0x0002

3.3.4 DAC Ramp Start, interrupts, Start Delay

DAC Ramp start is controlled by bits in the Ramp Control Register (RAMPCTRL) The DAC Ramp can be started by several events, listed above. These are all clearly described in the Front End Reference section of this document. The same register also contains a setting for pre-ramp delay, and bits which control interrupts for ramp events.

To enable the Ramp, it is also necessary to set the RAMP_EN bit in the RAMPCTRL register.

3.3.5 RAMPSTAT Register

The RAMPSTAT register has bits which indicate ramp completion and other ramp status events. The RAMPCTRL register can also be used to enable interrupts for ramp status events.

3.3.6 DAC RAMP when EADC is saturated

DACSATSTEP configures the DAC increment/decrement value when the EADC is saturated during the Automated Ramp.

If the EADC is saturated high (Verror = Vref – Vsense), the DAC setpoint is lowered by the DACSATSTEP value. The decrement will continue until the EADC is out of saturation. This decrement when the EADC is in saturation occurs periodically when the DAC would be updated with a new DAC value during the ramp.

If the EADC is saturated low, the DAC setpoint is incremented by the DACSATSTEP value. The increment will continue until the EADC is out of saturation. This increment when the EADC is in saturation occurs periodically when the DAC would be updated with a new DAC value during the ramp.

If the step value is carefully chosen, this mode may help to keep the EADC from saturating during a ramp up. It may, however, make the ramp timing undeterministic and non-monotonic.

3.3.7 Using Ramp Module for Peak Current Mode

The ramp module is also used for Analog Peak Current Mode (APCM). Normally the PCM_START_SEL bit is set so that a filter output is used to drive the starting point of the ramp. The ramp end point is set to a low value so that the ramp will always go downward.

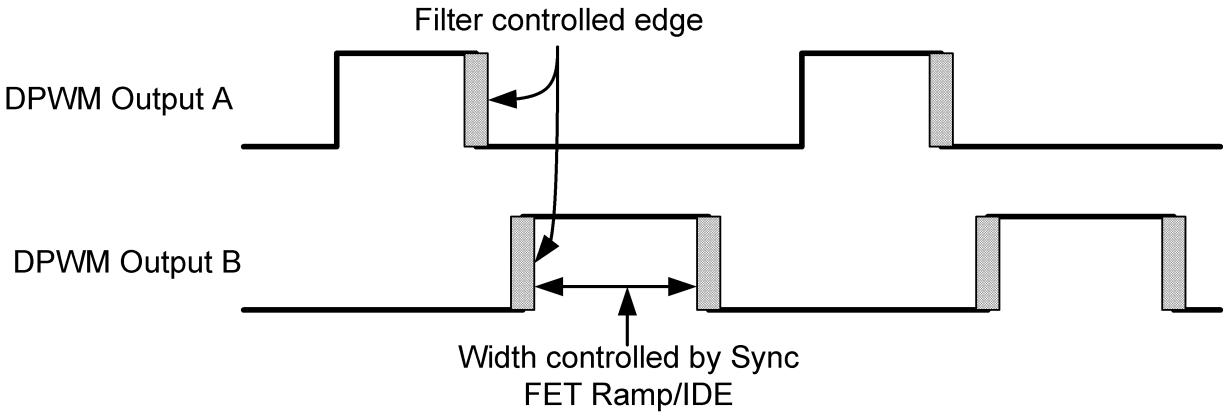
In this mode, the ramp trigger simply starts the ramp. The step comes from the Front End at a 32 nanosecond rate. There is a comparator in the Front End. This comparator compares the ramp value (in the DAC) to the EADC input value. When the EADC input exceeds the ramp value, the APCM fault output of the Front End goes active. This bit can be sent to the DPWM pins via the Loop Mux and Fault Mux.

The Front End drawing omits it for simplicity, but the DAC (and the input to the EADC amplifier) are actually differential. The PCM comparator, however, is single ended. So there is a differential to single ended converter between the DAC and the PCM comparator. This comparator must be enabled for PCM to work. The D2S_COMP_EN bit in the EADCCTRL register performs this function.

For additional information consult the reference firmware provided with UCD3138PSFBEVM-029 EVM and TI application note on Phase Shift Full Bridge (Peak Current mode control) implementation.

3.3.8 Sync FET Soft On/Off using Ramp Module

The Sync FET soft on/off can be used to control the on-time of DPWMB in normal mode. DPWMB can be ramped up and down. It can be used in conjunction with digital or analog IDE (Ideal Diode Emulation). These two modules control the width of DPWMB as shown below:



Ideal Diode Emulation (IDE) Module in UCD3138

The Sync FET Ramp is similar to the DAC Ramp, and uses the same hardware, but it needs a starting point, which is provided by the SYNC_FET_RAMP_START bits in the RAMPCTRL register. These bits are scaled at 1 high speed clock cycle per bit (nominally 4 nanoseconds). The RAMPDACEND.RAMP_DAC_VALUE register is used for the end of the Sync FET Ramp as well, with the same scaling as the start register.

The fractional position of the step size register is the same, which means that bit 10 in the step size register represents a 4 nanosecond step.

All the same start criteria can be used for the Sync FET Ramp. The difference is that the SYNC_FET_EN bit is set in the RAMPCTRL register, instead of the RAMP_EN bit.

The Sync FET ramp only works in normal mode. It cannot be used with Cycle By Cycle (CBC) current limit, or with any form of Peak Current mode. For Sync FET Ramp to work correctly, the rising edge of DPWMB must be controlled by the filter. The falling edge of DPWMB is calculated by the DPWM logic during the update window.

Any DPWM can be driven by any ramp generator, see the DPWM documentation for ramp selection as well.

The Ramp Module is also used in the DAC Ramp and in Prebias, so only one of these functions can be done by each Ramp Module at a time.

Note: Even if the Ramp Module is being used for Sync FET soft on/off, it is not possible to write to the EADCDAC for that front end while the Ramp Module is being used.

3.4 Successive Approximation Mode

The EADC and DAC together can be put into Successive Approximation Mode. The SA module takes control of the DAC and the EADC. It starts at a low gain, and attempts to measure the input voltage on the EADC precisely over the full range. It does this in a manner similar to a successive approximation ADC. Note that multiple samples are taken. If the input signal is changing rapidly, the SA module may not converge.

3.4.1 SAR Control Parameters

Firmware has the capability to program the following parameters used in the SAR Control algorithm:

- **Starting SAR Resolution** - Controls the AFE Gain used at the start of the SAR process

- **Final SAR Resolution** - Controls the final AFE Gain setting used at the completion of the SAR process
- **SAR Window 1 Range** - If error falls in the range of +/- **SAR Window 1 Range**, the AFE Gain is incremented to 0x1 as long as Final SAR Resolution does not equal 0x0.
- **SAR Window 2 Range** – If error falls in the range of +/- **SAR Window 2 Range**, the AFE Gain is incremented to 0x2 as long as Final SAR Resolution does not equal 0x1
- **SAR Range** – If error falls in the range of +/- **SAR Range**, the AFE Gain is incremented to 0x3 as long as the Final SAR Resolution does not equal 0x2
- **SAR Mode** – SAR algorithm configured in Non-Continuous Mode or Continuous Mode

3.4.2 SAR Algorithm Overview

Upon initiation of the SAR process, the SAR Control Module sets the AFE gain to the Starting SAR Resolution as programmed by firmware. Initially, the MSB of the 10-bit DAC value is set to '1' or the DAC setpoint is placed at the midpoint of its range. An EADC sample is captured and compared. Based on the polarity and magnitude of the EADC error, the AFE gain and DAC setpoint are adjusted.

3.4.3 Non-Continuous SAR Mode

UCD3138 features two modes when it attempts to use a SAR algorithm to determine an absolute voltage. The first mode is Non-Continuous SAR mode. In this mode, the SAR Control Module restarts the SAR algorithm on each sample trigger from the DPWM module. Upon receipt of a sample trigger from the DPWM modules, a new EADC sample is requested at an AFE gain of 0x0 and the DAC setpoint is reset to midpoint (as described in Section 8.2.3).

The Non-Continuous SAR Mode minimizes power consumption by only running the Analog Front End when a new measurement is needed. The SAR Control Module reruns the entire SAR algorithm on every sample trigger, which may add latency to the acquisition of the absolute voltage value compared to continuous mode.

3.4.4 Continuous SAR Mode

Continuous SAR Mode configures the SAR Control Module to continually acquire new EADC samples from the Analog Front. Upon receipt of a new sample trigger from the DPWM modules, if the error is within the final SAR window, a new absolute voltage can be generated quickly since the algorithm does not need to reset the DAC setpoint to midpoint and lower the AFE Gain to 0x0.

The result of the SAR calculation can be read from the EADC value register. To check for EADC overflow, read the EADC_SAT_HIGH and EADC_SAT_LOW bits in the same register:

```
if((FeCtrl0Regs.EADCVALUE.bit.EADC_SAT_HIGH
        && FeCtrl0Regs.EADCVALUE.bit.EADC_SAT_LOW) == 0)
        {
                eadc_absolute = FeCtrl0Regs.EADCVALUE.bit.ABS_VALUE;
        }
        else
        {
                //adjust EADCDAC and try again
        }
```

3.5 Absolute Value Without SAR

It is also possible to get absolute value data from the EADC without using SAR mode. For accurate data in this case, the Error ADC has to be within range of the EADC DAC setting.

Vabs = Veadcdac + Veadc

If EADC averaging is used, the average EADC value will be used to calculate the absolute value.

3.6 EADC Modes

There are several other front end modes for different applications.

The complete list is as follows:

- 0 = Standard mode, EADC samples based on sample triggers from DPWM module (Default)
- 1 = Averaging Mode, configured by AVG_MODE_SEL
- 2 = Non-continuous SAR Mode
- 3 = Continuous SAR Mode
- 4 = Reserved
- 5 = Digital Peak Current Mode
- 6 = Constant Power/Constant Current Control Mode (CPCC module controls switching between Standard Mode and Non-Continuous SAR Mode)
- 7 = Constant Power/Constant Current Control 2 Mode (CPCC module controls switching between Standard mode and Continuous SAR Mode)

4 Filter

The UCD3138 filter is a PID filter with many enhancements for power supply control. Some of its features include:

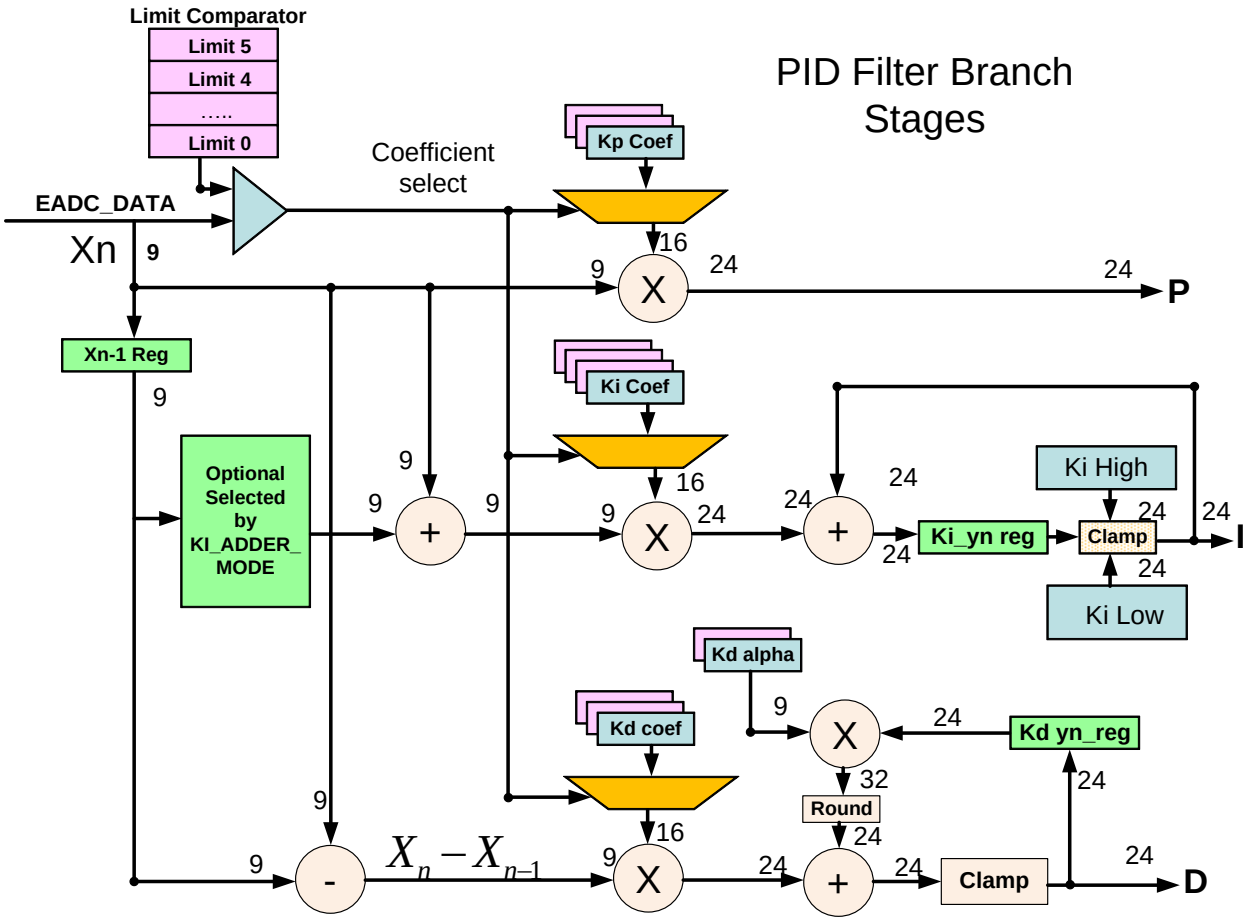
- PID Based Architecture
- Additional α coefficient and history in D branch
- Programmable Non-Linear Limits for automated modification of filter coefficients based on received EADC error
- Multiple coefficient sets fully configurable by firmware
- Full 24-bit precision throughout Filter calculations
- Programmable clamps on Integrator Branch and Filter Output
- Ability to load values into internal filter registers while system is running
- Ability to stall calculations on any of the individual filter branches
- Ability to clear and stall calculations on any of the individual filter branches
- Duty Cycle, Resonant Period, or phase shift generation based on filter output.
- Flux Balancing
- Voltage feed forward

4.1 Filter Math Details

The Filter uses binary arithmetic. In most cases the precision of the results is preserved at the highest level until the rounding/clamping at the output of the filter. The main exception to this is the extra pole, using Kalpha, which has to round to a decreased resolution immediately. The filter is relatively complex, so scaling is discussed in sections. After the filter math details are described, the registers which control the filter are documented.

4.1.1 Filter Input and Branch Calculations

Here is a block diagram of the first part of the filter, with bit width information:



All values shown in the filter are signed numbers, with the most significant bit going to the sign bit. All are treated as being normalized to 1.

The main input to the filter is a 9 bit signed value from an Error ADC. It is shown on the upper left as Xn. It goes to the input for filter calculations, and it also goes to a digital comparator. The Filter provides for nonlinear calculations, with up to 7 different coefficient sets selected by the Xn value. This can be used to change the compensation of the filter with different input error ranges. For a complete discussion of this feature, see Section 4.3.6 Nonlinear Mode, page 68.

4.1.2 Proportional Branch

The Xn value is used directly as an input to the Proportional (P) branch of the filter. It is multiplied by the 16 bit signed Kp coefficient, and the 24 bit result is used as the output of the P branch. When multiplying two signed numbers in binary arithmetic, an extra sign bit is generated. Because of this, 9 bits times 16 bits gives 24 meaningful bits, not 25.

No clamp is needed on the proportional branch. It is self-limiting, because it has no memory. It will never exceed 24 bits. If a lower maximum output is desired from the proportional branch, it can be achieved by reducing the value of Kp.

4.1.3 Integral Branch

There are two options for the use of Xn in the Integrator (I) input. The current Xn can be used by itself, or the current Xn can be added with the previous Xn-1. Doing the addition provides a trapezoidal approximation, which is sometimes considered theoretically superior to a single point. However, since the output of the adder is also 9 bits, if the Xn and Xn-1 values add up to more than 255 or less than -256, the output of the adder will be clamped at those values.

This will only occur at the lowest gain setting of the Error ADC. So if the lowest gain setting of the EADC is to be used, trapezoidal approximation may cause premature saturation on the input.

The Xn value, or the Xn + Xn-1 sum is multiplied times the Ki coefficient. Note that the trapezoidal mode will normally have double the output of the simple Xn value. This will change the overall gain of the I stage by a factor of two. This must be taken into account if the Xn addition mode is changed.

The output of this multiplication will always fit within 24 bits. This value is then added to the existing I value. The hardware will automatically clamp it at a 24 bit signed number, and there are high and low clamp registers available which can be used to clamp it to lower values. There are also status register bits that will be set if the input value exceeds the clamp.

The clamped value is fed to the next stage of the filter, and is also fed back to be added to the next Xn * Ki value when it is calculated.

4.1.4 Differential Branch

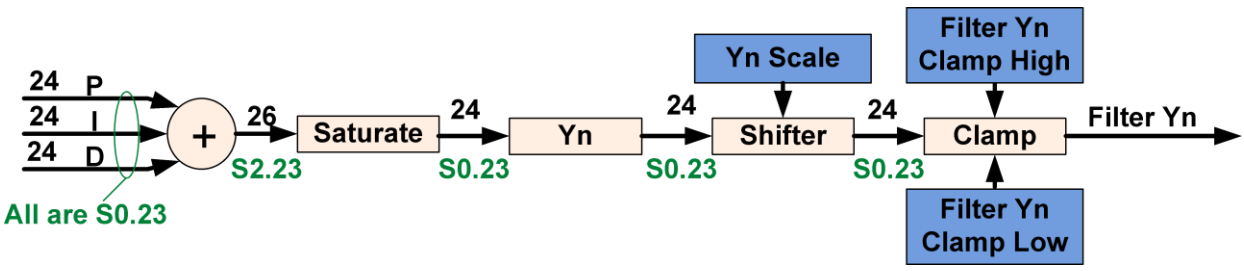
On the Differential (D) branch, Xn-1 is subtracted from Xn. The difference between the two most recent X values is then multiplied by Kd, giving a 24 bit signed number.

The D branch has an additional pole added after this multiplication, giving more control of the filter response to permit better matching to the power supply plant. This D alpha branch acts as an integrator on the output of the D stage. With each filter calculation, the 24 bit result of the previous D and D alpha calculation is multiplied by the 9 bit Kalpha (Kα). This gives a 32 bit signed result. To match the 24 bit data path, this must be rounded back down to 24 bits. This is the one rounding that actually takes place in the filter before the filter output.

There is also a simple clamp to prevent the K output from going outside a 24 bit signed number. Because of the integral element for the alpha stage, it is possible for it to exceed this range.

4.1.5 Add, Saturate, Scale and Clamp

Here is a diagram of the next section of the filter:



The S0.23 notation means a 24 bit number with 1 sign bits to the left of the binary point and 23 bits to the right of the point, meaning a range of $1-2^{-23}$ to -1. 2.23 means a number with 1 sign bit and 2 magnitude bits to the left of the binary point, and 23 magnitude bits to the right.

This section of the filter adds the P, I, and D outputs together, giving a potential 26 bit result. Saturation logic clamps this back down to 24 bits. If the value is above the maximum value for 24 bits, the output of the saturation logic will be set to the maximum (0x7ffff or 524287) Negative values out of range will be clamped to the most negative value.

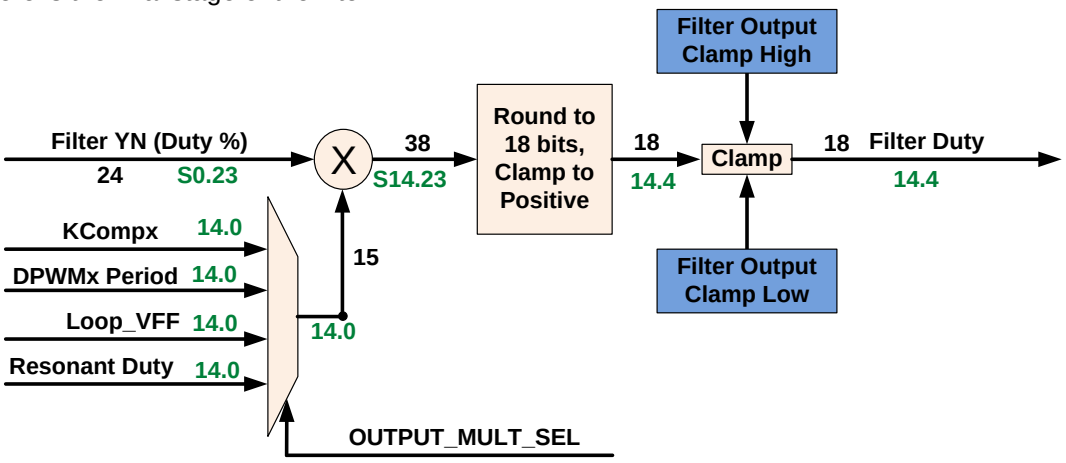
The output of the saturation section goes to a programmable shifter which can be programmed for 8 different shifts, including no shift at all. This can be used to compensate for the scaling of the filter coefficients.

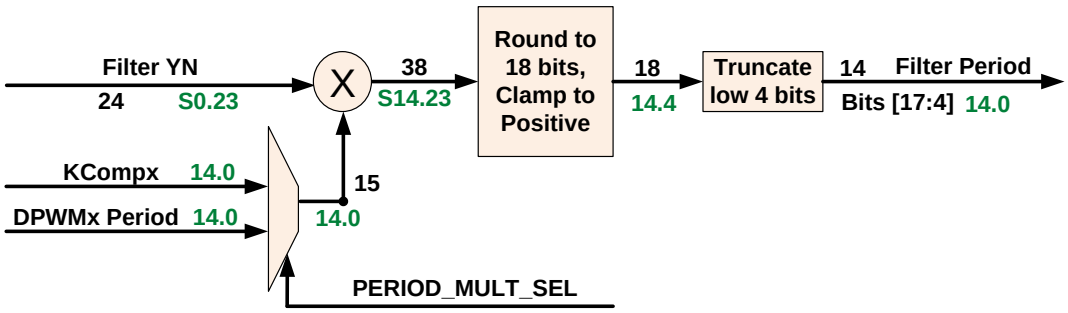
After the scaling, there is a clamp with independent clamp high and clamp low values which are set by writing to registers. This clamp also has status bits which are set when the clamp limits are exceeded.

Note however, that there is no saturation unit at this point. Bits over 24 are simply truncated and ignored. If the shifter is set to shift by 0, or to shift to the right, all input numbers will give the expected result. If a left shift is used, the programmer must make sure that the result will always fit within 24 bits, or results may be unexpected.

4.1.6 Filter Output Stage

Here is the final stage of the filter:





This stage converts the filter output to match the input requirements of the DPWM. Two different calculations are performed sequentially, using the same multiplier, but with different settings. One calculation provides a DPWM duty value, and the other provides a DPWM period value. In many topologies, only the duty value is used. In LLC, both values are used.

At the start of this stage, the PID output is multiplied by one of several 14 bit unsigned numbers, giving a 38 bit output. For the Filter Duty calculation, there are 4 numbers which can be used. See section 4.3.8 Output Multiplier Select on page 68 for a discussion of these numbers. For the Filter Period calculation, only 2 numbers can be selected.

After the multiplication, there is a 38 bit signed result. Negative values are clamped to zero and the sign bit is removed. This gives a 37 bit positive result. This number is rounded to the 18 most significant bits. This section is the same for both calculations.

After rounding and clamping, the two outputs are handled differently. The Filter Duty value is clamped using the values in the Filter Output Clamp High Register (FILTEROCLPHI) and the Filter Output Clamp Low Register (FILTEROCLPLO). After that, the Filter Duty value is used by the DPWM as a time value. It is considered a 14.4 bit value, with the low 4 bits going to the high resolution section of the DPWM. So the resolution of the Filter Duty value is 250 psec.

The Filter Period value gets no clamp. The DPWM Period does not support high resolution, so the low 4 bits from the 18 bit result are truncated. The Filter Period only presents the high 14 bits to the DPWM, giving a resolution of a nominal 4 nanoseconds.

Here is an example of a typical use of the Filter Output Stage:

Filter YN (50% Duty) 0x400000 or 4194304
X
DPWM Period (100 kHz) 0x9C4 or 2500
=
0x271000000 or 10485760000

Shift right by 19 bits and round:
0x4E20 or 20000
This result is what goes to the DPWM, with high resolution.

To convert it back to the period scale and check results, we can divide by 16, which is the same as shifting right by 4 bits. This gives:
0x4e2 or 1250,
which is half the period, so we do get a 50% duty cycle.

4.2 Filter Status Register

The Filter status register has 5 bits.

FILTER_BUSY
YN_LOW_CLAMP
YN_HIGH_CLAMP
KI_YN_LOW_CLAMP
KI_YN_HIGH_CLAMP

The FILTER_BUSY bit is high when the filter is calculating. This calculation time is very short, only a few instruction cycles. It is very difficult to reliably detect the high time of the Filter Busy bit.

The other bits are written to each time the filter calculation is complete. They reflect the result of the most recent filter calculation.

4.3 Filter Control Register

The Filter Control Register (FILTERCTRL) has 13 fields. They are used to configure the filter operation. Filter sources and destinations are set in the Loop Mux registers

KI_ADDER_MODE
PERIOD_MULT_SEL
OUTPUT_MULT_SEL
YN_SCALE
NL_MODE
KD_STALL
KI_STALL
KP_OFF
KD_OFF
KI_OFF
FORCE_START
USE_CPU_SAMPLE
FILTER_EN

4.3.1 Filter Enable

The Filter Enable (FILTER_EN) bit enables the filter. Unlike the DPWM and Front End, there are no filter enable bits in the GLBEN (Global Enable) Register in the Loop Mux registers. These bits are unnecessary for the filter because it only operates when it is triggered by the Front End or some other external event. The default for the Filter Enable bit is a 1, which enables the filter. If the filter is disabled after running for at least one cycle, the value sent to the DPWM will continue to control the DPWM. In addition, the last Filter Status state will also remain.

4.3.2 Use CPU Sample

The CPU Sample bit (USE_CPU_SAMPLE) is used for open loop testing of the Filter and DPWM configuration, or in other cases where a firmware input to the Filter is desired. If the USE_CPU_SAMPLE bit is set, the Filter input comes from the CPU_SAMPLE bit field in the CPU Xn register (CPUXN).

Here is an example of using CPU_SAMPLE:

```
Filter1Regs.FILTERCTRL.bit.USE_CPU_SAMPLE = 1; //enable CPU sample
Filter1Regs.CPUXN.bit.CPU_SAMPLE = -34; //put negative value into CPU sample
```

4.3.3 Force Start

The FORCE_START bit triggers a single filter calculation. It can be used with the CPU_SAMPLE value to run a controlled calculation in the filter. If CPU Sample is not enabled, it will use whatever input is selected for this filter.

4.3.4 Kp Off, Kd Off, Ki Off

The KP_OFF, KD_OFF, and KI_OFF bits disable these sections of the filter, and replace those values with a zero. They also clear any history to a zero where it is present (I and D).

4.3.5 Kd Stall, Ki Stall

The KD_STALL and KI_STALL registers stall these filter elements at their current value. They do not reset them. They are useful for suppressing response to transients when such response is not desirable.

4.3.6 Nonlinear Mode

The NL_MODE bit selects which nonlinear mode is used. 0 is for asymmetric mode, while 1 selects symmetric mode. Refer to sections 4.5 through 4.8 Mode section for more information.

4.3.7 Output Scaling

The 3 OUTPUT_SCALE bits permit shifting of the filter output. This gives flexibility in the scaling of the filter peripherals. It is a 2's complement number, where 0 means no shift, 1 means a shift right by 1, 2 means shift right by 2, -1 means shift left by 1, and so on.

Filter1Regs.FILTERCTRL.bit.OUTPUT_SCALE = -3; //shift filter output left by 3

4.3.8 Output Multiplier Select

The OUTPUT_MULT_SEL bits select what value is multiplied by the filter output to determine the DPWM pulse width. See the Filter Reference section for specific bit assignments. The options are:

1. KComp - This enables special scaling of the output to the DPWM independent of the period.
2. Switching Period – This results in the Filter output translating directly to a DPWM on-time percentage. Full scale on the filter output will equal a 100 % on time.
3. Feed Forward value – This permits the output of the filter to be controlled by the output of another filter. This could be, for example, a voltage feed-forward value
4. Resonant Duty value received from the DPWM module - This is used for resonant mode, for example for LLC architecture.

Note that the default is KComp. This is not intuitive, especially for users of the UCD3000 series digital power controller. They UCD3000 had no options in this area, period was always used. It is easy to overlook this bitfield when setting up for a simple period based system. The OUTPUT_MULT_SEL register works with the FILTERMUX register in the Loop Mux for value selections. FILTERMUX selects which KComp is used, which DPWM Period is used, and which Filter output is used for Feed Forward. Resonant Duty also comes from a DPWM module and is also selected by FILTERMUX. See 5.4 Filter Mux Register (FILTERMUX), page 78.

Switching Period is provided by the DPWM. The default is the value from the DPWM Period register, and this is used for most topologies. However, there are two other DPWM registers which can also be sent to the Filter for this value. See 2.17.3 Filter Duty Select, page 42, for more details.

4.3.9 Switching Period as Output multiplier

Using the Switching Period as an output multiplier leads to the DPWM duty being directly proportional to the Filter output, with a full range output being equal to about 100% of the period. Here is the bit pattern of the multiply:

The filter output is a 24 bit signed number, with a range from 0x7fffff (8388607) to 0x800000 (-8388608).

All of the output multipliers are unsigned 14 bit numbers with a range from 0x3fff (16383) to 0.

The product of these two numbers is a 38 bit number. This number is then scaled and rounded down to a 18 bit number and used for the high resolution events in the DPWM.

So suppose that the filter output is at about 50% or 4194304. If the period is the same as the example above, 2500, the product of the two will be 10485760000. To reduce this from a 38 bit signed number to a 18 bit unsigned number, we drop the sign bit off the top and divide by 2^{19}. Negative filter outputs make no sense in terms of DPWM timing, so they will be clamped to zero.

Dividing by 2^{19} gives a result of 20000. This is a high resolution value for the 4 GHz clock of the DPWM. To convert it to the lower resolution, 250 MHz clock used for the period, we need to divide by 16. This gives a result of 1250, or half the period. Other filter output values follow the exact same scaling.

There is a register in the Loop Mux, the FILTERMUX register, which selects the period source for each filter.

See the Loop Mux reference section for more information on this register. Here is an example of its use:

```
LoopMuxRegs.FILTERMUX.bit.FILTER0_PER_SEL = 2; //use DPWM2 period for filter 0
```

4.3.10 KComp as Output Multiplier

Using KComp as an output multiplier can be useful in places where the DPWM output is limited to less than 100%, for example. This can permit using the whole dynamic range of the Filter for a more limited range, and remove the need for output clamping. The scaling works exactly the same, except the 14 bit KCOMP value is used instead of the 14 bit period value.

This option also makes it possible to change the gain of the Filter dynamically without change pole and zero positions. It can also be used to increase the gain of the Filter beyond what the normal Filter structure supports. It is also used to match up the PWM and Resonant mode waveforms in the LLC configuration.

There are registers in the Loop Mux which contain KCOMP values and select which of 3 KCOMP values is used for each filter.

Here is an example of a code which would provide a maximum output of 50%:

```
#define SWITCHING_PERIOD 2500 // 250 MHz clock divided by period of 100 KHZ

    Dpwm0Regs.DPWMPRD.bit.PRD = SWITCHING_PERIOD;

    LoopMuxRegs.FILTERKCOMPA.bit.KCOMP0 = SWITCHING_PERIOD >> 1;
        //KCOMP = period/2

    LoopMuxRegs.FILTERMUX.bit.FILTER0_KCOMP_SEL = 0; //select KCOMP0 for filter 0

    Filter1Regs.FILTERCTRL.bit.OUTPUT_MULT_SEL = 0; //Multiply output by KCOMP
```

This approach yields 1 more bit of filter resolution than clamping the Filter output at 50%, which should reduce the size of any limit cycling.

4.3.11 Feed Forward as Output Multiplier

When the feed forward is selected as the output multiplier, the multiplier value is the most significant 14 bits of the filter output from a different filter. The FILTERMUX register in the Loop Mux is also used to select this filter. Configuring the link between the two filters is simple and is shown below. The actual filter settings and operation for feed forward are available in the Hard Switching Full Bridge EVM (UCD3138HSFBEVM-029) reference code from Texas Instruments.

Here is an example of link code:

```
LoopMuxRegs.FILTERMUX.bit.FILTER0_FFWD_SEL = 0; //select Filter 1 as ffwd input
Filter0Regs.FILTERCTRL.bit.OUTPUT_MULT_SEL = 2;
        //select feed forward as output multiplier
```

See the FILTERCTRL register in the reference section for more information on these bit fields.

4.3.12 Period Multiplier Select

The Filter has a second output. In addition to Filter Duty, there is Filter Period.

The PERIOD_MULT_SEL bit is used to select the multiplier for Filter Period.

The only options are DPWM Period and KCOMP. Filter Period is used in LLC topologies so that the Filter can control the switching frequency of the power supply

4.3.13 Ki Adder Mode

The KI_ADDER_MODE bit selects from two modes for calculating the input to Ki.

A 1 in KI_ADDER_MODE will select a trapezoidal mode which adds Xn and Xn-1. At the lowest AFE gain setting, this may lead to saturation of the calculation.

With a 0 in the KI_ADDER_MODE bit, only Xn is used as an input to the integrator. This does not provide trapezoidal calculations, but it does avoid any saturation issues. For a more complete description see 4.1.3 Integral Branch, page 64.

4.4 XN, YN Read and Write Registers

There are several registers which allow access to dynamic values inside the filter. For register formats, consult the Filter Reference section below.

4.4.1 CPU Xn Register

The CPUXN register is used in the CPU Sample mode described above. This is where the firmware writes the CPU controlled value in CPU Sample mode. See Section 4.3.2 Use CPU Sample on page 67.

4.4.2 Filter XN Read Register

This register provides both Xn and Xn-1 for read by the firmware.

4.4.3 Filter YN Read Registers

There are three read registers for internal filter results:

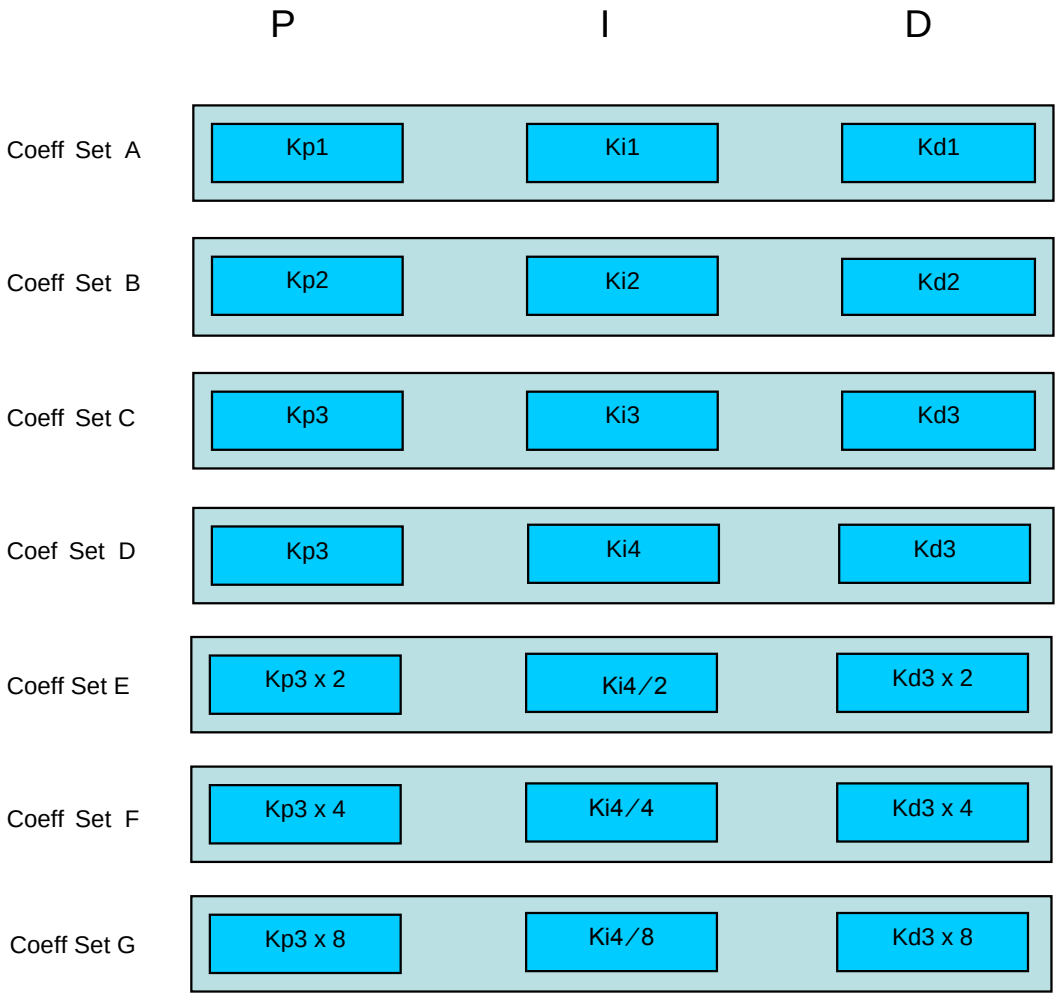
FILTERKIYNREAD
FILTERKDYNREAD
FILTERYNREAD

These provide the outputs of the Integrator, Differentiator, and the total filter.

The proportional output is not provided. It can be determined by multiplying Xn by KP, or by subtracting KiYn and KdYn from Yn.

4.5 Coefficient Configuration Register

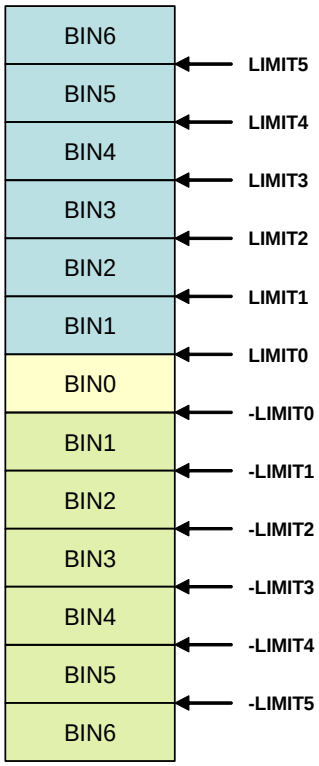
The COECONFIG register is used to configure filter coefficients for nonlinear mode. Each Filter coefficient has from 2 to 4 values which are programmable via Filter registers. Kp, Ki, and Kd are arranged into 7 coefficient sets as shown in the figure below.



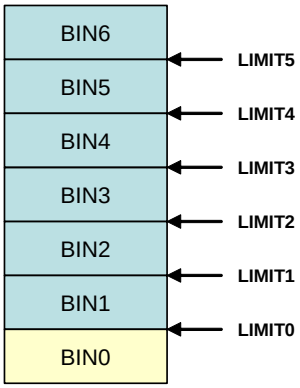
These sets are designed so that bandwidth increases as the set goes from A to G. These sets can be mapped in any possible combination into 7 bins, numbered from Bin 0 to Bin 6.

These bins are selected based on the nonlinear limit register contents and the Xn value into the filter. There are two options – symmetrical and non-symmetrical. Here are the bins for the two modes:

Symmetric (13 Bins)



Non-Symmetric (7 Bins)



There are many possible combinations. In symmetric mode, if bandwidth is to increase as error increases, then Bin 0 could be set to Coefficient Set A, Bin 1 set to Coefficient Set B, and so on.

If fewer bins are desired, then Bins 0 and 1 could both be set to Coefficient Set A, Bins 2 and 3 to B, and so on.

The default configuration is the non-symmetric mode, with all bins set to Coefficient Set A.

Limit values must be increasing, with limit 0 the lowest possible value, Limit 1 higher, and so on. In symmetric mode, all limit values must be positive.

Each bin has a separate bit which selects one of the 2 alpha values.

Here is a code example which uses all the Coefficient sets with increasing bandwidth for increasing error:

```
Filter0Regs.COEFCONFIG.bit.BIN0_CONFIG = 0; //coefficient set A
Filter0Regs.COEFCONFIG.bit.BIN1_CONFIG = 1; //coefficient set B
Filter0Regs.COEFCONFIG.bit.BIN2_CONFIG = 2; //coefficient set C
Filter0Regs.COEFCONFIG.bit.BIN3_CONFIG = 3; //coefficient set D
Filter0Regs.COEFCONFIG.bit.BIN4_CONFIG = 4; //coefficient set E
Filter0Regs.COEFCONFIG.bit.BIN5_CONFIG = 5; //coefficient set F
```

```
Filter0Regs.COEFCONFIG.bit.BIN6_CONFIG = 6; //coefficient set G

Filter0Regs.COEFCONFIG.bit.BIN0_ALPHA = 0; //alpha 0
Filter0Regs.COEFCONFIG.bit.BIN1_ALPHA = 0; //alpha 0
Filter0Regs.COEFCONFIG.bit.BIN2_ALPHA = 0; //alpha 0
Filter0Regs.COEFCONFIG.bit.BIN3_ALPHA = 0; //alpha 0
Filter0Regs.COEFCONFIG.bit.BIN4_ALPHA = 1; //alpha 1
Filter0Regs.COEFCONFIG.bit.BIN5_ALPHA = 1; //alpha 1
Filter0Regs.COEFCONFIG.bit.BIN6_ALPHA = 1; //alpha 1
```

4.6 Kp, Ki, and Kd Registers

There are several registers which hold the Kp, Ki, and Kd coefficients:

FILTERKPCOEF0
FILTERKPCOEF1
FILTERKICOEF0
FILTERKICOEF1
FILTERKDDOEF0
FILTERKDCOEF1

These registers hold all of the coefficients for the PID for the various coefficient sets as described above. For specific details, see the Filter Reference chapter below. All of the K coefficients are 16 bit signed numbers. They are stored 1 or 2 per register. Systems which do not use nonlinear mode only need to load Coefficient Set A. Here is an example:

```
Filter1Regs.FILTERKPCOEF0.bit.KP_COEF_0 = 500;

Filter1Regs.FILTERKICOEF0.bit.KI_COEF_0 = 150;

Filter1Regs.FILTERKDCOEF0.bit.KD_COEF_0 = 250;
```

4.7 Alpha Register

The FILTERKDALPHA register holds the two alpha coefficients which can be selected by the BINx_ALPHA bits in the COEFCONFIG register. Alpha is stored as a 9 bit signed number. Here is an example which only loads KD_ALPHA_0:

```
Filter1Regs.FILTERKDALPHA.bit.KD_ALPHA_0 = 134;
```

4.8 Filter Nonlinear Limit Registers

There are 6 nonlinear limits, as shown above in section 4.5 Coefficient Configuration Register on page 71. These are 9 bit signed numbers, although they must be positive for symmetric mode. They are stored 2 to a register in three registers:

FILTERNL0
FILTERNL1
FILTERNL2

Here is a code example loading them for symmetric mode:

```
Filter1Regs.FILTERNL2.bit.LIMIT5 = 218; //symmetric values
Filter1Regs.FILTERNL2.bit.LIMIT4 = 182;
Filter1Regs.FILTERNL1.bit.LIMIT3 = 145;
Filter1Regs.FILTERNL1.bit.LIMIT2 = 109;
Filter1Regs.FILTERNL0.bit.LIMIT1 = 72;
Filter1Regs.FILTERNL0.bit.LIMIT0 = 36;
```

4.9 Clamp Registers

There are 3 clamps in the filter structure, for the integrator, the output of the PID filter, and the output after the feed forward multiplier. The integrator and filter clamps are signed 24 bit numbers, like the output of the integrator and filter are. The overall output clamp is an unsigned 18 bit number, like the overall output.

Here is an example of clamping everything to a range from 10% to 50% of full scale.

```
Filter2Regs.FILTERYNCLPHI.bit.YN_CLAMP_HIGH = 0x400000; //50% of full scale
Filter2Regs.FILTERYNCLPLO.bit.YN_CLAMP_LOW = (int)(((float)0x800000) *.1);
        //10% of full scale

Filter2Regs.FILTERKICLPHI.bit.KI_CLAMP_HIGH = 0x400000; //50% of full scale
Filter2Regs.FILTERKICLPLO.bit.KI_CLAMP_LOW = (int)(((float)0x800000) *.1);
        //10% of full scale

Filter2Regs.FILTEROCLPHI.bit.OUTPUT_CLAMP_HIGH = 0x20000; //50% of full scale
Filter2Regs.FILTEROCLPLO.bit.OUTPUT_CLAMP_LOW = (int)(((float)0x40000) *.1);
        //10% of full scale
```

4.10 Filter Preset Register

The FILTERPRESET register is used to preset the values in several calculated registers within the filter. The preset register works between filter calculations. If the Filter is calculating when the Filter Preset is enabled, the target register in the Filter is not written to immediately. The hardware waits for the filter to stop calculating and then writes to the target register.

If the filter is not running, the Filter Preset takes effect immediately.

There are three bit fields in the Filter Preset Register.

The PRESET_EN bit is set to enable the preset, and can be polled to tell when it is complete.

The 3 PRESET_REG_SEL bits select which register will be preset, see the Filter Reference Section for the exact values.

Finally, the value to be preset is loaded into the PRESET_VALUE bits.

Here is an example code for using the preset register:

```
while(Filter0Regs.FILTERPRESET.bit.PRESET_EN == 1)
{
        ; //wait for previous preset to take effect
}
```

```
Filter0Regs.FILTERPRESET.bit.PRESET_VALUE = 15; //put a 15
Filter0Regs.FILTERPRESET.bit.PRESET_REG_SEL = 1; //into I holding register
Filter0Regs.FILTERPRESET.bit.PRESET_EN = 1; //set bit to make it happen
```

5 Loop Mux

The Loop Mux controls the connections between the different parts of the control loop – the Front End, the Filter, and the DPWM:

- Front End Control Mux 0, 1, 2 – controls how DPWMs trigger the front end ramp module and DAC dither.
- Sample Trigger Control Register – controls how DPWMs trigger the EADC
- External DAC control Register – controls what DAC setting is used for each Front End
- Filter Mux – Selects Sources of data for the filter
- DPWM Mux Register – Selects inputs for the DPWM

The Loop Mux also has several registers which control multiple modules in one register:

- Global Enable Register (GLBEN) – enables Front Ends and DPWMs simultaneously
- PWM Global Period Register (PWMGLBPRD) – permits changing multiple periods simultaneously
- Sync Control Register (SYNCCTRL) – Configures the SYNC pin

In addition, it controls several modules which tie multiple parts together and have logic of their own:

- Constant Power/Constant Current (CPCC) Module
- Cycle Adjustment Module (used for balancing current and flux)
- Light Load Module
- Analog Peak Current Mode (PCM) Module

Here is a table showing the connections of the Loop Mux. "I" indicates an input to the Loop Mux register or module, "O" indicates an output.

	Front End			**Filter**	**DPWM**	**Loop Mux**	
Registers	EADC	Ramp	DAC			CPCC	KCOMP
FECTRLxMUX	O	O		I	I		
SAMPTRIGCTRL	O				I		
EXTDACCTRL			IO	I		I	
FILTERMUX	I			IO	I		I
FILTERKCOMPx				O			
DPWMMUX		I		I	IO		
GLBEN	O	O	O		O		
PWMGLBPRD					O		
SYNCCTRL					IO		
Modules							
CPCC	I		I	IO	O		
Cycle Adjustment	I				IO		
Light Load	I			I	O		
Analog PCM	I	O	O	I	O		

This chapter covers the Loop Mux registers. The modules have chapters of their own.

5.1 Front End Control Muxes (FECTRL0MUX, FECTRL1MUX, FECTRL2MUX)

These registers select what DPWM signals are used to trigger DAC control functions in the Front end, Ramp and Dither. The selected signals are also used when the Ramp Module is used for Sync FET ramps. Two signals can be used:

1. Rising edges of DPWMA and DPWMB from all DPWM modules
2. Frame sync from all DPWM Modules

Frame sync occurs at the beginning of the DPWM period. It always occurs whenever the DPWM is running. DPWMA and DPWMB are dependent on the actual rising edges of DPWMA and DPWMB. If no DPWM pulse is occurring, then the trigger will not take place. DPWMA_F and DPWMB_F are used. These are the signals coming out of the Fault Block, as shown in 2.1, DPWM Block Diagram, page 13. Anything in the Timing or Fault modules which prevents DPWMA and DPWMB from going high will prevent triggering of the Front End by these signals. Anything further down in the signal chain, such as the Intra Mux or the Edge Generator will have no effect at all.

This trigger should not be confused with the sample trigger, which triggers the EADC conversion. Ideally the DAC control function should be triggered just after the end of the EADC conversion to allow maximum DAC settling time. For DAC settling time, please refer to the UCD3138 device datasheet.

The FECTRLxMUX registers also permit using the Nonlinear Select registers in the Filter to set the step points for Automatic Gain Shifting in the Front End.

For exact FECTRLxMUX bit assignments, see: 11.1, Front End Control 0 Mux Register (FECTRL0MUX), page 145.

5.2 Sample Trigger Control (SAMPTRIGCTRL)

The SAMPTRIGCTRL register has a bit for each combination of Front End and DPWM module. As a default, none of these bits are set, so no sample triggers are enabled. Any DPWM can trigger any Front End. Multiple triggers can be used for any Front End, and multiple Front Ends can use the same trigger. The DPWMs can generate two triggers (A and B). They can generate multiple triggers – oversampling. All of this is automatically transmitted to the Front End if the bit in SAMPTRIGCTRL is set. See 11.4Sample Trigger Control Register (SAMPTRIGCTRL), page 152 for the register details.

5.3 External DAC Control (EXTDACCTRL)

The EXTDACCTRL register permits control of the EADCDAC in each Front End from different sources. If the EXT_DACx_EN bit is 0, the Front End controls its own DAC. If EXT_DACx_EN is 1, other sources will have control:

1. Other EADCDACs – this can be used to slave two Front Ends together.
2. Output of Constant Power Module – this is used for constant power control
3. Filter x Output – this is used to put loops in series, for example, a voltage loop can control a current loop by using the voltage loop output to control the EADCDAC for the current loop.

See 11.5 External DAC Control Register (EXTDACCTRL), page 153 for bitfield details.

5.4 Filter Mux Register (FILTERMUX)

FILTERMUX controls some inputs to the Filters. It selects which Front End provides the error signal to each Filter.

FILTERMUX also selects values for multiplication in the Filter output stage (4.1.6 Filter Output Stage, page 65). For this function, FILTERMUX works together with the PERIOD_MULT_SEL and OUTPUT_MUL_SEL fields in the FILTERCTRL register.

For each Filter, FILTERMUX selects one of each from:

- FILTERx_KCOMPSEL selects from KCOMP0, KCOMP1, or KCOMP2
- FILTERx_FFWD_SEL selects the Feedforward value from one of the other 2 filters
- FILTERx_PER_SEL selects the Period from DPWM0, 1, 2, or 3.
- FILTERx_PER_SEL also selects the source for Resonant Duty.

Then OUTPUT_MULT_SEL bits select from these preselected values. OUTPUT_MULT_SEL can select any of the 4 inputs. PER_MULT_SEL can only select from Period or KComp.

5.5 Filter KComp Registers (FILTERKCOMPx)

There are two registers, FILTERKCOMPA and FILTERKCOMPB. FILTER KCOMPA holds both KCOMP0 and KCOMP1. FILTERKCOMPB holds only KCOMP3. All KComp values are 14 bit unsigned numbers.

5.6 DPWM Mux Register (DPWMMUX)

DPWMMUX selects inputs to the DPWM modules. It selects

- Ramp module which controls Synchronous FET ramp.
- Master DPWM which provides sync pulse if DPWM module is a slave
- Source which controls duty cycle/resonant period for DPWM. This source can be a Filter, the Constant Power Module, or the Light Load Control Module.

5.7 Global Enable Register (GLBEN)

GLBEN has bits which enable each DPWM and each Front End. These bits are anded with the individual enable bits in each DPWM and Front End. Both global and local bits must be set for the modules to start. For simultaneous, synchronous start up, first set all the local enable bits, and then write a single time to the GLBEN register. This simultaneous write can be done in at least two ways:

1. Define a temporary variable which has the same structure as GLBEN

   union GLBEN_REG glben_store; //collect global enable bits for simultaneous use

   glben_store.all = 0;

   glben_store.bit.DPWM0_EN = 1;
   glben_store.bit.DPWM1_EN = 1;

   glben_store.bit.FE_CTRL0_EN = 1;

   LoopMuxRegs.GLBEN = glben_store;

2. Simply write to GLBEN:

LoopMuxRegs.GLBEN = 0x13;

5.8 PWM Global Period Register (PWMGLBPRD)

If the Global Period Enable (GLOBAL_PERIOD_EN) bit is set in DPWMCTRL1 of a DPWM module, it will use the value in PWMGLBPRD for its period. This can be used to change the periods of multiple DPWMs with one C statement. This is useful for frequency dithering. Note that the period change takes effect at the end of the previous period. If DPWMs are out of phase, the frequency change will take place at a different time for each DPWM.

Also note that the if the Filter is using the Period from the DPWM for calculations, it will still use the DPWM Period Register even if the Global Period is enabled. So to use the Global Period, it is necessary to use the KCOMP register as a multiplier and to change both the Global Period Register and the KCOMP register at the same time. In fact, a careful sequence should be followed:

If the period is increasing – first change the Global Period Register, then wait 1 period, then change the KCOMP. This sequence guards against dead time violations.

For the same reason, when decreasing the period, change the KCOMP first.

For any frequency change, the order of changes should be carefully designed based on the actual topology and IC configuration.

5.9 Sync Control (SYNCCTRL)

SYNCTRL controls the Sync pin. The Sync pin can be an input or an output. It can output the Sync pulse from any DPWM, or it can be used as a general purpose output. It can also output some internal processor clocks for debugging purposes.

As an input, it can be used as a sync input to the DPWMs, and as a general purpose input. To use it as a sync input to the DPWMs, set the EXT_SYNC_EN bit in DPWMCTRL1.

5.10 Light Load (Burst) Mode

There are several registers in the Loop Mux related to Burst mode/Light Load Mode. This mode works based on the output of a selected filter. In its simplest form, it disables DPWM output pulses when the filter output goes below a threshold – LoopMuxRegs.LLDISTHRESH. It reenables them when the filter goes above another threshold – LoopMuxRegs.LLENTHRESH.bit.TURN_ON_THRESH. There are bits in the LLCTRL register to enable Light Load Mode, and to select which filter output is used to drive the Light Load control

To enable the single Light Load Module to control a DPWM module, the BURST_EN bit in DPWMCTRL1 must be set.

In normal mode, if PWM pulses get very short, they will stop altogether. The output voltage will drop by a small amount, and the filter output will rise again, and it will start up again. There are added features which permit output of fixed size pulses in burst mode. This function is very application specific. Consult the reference firmware code provided with the UCD3138 EVM for the desired topology for further information.

It may be necessary to adjust the thresholds as a function of Vin, for example.

5.11 Constant Current / Constant Power

Constant Current/Constant Power is very dependent on topology for configuration and utilization. Consult the appropriate EVM firmware for the appropriate Constant Current/Constant Power setup.

5.12 Analog Peak Current Mode

In the Loop Mux, there are two simple registers – PCMCTRL and APCMCTRL.

PCMCTRL has only one bitfield:

- PCM_FILTER_SEL. This field selects a filter output. The filter output is used for the start of the compensating ramp.

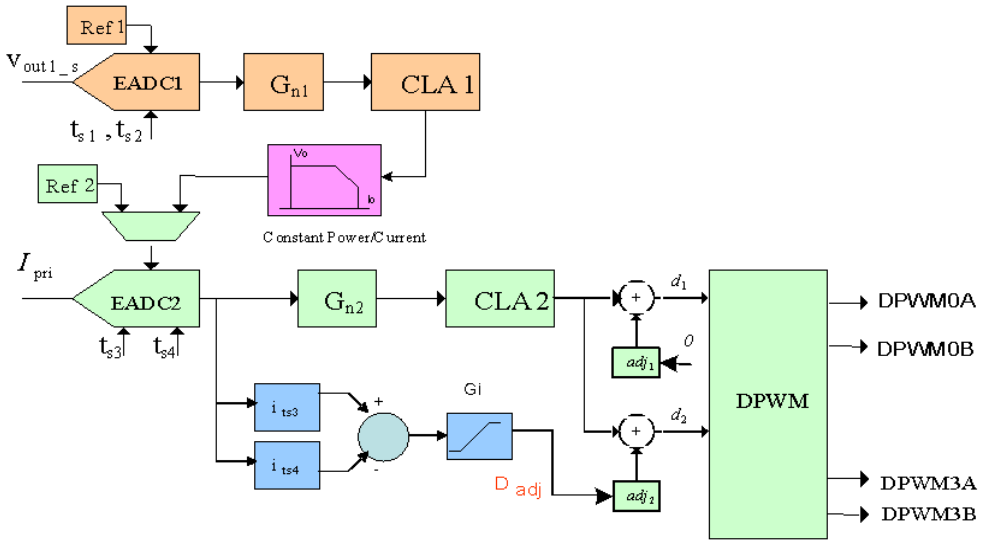
ADPCMCTRL has 3 bitfields:

- PCM_FE_SEL – selects which Front End is used to compare the compensation ramp to the power supply current
- PCM_LATCH_EN – enables the latching of the peak current detection to the end of the PCM frame
- PCM_EN – enables peak current mode

Refer to the reference firmware code provided with UCD3138PSFBEVM-027 and TI application note for Phase Shift Full Bridge peak current mode control implementation with UCD3138.

5.13 Automatic Cycle Adjustment

The Loop Mux contains registers which control and monitor automatic cycle adjustment. It can be used to balance current between two legs of a parallel topology, such as a multiphase PFC. It can also be used for flux balancing in bridge topologies. The figure below illustrates an example of it being used in a bridge topology. The cycle adjustment is shown on the bottom left hand side, connecting the output of EADC2 to D_{adj}. Current is being measured on each half cycle, so the two samples come from the same EADC. The output is being used to adjust DPWM3 Duty to maintain flux balance.



UCD3138 Flux Balancing Approach

5.13.1 Calculation

The output of this logic is a cycle adjustment number provided to the DPWM based on the difference between two samples from one or two front end EADCs. The equation is:

$D_{adj} = [\![(E]\!]_1 - E_2)2^{CYC_{ADJ_{GAIN}}}$

D_{adj} = Duty Cycle Adjust

where E_1 E_2 = EADC error values(i_{ts3} and i_{ts4}) shown in the figure
CYC_ADJ_GAIN = bitfield value in CYCADJCTRL register

5.13.2 Configuration

Most of the control is in the CYCADJCTRL register.

The measurement starts after a DPWMxA rising edge selected by CYC_ADJ_SYNC.

After the rising edge, the logic waits for a sample from the Front End selected by FIRST_SAMPLE_SEL.

After the first sample, the logic waits for a sample from the Front End selected by SECOND_SAMPLE_SEL. After that, it calculates D_{adj} and presents it to the DPWM modules.

All the bit-fields mentioned above are in CYCADJCTRL. There is also a CYC_ADJ_EN bit to enable automatic cycle adjustment.

To enable the DPWM to accept the adjustment, it is necessary to set the CLA_DUTY_ADJ_EN bit in DPWMCTRL1.

It is also necessary to provide sample triggers to the EADC, of course.

To prevent excessive adjustment in the event of a measurement failure, the Cycle Adjustment Limit Register (CYCADJLIM) provides upper and lower limits for the

5.13.3 Scaling

The EADC error signal is scaled at a nominal 1 mV. The output of the Automatic Cycle Adjust Module is scaled at normal resolution – 1 step = 4 ns.

So if $[\![(E]\!]_1 - E_2)$ is 1 mV, and CYC_ADJ_GAIN is 0, the cycle adjustment will be 4 nanoseconds. This will make the duty cycle on any DPWM with CLA_DUTY_ADJ_EN set 4 nanoseconds longer.

6 Fault Mux

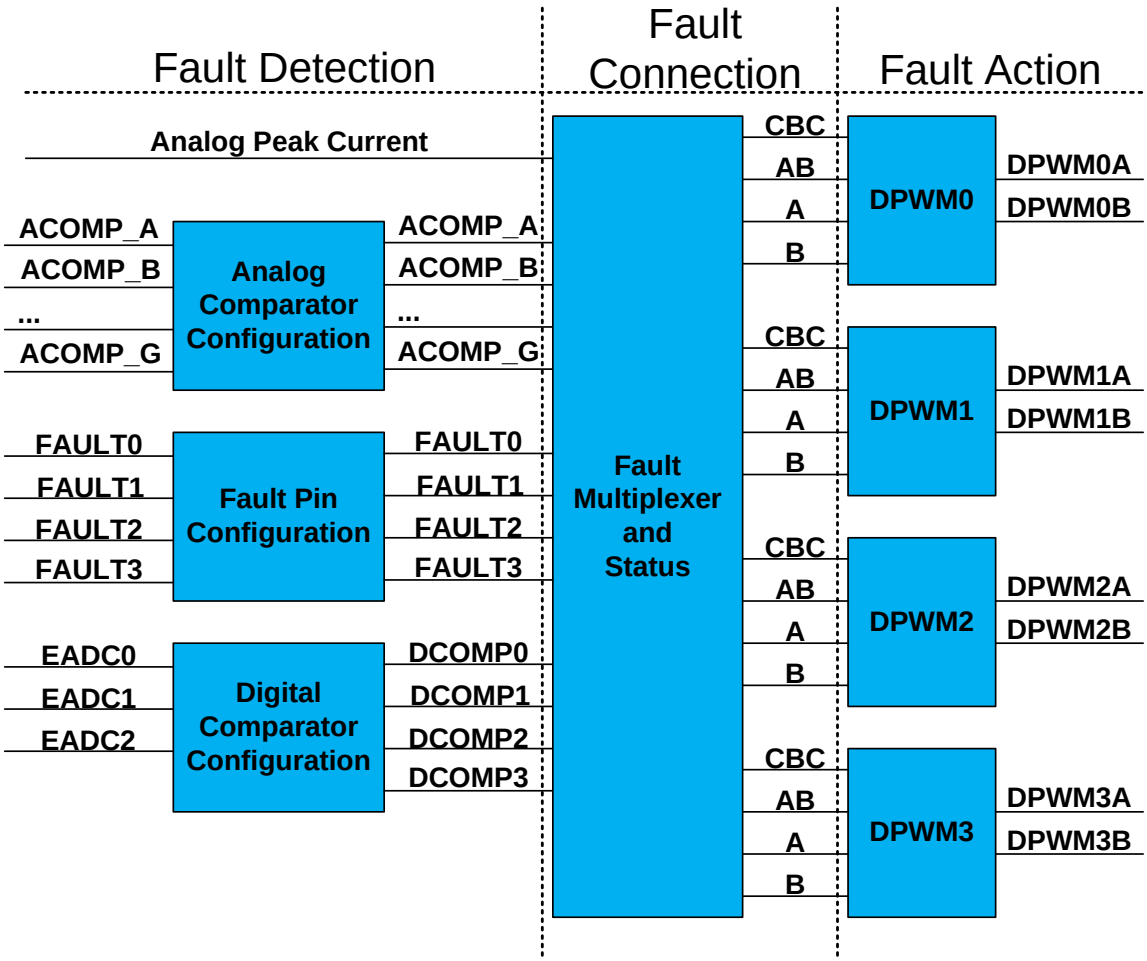
The Fault Mux registers control a multiplexer which connects power supply fault signals to DPWMs. They also perform several other functions

- Configuration of analog and digital comparators and fault pins for fault detection
- Monitoring of fault status

- Digital Ideal Diode Emulation circuit for synchronous rectification FETs
- Processor clock failure detection
- Support for analog peak current mode control

The Fault Mux is responsible for fault detection and connection, while the DPWM is responsible for the action taken to handle the fault. Even though most of the control for fault response action is based in the DPWM registers, it is discussed in this section (in this way all information relating to the Fault information is available in one location).

Here is an overview of the fault handling system in the UCD3138:



UCD3138 Fault Handling System

The system is very flexible and powerful. There are 7 analog comparators, 4 fault pins, and 4 digital comparators. Each DPWM has 4 fault inputs which affect its outputs in different ways. Any combination of fault detection outputs can be connected to drive any combination of DPWM fault inputs.

Here are three examples:

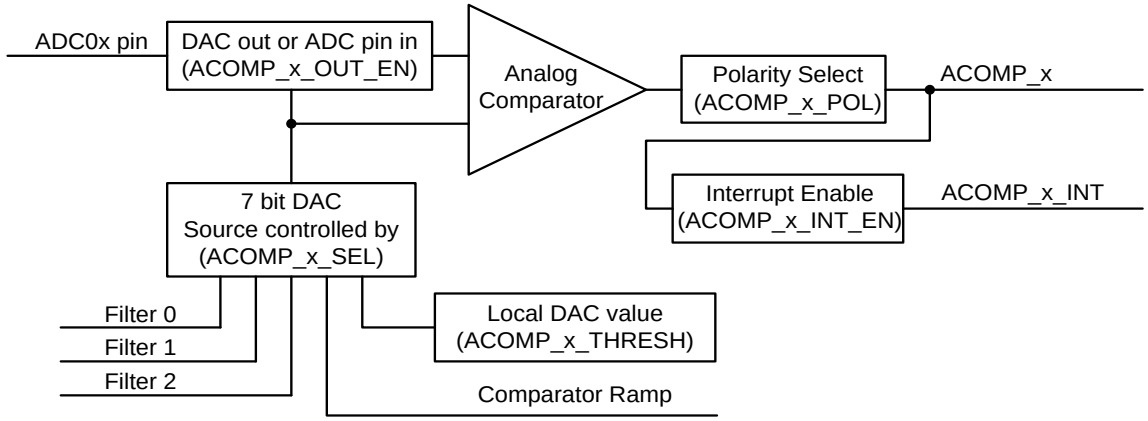
1. Many fault outputs mapped to a single fault input - An analog comparator in charge of over voltage protection, a digital comparator in charge of over current protection and an external digital fault pin can be all mapped to a fault-A signal connected to a single DPWM fault input and shut down DPWM1-A.

2. Single fault output mapped to many fault inputs inside many DPWM modules - An analog comparator in charge of over current protection can be mapped to all DPWM-0 through DPWM-3 through several fault modules.

3. Many fault sources mapped to a many fault modules inside many DPWM modules. A flexible combination of both above mentioned alternatives.

6.1 Analog Comparator Configuration

The analog comparators are controlled by the ACOMPCTRL0 to ACOMPCTRL3 registers. This figure shows how the control works:



UCD3138 Analog Comparator Control

All the names in parentheses on the drawing above are bitfield names in the ACOMPCTRL registers. The Analog Comparators are sampled at the HFO rate (nominal 250 MHz). Any fault on the Analog Comparators will be transmitted to the Fault Mux regardless of the DPWM timing.

6.1.1 ACOMP_EN

The first step in starting the analog comparators is to set the ACOMP_EN bit in ACOMPCTRL0.

```
FaultMuxRegs.ACOMPCTRL0.bit.ACOMP_EN = 1;
```

This bit enables all the analog comparators.

6.1.2 ACOMP_x_THRESH

For typical operation - detecting an overcurrent or over voltage fault - only the ACOMP_x_THRESH register needs to be written. It is written with a value that corresponds to the fault level on the input pin.

```
FaultMuxRegs.ACOMPCTRL1.bit.ACOMP_C_THRESH = OVER_VOLTAGE_THRESH;
```

All the other registers are set to defaults which work for this application.

6.1.3 ACOMP_x_POL

To detect a fault caused by a voltage going below a threshold, rather than above, clear the ACOMP_x_POL bit. A zero in this bit causes the ACOMP_x signal to go active when the ADC pin goes below the comparator threshold.

6.1.4 ACOMP_x_INT_EN

The ACOMP_x_INT_EN bit, when set enables an interrupt from the Analog Comparator.

6.1.5 ACOMP_x_OUT_EN

The ACOMP_x_OUT_EN bit when set, puts the DAC value out on the ADC pin, which can be used as an external reference. Consult the UCD3138 device datasheet for additional information. When this bit is enabled, obviously the comparator output signals are not valid.

6.1.6 ACOMP_x_SEL

The comparator DAC can also be driven by other data – Filter outputs and a comparator ramp engine. The ACOMP_x_SEL register selects which of these sources is used.

6.1.7 ACOMP_F_REF_SEL

Analog Comparator F is a special case. It can be configured to use AD07 as a reference instead of the DAC. To enable this, set the ACOMP_F_REF_SEL bit in ACOMPCTRL2.

6.1.8 ACOMPCTRL Register Arrangement

There are 7 Analog Comparators, but only 4 ACOMPCTRL registers. The comparators are organized 2 to a register.

6.2 Analog Comparator Ramp

The analog comparator ramp logic is a digital circuit which can provide a ramping value to the comparator reference DACs. It is a simpler, lower resolution version of the ramp engines in the Front Ends (for information regarding the Front End ramp engines, refer to Section 3.3 Ramp Module, page 56). The key differentiating features of the Analog Comparator Ramp are as follows:

- Only 7 bits of resolution
- Ramp steps are triggered by MCLK (Nominal 31.25 MHz.)
- Ramp start is triggered by DPWMx frame start as selected by DPWMx_TRIG_EN bits.
- Ramp always rises, ramp end value is always 0x7f (DAC maximum)

6.3 Digital Comparator Configuration

The Digital Comparator is another fault detection mechanism. Instead of a direct analog input, it uses the result of the Front End EADC measurement to detect faults.

There are 3 Digital Comparators, controlled by the DCOMPCTRL0, 1, and 2 registers

They use the FE_SEL bitfield to select which Front End is used as a source, and whether the absolute or error data from that Front End is used.

Like the Analog Comparators, they can be programmed to detect a fault either above or below the threshold. The COMP_POL bit is used to select this.

There is also an INT_EN bit to enable the interrupt.

Each Digital Comparator has its own COMP_EN bit to enable it.

The reference threshold for the comparator is much simpler, it only comes from the THRESH bit-field. It does have 11 bits of resolution, more than the Analog comparator.

The Digital Comparator adds a counter that can require several sequential fault detections before the signal is passed on to the Fault Mux.

The CNT_THRESH bitfield controls the number of fault detections required. Writing a 1 to the CNT_CLR bit will clear the counter and the associated fault.

If the counter reaches the CNT_THRESH value, it will be locked, and the DCOMP_x signal will be sent to the Fault Mux.

The Digital Comparator performs its comparison on each sample from the selected Front End. Fault detection can only occur after each sample from the Front End.

The CNT_CONFIG bit controls handling of sequences of samples which contain some fault samples and some non-fault samples. In the default mode – CNT_CONFIG = 0 – a non-fault sample will clear the counter (assuming it hasn't reached CNT_THRESH).

If CNT_CONFIG = 1, a non-fault event will decrement the counter, unless the counter is already zero. With this setting, if the fault occurs more than 50% of the time, eventually the counter will reach the threshold.

There is also a DCOMPCNTSTAT register which gives the value in each of the counters. This register is read only.

6.4 Fault Pin Configuration

There are 4 fault pins, Fault 0 to Fault 3. Their configuration is very simple.
- FAULTx_POL sets polarity
- FAULTx_INT_EN enables the interrupt
- FAULTx_DET_EN enables fault detection.

All these bits are in the EXTFAULTCTRL register. Like the Analog Comparators, the fault pins are sampled at the MCLK rate.

6.5 Analog Peak Current

Analog Peak Current is another input to the Fault Mux. It is not technically a fault, since it is controls the normal operation of a power supply based on peak current mode control. The Analog Peak Current signal comes from a Front End, and can only be routed to the CBC (Cycle by Cycle) input of the DPWM. For additional information consult the reference firmware provided with UCD3138PSFBEVM-029 EVM and TI application note on Phase Shift Full Bridge (Peak Current mode control) implementation.

6.6 Fault Status Registers

There are two registers which give the fault detection status: FAULTMUXINTSTAT and FAULTMUXRAWSTAT.

Both have the same bits, but they mean different things.

FAULTMUXRAWSTAT shows the instantaneous status of each fault.

FAULTMUXINTSTAT shows any faults which:
- Have occurred since the last read of FAULTMUXINTSTAT
- Have interrupts enabled.

This is especially useful for detecting faults which may occur only for short times during a period. Reading from this register clears the fault from the fault detection interrupt logic. This interrupt logic is independent of the signals routed to the Fault Mux and to the DPWM. These signals are latched only in the DPWM logic, not anywhere else.

The registers also have bits for LFO_FAIL (Low Frequency Oscillator Fail) and for DCM_DETECT (Discontinuous Mode Detected). These sources are described elsewhere. Neither of these signals is used as an input to the Fault Mux.

6.7 Fault Mux Control Registers

There are 4 DPWM modules, 0-3. Each DPWM module has 4 fault inputs, CLIM, AB, A, and B.

There are 3 fault Mux registers for each DPWM:
- DPWMxCLIM – controls CLIM, also known as CBC
- DPWMxFLTABDET – controls the AB fault input
- DPWMxFAULTDET – controls the A and B fault inputs.

Programming these registers is very simple. There is a bit for each fault detection source in each register. Setting it connects that fault detection source to the fault input and DPWM for that register. Here is an example:

```
FaultMuxRegs.DPWM0FLTABDET.bit.ACOMP_B_EN = 1;
        // Connect analog comp B to DPWM0 fault input AB
```

Controlling the A and B fault inputs in the same register works like this:

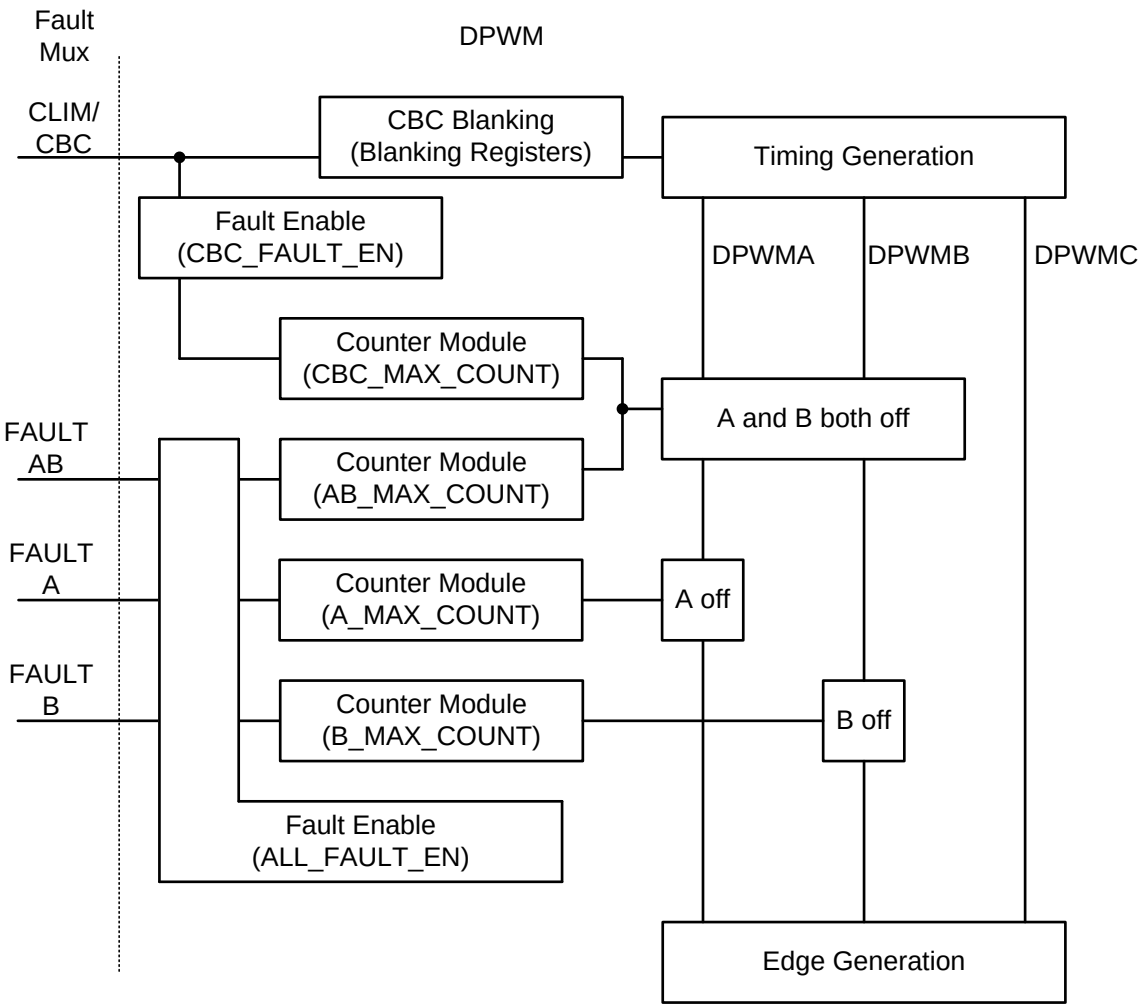
```
FaultMuxRegs.DPWM0FAULTDET.bit.PWMA_ACOMP_B_EN = 1;
        //Connect analog comparator B to DPWM0 fault A

FaultMuxRegs.DPWM0FAULTDET.bit.PWMB_ACOMP_B_EN = 1;
        //Connect analog comparator B to DPWM0 fault B
```

Almost any fault detection circuit can be connected to any fault input on any DPWM. The only exception is the Analog Peak Current mode, which can only be connected to the CLIM fault input:

```
FaultMuxRegs.DPWM0CLIM.bit.ANALOG_PCM_EN   = 1;
```

6.8 DPWM Fault Action

The final section in the fault chain is the fault action, which takes place in the DPWM module. Here is a drawing showing the main points of fault action:



UCD3138 DPWM Fault Action

This drawing fits in with the overview of the DPWM in Section 2.1 DPWM Block Diagram, page 13. The portion expanded here is the fault handler portion. The connection of the CLIM/CBC signal to the Timing Generation Module is also shown.

For information on the effect of CLIM/CBC in the timing module, see Section 2.15.3 Cycle by Cycle Current Limit Enable, page 33. The bits described in that section affect the CLIM/CBC signal which is sent to the Timing Generator. The DPWM section also describes the Blanking Registers in the DPWM, which permit blanking of the CLIM/CBC signal to the Timing Generation section. These registers are used to prevent switching noise from causing false triggers of the CBC logic. They can also be used to synchronize CBC triggers between DPWMs with different on-times. The blanking registers affect different edges depending on topology. The effects are as follows:

– For normal and resonant modes, blanking A and B windows are applied to PWM-A only
– For triangular mode, blanking A and B windows are applied to PWM-B only
– For all other modes, blanking A and B windows are applied to PWM-A and PWM-B respectively

CLIM/CBC is also used by the Fault Handler, which is described below. The two mechanisms are completely independent of each other, except they have the same input signal. The Blanking Registers do not affect the CLIM/CBC signal which goes to the Fault Handler.

This section will describe the logic in the fault handling portion of the DPWM.

All 4 signals, CLIM/CBC, AB,A, and B can be used as fault signals, and all are used in exactly the same way, except they shut off different DPWM signals.

As shown, there are 2 enable bits, CBC_FAULT_EN for CLIM/CBC, and ALL_FAULT_EN for the other 3. Each fault has its own 5 bit counter, with a maximum value set by a dedicated x_MAX_COUNT bit-field. The fault lines are monitored continuously, but only one event per DPWM period is counted. If the x_MAX_COUNT value is set to 0, the first fault event will shut off the appropriate DPWM pins. The maximum number of sequential fault periods is 31, if the x_MAX_COUNT field is loaded with a 0x1f.

The faults must occur sequentially. If any period completes without a fault, the counter will be reset.

The faults handler is much simpler than the CLIM/CBC in the timing generator. They simply latch off either 1 or 2 of the DPWM pins. To restart the DPWM, it is necessary to disable it using either the global enable register:

```
void global_enable(void)
{
        //Enable DPWM0, DPWM1, DPWM2, DPWM3, FE_CTRL0 AND FE_CTRL1
simultaneously.
        LoopMuxRegs.GLBEN.all = 0x30F;
}

void global_disable(void)
{
        //Disable DPWM0, DPMW1, DPWM2 and DPWM3 simultaneously.
        LoopMuxRegs.GLBEN.all = 0x300;
}
```

Or the local DPWM enable register:

```
Dpwm0Regs.DPWMCTRL0.bit.PWM_EN = 0;
Dpwm0Regs.DPWMCTRL0.bit.PWM_EN = 1;
```

The DPWMINT register can be used to configure Fault interrupts, as well as other interrupts. It can also be used to read the status of those interrupts. The interrupt bits are cleared by a read. The DPWMFLTSTAT register shows the status of the faults. These bits are also clear on read bits. See the reference section for bit mapping of these registers.

If the fault is enabled by the ALL_FAULT_EN bit, and it occurs, the FLT_A, FLT_B, FLT_AB flags will be set. If the appropriate INT_EN bit is set, the DPWM will send and interrupt to the Central Interrupt Module (CIM). If the interrupt for that DPWM is enabled in the CIM, then an interrupt will be given to the processor.

6.9 IDE /DCM Detection Control

In addition to the fault detection and connection described above, there are other registers in the Fault Mux Registers that control other functions. One of these functions is IDE/DCM detection. IDE stands for Ideal Diode Emulation. DCM stands for Discontinuous Mode. They are both controlled by the IDECTRL register in the Fault Mux register set.

Some isolated power topologies simple employ rectification diodes on the secondary side. In Ideal Diode emulation, FETs are used instead of diodes. They are turned on when the diode would be conducting and turned off when the diode would be reverse biased. This increases efficiency because the voltage drop across the FET is lower than the drop across the diode. This is called Synchronous Rectification, so the FETs are called Sync FETs for short.

In continuous mode, current is always flowing, and the sync FET can be turned on for the entire time when the primary side is off, except for dead times. This function is served perfectly by the Normal Mode of the DPWM module. Note that IDE/DCM Detection only works in Normal Mode.

In discontinuous mode, however, current is not flowing continuously, so the sync FET must be turned off before the end of the period to emulate the diode. Otherwise energy can flow back from the secondary to the primary.

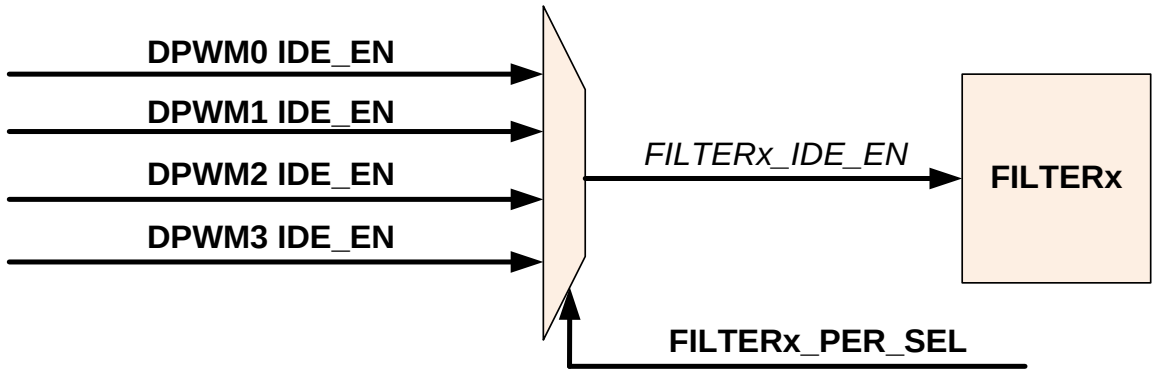
In discontinuous mode, the on time(duty) for the sync FET (Db) is proportional to the DPWMA on-time (Da). The multiplying factor depends on the topology, the circuit configuration and on Vin and Vout. This multiplying factor needs to be frequently calculated by firmware and placed in the IDE_KD register.

FaultMuxRegs.IDECTRL.bit.IDE_KD = kd_value;

IDE must also be enabled in the DPWM module:

Dpwm1Regs.DPWMCTRL2.bit.IDE_DUTY_B_EN = 1; //enable ide

Db is calculated by Da (Filter Duty) times IDE_KD. KD is an unsigned value with 4 integer bits and 9 fractional bits. For example, a 0b0001.000000000 would equate to a multiplier of 1 ("0b" signifies binary, and the "." is used to divide the fractional from the integer part). This would correspond to a hex value of 0x200. For this value of Kd, Db would be exactly the same as Da. There is only one IDE_KD register, but each Filter can can calculate using the KD. Each Filter's output of the IDE value is controlled by the IDE_EN bit in a DPWM module. The DPWM module is selected by the LoopMux.FILTERMUX.bit.FILTERx_PER_SEL bitfield as shown below:



Normally FILTERx_PER_SEL will already be pointing at the right Filter, because it is also used to provide the period for the Filter to use in calculating the duty value.

In some cases, however, for example where KCOMP is used instead of period, it is still necessary to set FILTERx_PER_SEL so that IDE_EN can be multiplexed properly.

Note also that IDE_EN still needs to be set on any DPWM which is using IDE, even though that DPWM may not be providing IDE_EN to the Filter. If IDE_EN is not set, the normal dead times will be used to control DPWMB.

The IDECTRL register also contains a means to detect DCM. As mentioned before, in continuous mode, the sync FET is on for the entire time that DPWMA is off. So Db = 1-Da. In discontinuous mode, Db < 1-Da. So the DCM detection logic triggers an interrupt when Db < 1-Da. Hysteresis is provided to prevent the interrupt from triggering repeatedly when steady state is close to the boundary between continuous and discontinuous. This is done with the DCM_LIMIT_H and DCIM_LIMIT_L registers.

The DCM_DETECT bit is set when:

Db < ((1-Da) – DCIM_LIMIT_L

It is reset when:

Db > ((1-Da) + DCIM_LIMIT_H

The DCM_DETECT bit can be monitored in the FAULTMUXRAWSTAT register. The status of the interrupt can be read in the FAULTMUXINTSTAT register. The interrupt is enabled by DCM_INT_EN in the IDECTRL register.

6.10 Oscillator Failure Detection

The Fault Mux Module provides the capability to detect failures of the High Frequency and Low Frequency Oscillator blocks. Detection of a High Frequency Oscillator failure can be configured to generate a chip reset. Firmware can configure the Fault Mux Module to generate an interrupt upon detection of a Low Frequency Oscillator Failure.

6.10.1 High Frequency Oscillator Failure Detection

Two counters are used to detect a failure with the High Frequency Oscillator block. One counter is implemented in the High Frequency Oscillator clock domain, while the other counter is implemented in the Low Frequency Oscillator clock domain. The High Frequency Oscillator counter generates a clear signal once the counter reaches a firmware programmable 17-bit threshold. This clear signal clears the free running Low Frequency Oscillator counter. In the case of a High Frequency Oscillator failure, no clear signal is generated and the Low Frequency Oscillator counter will overflow, generating an oscillator fail flag to the SYS module. Based on the SYS module setup, a chip reset may be generated from the oscillator failure.

There are 2 bitfields in the HFO Failure detection register HFOFAILDET.

HFO_FAIL_THRESH – Configures threshold where a clear flag is used to clear a counter in the Low Frequency Oscillator domain (if LFO counter overflows, a reset will be generated), resolution of threshold equals High Frequency Oscillator period

Bit 0: HFO_DETECT_EN – a 1 enables High Frequency Oscillator Failure Detection logic, device will be reset upon detection of an oscillator failure

There is no interrupt or status bit for HFO failure. This is because if the HFO fails, the processor will not be working.

6.10.2 Low Frequency Oscillator Failure Detection

The Low Frequency Oscillator is used for the watchdog timer, and to test the functionality of the HFO as described above. As with the High Frequency Oscillator Failure detection, two counters are used to detect a failure with the Low Frequency Oscillator block. The counter roles are reversed in the Low Frequency Oscillator failure detection with the Low Frequency Oscillator clock generating a clear signal once the counter reaches a firmware programmable 5-bit threshold. This clear signal clears the free running High Frequency Oscillator counter. In the case of a Low Frequency Oscillator failure, no clear signal is generated and the High Frequency Oscillator counter will overflow. Firmware can detect the Low Frequency Oscillator Failure through the Fault Mux interrupt or through polling the status register in the Fault Mux Registers. There are three bit fields in the LFOFAILDET register:

- LFO_FAIL_THRESH – Configures threshold where a clear flag is used to clear a counter in the High Frequency Oscillator domain (if HFO counter overflows, a reset will be generated), resolution of threshold equals Low Frequency Oscillator period
- LFO_FAIL_INT_EN – a 1 enables Interrupt Generation upon LFO Failure Detection
- LFO_DETECT_EN - a 1 enables the LFO failure detection circuitry.

There are LFO_FAIL bits in the FAULTMUXRAWSTAT and FAULTMUXINTSTAT registers, giving status of the LFO fault detection status and interrupt status.

7 GIO Module

The GIO Module offers general purpose input/output pins. These pins can also be used as inputs to the fault logic above. These pins can also be used for fault interrupts. The GIO registers also control and monitor the external interrupt pin. They are similar to GPIO functions on many microcontrollers. For more information, see section 13, GIO – General Purpose Input/Output Module, page 218.

8 DPWM 0-3 Registers Reference

8.1 DPWM Control Register 0 (DPWMCTRL0)

Address 00050000 – DPWM 3 Control Register 0
Address 00070000 – DPWM 2 Control Register 0
Address 000A0000 – DPWM 1 Control Register 0
Address 000D0000 – DPWM 0 Control Register 0

Bit Number	31:28
Bit Name	PWM_B_INTRA_MUX
Access	R/W
Default	0000

Bit Number	27:24	23	22
Bit Name	PWM_A_INTR4_MUX	CBC_PWM_C_EN	MULTI_MODE_CLA_B_OFF
Access	R/W	R/W	R/W
Default	0000	000	0

Bit Number	21	20	19

Bit Name	MULTI_MODE_CLA_A_OFF	CBC_PWM_AB_EN	CBC_ADV_CNT_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18:17	16	15
Bit Name	MIN_DUTY_MODE	MASTER_SYNC_CNTL_SEL	MSYNC_SLAVE_EN
Access	R/W	R/W	R/W
Default	00	0	0

Bit Number	14	13
Bit Name	D_ENABLE	CBC_SYNC_CUR_LIMIT_EN
Access	R/W	R/W
Default	0	0

Bit Number	12	11	10
Bit Name	RESON_MODE_FIXED_DUTY_EN	PWM_B_FLT_POL	PWM_A_FLT_POL
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	9	8	7:4
Bit Name	BLANK_B_EN	BLANK_A_EN	PWM_MODE
Access	R/W	R/W	R/W
Default	0	0	0010

Bit Number	3	2	1	0
Bit Name	PWM_B_INV	PWM_A_INV	CLA_EN	PWM_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	1	0

Bits 31-28: PWM_B_INTRA_MUX – Interchanges DPWM signals post edge generation
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bits 27-24: PWM_A_INTRA_MUX – Combines DPWM signals are prior to HR module
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C

6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bit 23: CBC_PWM_C_EN – Sets if Fault CBC changes output waveform for PWM-C
0 = PWM-C unaffected by Fault CBC (Default)
1 = PWM-C affected by Fault CBC
Bit 22: MULTI_MODE_CLA_B_OFF – Configures control of PWM B output in Multi-Output Mode when CLA_ENABLE is asserted
0 = PWM B pulse width controlled by Filter Calculation (Default)
1 = PWM B pulse width controlled by Event3 and Event4 registers
Bit 21: MULTI_MODE_CLA_A_OFF – Configures control of PWM A output in Multi-Output Mode when CLA_ENABLE is asserted
0 = PWM A pulse width controlled by Filter Calculation (Default)
1 = PWM A pulse width controlled by Event1 and Event2 registers
Bit 20: CBC_PWM_AB_EN – Sets if Fault CBC changes output waveform for PWM-A and PWM-B
0 **=** PWM-A and PWM-B unaffected by Fault CBC (Default)
1 **=** PWM-A and PWM-B affected by Fault CBC

Bit 19: CBC_ADV_CNT_EN – Selects cycle-by-cycle of operation
Normal Mode
0 = CBC disabled (Default)
1 = CBC enabled
Multi and Resonant Modes
0 = PWM-A and PWM-B operate independently (Default)
1 = PWM-A and PWM-B pulse matching enabled
Bits 18-17: MIN_DUTY_MODE – Minimum Duty Cycle Mode
00 = Suppression of minimum duty cycles is disabled (Default)
01 = CLA value is clamped to zero when below input value is less than MIN_DUTY_LOW
10 = CLA value is clamped to MIN_DUTY_LOW register value when input value is less than MIN_DUTY_LOW
Bit 16: MASTER_SYNC_CNTL_SEL – Configures master sync location
0 = Master Sync controlled by Phase Trigger Register (Default)
1 = Master Sync controlled by CLA value
Bit 15: MSYNC_SLAVE_EN – Multi-Sync Slave Mode Control
0 = PWM not synchronized to another PWM channel (Default)
1 = Enable Multi-Sync Slave Mode, current channel will be slaved from corresponding channel
Bit 14: D_ENABLE – Converts CLA duty value to DPWM as period-CLA duty value
0 = Value used for event calculations if CLA Duty (Default)
1 = Value used for event calculations is period minus CLA duty value
Bit 13: SYNC_CUR_LIM_EN – Sets how current limit affects slave sync
0 = Slave sync is unaffected during current limit (Default)
1 = Slave sync is advanced during current limit.
Bit 12: RESON_MODE_FIXED_DUTY_EN – Configures how duty cycle is controlled in Resonance Mode
0 = Resonant mode duty cycle set by Filter duty (Default)
1 = Resonant mode duty cycle set by Auto Switch High Register
Bit 11: PWM_B_FLT_POL – Sets the fault output polarity during a disable condition (i.e. fault or module disabled)
0 = PWM B fault output polarity is set to low (Default)
1 = PWM B fault output polarity is set to high

Bit 10: PWM_A_FLT_POL – Sets the fault output polarity during a disable condition (i.e. fault or module disabled)

0 = PWM A fault output polarity is set to low (Default)
1 = PWM A fault output polarity is set to high

Bit 9: BLANK_B_EN – Comparator Blanking Window B Enable

0 = Comparator Blanking Window for PWM-B Disabled (Default)
1 = Comparator Blanking Window for PWM-B Enabled

Bit 8: BLANK_A_EN – Comparator Blanking Window A Enable

0 = Comparator Blanking Window for PWM-A Disabled (Default)
1 = Comparator Blanking Window for PWM-B Enabled

Bits 7-4: PWM_MODE – DPWM Mode

0 = Normal Mode
1 = Resonant Mode
2 = Multi-Output Mode (Default)
3 = Triangular Mode
4 = Leading Mode

Bit 3: PWM_B_INV – PWM B Output Polarity Control

0 = Non-inverted PWM B output (Default)
1 = Inverts PWM B output

Bit 2: PWM_A_INV – PWM A Output Polarity Control

0 = Non-inverted PWM A output (Default)
1 = Inverted PWM A output

Bit 1: CLA_EN– CLA Processing Enable

0 = Generate PWM waveforms from PWM Register values
1 = Enable CLA input (Default)

Bit 0: PWM_EN – PWM Processing Enable

0 = Disable PWM module, outputs zero (Default)
1 = Enable PWM operation

8.2 DPWM Control Register 1 (DPWMCTRL1)

Address 00050004 – DPWM 3 Control Register 1
Address 00070004 – DPWM 2 Control Register 1
Address 000A0004 – DPWM 1 Control Register 1
Address 000D0004 – DPWM 0 Control Register 1

Bit Number	31	30	29	28
Bit Name	PRESET_EN	SYNC_FET_EN	BURST_EN	CLA_DUTY_ADJ_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	27:24	23:21	20	19
Bit Name	SYNC_OUT_DIV_SEL	CLA_SCALE	EXT_SYNC_EN	CBC_BSIDE_ACTIVE EN
Access	R/W	R/W	R/W	R/W
Default	0000	000	0	0

Bit Number	18	17:16	15	14
Bit Name	AUTO_MODE_SEL	EVENT_UP_SEL	CHECK_OVERRIDE	GLOBAL_PERIOD_EN
Access	R/W	R/W	R/W	R/W
Default	0	01	1	0

Bit Number	13	12	11	10	9
Bit Name	PWM_B_OE	PWM_A_OE	GPIO_B_VAL	GPIO_B_EN	GPIO_A_VAL
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	8	7	6	5
Bit Name	GPIO_A_EN	PWM_HR_MULTI_OUT_EN	SFRAME_EN	PWM_B_PROT_DIS
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	4	3:2	1	0
Bit Name	PWM_A_PROT_DIS	HIRES_SCALE	ALL_PHASE_CLK_ENA	HIRES_DIS
Access	R/W	R/W	R/W	R/W
Default	0	00	1	0

Bit 31: PRESET_EN – Counter Preset Enable
0 = Counter reset to 0 upon detection of sync (Default)
1 = Counter preset to Preset Count Value upon detection of sync
Bit 30: SYNC_FET_EN – SyncFET Mode Enabled
0 = SyncFET Mode Disabled (Default)
1 = SyncFET Mode Enabled (Default)
Bit 29: BURST_EN – Burst (Light Load) Mode Detection Enable
0 = Burst Mode (Light Load) Detection disabled (Default)
1 = Burst Mode (Light Load) Detection enabled
Bit 28: CLA_DUTY_ADJ_EN – Enables CLA Duty Adjust from Current/Flux Balancing
0 = CLA Duty Adjust not enabled (Default)
1 = CLA Duty Adjust enabled

Bits 27-24: SYNC_OUT_DIV_SEL – Sets the divider for generating the Sync Out pulse.
0000 = Sync Out generated on every switching cycle (Default)
0001 = Sync Out generated once every 2 switching cycles
0010 = Sync Out generated once every 3 switching cycles
…….
1111 = Sync Out generated once every 16 switching cycles

Bits 23-21: CLA_SCALE – Scaling for CLA Input Data
000 = CLA Value (Default)
001 = CLA Value multiplied by 2
010 = CLA Value divided by 2
011 = CLA Value multiplied by 4
100 = CLA Value divided by 4
101 = CLA Value multiplied by 8
110 = CLA Value divided by 8
111 = CLA Value

Bit 20: EXT SYNC_EN – Slave DPWM to external sync
0 = DPWM not synchronized to external sync (Default)
1 = Slave DPWM to external sync

Bit 19: CBC_BSIDE_ACTIVE_EN – Sets if CBC responds to Fault CBC when PWM-B is active, only available in Multi and Reson modes
0 = Response to Fault CBC when PWM-A active (Default)
1 = Response to Fault CBC when PWM-A or PWM-B active

Bit 18: AUTO_MODE_SEL – Auto Switching Mode Select
0 = Auto Switching Mode disabled (Default)
1 = Auto Switching Mode enabled

Bits 17-16: EVENT_UP_SEL – Update End Period Mode
00 = Events updated anytime
01 = Events updated at End of Period (Default)
10 = Events updated at count value equal to Sample Trigger 2 register
11 = Events updated at End of Period and Sample Trigger 2 position

Bit 15: CHECK_OVERRIDE – PWM Check Override
0 = DPWM checks mathematical settings within module, correct placement of Event settings/period settings. Invalid configurations are not allowed.
1 = Overrides checking for invalid configurations and turns off PWM mathematical checking functions (Default)

Bit 14: GLOBAL_PERIOD_EN
0 = Event calculations use DPWM Period register (Default)
1 = Event calculations use Global Period register

Bit 13: PWM_B_OE – Direction for PWM B pin
0 = PWM B configured as output (Default)
1 = PWM B configured as input

Bit 12: PWM_A_OE – Direction for PWM A pin
0 = PWM A configured as output (Default)
1 = PWM A configured as input

Bit 11: GPIO_B_VAL – Sets value of PWM B output in GPIO mode
0 = PWM B driven low in GPIO mode (Default)
1 = PWM B driven high in GPIO mode

Bit 10: GPIO_B_EN – Enables GPIO mode for PWM B output
0 = PWM B in DPWM mode (Default)
1 = PWM B in GPIO mode

Bit 9: GPIO_A_VAL – Sets value of PWM A output in GPIO mode
0 = PWM A driven low in GPIO mode (Default)
1 = PWM A driven high in GPIO mode

Bit 8: GPIO_A_EN – Enables GPIO mode for PWM A output

0 = PWM A in DPWM mode (Default)
1 = PWM A in GPIO mode

Bit 7: PWM_HR_MULT_OUT_EN – Control bit for Hi-Res Block
0 = Disabled (Default)
1 = Enabled

Bit 6: SFRAME_EN – PWM Single Step Frame Mode Enable
0 = Disable Single Frame Mode (Default)
1 = Enable Single Step Frame Mode. One EADC sample is requested, CLA then Filters, then one PWM duty cycle performed, then wait on Single Frame Trigger toggle before advancing to next frame.

Bit 5: PWM_B_PROT_DIS – PWM B Asynchronous Protection Disable
0 = Allows asynchronous protection to turn off PWM B Output (Default)
1 = Disables asynchronous protection from turning off PWM B Output

Bit 4: PWM_A_PROT_DIS – PWM A Asynchronous Protection Disable
0 = Allows asynchronous protection to turn off PWM A Output (Default)
1 = Disables asynchronous protection from turning off PWM A Output

Bits 3-2: HIRES_SCALE – Determines resolution of high resolution steps
00 = Resolution of 16 phases. Full resolution enabled. Resolution step = PCLK/16 (Default)
11 = Resolution of 2 phases. Resolution step = PCLK/2
10 = Resolution of 4 phases. Resolution step = PCLK/4
01 = Resolution of 8 phases. Resolution step = PCLK/8
00 = Resolution of 16 phases. Full Resolution enabled. Resolution step = PCLK/16

Bit 1: ALL_PHASE_CLK_EN – High Speed Oscillator Phase Enable
0 = Enables only required phases of clock when needed
1 = Enables all phases of high resolution clock from oscillator (Default)

Bit 0: HIRES_DIS – PWM High Resolution Disable
0 **=** Enable High Resolution logic (Default)
1 **=** Disable High Resolution logic

8.3 DPWM Control Register 2 (DPWMCTRL2)

Address 00050008 – DPWM 3 Control Register 2
Address 00070008 – DPWM 2 Control Register 2
Address 000A0008 – DPWM 1 Control Register 2
Address 000D0008 – DPWM 0 Control Register 2

Bit Number	15:12	11	10
Bit Name	SYNC_IN_DIV_RATIO	Reserved	RESON_DEADTIME_COMP_EN
Access	R/W	-	R/W
Default	0000	0	0

Bit Number	9:8	7	6
Bit Name	FILTER_DUTY_SEL	IDE_DUTY_B_EN	RESERVED
Access	R/W	R/W	-
Default	00	0	0

Bit Number	5:4	3:2
Bit Name	SAMPLE_TRIG1_OVERSAMPLE	SAMPLE_TRIG1_MODE
Access	R/W	R/W
Default	00	00

Bit Number	1	0
Bit Name	SAMPLE_TRIG_2_EN	SAMPLE_TRIG_1_EN
Access	R/W	R/W
Default	0	1

Bits 15-12: SLAVE_SYNC_IN_DIV_RATIO – Sets the number of syncs to be masked before a resync

Bit 10: RESON_DEADTIME_COMP_EN – Sets the method at which High Side CLA-Duty is used in calculations

0 = CLA Duty from Filter (Default)
1 = CLA Duty from Filter minus deadtime adjustment

Bits 9-8: FILTER_DUTY_SEL – Sets which register is sent to the Resonant Duty input of the Filter. Settings of 0 and 1 enable the 16 bit signed value of the Resonant Duty register to be added to the Filter Period value for period adjustment in resonant mode.

0 = PWM Period Register (Default)
1 = Event 2
2 = DPWM Resonant Duty Register (Bits 13:0)

Bit 7: IDE_DUTY_B_EN – IDE Duty Cycle Side B Enable

0 = Disabled (Default)
1 = Enabled

Bits 5-4: SAMPLE_TRIG1_OVERSAMPLE – Oversample Select for Sample Trigger 1

00 = Trigger an EADC Sample at PWM Sample Trig Register value (Default)
01 = Trigger an EADC Sample at PWM Sample Trig Register value and at PWM Sample Trig Register value divided by 2
10 = Trigger a EADC Sample at PWM Sample Trig Register value, at PWM Sample Trig Register value divided by 2 and at PWM Sample Trig Register value divided by 4
11 = Trigger a EADC Sample at PWM Sample Trig Register value, at PWM Sample Trig Register value divided by 2, at PWM Sample Trig Register value divided by 4 and at PWM Sample Trig Register value divided by 8

Bits 3-2: SAMPLE_TRIG1_MODE – Mode select for Sample Trigger 1

00 = Trigger value is set using PWM Sample Trig Register value (Default)
01 = Trigger value is adaptive midpoint (EV1+CLA_DUTY/2 + Adaptive Offset) and uses current CLA value at update event
10 = Trigger value is adaptive midpoint (EV1+CLA_DUTY/2 + Adaptive Offset) and uses previous CLA value at update event
11 = Trigger value is adaptive midpoint (EV1+CLA_DUTY + Fixed offset + Adaptive Offset) and uses current CLA value at update event

Bit 1: SAMPLE_TRIG_2_EN – Sample Trigger 2 Enable
0 = Disable Sample Trigger 2 (Default)
1 = Enable Sample Trigger 2

Bit 0: SAMPLE_TRIG_1_EN – Sample Trigger 1 Enable
0 = Disable Sample Trigger 1
1 = Enable Sample Trigger 1 (Default)

8.4 DPWM Period Register (DPWMPRD)

Address 0005000C – DPWM 3 Period Register
Address 0007000C – DPWM 2 Period Register
Address 000A000C – DPWM 1 Period Register
Address 000D000C – DPWM 0 Period Register

Bit Number	17:4	3:0
Bit Name	PRD	RESERVED
Access	R/W	-
Default	00_0011_0100_0001	0000

Bits 17-4: PRD – PWM Period. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.5 DPWM Event 1 Register (DPWMEV1)

Address 00050010 – DPWM 3 Event 1 Register
Address 00070010 – DPWM 2 Event 1 Register
Address 000A0010 – DPWM 1 Event 1 Register
Address 000D0010 – DPWM 0 Event 1 Register

Bit Number	17:4	3:0
Bit Name	EVENT1	RESERVED
Access	R/W	-
Default	00_0000_0001_0100	0000

Bits 17-4: EVENT1 – Configures the location of Event 1. Low resolution register, last 4 bits are unused. Refer to DPWM app note for additional information.
Bits 3-0: RESERVED – Unused bits

8.6 DPWM Event 2 Register (DPWMEV2)

Address 00050014 – DPWM 3 Event 2 Register
Address 00070014 – DPWM 2 Event 2 Register
Address 000A0014 – DPWM 1 Event 2 Register
Address 000D0014 – DPWM 0 Event 2 Register

Bit Number	17:0
Bit Name	EVENT2
Access	R/W
Default	0_0000_0011_0000_0000

Bits 17-0: EVENT2 – Configures the location of Event 2. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0 (dependent on Bits 3:2 of DPWM Control Register 2). Refer to DPWM app note for additional information.

8.7 DPWM Event 3 Register (DPWMEV3)

Address 00050018 – Loop 4 DPWM Event 3 Register
Address 00070018 – Loop 3 DPWM Event 3 Register
Address 000A0018 – Loop 2 DPWM Event 3 Register
Address 000D0018 – Loop 1 DPWM Event 3 Register

Bit Number	17:0
Bit Name	EVENT3
Access	R/W
Default	00_0000_0011_1110_0000

Bits 17-0: EVENT3 – Configures the location of Event 3. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0. Refer to DPWM app note for additional information.

8.8 DPWM Event 4 Register (DPWMEV4)

Address 0005001C – Loop 4 DPWM Event 4 Register
Address 0007001C – Loop 3 DPWM Event 4 Register
Address 000A001C – Loop 2 DPWM Event 4 Register
Address 000D001C – Loop 1 DPWM Event 4 Register

Bit Number	17:0
Bit Name	EVENT4
Access	R/W
Default	00_0000_0111_0000_0000

Bits 17-0: EVENT4 – Configures the location of Event 4. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0. Refer to DPWM app note for additional information.

8.9 DPWM Sample Trigger 1 Register (DPWMSAMPTRIG1)

Address 00050020 – DPWM 3 Sample Trigger 1 Register
Address 00070020 – DPWM 2 Sample Trigger 1 Register
Address 000A0020 – DPWM 1 Sample Trigger 1 Register
Address 000D0020 – DPWM 0 Sample Trigger 1 Register

Bit Number	17:6	5:0
Bit Name	SAMPLE_TRIGGER	RESERVED
Access	R/W	-
Default	0000_0010_0000	00_0000

Bits 17-6: SAMPLE_TRIGGER – Configures the location of the sample trigger within a PWM period. Value equals the number of PCLK clock periods. Enables start of conversion for EADC. Refer to DPWM app note for additional information. Low resolution register, last 6 bits are read-only.
Bits 5-0: RESERVED – Unused bits

8.10 DPWM Sample Trigger 2 Register (DPWMSAMPTRIG2)

Address 00050024 – DPWM 3 Sample Trigger 1 Register
Address 00070024 – DPWM 2 Sample Trigger 1 Register
Address 000A0024 – DPWM 1 Sample Trigger 1 Register
Address 000D0024 – DPWM 0 Sample Trigger 1 Register

Bit Number	17:6	5:0
Bit Name	SAMPLE_TRIGGER	RESERVED
Access	R/W	-
Default	0000_0010_0000	00_0000

Bits 17-6: SAMPLE_TRIGGER – Configures the location of the sample trigger within a PWM period. Value equals the number of PCLK clock periods. Enables start of conversion for EADC. Refer to DPWM app note for additional information. Low resolution register, last 6 bits are read-only.
Bits 5-0: RESERVED – Unused bits

8.11 DPWM Phase Trigger Register (DPWMPHASETRIG)

Address 00050028 – DPWM 3 Phase Trigger Register
Address 00070028 – DPWM 2 Phase Trigger Register
Address 000A0028 – DPWM 1 Phase Trigger Register
Address 000D0028 – DPWM 0 Phase Trigger Register

Bit Number	17:4	3:0
Bit Name	PHASE_TRIGGER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bits 17-4: PHASE_TRIGGER – Configures the phase trigger delay within multi-output mode. Value equals the number of PCLK clock periods. Refer to DPWM app note for additional information. Low resolution register, last 4 bits are read-only
Bits 3-0: RESERVED – Unused bits

8.12 DPWM Cycle Adjust A Register (DPWMCYCADJA)

Address 0005002C – DPWM 3 Cycle Adjust A Register
Address 0007002C – DPWM 2 Cycle Adjust A Register
Address 000A002C – DPWM 1 Cycle Adjust A Register
Address 000D002C – DPWM 0 Cycle Adjust A Register

Bit Number	15:0
Bit Name	CYCLE_ADJUST_A
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: CYCLE_ADJUST_A – Adjusts PWM A output signal. 16-bit signed number allows output signal to be delayed or sped up. Refer to DPWM app note for additional information.

8.13 DPWM Cycle Adjust B Register (DPWMCYCADJB)

Address 00050030 – DPWM 3 Cycle Adjust B Register
Address 00070030 – DPWM 2 Cycle Adjust B Register
Address 000A0030 – DPWM 1 Cycle Adjust B Register
Address 000D0030 – DPWM 0 Cycle Adjust B Register

Bit Number	15:0
Bit Name	CYCLE_ADJUST_B
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: CYCLE_ADJUST_B – Adjusts the PWM B output signal. 16-bit signed number allows output signal to be delayed or sped up. Refer to DPWM app note for additional information.

8.14 DPWM Resonant Duty Register (DPWMRESDUTY)

Address 00050034 – DPWM 3 Resonant Duty Register
Address 00070034 – DPWM 2 Resonant Duty Register
Address 000A0034 – DPWM 1 Resonant Duty Register
Address 000D0034 – DPWM 0 Resonant Duty Register

Bit Number	15:0
Bit Name	RESONANT_DUTY
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: RESONANT_DUTY – Controls the DPWM duty. 16-bit signed number is used as a Filter Output Multiplier in Resonant Mode.

8.15 DPWM Fault Control Register (DPWMFLTCTRL)

Bit Number	31	30	29	28:24
Bit Name	ALL_FAULT_EN	CBC_FAULT_EN	RESERVED	CBC_MAX_COUNT
Access	R/W	R/W	-	R/W
Default	0	0	00	0_0000

Bit Number	23:21	20:16	15:13	12:8

Bit Name	RESERVED	AB_MAX_COUNT	RESERVED	B_MAX_COUNT
Access	-	R/W	-	R/W
Default	000	0_0000	000	0_0000

Bit Number	7:5	4:0
Bit Name	RESERVED	A_MAX_COUNT
Access	-	R/W
Default	000	0_0000

Bit 31: ALL_FAULT_EN – DPWM Fault Module enable
0 = All DPWM Fault Modules disabled (Default)
1 = All DPWM Fault Modules enabled
Bit 30: CBC_FAULT_EN – Cycle by cycle Fault Enable
0 = Cycle by cycle just shortens DPWM pulses
1 = Consecutive cycle by cycle events beyond CBC_MAX_COUNT will cause the DPWM to shut off as with any other fault.
Bit 29: RESERVED – Unused bit
Bits 28-24: CBC_MAX_COUNT – Cycle-by-Cycle Fault Count, sets the number of received sequential faults on Cycle-by-Cycle Fault input before asserting the fault
Bits 23-21: RESERVED – Unused bits
Bits 20-16: AB_MAX_COUNT – Fault AB Count, sets the number of received sequential faults on Fault AB input before asserting the fault
Bits 15-13: RESERVED – Unused bits
Bits 12-8: B_MAX_COUNT – Fault B Count, sets the number of received sequential faults on Fault B input before asserting the fault
Bits 7-5: RESERVED – Unused bits
Bits 4-0: A_MAX_COUNT – Fault A Count, sets the number of received sequential faults on Fault A input before asserting the fault

8.16 DPWM Overflow Register (DPWMOVERFLOW)

Address 0005003C – DPWM 3 Overflow Register
Address 0007003C – DPWM 2 Overflow Register
Address 000A003C – DPWM 1 Overflow Register
Address 000D003C – DPWM 0 Overflow Register

Bit Number	7	6	5	4	3:0
Bit Name	PWM_B_CHECK	PWM_A_CHECK	GPIO_B_IN	GPIO_A_IN	OVERFLOW
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit 7: PWM_B_CHECK – Value of PWM B internal check
0 = Passed checks
1 = Failed checks (override required to enable output)
Bit 6: PWM_A_CHECK – Value of PWM B input
0 = Passed check
1 = Failed check (override required to enable output)
Bit 5: GPIO_B_IN0 – Value of PWM B input
0 = Low signal on PWM B
1 = High signal on PWM B
Bit 4: GPIO_A_IN – Value of PWM A input
0 = Low signal on PWM A
1 = High value on PWM A
Bit 3: OVERFLOW – PWM Event 4 Overflow Status
0 = CLA Event 4 has not overflowed
1 = Overflow condition found on CLA Event 4
Bit 2: OVERFLOW[2] – CLA Event 4 Overflow Status
0 = PWM Event 4 has not overflowed
1 = Overflow condition found on PWM Event 4
Bit 1: OVERFLOW[1] – CLA Event 3 Overflow Status
0 = CLA Event 3 has not overflowed
1 = Overflow condition found on CLA Event 3
Bit 0: OVERFLOW[0] – CLA Event 2 Overflow Status
0 = CLA Event 2 has not overflowed
1 = Overflow condition found on CLA Event 2

8.17 DPWM Interrupt Register (DPWMINT)

Address 00050040 – DPWM 3 Interrupt Register
Address 00070040 – DPWM 2 Interrupt Register
Address 000A0040 – DPWM 1 Interrupt Register
Address 000D0040 – DPWM 0 Interrupt Register

Bit Number	22	21	20	19	18	17	16
Bit Name	MODE_SWITCH	FLT_A	FLT_B	FLT_AB	FLT_CBC	PRD	INT
Access	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-

Bit Number	15:12	11	10
Bit Name	RESERVED	MODE_SWITCH_FLAG_CLR	MODE_SWITCH_FLAG_EN
Access	-	R/W	R/W
Default	0000	0	0

Bit Number	9	8	7
Bit Name	MODE_SWITCH_INT_EN	FLT_A_INT_EN	FLT_B_INT_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	6	5	4	3:0
Bit Name	FLT_AB_INT_EN	FLT_CBC_INT_EN	PRD_INT_EN	PRD_INT_SCALE
Access	R/W	R/W	R/W	R/W
Default	0	0	0	1111

Bit 22: MODE_SWITCH – Mode Switching Flag
0 = Flag is not asserted
1 = Flag is set
Bit 21: FLT_A – Fault A Flag
0 = Flag is not asserted
1 = Flag is set
Bit 20: FLT_B – Fault B Flag
0 = Flag is not asserted
1 = Flag is set
Bit 19: FLT_AB – Fault AB Flag
0 = Flag is not asserted
1 = Flag is set
Bit 18: FLT_CBC – Fault Cycle-by-Cycle Flag
0 = Flag is not asserted
1 = Flag is set
Bit 17: PRD – PWM Period Interrupt Flag
0 = PWM Period Interrupt Flag is not asserted
1 = PWM Period Interrupt Flag is set
Bit 16: INT– Interrupt Out
0 = INT is not asserted
1 = INT is set
Bits 15-12: RESERVED – Unused bits
Bit 11: MODE_SWITCH_FLAG_CLR– Mode Switching Flag Clear
0 = (Default)
1 = Risedge 0-1 clears flag generated.

Bit 10: MODE_SWITCH_FLAG_EN– Mode Switching Flag Enable
0 = Disables generation of flag for Mode Switching (Default)
1 = Enables generation of flag for Mode Switching.
Bit 9: MODE_SWITCH_INT_EN – Mode Switching Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 8: FLT_A_INT_EN – Fault A Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 7: FLT_B_INT_EN – Fault B Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 6: FLT_AB_INT_EN – Fault AB Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 5: FLT_CBC_INT_EN – Fault Cycle-by-Cycle Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 4: PRD_INT_EN – PWM Period Interrupt Enable
0 = Disables generation of periodic PWM interrupt (Default)
1 = Enables generation of periodic PWM interrupt
Bits 3-0: PRD_INT_SCALE – This value scales the period interrupt signal from an interrupt every switching cycle to 16 switching cycles
0000 = Period Interrupt generated every switching cycle (Default)
0001 = Period Interrupt generated once every 2 switching cycles
0010 = Period Interrupt generated once every 4 switching cycles
0011 = Period Interrupt generated once every 6 switching cycles
0100 = Period Interrupt generated once every 8 switching cycles
0101 = Period Interrupt generated once every 16 switching cycles
0110 = Period Interrupt generated once every 32 switching cycles
0111 = Period Interrupt generated once every 48 switching cycles
1000 = Period Interrupt generated once every 64 switching cycles
1001 = Period Interrupt generated once every 80 switching cycles
1010 = Period Interrupt generated once every 96 switching cycles
1011 = Period Interrupt generated once every 128 switching cycles
1100 = Period Interrupt generated once every 160 switching cycles
1101 = Period Interrupt generated once every 192 switching cycles
1110 = Period Interrupt generated once every 224 switching cycles
1111 = Period Interrupt generated once every 256 switching cycles

8.18 DPWM Counter Preset Register (DPWMCNTPRE)

Address 00050044 – DPWM 3 Counter Preset Register
Address 00070044 – DPWM 2 Counter Preset Register
Address 000A0044 – DPWM 1 Counter Preset Register
Address 000D0044 – DPWM 0 Counter Preset Register

Bit Number	17:4	3:0
Bit Name	PRESET	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: PRESET – Counter preset value, counter reset to this value upon detection of sync when PRESET_EN bit in DPWMCTRL2 is enabled. Low resolution register, last 4 bits are read-only
Bits 3-0: RESERVED – Unused bits

8.19 DPWM Blanking A Begin Register (DPWMBLKABEG)

Address 00050048 – DPWM 3 Blanking A Begin Register
Address 00070048 – DPWM 2 Blanking A Begin Register
Address 000A0048 – DPWM 1 Blanking A Begin Register
Address 000D0048 – DPWM 0 Blanking A Begin Register

Bit Number	17:4	3:0
Bit Name	BLANK_A_BEGIN	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_A_BEGIN – Configures start of Comparator Blanking Window for PWM A**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.20 DPWM Blanking A End Register (DPWMBLKAEND)

Address 0005004C – DPWM 3 Blanking A End Register
Address 0007004C – DPWM 2 Blanking A End Register
Address 000A004C – DPWM 1 Blanking A End Register
Address 000D004C – DPWM 0 Blanking A End Register

Bit Number	17:4	3:0
Bit Name	BLANK_A_END	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_A_END – Configures end of Comparator Blanking Window for PWM A**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.21 DPWM Blanking B Begin Register (DPWMBLKBBEG)

Address 00050050 – DPWM 3 Blanking B Begin Register
Address 00070050 – DPWM 2 Blanking B Begin Register
Address 000A0050 – DPWM 1 Blanking B Begin Register
Address 000D0050 – DPWM 0 Blanking B Begin Register

Bit Number	17:4	3:0
Bit Name	BLANK_B_BEGIN	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_B_BEGIN – Configures start of Comparator Blanking Window for PWM B**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.22 DPWM Blanking B End Register (DPWMBLKBEND)

Address 00050054 – DPWM 3 Blanking B End Register
Address 00070054 – DPWM 2 Blanking B End Register
Address 000A0054 – DPWM 1 Blanking B End Register
Address 000D0054 – DPWM 0 Blanking B End Register

Bit Number	17:4	3:0
Bit Name	BLANK_B_END	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_B_END – Configures end of Comparator Blanking Window for PWM B**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.23 DPWM Minimum Duty Cycle High Register (DPWMMINDUTYHI)

Address 00050058 – DPWM 3 Minimum Duty Cycle High Register
Address 00070058 – DPWM 2 Minimum Duty Cycle High Register
Address 000A0058 – DPWM 1 Minimum Duty Cycle High Register
Address 000D0058 – DPWM 0 Minimum Duty Cycle High Register

Bit Number	17:4	3: 0
Bit Name	MIN_DUTY_HIGH	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: MIN_DUTY_HIGH– Configures upper threshold for minimum duty cycle logic. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.24 DPWM Minimum Duty Cycle Low Register (DPWMMINDUTYLO)

Address 0005005C – DPWM 3 Minimum Duty Cycle Low Register
Address 0007005C – DPWM 2 Minimum Duty Cycle Low Register
Address 000A005C – DPWM 1 Minimum Duty Cycle Low Register
Address 000D005C – DPWM 0 Minimum Duty Cycle Low Register

Bit Number	17:4	3: 0
Bit Name	MIN_DUTY_LOW	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: MIN_DUTY_LOW– Configures lower threshold for minimum duty cycle logic. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.25 DPWM Adaptive Sample Register (DPWMADAPTIVE)

Address 00050060 – DPWM 3 Adaptive Sample Register
Address 00070060 – DPWM 2 Adaptive Sample Register
Address 000A0060 – DPWM 1 Adaptive Sample Register
Address 000D0060 – DPWM 0 Adaptive Sample Register

Bit Number	13:0
Bit Name	ADAPT_SAMP
Access	R/W
Default	00_0000_0000_0000

Bit 13-0: ADAPT_SAMP – Configures Adaptive Sample Adjust

8.26 DPWM Fault Status (DPWMFLTSTAT)

Address 00050064 – DPWM 3 Fault Input Status Register
Address 00070064 – DPWM 2 Fault Input Status Register
Address 000A0064 – DPWM 1 Fault Input Status Register
Address 000D0064 – DPWM 0 Fault Input Status Register

Bit Number	5	4	3	2	1	0
Bit Name	BURST	IDE_DETECT	FLT_A	FLT_B	FLT_AB	FLT_CBC
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit 5: BURST – Burst Mode Detection Status
0 = Burst Mode Detection is not asserted
1 = Burst Mode Detection is set
Bit 4: IDE_DETECT – IDE Detection Status (from Analog Comparators)
0 = IDE Detection is not asserted
1 = IDE Detection is set
Bit 3: FLT_A – Fault A Detection Status
0 = Fault A Detection is not asserted
1 = Fault A Detection is set
Bit 2: FLT_B – Fault B Detection Status
0 = Fault B Detection is not asserted
1 = Fault B Detection is set

Bit 1: FLT_AB – Fault AB Detection Status
0 = Fault AB Detection is not asserted
1 = Fault AB Detection is set
Bit 0: FLT_CBC – Current Limit Detection Status
0 = Current Limit Detection is not asserted
1 = Current Limit Detection is set

8.27 DPWM Auto Switch High Upper Thresh Register (DPWMAUTOSWHIUPTHRESH)

Address 00050068 – DPWM 3 Auto Switch High Upper Thresh Register
Address 00070068 – DPWM 2 Auto Switch High Upper Thresh Register
Address 000A0068 – DPWM 1 Auto Switch High Upper Thresh Register
Address 000D0068 – DPWM 0 Auto Switch High Upper Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_HIGH_UPPER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: AUTO_SWITCH_HIGH_UPPER– Configures upper threshold for Auto Switch Mode High operation. Mode switching does not occur between Auto Switch High Upper and Auto Switch High Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.28 DPWM Auto Switch High Lower Thresh Register (DPWMAUTOSWHILOWTHRESH)

Address 0005006C – DPWM 3 Auto Switch High Lower Thresh Register
Address 0007006C – DPWM 2 Auto Switch High Lower Thresh Register
Address 000A006C – DPWM 1 Auto Switch High Lower Thresh Register
Address 000D006C – DPWM 0 Auto Switch High Lower Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_HIGH_LOWER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: AUTO_SWITCH_HIGH_LOWER– Configures lower threshold for Auto Switch Mode High operation. Mode switching does not occur between Auto Switch High Upper and Auto Switch High Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.29 DPWM Auto Switch Low Upper Thresh Register (DPWMAUTOSWLOUPTHRESH)

Address 00050070 – DPWM 3 Auto Switch Low Upper Thresh Register
Address 00070070 – DPWM 2 Auto Switch Low Upper Thresh Register
Address 000A0070 – DPWM 1 Auto Switch Low Upper Thresh Register
Address 000D0070 – DPWM 0 Auto Switch Low Upper Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_LOW_UPPER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 29-16: AUTO_SWITCH_LOW_UPPER– Configures upper threshold for Auto Switch Mode Low operation. Mode switching does not occur between Auto Switch Low Upper and Auto Switch Low Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.30 DPWM Auto Switch Low Lower Thresh Register (DPWMAUTOSWLOLOWTHRESH)

Address 00050074 – DPWM 3 Auto Switch Low Lower Thresh Register
Address 00070074 – DPWM 2 Auto Switch Low Lower Thresh Register
Address 000A0074 – DPWM 1 Auto Switch Low Lower Thresh Register
Address 000D0074 – DPWM 0 Auto Switch Low Lower Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_LOW_LOWER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 29-16: AUTO_SWITCH_LOW_LOWER– Configures lower threshold for Auto Switch Mode Low operation. Mode switching does not occur between Auto Switch Low Upper and Auto Switch Low Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

8.31 DPWM Auto Config Max Register (DPWMAUTOMAX)

Address 00050078 – DPWM 3 Auto Config Max Register
Address 00070078 – DPWM 2 Auto Config Max Register
Address 000A0078 – DPWM 1 Auto Config Max Register
Address 000D0078 – DPWM 0 Auto Config Max Register

Bit Number	31:28	27:24	23
Bit Name	PWM_B_INTRA_MUX	PWM_A_INTRA_MUX	CBC_PWM_C_EN
Access	R/W	R/W	R/W
Default	000	000	000

Bit Number	22	21	20
Bit Name	MULTI_MODE_CLA_B_OFF	RESERVED	CBC_PWM_AB_EN
Access	R/W	-	R/W
Default	0	0	0

Bit Number	19	18:17	16
Bit Name	CBC_ADV_CNT_EN	RESERVED	MASTER_SYNC_CNTL_SEL
Access	R/W	-	R/W
Default	0	00	0

Bit Number	15:14	13	12
Bit Name	RESERVED	CBC_SYNC_CUR_LIMIT_EN	RESON_MODE_FIXED_DUTY_EN
Access	-	R/W	R/W
Default	00	0	0

Bit Number	11:7	6:4	3:2	1	0
Bit Name	RESERVED	PWM_MODE	RESERVED	CLA_EN	RESERVED
Access	-	R/W	-	R/W	-
Default	0000_0	000	00	0	0

Bits 31-28: PWM_B_INTRA_MUX – Interchanges DPWM signals post edge generation
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bits 27-24: PWM_A_INTRA_MUX – Combines DPWM signals are prior to HR module
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A

5 = Pass-through below B
6 = Pass-through below C
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bit 23: CBC_PWM_C_EN – Sets if Fault CBC changes output waveform for PWM-C
0 = PWM-C unaffected by Fault CBC (Default)
1 = PWM-C affected by Fault CBC

Bit 22: MULTI_MODE_CLA_B_OFF – Configures control of PWM B output in Multi-Output Mode when CLA_ENABLE is asserted
0 = PWM B pulse width controlled by Filter Calculation (Default)
1 = PWM B pulse width controlled by Event3 and Event4 registers

Bit 21: RESERVED – Unused Bit

Bit 20: CBC_PWM_AB_EN – Sets if Fault CBC changes output waveform for PWM-A and PWM-B
0 **=** PWM-A and PWM-B unaffected by Fault CBC (Default)
1 **=** PWM-A and PWM-B affected by Fault CBC

Bit 19: CBC_ADV_CNT_EN – Selects cycle-by-cycle of operation
Normal Mode
0 = CBC disabled (Default)
1 = CBC enabled
Multi and Resonant Modes
0 = PWM-A and PWM-B operate independently (Default)
1 = PWM-A and PWM-B pulse matching enabled

Bits 18-17: RESERVED – Unused Bits

Bit 16: MASTER_SYNC_CNTL_SEL – Configures master sync location
0 = Master Sync controlled by Phase Trigger Register (Default)
1 = Master Sync controlled by CLA value

Bits 15-14: RESERVED – Unused Bits

Bit 13: CBC_SYNC_CUR_LIM_EN – Sets how current limit affects slave sync
0 = Slave sync is unaffected during current limit (Default)
1 = Slave sync is advanced during current limit.

Bit 12: RESON_MODE_FIXED_DUTY_EN – Configures how duty cycle is controlled in Resonance Mode
0 = Resonant mode duty cycle set by Filter duty (Default)
1 = Resonant mode duty cycle set by Auto Switch High Register

Bits 11-7: RESERVED – Unused Bits

Bits 6-4: PWM_MODE – DPWM Mode
0 = Normal Mode (Default)
1 = Resonant Mode
2 = Multi-Output Mode
3 = Triangular Mode
4 = Leading Mode

Bits 3-2: RESERVED – Unused Bits

Bit 1: CLA_EN– CLA Processing Enable
0 = Generate PWM waveforms from PWM Register values (Default)
1 = Enable CLA input

Bit 0: RESERVED – Unused bit

8.32 DPWM Auto Config Mid Register (DPWMAUTOMID)

Address 0005007C – DPWM 3 Auto Config Mid Register
Address 0007007C – DPWM 2 Auto Config Mid Register
Address 000A007C – DPWM 1 Auto Config Mid Register
Address 000D007C – DPWM 0 Auto Config Mid Register

Bit Number	31:28	27:24	23

Bit Name	PWM_B_INTRA_MUX	PWM_A_INTRA_MUX	CBC_PWM_C_EN
Access	R/W	R/W	R/W
Default	000	000	000

Bit Number	22	21	20
Bit Name	MULTI_MODE_CLA_B_OFF	RESERVED	CBC_PWM_AB_EN
Access	R/W	-	R/W
Default	0	0	0

Bit Number	19	18:17	16
Bit Name	CBC_ADV_CNT_EN	RESERVED	MASTER_SYNC_CNTL_SEL
Access	R/W	-	R/W
Default	0	00	0

Bit Number	15:14	13	12
Bit Name	RESERVED	CBC_SYNC_CUR_LIMIT_EN	RESON_MODE_FIXED_DUTY_EN
Access	-	R/W	R/W
Default	00	0	0

Bit Number	11:7	6:4	3:2	1	0
Bit Name	RESERVED	PWM_MODE	RESERVED	CLA_EN	RESERVED
Access	-	R/W	-	R/W	-
Default	0000_0	000	00	1	0

Bits 31-28: PWM_B_INTRA_MUX – Interchanges DPWM signals post edge generation
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bits 27-24: PWM_A_INTRA_MUX – Combines DPWM signals are prior to HR module
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bit 23: CBC_PWM_C_EN – Sets if Fault CBC changes output waveform for PWM-C
0 = PWM-C unaffected by Fault CBC (Default)
1 = PWM-C affected by Fault CBC

Bit 22: MULTI_MODE_CLA_B_OFF – Configures control of PWM B output in Multi-Output Mode when CLA_ENABLE is asserted
0 = PWM B pulse width controlled by Filter Calculation (Default)
1 = PWM B pulse width controlled by Event3 and Event4 registers
Bit 21: RESERVED – Unused Bit
Bit 20: CBC_PWM_AB_EN – Sets if Fault CBC changes output waveform for PWM-A and PWM-B
0 **=** PWM-A and PWM-B unaffected by Fault CBC (Default)
1 **=** PWM-A and PWM-B affected by Fault CBC
Bit 19: CBC_ADV_CNT_EN – Selects cycle-by-cycle of operation
Normal Mode
0 = CBC disabled (Default)
1 = CBC enabled
Multi and Resonant Modes
0 = PWM-A and PWM-B operate independently (Default)
1 = PWM-A and PWM-B pulse matching enabled
Bits 18-17: RESERVED – Unused Bits
Bit 16: MASTER_SYNC_CNTL_SEL – Configures master sync location
0 = Master Sync controlled by Phase Trigger Register (Default)
1 = Master Sync controlled by CLA value
Bits 15-14: RESERVED – Unused Bits
Bit 13: CBC_SYNC_CUR_LIM_EN – Sets how current limit affects slave sync
0 = Slave sync is unaffected during current limit (Default)
1 = Slave sync is advanced during current limit.
Bit 12: RESON_MODE_FIXED_DUTY_EN – Configures how duty cycle is controlled in Resonance Mode
0 = Resonant mode duty cycle set by Filter duty (Default)
1 = Resonant mode duty cycle set by Auto Switch High Register
Bits 11-7: RESERVED – Unused Bits
Bits 6-4: PWM_MODE – DPWM Mode
0 = Normal Mode (Default)
1 = Resonant Mode
2 = Multi-Output Mode
3 = Triangular Mode
4 = Leading Mode
Bits 3-2: RESERVED – Unused Bits
Bit 1: CLA_EN– CLA Processing Enable
0 = Generate PWM waveforms from PWM Register values
1 = Enable CLA input (Default)
Bit 0: RESERVED – Unused bit

8.33 DPWM Edge PWM Generation Control Register (DPWMEDGEGEN)

Address 00050080 – DPWM 3 Edge PWM Generation Control Register
Address 00070080 – DPWM 2 Edge PWM Generation Control Register
Address 000A0080 – DPWM 1 Edge PWM Generation Control Register
Address 000D0080 – DPWM 0 Edge PWM Generation Control Register

Bit Number	16	15	14:12	11
Bit Name	EDGE_EN	RESERVED	A_ON_EDGE	RESERVED
Access	R/W	-	R/W	-
Default	0	0	000	0

Bit Number	10:8	7	6:4	3	2:0

Bit Name	A_OFF_EDGE	RESERVED	B_ON_EDGE	RESERVED	B_OFF_EDGE
Access	R/W	-	R/W	-	R/W
Default	01	0	10	0	11

Bit 16: EDGE_EN – Enables edge generate module. When combining dpwm's, all modules must have this bit enabled.
Bits 14-12: A_ON_EDGE – Select input edge to trigger A ON output edge
0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B
Bit 15: RESERVED – Unused bit
Bits 10-8: A_OFF_EDGE – Select input edge to trigger A OFF output edge
0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B
Bit 7: RESERVED – Unused bit
Bits 6-4: B_ON_EDGE – Select input edge to trigger B ON output edge
0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B
Bit 3: RESERVED – Unused bit
Bit 2-0: B_OFF_EDGE – Select input edge to trigger B OFF output edge
0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B

8.34 DPWM Filter Duty Read Register (DPWMFILTERDUTYREAD)

Address 00050084 – DPWM 3 Filter Duty Read Register
Address 00070084 – DPWM 2 Filter Duty Read Register
Address 000A0084 – DPWM 1 Filter Duty Read Register
Address 000D0084 – DPWM 0 Filter Duty Read Register

Bit Number	17:0
Bit Name	FILTER_DUTY

Access	R
Default	-

Bits 17-0: FILTER_DUTY – Filter Duty value received by DPWM Module

8.35 DPWM BIST Status Register (DPWMBISTSTAT)

Address 00050088 – DPWM 3 BIST Status Register
Address 00070088 – DPWM 2 BIST Status Register
Address 000A0088 – DPWM 1 BIST Status Register
Address 000D0088 – DPWM 0 BIST Status Register

Bit Number	14:0
Bit Name	BIST_CNT
Access	R
Default	-

Bits 14-0: BIST_CNT– BIST Count accumulated during BIST test

9 Front End Control Registers

Registers for Front End Control modules 0-2 are identical in their bit definitions

9.1 Ramp Control Register (RAMPCTRL)

Address 0x0008_0000 – Front End Control 2 Ramp Control Register
Address 0x000B_0000 – Front End Control 1 Ramp Control Register
Address 0x000E_0000 – Front End Control 0 Ramp Control Register

Bit Number	29:16	15:13	12
Bit Name	SYNC_FET_RAMP_START	RESERVED	RAMP_SAT_EN
Access	R/W	-	R/W
Default	00_0000_0000_0000	00	0

Bit Number	11	10	9
Bit Name	RAMP_COMP_INT_EN	RAMP_DLY_INT_EN	PREBIAS_INT_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	8	7	6:5	4
Bit Name	PCM_START_SEL	SYNC_FET_EN	MASTER_SEL	SLAVE_COMP_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	00	0

Bit Number	3	2	1	0
Bit Name	SLAVE_DELAY_EN	CONTROL_EN	FIRMWARE_START	RAMP_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bits 29-16: SYNC_FET_RAMP_START – Provides the starting value for the SyncFET Ramp with a resolution of High Frequency Oscillator Period/bit
Bits 15-13: RESERVED – Unused Bits
Bit 12: RAMP_SAT_EN – Enables addition or subtraction of DAC Saturation Step when EADC is in saturation.

0 = DAC Saturation Step logic is disabled, DAC incremented/decremented by value calculated by Ramp logic when EADC is in saturation (Default)

1 = DAC Saturation Step logic is enabled, DAC incremented/decremented by value stored in DAC Saturation Step register when EADC is in saturation

Bit 11: RAMP_COMP_INT_EN – Enables Ramp I/F Interrupt when soft-start/power-down ramp procedure is complete

0 = Soft-start/Power-Down Ramp Complete Interrupt is disabled (Default)
1 = Soft-start/Power-Down Ramp Complete Interrupt is enabled

Bit 10: RAMP_DLY_INT_EN – Enables Ramp I/F Interrupt when ramp delay procedure is complete

0 = Soft-start/Power-Down Ramp Delay Complete Interrupt is disabled (Default)
1 = Soft-start/Power-Down Ramp Delay Complete Interrupt is enabled

Bit 9: PREBIAS_INT_EN – Enables Ramp I/F Interrupt when Pre-Bias procedure is completed

0 = Pre-bias Complete Interrupt is disabled (Default)
1 = Pre-bias Complete Interrupt is enabled

Bit 8: PCM_START_SEL – Peak Current Mode Ramp Start Value Select

0 = Ramp starts from value programmed in DAC_VALUE bits in EADC_DAC_VALUE Register (Default)
1 = Ramp starts from filter output selected by PCM_FILTER_SEL bits in Loop Mux register PCMCTRL

Bit 7: SYNC_FET_EN – Enables SyncFET Ramp Operation

0 = SyncFET Ramp Operation disabled (Default)
1 = SyncFET Ramp Operation enabled

Bits 6-5: MASTER_SEL – Selects Master Ramp I/F in slave mode

0 = Front End Control 0 acts as master (Default)
1 = Front End Control 1 acts as master
2 = Front End Control 2 acts as master

Bit 4: SLAVE_COMP_EN – Enables syncing of ramp start to Master Ramp I/F Complete pulse

0 = Ramp initiated by Master Ramp Complete pulse disabled (Default)
1 = Ramp initiated by Master Ramp Complete pulse enabled

Bit 3: SLAVE_DELAY_EN – Enables syncing of ramp start to Master Ramp I/F Delay Complete pulse

0 = Ramp initiated by Master Ramp Delay Complete pulse disabled (Default)
1 = Ramp initiated by Master Ramp Delay Complete pulse enabled

Bit 2: CONTROL_EN – Enables PMBus Control line to initiate ramp

0 = PMBus Control does not initiate ramp (Default)
1 = PMBus Control initiates ramp

Bit 1: FIRMWARE_START – Ramp start bit, self-clearing by ramp logic

0 = No ramp sequence initiated by firmware (Default)
1 = Ramp sequence initiated by firmware

Bit 0: RAMP_EN – Enable Ramp Logic (Pre-biasing should be disabled before asserting ramp, bit 16 of Pre-Bias Control Register)

0 = No soft start or power-down ramp controlled by hardware (Default)
1 = Enables hardware control of soft start or power-down ramp

9.2 Ramp Status Register (RAMPSTAT)

Address 0x0008_0004 – Front End Control 2 Ramp Status Register
Address 0x000B_0004 – Front End Control 1 Ramp Status Register
Address 0x000E_0004 – Front End Control 0 Ramp Status Register

Bit Number	11	10	9
Bit Name	EADC_DONE_RAW	RAMP_COMP_INT_STATUS	RAMP_DLY_INT_STATUS
Access	R	R	R
Default	-	-	-

Bit Number	8	7	6
Bit Name	PREBIAS_INT_STATUS	EADC_SAT_HIGH	EADC_SAT_LOW
Access	R	R	R
Default	-	-	-

Bit Number	5	4	3
Bit Name	EADC_EOC	PREBIAS_BUSY	RAMP_BUSY
Access	R	R	R
Default	-	-	-

Bit Number	2	1	0
Bit Name	RAMP_COMP_STATUS	RAMP_DLY_STATUS	PREBIAS_STATUS
Access	R	R	R
Default	-	-	-

Bit 11: EADC_DONE_RAW – EADC Conversion Done Raw Status
0 = EADC Conversion has not completed
1 = EADC Conversion has completed
Bit 10: RAMP_COMP_INT_STATUS – Ramp Complete latched status
0 = No Ramp Complete has been declared
1 = Ramp Complete has been declared
Bit 9: RAMP_DLY_INT_STATUS – Ramp Delay Complete latched status
0 = No Ramp Delay Complete has been declared
1 = Ramp Delay Complete has been declared
Bit 8: PREBIAS_INT_STATUS – Pre-Bias Complete latched status
0 = No Pre-Bias Complete has been declared
1 = Pre-Bias Complete has been declared
Bit 7: EADC_SAT_HIGH – EADC Saturation High Indicator
0 = EADC output is not saturated at high limit
1 = EADC output is saturated at high limit
Bit 6: EADC_SAT_LOW – EADC Saturation Low Indicator
0 = EADC output is not saturated at low limit
1 = EADC output is saturated at low limit
Bit 5: EADC_EOC – Indicates EADC end of conversion
Bit 4: PRE_BIAS_BUSY – Pre-Bias Busy
0 = Pre-Bias is not in progress
1 = Pre-Bias in progress
Bit 3: RAMP_BUSY – Ramp Busy
0 = Soft-Start/Power-Down Ramp is not in progress
1 = Soft-Start/Power-Down Ramp is in progress
Bit 2: RAMP_COMP_STATUS – Ramp Complete, Raw Status

0 = Ramp procedure is not complete
1 = Ramp procedure is complete

Bit 1: RAMP_DLY_STATUS – Ramp Delay Complete, Raw Status
0 = Ramp delay procedure is not complete
1 = Ramp delay procedure is complete

Bit 0: PRE_BIAS_STATUS – Pre-Bias Complete, Raw Status
0 = Pre-Bias is not completed
1 = Pre-Bias is completed

9.3 Ramp Cycle Register (RAMPCYCLE)

Address 0x0008_0008 – Front End Control 2 Ramp Cycle Register
Address 0x000B_0008 – Front End Control 1 Ramp Cycle Register
Address 0x000E_0008 – Front End Control 0 Ramp Cycle Register

Bit Number	23:8	7	6:0
Bit Name	DELAY_CYCLES	RESERVED	SWITCH_CYC_PER_STEP
Access	R/W	-	R/W
Default	0000_0000_0000_0000	0	000_0000

Bits 23-8: DELAY_CYCLES – Configures the number of delay cycles before an initiation of ramp sequence. Each delay cycle consists of n switching cycles, as specified by SWITCH_CYC_PER_STEP (Bits 6-0). Number of delay cycles can vary from 0 to 65535
0 = Ramp starts without delay (Default)
1 = Ramp starts after (1*SWITCH_CYC_PER_STEP) switching cycles
2 = Ramp starts after (2*SWITCH_CYC_PER_STEP) switching cycles
…….
65535 = Ramp starts after (65535*SWITCH_CYC_PER_STEP) switching cycles

Bit 7: RESERVED

Bits 6-0: SWITCH_CYC_PER_STEP – Selects number of switching cycles per DAC step. Number of subcycles can vary from 1 to 128.
0 = 1 switching cycle per step (Default)
1 = 2 subcycles per cycle
2 = 3 subcycles per cycle
…….
127 = 128 subcycles per cycle

9.4 EADC DAC Value Register (EADCDAC)

Address 0x0008_000C – Front End Control 2 EADC DAC Value Register
Address 0x000B_000C – Front End Control 1 EADC DAC Value Register
Address 0x000E_000C– Front End Control 0 EADC DAC Value Register

Bit Number	15	14	13:0
Bit Name	DAC_DITHER_EN	RESERVED	DAC_VALUE
Access	R/W	-	R/W
Default	0	0	00_1111_1111_0000

Bit 15: DAC_DITHER_EN – DAC Dithering Enable
0 = DAC Dithering disabled (Default)
1 = DAC Dithering enabled
Bit 15: RESERVED
Bits 13-0: DAC_VALUE - Programmable DAC Value, effective LSB equals 0.09765625mV

9.5 Ramp DAC Ending Value Register (RAMPDACEND)

Address 0x0008_0010 – Front End Control 2 Ramp DAC Ending Register
Address 0x000B_0010 – Front End Control 1 Ramp DAC Ending Register
Address 0x000E_0010 – Front End Control 0 Ramp DAC Ending Register

Bit Number	13:0
Bit Name	RAMP_DAC_VALUE
Access	R/W
Default	00_0000_0000_0000

Bits 13-0: RAMP_DAC_VALUE – Programmable Ramp Ending DAC Value, LSB equals 0.09765625mV

9.6 DAC Step Register (DACSTEP)

Address 0x0008_0014 – Front End Control 2 DAC Step Register
Address 0x000B_0014 – Front End Control 1 DAC Step Register
Address 0x000E_0014 – Front End Control 0 DAC Step Register

Bit Number	17:0
Bit Name	DAC_STEP
Access	R/W
Default	00_0000_0000_0000_0000

Bits 17-0: DAC_STEP – Programmable 18-bit unsigned DAC Step. Bits 17:10 represent the real portion of the DAC Step (0-255 DAC counts at bit resolution of 0.09765625mV). Bits 9:0 represent the fractional portion of the DAC Step.

9.7 DAC Saturation Step Register (DACSATSTEP)

Address 0x0008_0018 – Front End Control 2 DAC Saturation Step Register
Address 0x000B_0018 – Front End Control 1 DAC Saturation Step Register
Address 0x000E_0018 – Front End Control 0 DAC Saturation Step Register

Bit Number	13:0
Bit Name	DAC_SAT_STEP
Access	R/W
Default	00_0000_0000_0000

Bits 13-0: DAC_SAT_STEP – Programmable DAC Saturation Step, LSB equals 0.009765625mV

0 = DAC not adjusted on EADC saturation during ramp (Default)
1 = DAC adjusted by 1 DAC count on EADC saturation during ramp
…..
1023 = DAC adjusted by 1023 DAC counts on EADC saturation during ramp

9.8 EADC Trim Register (EADCTRIM) – (For Factory Test Use Only)

Address 0x0008_001C – Front End Control 2 EADC Trim Register
Address 0x000B_001C – Front End Control 1 EADC Trim Register
Address 0x000E_001C – Front End Control 0 EADC Trim Register

Bit Number	29:24	23:22	21:16	15:14
Bit Name	GAIN3_TRIM	RESERVED	GAIN2_TRIM	RESERVED
Access	R/W	-	R/W	-
Default	01_1000	00	01_1000	00

Bit Number	13:8	7:6	5:0
Bit Name	GAIN1_TRIM	RESERVED	GAIN0_TRIM
Access	R/W	-	R/W
Default	01_1000	00	01_1000

Bits 29-24: GAIN3_TRIM – Sets trim for 8X AFE Gain. Register will be programmed during test and should not be overwritten by firmware.
Bits 23-22: RESERVED – Unused Bits
Bits 21-16: GAIN2_TRIM – Sets trim for 4X AFE Gain. Register will be programmed during test and should not be overwritten by firmware.
Bits 15-14: RESERVED – Unused Bits
Bits 13-8: GAIN1_TRIM – Sets trim for 2X AFE Gain. Register will be programmed during test and should not be overwritten by firmware.
Bits 7-6: RESERVED – Unused Bits
Bits 5-0: GAIN0_TRIM – Sets trim for 1X AFE Gain. Register will be programmed during test and should not be overwritten by firmware.

9.9 EADC Control Register (EADCCTRL)

Address 0x0008_0020 – Front End Control 2 EADC Control Register
Address 0x000B_0020 – Front End Control 1 EADC Control Register
Address 0x000E_0020 – Front End Control 0 EADC Control Register

Bit Number	28	27	26
Bit Name	D2S_COMP_EN	EN_HYST_HIGH	EN_HYST_LOW
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	25:22	21	20
Bit Name	SAMP_TRIG_SCALE	FRAME_SYNC_EN	SCFE_CNT_RST
Access	R/W	R/W	R/W
Default	0000	0	0

Bit Number	19:16	15	14
Bit Name	SCFE_CNT_INIT	EADC_INV	AUTO_GAIN_SHIFT_MODE
Access	R/W	R/W	R/W
Default	0000	0	0

Bit Number	13	12	11
Bit Name	AUTO_GAIN_SHIFT_EN	AVG_WEIGHT_EN	AVG_SPATIAL_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10:9	8:6	5:4
Bit Name	AVG_MODE_SEL	EADC_MODE	AFE_GAIN
Access	R/W	R/W	R/W
Default	00	000	11

Bit Number	3	2	1	0
Bit Name	SCFE_GAIN_FILTER_SEL	SCFE_CLK_DIV_2	SCFE_ENA	EADC_ENA
Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit 28: D2S_COMP_EN – Analog Front End Ramp Comparator Enable
0 = Analog Front End Ramp Comparator disabled (Default)
1 = Analog Front End Ramp Comparator enabled
Bit 27: EN_HYST_HIGH – Increase comparator trip point by ~70mV
0 = Disables increase of ramp comparator trip point (Default)
1 = Enables increase of ramp comparator trip point
Bit 26: EN_HYST_LOW – Decrease comparator trip point by ~70mV
0 = Disables decrease of ramp comparator trip point (Default)
1 = Enables decrease of ramp comparator trip point

Bits 25-22: SAMP_TRIG_SCALE – Provides capability to mask incoming sample triggers to Front End Control

0 = EADC conversion initiated on every received sample trigger (Default)
1 = EADC conversion initiated once every 2 received sample triggers
2 = EADC conversion initiated once every 3 received sample triggers
…..
15 = EADC conversion initiated once every 16 received sample triggers

Bit 21: FRAME_SYNC_EN – Enable synchronization of switched cap front end counter to Switching Cycle Frame boundary

0 = Switch Cap Front End Counter not synchronized to frame (Default)
1 = Switch Cap Front End Counter synchronized to frame boundary

Bit 20: SCFE_CNT_RST – Force reset of Switched Cap Front End Counter

0 = Switch Cap Front End Counter operational (Default)
1 = Switch Cap Front End Counter reset

Bits 19-16: SCFE_CNT_INIT – Configures initial Switched Cap Front End Counter value out of reset or at start of switching cycle in Peak Current mode

Bit 15: EADC_INV – Enables EADC Data Inversion on data to filter module

0 = EADC Data is not inverted (Default)
1 = EADC Data Inverted

Bit 14: AUTO_GAIN_SHIFT_MODE – Configures Automatic Gain Shifting mode

0 = Fixed mode, gain shifting dependent on saturation of EADC for decreasing gain and less than 1/4 of dynamic range for increasing gain (Default)
1 = NL mode, gain shifting dependent on Non-Linear limit thresholds

Bit 13: AUTO_GAIN_SHIFT_EN – Enables Automatic Gain Shifting mode

0 = Automatic Gain Shifting Mode disabled (Default)
1 = Automatic Gain Shifting Mode enabled

Bit 12: AVG_WEIGHT_EN – Enables weighted averaging in EADC averaging mode, only applicable in 4x and 8x averaging mode. For 4x averaging, two oldest samples are each weighted by 1/8, the next oldest sample has a weight of ¼ and the newest sample is weighted by ½. For 8x averaging, the four oldest samples are each weighted by 1/16, the next 2 oldest samples are weighted by 1/8, and the two newest samples are weighted by 1/4.

0 = Weighted averaging disabled (Default)
1 = Weighted averaging enabled

Bit 11: AVG_SPATIAL_EN – Enables spatial mode in EADC averaging mode

0 = Consecutive EADC samples averaged based on every received sample trigger from DPWM modules (Default)
1 = EADC samples averaged based on received sample triggers from DPWM modules. 2 sample triggers required for a single averaged sample to filter. 4 sample triggers required for a single averaged sample to filter module

Bit 10-9: AVG_MODE_SEL – Averaging Mode Configuration

0 = 2x Averaging (Default)
1 = 4x Averaging
2 = 8x Averaging

Bits 8-6: EADC_MODE – Selects EADC Mode Operation

0 = Standard mode, EADC samples based on sample triggers from DPWM module (Default)
1 = Averaging Mode, configured by AVG_MODE_SEL
2 = Non-continuous SAR Mode
3 = Continuous SAR Mode
4 = Reserved
5 = Peak Current Mode
6 = Constant Power/Constant Current Control Mode (CPCC module controls switching between Standard Mode and Non-Continuous SAR Mode)
7 = Constant Power/Constant Current Control 2 Mode (CPCC module controls switching between Standard mode and Continuous SAR Mode)

Bits 5-4: AFE_GAIN – AFE Front End Gain Setting
0 = 1x Gain, 8mV/LSB
1 = 2x Gain, 4mV/LSB
2 = 4x Gain, 2mV/LSB
3 = 8x Gain, 1mV/LSB (Default)

Bit 3: SCFE_GAIN_FILTER_SEL – Switched Cap Noise Filter Enable
0 = Disables Switch Cap Noise Filter
1 = Enables Switch Cap Noise Filter (Default)

Bit 2: SCFE_CLK_DIV_2 – Switched Cap Front End Clock Divider Select
0 = Switch Cap Clock divide by 1
1 = Switch Cap Clock divide by 2 (Default)

Bit 1: SCFE_ENA – Switch Cap Front Enable
0 = Disables Switch Cap Front End logic
1 = Enables Switch Cap Front End logic (Default)

Bit 0: EADC_ENA – EADC Enable
0 = Disables EADC
1 = Enables EADC (Default)

9.10 Analog Control Register (ACTRL) (For Test Use Only)

Address 0x0008_0024 – Front End Control 2 Analog Control Register
Address 0x000B_0024 – Front End Control 1 Analog Control Register
Address 0x000E_0024 – Front End Control 0 Analog Control Register

Bit Number	15:10	9	8
Bit Name	EADC_REF_TRIM	EADC_REF_RESET	EADC_REF_EN
Access	R/W	R/W	R/W
Default	000000	1	0

Bit Number	7:5	4	3
Bit Name	RESERVED	EADC_GAIN_CAL	EADC_OFFSET_CAL
Access	-	R/W	R/W
Default	000	0	0

Bit Number	2	1	0
Bit Name	INT_REF_SEL	EXT_V_SE_SEL	ANALOG_ENA
Access	R/W	R/W	R/W
Default	1	0	1

Bits 15-10: EADC_REF_TRIM – EADC Reference Trim Value. Bits will be programmed during test and should not be overwritten by firmware.
Bit 9: EADC_REF_RESET – EADC Reference Reset
0 = Reference not in reset
1 = Resets Reference (Default)
Bit 8: EADC_REF_EN – EADC Reference Enable
0 = Disables EADC Reference (Default)
1 = Enables EADC Reference
Bits 7-5: RESERVED – Unused Bits
Bit 4: EADC_GAIN_CAL – EADC Gain Calibration Mode Enable
0 = Disables Gain Calibration Mode (Default)
1 = Enables Gain Calibration Mode
Bit 3: EADC_OFFSET_CAL – EADC Offset Calibration Mode Enable
0 = Disables Offset Calibration Mode (Default)
1 = Enables Offset Calibration Mode
Bit 2: INT_REF_SEL – EADC Reference Select
0 = Selects External Reference for EADC from AD8-AD9 pins. In external mode, DAC_P tied to AD8 and DAC_N tied to AD9.
1 = Selects Internal Reference for EADC from DAC (Default)
Bit 1: EXT_V_SE_SEL – EADC Select
0 = Selects Internal V_SE, output from EADC (Default)
1 = Selects External V_SE, bypass EADC
Bit 0: ANALOG_ENA – Analog Front End Enable
0 = Disables Analog Front End
1 = Enables Analog Front End (Default)

9.11 Pre-Bias Control Register 0 (PREBIASCTRL0)

Address 0x0008_0028 – Front End Control 2 Pre-Bias Control Register 0
Address 0x000B_0028 – Front End Control 1 Pre-Bias Control Register 0
Address 0x000E_0028 – Front End Control 0 Pre-Bias Control Register 0

Bit Number	17	16	15:8	7:0

Bit Name	PRE_BIAS_POL	PRE_BIAS_EN	PRE_BIAS_RANGE	PRE_BIAS_LIMIT
Access	R/W	R/W	R/W	R/W
Default	0	0	1111_1111	0000_0000

Bit 17: PRE_BIAS_POL – Configures polarity of received error voltage
0 = Error equals Vref-Vin (Default)
1 = Error equals Vin-Vref
Bit 16: PRE_BIAS_EN – Enable Pre-Biasing of Error ADC (Ramp should be disabled during pre-biasing, bit 0 of Ramp Control Register)
0 = Pre-Biasing has not been initiated (Default)
1 = Pre-Biasing by hardware has been enabled
Bits 15-8: PRE_BIAS_RANGE – Sets the acceptable range around the zero error point. If Error ADC value stays in range for number of samples specified by **PRE_BIAS_LIMIT** (Bits 7:0), **PREBIAS_STATUS** (Bit 0 of Ramp Status Register) is enabled. Range will be +/- **PRE_BIAS_RANGE** around zero error point.
Bits 7-0: PRE_BIAS_LIMIT – Sets the acceptable number of samples in which the Error ADC value stays in range before asserting **PREBIAS_STATUS** (Bit 0 of Ramp Status Register). Counter limit ranges from 0 to 255. If **PREBIAS_STATUS** is set, it will take **PRE_BIAS_LIMIT** samples outside of acceptable range before clearing **PREBIAS_STATUS**.

9.12 Pre-Bias Control Register 1 (PREBIASCTRL1)

Address 0x0008_002C – Front End Control 2 Pre-Bias Control Register 1
Address 0x000B_002C – Front End Control 1 Pre-Bias Control Register 1
Address 0x000E_002C – Front End Control 0 Pre-Bias Control Register 1

Bit Number	23:16	15:14	13:0
Bit Name	SAMPLES_PER_ADJ	RESERVED	MAX_DAC_ADJ
Access	R/W	-	R/W
Default	0000_0000	00	00_0000_0000_0000

Bits 23-16: SAMPLES_PER_ADJ – Configures the number of EADC samples between Pre-Bias DAC setpoint adjustments
0 = DAC Setpoint adjustment on each EADC sample
1 = DAC Setpoint adjustment after 2 EADC sample
2 = DAC Setpoint adjustment after 3 EADC samples
…….
255 = DAC Setpoint adjustment after 256 EADC samples
Bits 15-14: RESERVED – Unused Bits
Bits 13-0: MAX_DAC_ADJ – Configures the maximum DAC setpoint adjustment step

9.13 SAR Control Register (SARCTRL)

Address 0x0008_0030 – Front End Control 2 SAR Control Register
Address 0x000B_0030 – Front End Control 1 SAR Control Register
Address 0x000E_0030 – Front End Control 0 SAR Control Register

Bit Number	31:24	23:16	15:8
Bit Name	EADC_WINDOW_2	EADC_WINDOW_1	SAR_RANGE
Access	R/W	R/W	R/W
Default	0010_1000	0110_0000	0000_0000

Bit Number	7:2	1:0

Bit Name	RESERVED	SAR_RESOLUTION
Access	-	R/W
Default	0000_00	00

Bits 31-24: EADC_WINDOW_2 – Configures acceptable range of error values to transition to AFE Gain of 2 during SAR process
Bits 23-16: EADC_WINDOW_1 – Configures acceptable range of error values to transition to AFE Gain of 1 during SAR process
Bits 15-8: SAR_RANGE – Configures acceptable range of error values before declaring SAR completion
Bits 7-2: RESERVED – Unused bits
Bits 1-0: SAR_RESOLUTION – Configures the final resolution for SAR Conversions
0 = 8mV Resolution, 1x AFE Gain
1 = 4mV Resolution, 2x AFE Gain
2 = 2mV Resolution, 4x AFE Gain
3 = 1mV Resolution, 8x AFE Gain

9.14 SAR Timing Register (SARTIMING)

Address 0x0008_0034 – Front End Control 2 SAR Timing Register
Address 0x000B_0034– Front End Control 1 SAR Timing Register
Address 0x000E_0034 – Front End Control 0 SAR Timing Register

Bit Number	10:8	7
Bit Name	SAR_TIMING_UPPER	RESERVED
Access	R/W	-
Default	100	0

Bit Number	6:4	3	2:0
Bit Name	SAR_TIMING_MID	RESERVED	SAR_TIMING_LOWER
Access	R/W	-	R/W
Default	011	0	010

Bits 10-8: SAR_TIMING_UPPER – Configures timing for Bits 9:8 of DAC setpoint for SAR Algorithm
Bit 7: RESERVED – Unused bit
Bits 6-4: SAR_TIMING_MID – Configures timing for Bits 7:6 of DAC setpoint for SAR Algorithm
Bit 3: RESERVED – Unused bit
Bits 2-0: SAR_TIMING_LOWER – Configures timing for Bits 5:0 of DAC setpoint for SAR Algorithm

9.15 EADC Value Register (EADCVALUE)

Address 0x0008_0038 – Front End Control 2 EADC Value Register
Address 0x000B_0038 – Front End Control 1 EADC Value Register
Address 0x000E_0038 – Front End Control 0 EADC Value Register

Bit Number	25:16	15	14
Bit Name	ABS_VALUE	EADC_SAT_HIGH	EADC_SAT_HIGH
Access	R	R	R
Default	-	-	-

Bit Number	13:9	8:0
Bit Name	RESERVED	ERROR_VALUE
Access	-	R
Default	00_000	-

Bits 25-16: ABS_VALUE – 10-bit Absolute Value calculated by Front End Control Module with a resolution of 1.5625mV/bit
Bit 15: EADC_SAT_HIGH – EADC Saturation High Indicator
0 = EADC output is not saturated at high limit
1 = EADC output is saturated at high limit
Bit 14: EADC_SAT_LOW – EADC Saturation Low Indicator
0 = EADC output is not saturated at low limit
1 = EADC output is saturated at low limit
Bits 13-9: RESERVED – Unused bits
Bits 8-0: ERROR_VALUE – Signed 9-bit Error value measured by Front End Control Module with a resolution of 1mV/bit

9.16 EADC Raw Value Register (EADCRAWVALUE)

Address 0x0008_003C – Front End Control 2 EADC Raw Value Register
Address 0x000B_003C – Front End Control 1 EADC Raw Value Register
Address 0x000E_003C – Front End Control 0 EADC Raw Value Register

Bit Number	8:0
Bit Name	RAW_ERROR_VALUE
Access	R
Default	-

Bits 8-0: RAW_ERROR_VALUE – Signed 9-bit Error value measured by Front End Control Module with a resolution of 1mV/bit. Value is raw EADC data before averaging.

9.17 DAC Status Register (DACSTAT)

Address 0x0008_0040 – Front End Control 2 DAC Status Register
Address 0x000B_0040 – Front End Control 1 DAC Status Register
Address 0x000E_0040 – Front End Control 0 DAC Status Register

Bit Number	9:0
Bit Name	DAC_VALUE
Access	R
Default	00_0000_0000

Bits 9-0: DAC_VALUE – Current 10-bit Value sent to DAC

10 Filter Registers Reference

Registers for Filter Modules 0-2 are identical in their bit definitions.

10.1 Filter Status Register (FILTERSTATUS)

Address 00060000 – Filter 2 Status Register
Address 00090000 – Filter 1 Status Register
Address 000C0000 – Filter 0 Status Register

Bit Number	4	3	2
Bit Name	FILTER_BUSY	YN_LOW_CLAMP	YN_HIGH_CLAMP
Access	R	R	R
Default	-	-	-

Bit Number	1	0
Bit Name	KI_YN_LOW_CLAMP	KI_YN_HIGH_CLAMP
Access	R	R
Default	-	-

Bit 4: FILTER_BUSY – Filter Busy Indicator
0 = Filter is waiting for new data
1 = Filter busy calculating
Bit 3: YN_LOW_CLAMP – PID Output Low Rail Indicator
0 = PID Output not equal to low rail
1 = PID Output equal to low rail
Bit 2: YN_HIGH_CLAMP – PID Output High Rail Indicator

0 = PID Output not equal to high rail
1 = PID Output equal to high rail

Bit 1: KI_YN_LOW_CLAMP – KI Feedback Low Rail Indicator
0 = KI Feedback not equal to low rail
1 = KI Feedback equal to low rail

Bit 0: KI_YN_HIGH_CLAMP – KI Feedback High Rail Indicator
0 = KI Feedback not equal to high rail
1 = KI Feedback equal to high rail

10.2 Filter Control Register (FILTERCTRL)

Address 00060004 – Filter 2 Control Register
Address 00090004 – Filter 1 Control Register
Address 000C0004 – Filter 0 Control Register

Bit Number	15	14	13:12
Bit Name	KI_ADDER_MODE	PERIOD_MULT_SEL	OUTPUT_MULT_SEL
Access	R/W	R/W	R/W
Default	1	0	00

Bit Number	11:9	8	7	6	5
Bit Name	YN_SCALE	NL_MODE	KD_STALL	KI_STALL	KP_OFF
Access	R/W	R/W	R/W	R/W	R/W
Default	000	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	KD_OFF	KI_OFF	FORCE_START	USE_CPU_SAMPLE	FILTER_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1

Bit 15: KI_ADDER_MODE – Configures addition of Xn and Xn-1 in Integral branch
0 = Only Xn used for addition (Xn + 0)
1 = Xn + Xn-1 used for addition (Default)
Bit 14: PERIOD_MULT_SEL – Selects output multiplicand used for multiplying with filter output to calculate DPWM Period value in Resonant Mode
0 = Switching period received from Loop Mux module (Default)
1 = KComp received from Loop Mux module
Bits 13-12: OUTPUT_MULT_SEL – Selects output multiplicand used for multiplying with filter output to calculate DPWM Duty value
0 = KComp received from Loop Mux module (Default)
1 = Switching period received from Loop Mux module
2 = Feed-Forward value received from Loop Mux module
3 = Resonant Duty value received from DPWM Module
Bit 11-9: OUTPUT_SCALE – Controls scaling of Yn value to compensate for filter coefficient scaling
-4 = Filter output (Yn) left shifted by 4
-3 = Filter output (Yn) left shifted by 3
-2 = Filter output (Yn) left shifted by 2
-1 = Filter output (Yn) left shifted by 1
0 = Filter output (Yn) not scaled (Default)
1 = Filter output (Yn) right shifted by 1
2 = Filter output (Yn) right shifted by 2
3 = Filter output (Yn) right shifted by 3
Bit 8: NL_MODE – Sets non-linear gain table configuration. Coefficient Bin mapping is controlled by Coefficient Configuration Register. Limit configuration is controlled by the Filter Nonlinear Limit Registers (See Sections 8.16-8.18)
0 = Non-symmetric mode (Default)
1 = Symmetric mode
Bit 7: KD_STALL – Freezes KD Branch, KD_YN remains at current value
0 = KD_YN recalculated on each filter update (Default)
1 = KD_YN stalled at present value
Bit 6: KI_STALL – Freezes KI Branch, KI_YN remains at current value

0 = KI_YN recalculated on each filter update (Default)
1 = KI_YN stalled at present value

Bit 5: KP_OFF – Turns off the KP branch
0 = KP branch calculating new outputs (Default)
1 = KP branch turned off

Bit 4: KD_OFF – Turns off the KD branch, KD_YN cleared to zero
0 = KD branch calculating new outputs (Default)
1 = KD branch turned off

Bit 3: KI_OFF – Turns off the KI branch, KI_YN cleared to zero
0 = KI branch calculating new outputs (Default)
1 = KI branch halted

Bit 2: FORCE_START – Initiates a filter calculation under firmware control
0 = No calculation started (Default)
1 = Calculation started

Bit 1: USE_CPU_SAMPLE – Forces filter to use error sample from CPU XN register (Section 8.3)
0 = Filter Mode, input data received from EADC (Default)
1 = CPU Mode, input data based on CPU XN register

Bit 0: FILTER_EN – Filter Enable
0 = Disables Filter operation
1 = Enables Filter operation (Default)

10.3 CPU XN Register (CPUXN)

Address 00060008 – Filter 2 CPU XN Register
Address 00090008 – Filter 1 CPU XN Register
Address 000C0008 – Filter 0 CPU XN Register

Bit Number	8:0
Bit Name	CPU_SAMPLE
Access	R/W
Default	0_0000_0000

Bits 8-0: CPU_SAMPLE – Forced X_n value, allows processor to use filter as ALU. Set Bit 2 of Filter Control Register to '1' to force CPU_SAMPLE as input to Filter.

10.4 Filter XN Read Register (FILTERXNREAD)

Address 0006000C – Filter 2 XN Read Register
Address 0009000C – Filter 1 XN Read Register
Address 000C000C – Filter 0 XN Read Register

Bit Number	24:16	15:9	8:0
Bit Name	XN_M1	RESERVED	XN
Access	R	-	R
Default	-	000_0000	-

Bits 24-16: XN_M1 – 9-bit signed XN_M1 register value, read-only
Bits 15-9: RESERVED
Bits 8-0: XN – 9-bit signed XN register value, read-only

10.5 Filter KI_YN Read Register (FILTERKIYNREAD)

Address 00060010 – Filter 2 KI_YN Read Register
Address 00090010 – Filter 1 KI_YN Read Register
Address 000C0010 – Filter 0 KI_YN Read Register

Bit Number	23:0
Bit Name	KI_YN
Access	R
Default	-

Bits 23-0: KI_YN – 24-bit signed KI_YN register value, read-only

10.6 Filter KD_YN Read Register (FILTERKDYNREAD)

Address 00060014 – Filter 2 KD_YN Register
Address 00090014 – Filter 1 KD_YN Register
Address 000C0014 – Filter 0 KD_YN Register

Bit Number	23:0
Bit Name	KD_YN
Access	R
Default	-

Bits 23-0: KD_YN – 24-bit signed KD_YN register value, read-only

10.7 Filter YN Read Register (FILTERYNREAD)

Address 00060018 – Filter 2 YN Read Register
Address 00090018 – Filter 1 YN Read Register
Address 000C0018 – Filter 0 YN Read Register

Bit Number	23:0
Bit Name	YN
Access	R
Default	-

Bits 23-0: YN – 24-bit signed YN register value, read-only

10.8 Coefficient Configuration Register (COEFCONFIG)

Address 0006001C – Filter 2 Coefficient Configuration Register
Address 0009001C – Filter 1 Coefficient Configuration Register
Address 000C001C – Filter 0 Coefficient Configuration Register

Bit Number	27	26:24	23	22:20
Bit Name	BIN6_ALPHA	BIN6_CONFIG	BIN5_ALPHA	BIN5_CONFIG
Access	R/W	R/W	R/W	R/W
Default	0	000	0	000

Bit Number	19	18:16	15	14:12	11
Bit Name	BIN4_ALPHA	BIN4_CONFIG	BIN3_ALPHA	BIN3_CONFIG	BIN2_ALPHA
Access	R/W	R/W	R/W	R/W	R/W
Default	0	000	0	000	0

Bit Number	10:8	7	6:4	3	2:0
Bit Name	BIN2_CONFIG	BIN1_ALPHA	BIN1_CONFIG	BIN0_ALPHA	BIN0_CONFIG
Access	R/W	R/W	R/W	R/W	R/W
Default	000	0	000	0	000

Bit 27: BIN6_ALPHA – Selects which alpha value to use in Bin 6 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 26-24: BIN6_CONFIG – Selects which coefficient set to place in Bin 6 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 23: BIN5_ALPHA – Selects which alpha value to use in Bin 5 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)

1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 22-20: BIN5_CONFIG – Selects which coefficient set to place in Bin 5 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 19: BIN4_ALPHA – Selects which alpha value to use in Bin 4 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 18-16: BIN4_CONFIG – Selects which coefficient set to place in Bin 4 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 15: BIN3_ALPHA – Selects which alpha value to use in Bin 3 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 14-12: BIN3_CONFIG – Selects which coefficient set to place in Bin 3 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 11: BIN2_ALPHA – Selects which alpha value to use in Bin 2 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 10-8: BIN2_CONFIG – Selects which coefficient set to place in Bin 2 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 7: BIN1_ALPHA – Selects which alpha value to use in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 6-4: BIN1_CONFIG – Selects which coefficient set to place in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 3: BIN0_ALPHA – Selects which alpha value to use in Bin 0 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 2-0: BIN1_CONFIG – Selects which coefficient set to place in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

10.9 Filter KP Coefficient 0 Register (FILTERKPCOEF0)

Address 00060020 – Filter 2 KP Coefficient 0 Register
Address 00090020 – Filter 1 KP Coefficient 0 Register
Address 000C0020 – Filter 0 KP Coefficient 0 Register

Bit Number	31:16	15:0
Bit Name	KP_COEF_1	KP_COEF_0
Access	R/W	R/W
Default	0000_0000_0000_0000	0100_0010_0011_0100

Bits 31-16: KP_COEF_1 – KP Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KP_COEF_0 – KP Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

10.10 Filter KP Coefficient 1 Register (FILTERKPCOEF1)

Address 00060024 – Filter 2 KP Coefficient 1 Register
Address 00090024 – Filter 1 KP Coefficient 1 Register
Address 000C0024 – Filter 0 KP Coefficient 1 Register

Bit Number	15:0
Bit Name	KP_COEF_2
Access	R/W

Default	0000_0000_0000_0000

Bits 15-0: KP_COEF_2 – KP Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

10.11 Filter KI Coefficient 0 Register (FILTERKICOEF0)

Address 00060028 – Filter 2 KI Coefficient 0 Register
Address 00090028 – Filter 1 KI Coefficient 0 Register
Address 000C0028 – Filter 0 KI Coefficient 0 Register

Bit Number	31:16	15:0
Bit Name	KI_COEF_1	KI_COEF_0
Access	R/W	R/W
Default	0000_0000_0000_0000	0010_0100_0001_0010

Bits 31-16: KI_COEF_1 – KI Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KI_COEF_0 – KI Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

10.12 Filter KI Coefficient 1 Register (FILTERKICOEF1)

Address 0006002C – Filter 2 KI Coefficient 1 Register
Address 0009002C – Filter 1 KI Coefficient 1 Register
Address 000C002C – Filter 0 KI Coefficient 1 Register

Bit Number	31:16	15:0
Bit Name	KI_COEF_3	KI_COEF_2
Access	R/W	R/W
Default	0000_0000_0000_0000	0000_0000_0000_0000

Bits 31-16: KI_COEF_3 – KI Coefficient 3, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KI_COEF_2 – KI Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

10.13 Filter KD Coefficient 0 Register (FILTERKDCOEF0)

Address 00060030 – Filter 2 KD Coefficient 0 Register
Address 00090030 – Filter 1 KD Coefficient 0 Register
Address 000C0030 – Filter 0 KD Coefficient 0 Register

Bit Number	31:16	15:0
Bit Name	KD_COEF_1	KD_COEF_0
Access	R/W	R/W
Default	0000_0000_0000_0000	1100_0100_0000_0001

Bits 31-16: KD_COEF_1 – KD Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KD_COEF_0 – KD Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

10.14 Filter KD Coefficient 1 Register (FILTERKDCOEF1)

Address 00060034 – Filter 2 KD Coefficient 1 Register
Address 00090034 – Filter 1 KD Coefficient 1 Register
Address 000C0034 – Filter 0 KD Coefficient 1 Register

Bit Number	15:0
Bit Name	KD_COEF_2
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: KD_COEF_2 – KD Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

10.15 Filter KD Alpha Register (FILTERKDALPHA)

Address 00060038 – Filter 2 KD Alpha Register
Address 00090038 – Filter 1 KD Alpha Register
Address 000C0038 – Filter 0 KD Alpha Register

Bit Number	24:16	15:9	8:0
Bit Name	KD_ALPHA_1	RESERVED	KD_ALPHA_0
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_0101_0010

Bits 24-16: KD_ALPHA_1 – Bank 1 KD Alpha, 9-bit signed value, configurable to any bin using the Coefficient Control Register
Bits 15-9: RESERVED
Bits 8-0: KD_ALPHA_0 – Bank 0 KD Alpha, 9-bit signed value, configurable to any bin using the Coefficient Control Register

10.16 Filter Nonlinear Limit Register 0 (FILTERNL0)

Address 0006003C – Filter 2 Nonlinear Limit Register 0
Address 0009003C – Filter 1 Nonlinear Limit Register 0
Address 000C003C – Filter 0 Nonlinear Limit Register 0

Bit Number	24:16	15:9	8:0
Bit Name	LIMIT1	RESERVED	LIMIT0
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_1111_1111

Bits 24-16: LIMIT1 – Configures LIMIT1 in Nonlinear Coefficient tables
Bits 15-9: RESERVED
Bits 8-0: LIMIT0 – Configures LIMIT0 in Nonlinear Coefficient tables

10.17 Filter Nonlinear Limit Register 1 (FILTERNL1)

Address 00060040 – Filter 2 Nonlinear Limit Register 1
Address 00090040 – Filter 1 Nonlinear Limit Register 1
Address 000C0040 – Filter 0 Nonlinear Limit Register 1

Bit Number	24:16	15:9	8:0
Bit Name	LIMIT3	RESERVED	LIMIT2
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_0000_0000

Bits 24-16: LIMIT3 – Configures LIMIT3 in Nonlinear Coefficient tables
Bits 15-9: RESERVED
Bits 8-0: LIMIT2 – Configures LIMIT2 in Nonlinear Coefficient tables

10.18 Filter Nonlinear Limit Register 2 (FILTERNL2)

Address 00060044 – Filter 2 Nonlinear Limit Register 2
Address 00090044 – Filter 1 Nonlinear Limit Register 2
Address 000C0044 – Filter 0 Nonlinear Limit Register 2

Bit Number	24:16	15:9	8:0
Bit Name	LIMIT5	RESERVED	LIMIT4
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_0000_0000

Bits 24-16: LIMIT5 – Configures LIMIT5 in Nonlinear Coefficient tables
Bits 15-9: RESERVED
Bits 8-0: LIMIT4 – Configures LIMIT4 in Nonlinear Coefficient tables

10.19 Filter KI Feedback Clamp High Register (FILTERKICLPHI)

Address 00060048 – Filter 2 KI Feedback Clamp High Register
Address 00090048 – Filter 1 KI Feedback Clamp High Register
Address 000C0048 – Filter 0 KI Feedback Clamp High Register

Bit Number	23:0
Bit Name	KI_CLAMP_HIGH
Access	R/W
Default	0111_1111_1111_1111_1111_1111

Bits 23-0: KI_CLAMP_HIGH – Sets the upper limit of KI_YN value. If calculated KI_YN exceeds this threshold, the KI_YN register will be set to KI_CLAMP_HIGH

10.20 Filter KI Feedback Clamp Low Register (FILTERKICLPLO)

Address 0006004C– Filter 2 KI Feedback Clamp Low Register
Address 0009004C– Filter 1 KI Feedback Clamp Low Register
Address 000C004C – Filter 0 KI Feedback Clamp Low Register

Bit Number	23:0
Bit Name	KI_CLAMP_LOW
Access	R/W
Default	0000_0000_0000_0000_0000_0000

Bits 23-0: KI_CLAMP_LOW – Sets the lower limit of KI_YN value. If calculated KI_YN falls below this threshold, the KI_YN register will be set to KI_CLAMP_LOW

10.21 Filter YN Clamp High Register (FILTERYNCLPHI)

Address 00060050 – Filter 2 YN Clamp High Register
Address 00090050 – Filter 1 YN Clamp High Register
Address 000C0050 – Filter 0 YN Clamp High Register

Bit Number	23:0
Bit Name	YN_CLAMP_HIGH
Access	R/W
Default	0111_1111_1111_1111_1111_1111

Bits 23-0: YN_CLAMP_HIGH – Sets the upper limit of YN value. If calculated YN exceeds this threshold, the YN register will be set to YN_CLAMP_HIGH

10.22 Filter YN Clamp Low Register (FILTERYNCLPLO)

Address 00060054 – Filter 2 YN Clamp Low Register
Address 00090054 – Filter 1 YN Clamp Low Register
Address 000C0054 – Filter 0 YN Clamp Low Register

Bit Number	23:0
Bit Name	YN_CLAMP_LOW
Access	R/W
Default	0000_0000_0000_0000_0000_0000

Bits 23-0: YN_CLAMP_LOW – Sets the lower limit of YN value. If calculated YN falls below this threshold, the YN register will be set to YN_CLAMP_LOW

10.23 Filter Output Clamp High Register (FILTEROCLPHI)

Address 00060058 – Filter 2 Output Clamp High Register
Address 00090058 – Filter 1 Output Clamp High Register
Address 000C0058 – Filter 0 Output Clamp High Register

Bit Number	17:0
Bit Name	OUTPUT_CLAMP_HIGH
Access	R/W
Default	11_1111_1111_1111_1111

Bits 17-0: OUTPUT_CLAMP_HIGH – Sets the upper limit of filter output value. If calculated filter output exceeds this threshold, the filter output will be set to OUTPUT_CLAMP_HIGH

10.24 Filter Output Clamp Low Register (FILTEROCLPLO)

Address 0006005C – Filter 2 Output Clamp Low Register
Address 0009005C – Filter 1 Output Clamp Low Register
Address 000C005C – Filter 0 Output Clamp Low Register

Bit Number	17:0
Bit Name	OUTPUT_CLAMP_LOW
Access	R/W
Default	00_0000_0000_0000_0000

Bits 17-0: OUTPUT_CLAMP_LOW – Sets the lower limit of filter output value. If calculated filter output falls below this threshold, the filter output will be set to OUTPUT_CLAMP_LOW

10.25 Filter Preset Register (FILTERPRESET)

Address 00060060 – Filter 2 Filter Preset Register
Address 00090060 – Filter 1 Filter Preset Register
Address 000C0060 – Filter 0 Filter Preset Register

Bit Number	27	26:24	23:0
Bit Name	PRESET_EN	PRESET_REG_SEL	PRESET_VALUE
Access	R/W	R/W	R/W
Default	00	000	0000_0000_0000_0000_0000_0000

Bit 27: PRESET_EN – Set to '1' to initiate write of internal filter register (Self cleared by hardware after successful programming)
Bits 26-24: PRESET_REG_SEL – Selects internal filter register to preset by processor
0 = XN_M1 Register (only bits 10:0 of PRESET_VALUE will be programmed into register)
1 = KI_YN Register
2 = KD_YN Register
3 = YN Register
4 = 18-bit Filter Data Register (after multiplication)
Bits 23-0: PRESET_VALUE – Value to preset into selected register

11 Loop Mux Registers Reference

11.1 Front End Control 0 Mux Register (FECTRL0MUX)

Address 00020000

Bit Number	13:12	11
Bit Name	NL_SEL	DPWM3_FRAME_SYNC_EN
Access	R/W	R/W
Default	00	0

Bit Number	10	9
Bit Name	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	DPWM0_FRAME_SYNC_EN	DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bits 13-12: NL_SEL – Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting

0 = Filter 0 NL Results used
1 = Filter 1 NL Results used
2 = Filter 2 NL Results used (Default)

Bit 11: DPWM3_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control

0 = DPWM 3 Frame Sync not routed to Front End Control (Default)
1 = DPWM 3 Frame Sync routed to Front End Control

Bit 10: DPWM2_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control

0 = DPWM 2 Frame Sync not routed to Front End Control (Default)
1 = DPWM 2 Frame Sync routed to Front End Control

Bit 9: DPWM1_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control

0 = DPWM 1 Frame Sync not routed to Front End Control (Default)
1 = DPWM 1 Frame Sync routed to Front End Control

Bit 8: DPWM0_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control

0 = DPWM 0 Frame Sync not routed to Front End Control (Default)
1 = DPWM 0 Frame Sync routed to Front End Control

Bit 7: DPWM3_B_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control

0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-B trigger routed to Front End Control

Bit 6: DPWM2_B_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control

0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-B trigger routed to Front End Control

Bit 5: DPWM1_B_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control

0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-B trigger routed to Front End Control

Bit 4: DPWM0_B_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-B trigger routed to Front End Control

Bit 3: DPWM3_A_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control

0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-A trigger routed to Front End Control

Bit 2: DPWM2_A_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control

0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-A trigger routed to Front End Control

Bit 1: DPWM1_A_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control

0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-A trigger routed to Front End Control

Bit 0: DPWM0_A_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-A trigger routed to Front End Control

11.2 Front End Control 1 Mux Register (FECTRL1MUX)

Address 00020004

Bit Number	13:12	11
Bit Name	NL_SEL	DPWM3_FRAME_SYNC_EN
Access	R/W	R/W
Default	01	0

Bit Number	10	9
Bit Name	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	DPWM0_FRAME_SYNC_EN	DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bits 13-12: NL_SEL – Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting

0 = Filter 0 NL Results used
1 = Filter 1 NL Results used
2 = Filter 2 NL Results used (Default)

Bit 11: DPWM3_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control

0 = DPWM 3 Frame Sync not routed to Front End Control (Default)
1 = DPWM 3 Frame Sync routed to Front End Control

Bit 10: DPWM2_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control

0 = DPWM 2 Frame Sync not routed to Front End Control (Default)
1 = DPWM 2 Frame Sync routed to Front End Control

Bit 9: DPWM1_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control

0 = DPWM 1 Frame Sync not routed to Front End Control (Default)
1 = DPWM 1 Frame Sync routed to Front End Control

Bit 8: DPWM0_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control

0 = DPWM 0 Frame Sync not routed to Front End Control (Default)
1 = DPWM 0 Frame Sync routed to Front End Control

Bit 7: DPWM3_B_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control
0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-B trigger routed to Front End Control
Bit 6: DPWM2_B_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control
0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-B trigger routed to Front End Control
Bit 5: DPWM1_B_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control
0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-B trigger routed to Front End Control
Bit 4: DPWM0_B_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control
0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-B trigger routed to Front End Control
Bit 3: DPWM3_A_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control
0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-A trigger routed to Front End Control
Bit 2: DPWM2_A_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control
0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-A trigger routed to Front End Control
Bit 1: DPWM1_A_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control
0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-A trigger routed to Front End Control
Bit 0: DPWM0_A_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control
0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-A trigger routed to Front End Control

11.3 Front End Control 2 Mux Register (FECTRL2MUX)

Address 00020008

Bit Number	13:12	11
Bit Name	NL_SEL	DPWM3_FRAME_SYNC_EN
Access	R/W	R/W
Default	10	0

Bit Number	10	9
Bit Name	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	DPWM0_FRAME_SYNC_EN	DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bits 13-12: NL_SEL – Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting

0 = Filter 0 NL Results used
1 = Filter 1 NL Results used
2 = Filter 2 NL Results used (Default)

Bit 11: DPWM3_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control

0 = DPWM 3 Frame Sync not routed to Front End Control (Default)
1 = DPWM 3 Frame Sync routed to Front End Control

Bit 10: DPWM2_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control

0 = DPWM 2 Frame Sync not routed to Front End Control (Default)
1 = DPWM 2 Frame Sync routed to Front End Control

Bit 9: DPWM1_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control

0 = DPWM 1 Frame Sync not routed to Front End Control (Default)
1 = DPWM 1 Frame Sync routed to Front End Control

Bit 8: DPWM0_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control

0 = DPWM 0 Frame Sync not routed to Front End Control (Default)
1 = DPWM 0 Frame Sync routed to Front End Control

Bit 7: DPWM3_B_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control
0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-B trigger routed to Front End Control
Bit 6: DPWM2_B_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control
0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-B trigger routed to Front End Control
Bit 5: DPWM1_B_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control
0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-B trigger routed to Front End Control
Bit 4: DPWM0_B_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control
0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-B trigger routed to Front End Control
Bit 3: DPWM3_A_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control
0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-A trigger routed to Front End Control
Bit 2: DPWM2_A_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control
0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-A trigger routed to Front End Control
Bit 1: DPWM1_A_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control
0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-A trigger routed to Front End Control
Bit 0: DPWM0_A_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control
0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-A trigger routed to Front End Control

11.4 Sample Trigger Control Register (SAMPTRIGCTRL)

Address 0002000C

Bit Number	11	10	9
Bit Name	FE2_TRIG_DPWM3_EN	FE2_TRIG_DPWM2_EN	FE2_TRIG_DPWM1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	8	7	6
Bit Name	FE2_TRIG_DPWM0_EN	FE1_TRIG_DPWM3_EN	FE1_TRIG_DPWM2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	FE1_TRIG_DPWM1_EN	FE1_TRIG_DPWM0_EN	FE0_TRIG_DPWM3_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	FE0_TRIG_DPWM2_EN	FE0_TRIG_DPWM1_EN	FE0_TRIG_DPWM0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 11: FE2_TRIG_DPWM3_EN – Enables Sample Trigger from DPWM 3 to Front End Control 2
0 = DPWM 3 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 3 Sample Trigger routed to Front End Control 2
Bit 10: FE2_TRIG_DPWM2_EN – Enables Sample Trigger from DPWM 2 to Front End Control 2
0 = DPWM 2 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 2 Sample Trigger routed to Front End Control 2
Bit 9: FE2_TRIG_DPWM1_EN – Enables Sample Trigger from DPWM 1 to Front End Control 2
0 = DPWM 1 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 1 Sample Trigger routed to Front End Control 2
Bit 8: FE2_TRIG_DPWM0_EN – Enables Sample Trigger from DPWM 0 to Front End Control 2
0 = DPWM 0 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 0 Sample Trigger routed to Front End Control 2
Bit 7: FE1_TRIG_DPWM3_EN – Enables Sample Trigger from DPWM 3 to Front End Control 1
0 = DPWM 3 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 3 Sample Trigger routed to Front End Control 1
Bit 6: FE1_TRIG_DPWM2_EN – Enables Sample Trigger from DPWM 2 to Front End Control 1
0 = DPWM 2 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 2 Sample Trigger routed to Front End Control 1
Bit 5: FE1_TRIG_DPWM1_EN – Enables Sample Trigger from DPWM 1 to Front End Control 1
0 = DPWM 1 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 1 Sample Trigger routed to Front End Control 1

Bit 4: FE1_TRIG_DPWM0_EN – Enables Sample Trigger from DPWM 0 to Front End Control 1
0 = DPWM 0 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 0 Sample Trigger routed to Front End Control 1
Bit 3: FE0_TRIG_DPWM3_EN – Enables Sample Trigger from DPWM 3 to Front End Control 0
0 = DPWM 3 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 3 Sample Trigger routed to Front End Control 0
Bit 2: FE0_TRIG_DPWM2_EN – Enables Sample Trigger from DPWM 2 to Front End Control 0
0 = DPWM 2 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 2 Sample Trigger routed to Front End Control 0
Bit 1: FE0_TRIG_DPWM1_EN – Enables Sample Trigger from DPWM 1 to Front End Control 0
0 = DPWM 1 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 1 Sample Trigger routed to Front End Control 0
Bit 0: FE0_TRIG_DPWM0_EN – Enables Sample Trigger from DPWM 0 to Front End Control 0
0 = DPWM 0 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 0 Sample Trigger routed to Front End Control 0

11.5 External DAC Control Register (EXTDACCTRL)

Address 00020010

Bit Number	26:24	23:19	18:16	15:11	10:8
Bit Name	DAC2_SEL	RESERVED	DAC1_SEL	RESERVED	DAC0_SEL
Access	R/W	-	R/W	-	R/W
Default	000	0_0000	000	0_0000	000

Bit Number	7:3	2	1	0
Bit Name	RESERVED	EXT_DAC2_EN	EXT_DAC1_EN	EXT_DAC0_EN
Access	-	R/W	R/W	R/W
Default	0_0000	0	0	0

Bits 26-24: DAC2_SEL – Configures DAC 2 setpoint in External DAC Mode
0 = DAC 0 Setpoint Selected (Default)
1 = DAC 1 Setpoint Selected
3 = Output of Constant Power Module Selected
4 = Filter 0 Output Selected
5 = Filter 1 Output Selected
6 = Filter 2 Output Selected
Bits 23-19: RESERVED – Unused bits
Bits 18-16: DAC1_SEL – Configures DAC 1 setpoint in External DAC Mode
0 = DAC 0 Setpoint Selected (Default)
2 = DAC 2 Setpoint Selected
3 = Output of Constant Power Module Selected
4 = Filter 0 Output Selected
5 = Filter 1 Output Selected
6 = Filter 2 Output Selected
Bits 15-11: RESERVED – Unused bits
Bits 10-8: DAC0_SEL – Configures DAC 0 setpoint in External DAC Mode
1 = DAC 1 Setpoint Selected
2 = DAC 2 Setpoint Selected
3 = Output of Constant Power Module Selected

4 = Filter 0 Output Selected
5 = Filter 1 Output Selected
6 = Filter 2 Output Selected

Bits 7-3: RESERVED – Unused bits

Bit 2: EXT_DAC2_EN – External DAC 2 Mode Enable
0 = External DAC Mode disabled. DAC 2 setpoint driven from Front End Control Module (Default)
1 = External DAC Mode enabled, DAC 2 setpoint driven by DAC2_SEL configuration

Bit 1: EXT_DAC1_EN – External DAC 1 Mode Enable
0 = External DAC Mode disabled. DAC 1 setpoint driven from Front End Control Module (Default)
1 = External DAC Mode enabled, DAC 1 setpoint driven by DAC1_SEL configuration

Bit 0: EXT_DAC0_EN – External DAC 0 Mode Enable
0 = External DAC Mode disabled. DAC 0 setpoint driven from Front End Control Module (Default)
1 = External DAC Mode enabled, DAC 0 setpoint driven by DAC0_SEL configuration

11.6 Filter Mux Register (FILTERMUX)

Address 00020014

Bit Number	29:28	27:26	25:24
Bit Name	FILTER2_KCOMP_SEL	FILTER1_KCOMP_SEL	FILTER0_KCOMP_SEL
Access	R/W	R/W	R/W
Default	00	00	00

Bit Number	23:19	18	17	16
Bit Name	RESERVED	FILTER2_FFWD_SEL	FILTER1_FFWD_SEL	FILTER0_FFWD_SEL
Access	R/W	R/W	R/W	R/W
Default	0_0000	0	0	0

Bit Number	15:14	13:12	11:10	9:8
Bit Name	RESERVED	FILTER2_PER_SEL	FILTER1_PER_SEL	FILTER0_PER_SEL
Access	R/W	R/W	R/W	R/W
Default	00	00	00	00

Bit Number	7:6	5:4	3:2	1:0
Bit Name	RESERVED	FILTER2_FE_SEL	FILTER1_FE_SEL	FILTER0_FE_SEL
Access	-	R/W	R/W	R/W
Default	00	10	01	00

Bits 29-28: FILTER2_KCOMP_SEL – Selects KComp value routed to Filter 2 Module
0 = KComp 0 Value Selected (Default)
1 = KComp 1 Value Selected
2 = KComp 2 Value Selected

Bits 27-26: FILTER1_KCOMP_SEL – Selects KComp value routed to Filter 1 Module
0 = KComp 0 Value Selected (Default)
1 = KComp 1 Value Selected
2 = KComp 2 Value Selected

Bits 25-24: FILTER0_KCOMP_SEL – Selects KComp value routed to Filter 0 Module
0 = KComp 0 Value Selected (Default)
1 = KComp 1 Value Selected
2 = KComp 2 Value Selected

Bits 23-19: RESERVED – Unused bits

Bit 18: FILTER2_FFWD_SEL – Configures Feedforward value routed to Filter 2 Module
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected

Bit 17: FILTER1_FFWD_SEL – Configures Feedforward value routed to Filter 1 Module
0 = Filter 0 Output Selected (Default)
1 = Filter 2 Output Selected

Bit 16: FILTER0_FFWD_SEL – Configures Feedforward value routed to Filter 0 Module
0 = Filter 1 Output Selected (Default)
1 = Filter 2 Output Selected

Bits 15-14: RESERVED – Unused bits

Bits 13-12: FILTER2_PER_SEL – Selects source of switching cycle period for Filter 2 Module
0 = DPWM 0 Switching Period (Default)
1 = DPWM 1 Switching Period
2 = DPWM 2 Switching Period

3 = DPWM 3 Switching Period

Bits 11-10: FILTER1_PER_SEL – Selects source of switching cycle period for Filter 1 Module

0 = DPWM 0 Switching Period (Default)
1 = DPWM 1 Switching Period
2 = DPWM 2 Switching Period
3 = DPWM 3 Switching Period

Bits 9-8: FILTER0_PER_SEL – Selects source of switching cycle period for Filter 0 Module

0 = DPWM 0 Switching Period (Default)
1 = DPWM 1 Switching Period
2 = DPWM 2 Switching Period
3 = DPWM 3 Switching Period

Bits 7-6: RESERVED – Unused bits

Bits 5-4: FILTER2_FE_SEL – Selects which Front End Module provides data for Filter 2 Module

0 = Front End Module 0 provides data to Filter
1 = Front End Module 1 provides data to Filter
2 = Front End Module 2 provides data to Filter (Default)

Bits 3-2: FILTER1_FE_SEL – Selects which Front End Module provides data for Filter 1 Module

0 = Front End Module 0 provides data to Filter
1 = Front End Module 1 provides data to Filter (Default)
2 = Front End Module 2 provides data to Filter

Bits 1-0: FILTER0_FE_SEL – Selects which Front End Module provides data for Filter 0 Module

0 = Front End Module 0 provides data to Filter (Default)
1 = Front End Module 1 provides data to Filter
2 = Front End Module 2 provides data to Filter

11.7 Filter KComp A Register (FILTERKCOMPA)

Address 00020018

Bit Number	29:16	15:14	13:0
Bit Name	KCOMP1	RESERVED	KCOMP0
Access	R/W	-	R/W
Default	00_0000_0000_0000	00	00_0000_0111_1101

Bits 29-16: KCOMP1 – 14-bit value used in filter output calculations replacing the DPWM switching period value
Bits 15-14: RESERVED – Unused bits
Bits 13-0: KCOMP0 – 14-bit value used in filter output calculations replacing the DPWM switching period value

11.8 Filter KComp B Register (FILTERKCOMPB)

Address 0002001C

Bit Number	13:0
Bit Name	KCOMP2
Access	R/W
Default	00_0000_0000_0000

Bits 13-0: KCOMP2 – 14-bit value used in filter output calculations replacing the DPWM switching period value

11.9 DPWM Mux Register (DPWMMUX)

Address 00020020

Bit Number	31:30	29:28
Bit Name	DPWM3_SYNC_FET_SEL	DPWM2_SYNC_FET_SEL
Access	R/W	R/W
Default	00	00

Bit Number	27:26	25:24
Bit Name	DPWM1_SYNC_FET_SEL	DPWM0_SYNC_FET_SEL
Access	R/W	R/W
Default	00	00

Bit Number	23:20	19:18	17:16
Bit Name	RESERVED	DPWM3_SYNC_SEL	DPWM2_SYNC_SEL
Access	-	R/W	R/W
Default	0000	00	00

Bit Number	15:14	13:12	11:9
Bit Name	DPWM1_SYNC_SEL	DPWM0_SYNC_SEL	DPWM3_FILTER_SEL
Access	R/W	R/W	R/W
Default	00	00	010

Bit Number	8:6	5:3	2:0
Bit Name	DPWM2_FILTER_SEL	DPWM1_FILTER_SEL	DPWM0_FILTER_SEL
Access	R/W	R/W	R/W
Default	010	001	000

Bits 31-30: DPWM3_SYNC_FET_SEL – Selects Ramp source for DPWM3 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected

Bits 29-28: DPWM2_SYNC_FET_SEL – Selects Ramp source for DPWM2 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected

Bits 27-26: DPWM1_SYNC_FET_SEL – Selects Ramp source for DPWM1 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected

Bits 25-24: DPWM0_SYNC_FET_SEL – Selects Ramp source for DPWM0 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected

Bits 23-20: RESERVED – Unused bits

Bits 19-18: DPWM3_SYNC_SEL – Selects Master Sync for DPWM 3 when DPWM 3 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 17-16: DPWM2_SYNC_SEL – Selects Master Sync for DPWM 2 when DPWM 2 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 15-14: DPWM1_SYNC_SEL – Selects Master Sync for DPWM 1 when DPWM 1 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 13-12: DPWM0_SYNC_SEL – Selects Master Sync for DPWM 0 when DPWM 0 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 11-9: DPWM3_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 3
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register
Bits 8-6: DPWM2_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 2
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register
Bits 5-3: DPWM1_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 1
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register
Bits 2-0: DPWM0_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 0
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register

11.10 Constant Power Control Register (CPCTRL)

Address 00020024

Bit Number	15	14	13	12
Bit Name	DAC_COMP_EN	FW_DIVISOR_EN	LOWER_COMP_EN	VLOOP_FREEZE_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	11:10	9:8	7:5	4:3
Bit Name	VLOOP_SEL	CLOOP_SEL	THRESH_SEL	DIVISOR_SEL
Access	R/W	R/W	R/W	R/W
Default	00	00	000	00

Bit Number	2	1	0
Bit Name	CPCC_INT_EN	CPCC_CONFIG	CPCC_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 15: DAC_COMP_EN – Enables comparison of DAC Setpoint and quotient of Max Power/Sense Current in Loop Switching Mode. Minimum of DAC setpoint and calculated quotient sets voltage loop setpoint in Constant Voltage and Constant Power modes

0 = Operating Mode controls Voltage Loop DAC Setpoint (Default)
1 = Minimum of DAC setpoint and calculated quotient used as Voltage Loop DAC Setpoint

Bit 14: FW_DIVISOR_EN – Enables Firmware value for divisor in Constant Power calculations

0 = Divisor selected by **DIVISOR_SEL** (Bits 7:6) (Default)
1 = Divisor driven by Firmware Current Register

Bit 13: LOWER_COMP_EN – Enables output of lowest duty from current or voltage loop when Constant Power/Constant Current module controls loop output

0 = Loop output controlled by mode selection, voltage loop selected in constant voltage and constant power mode, current loop selected in constant current mode (Default)
1 = Loop output controlled by lowest duty from voltage or current loops

Bit 12: VLOOP_FREEZE_EN – Enables freezing of Voltage Loop Integrator when current loop selected in Loop Switching configuration

0 = Freezing of Voltage Loop Integrator disabled (Default)
1 = Freezing of Voltage Loop Integrator enabled

Bits 11-10: VLOOP_SEL – Configures voltage loop for loop switching mode

0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected

Bits 9-8: CLOOP_SEL – Configures current loop for loop switching mode

0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected

Bits 7-5: THRESH_SEL – Configures input threshold selected for use in Constant Power comparison

0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Front End 0 Absolute Value Data Selected
4 = Front End 1 Absolute Value Data Selected
5 = Front End 2 Absolute Value Data Selected

Bits 4-3: DIVISOR_SEL – Configures value used for divisor in Constant Power calculations

0 = Front End 0 Absolute Value Data Selected (Default)
1 = Front End 1 Absolute Value Data Selected
2 = Front End 2 Absolute Value Data Selected

Bit 2: CPCC_INT_EN – Constant Power/Constant Current Interrupt Enable
0 = Interrupt disabled on mode switches (Default)
1 = Interrupt enabled on mode switches

Bit 1: CPCC_CONFIG – Controls Constant Power/Constant Current module configuration
0 = Average Current Mode (Default)
1 = Constant Power Module controls selection of voltage/current loop

Bit 0: CPCC_EN – Constant Power Constant/Current Module Enable
0 = Constant Power/Constant Current Module disabled (Default)
1 = Constant Power/Constant Current Module enabled

11.11 Constant Power Nominal Threshold Register (CPNOM)

Address 00020028

Bit Number	25:16	15:10	9:0
Bit Name	NOM_CURRENT_UPPER	RESERVED	NOM_CURRENT_LOWER
Access	R/W	-	R/W
Default	00_0000_0000	00_0000	00_0000_0000

Bits 25-16: NOM_CURRENT_UPPER – Configures I_{NOM} value used in Constant Power/Constant Current Calculations, when sensed value exceeds NOM_CURRENT_UPPER in Constant Voltage mode, setpoint will switch to Constant Power mode
Bits 15-10: RESERVED – Unused Bits
Bits 9-0: NOM_CURRENT_LOWER – Configures I_{NOM} value used in Constant Power/Constant Current Calculations, when sensed value falls below NOM_CURRENT_LOWER in Constant Power mode, setpoint will switch to Constant Voltage mode

11.12 Constant Power Max Threshold Register (CPMAX)

Address 0002002C

Bit Number	25:16	15:10	9:0
Bit Name	MAX_CURRENT_UPPER	RESERVED	MAX_CURRENT_LOWER
Access	R/W	-	R/W
Default	00_0000_0000	00_0000	00_0000_0000

Bits 25-16: MAX_CURRENT_UPPER – Configures I_{MAX} value used in Constant Power/Constant Current Calculations, when sensed value exceeds MAX_CURRENT_UPPER in Constant Power mode, setpoint will switch to Max Current mode
Bits 15-10: RESERVED – Unused Bits
Bits 9-0: MAX_CURRENT_LOWER – Configures I_{MAX} value used in Constant Power/Constant Current Calculations, when sensed value falls below MAX_CURRENT_LOWER in Max Current mode, setpoint will switch to Constant Power mode

11.13 Constant Power Configuration Register (CPCONFIG)

Address 00020030

Bit Number	25:16	15:10	9:0

Bit Name	MAX_CURRENT	RESERVED	NOM_VOLTAGE
Access	R/W	-	R/W
Default	00_0000_0000	00_0000	00_0000_0000

Bits 25-16: MAX_CURRENT – Configures I_{MAX} setpoint used in Constant Power/Constant Current Calculations in Max Current mode
Bits 15-10: RESERVED – Unused Bits
Bits 9-0: NOM_VOLTAGE – Configures V_{NOM} setpoint used in Constant Power/Constant Current Calculations in Constant Voltage mode (Loop Oring configuration selected)

11.14 Constant Power Max Power Register (CPMAXPWR)

Address 00020034

Bit Number	19:0
Bit Name	MAX_POWER
Access	R/W
Default	0000_0000_0000_0000_0000

Bits 19-0: MAX_POWER – Configures P_{MAX} value used in Constant Power/Constant Current calculations in Constant Power mode

11.15 Constant Power Integrator Threshold Register (CPINTTHRESH)

Address 00020038

Bit Number	23:0
Bit Name	INT_THRESH
Access	R/W
Default	0000_0000_0000_0000_0000

Bits 23-0: INT_THRESH – 24-bit signed value added to Current Loop Duty value to determine when to freeze Current Loop Integrator

11.16 Constant Power Firmware Divisor Register (CPFWDIVISOR)

Address 0002003C

Bit Number	9:0
Bit Name	FW_DIVISOR
Access	R/W
Default	00_0000_0000

Bits 9-0: FW_DIVISOR– 10-bit value used in Constant Power calculation when firmware value is selected in Bit 17 of Constant Power Control Register

11.17 Constant Power Status Register (CPSTAT)

Address 00020040

Bit Number	8	7	6
Bit Name	CONSTANT_CUR	CONSTANT_PWR	CONSTANT_VOLT
Access	R	R	R
Default	-	-	-

Bit Number	5	4	3
Bit Name	CC_TO_CV_INT	CV_TO_CC_INT	CC_TO_CP_INT
Access	R	R	R
Default	-	-	-

Bit Number	2	1	0
Bit Name	CP_TO_CC_INT	CP_TO_CV_INT	CV_TO_CP_INT
Access	R	R	R
Default	-	-	-

Bit 8: CONSTANT_CUR – Constant Current Mode Indication
0 = Constant Current Mode not enabled
1 = Constant Current Mode enabled
Bit 7: CONSTANT_PWR – Constant Power Mode Indication
0 = Constant Power Mode not enabled
1 = Constant Power Mode enabled
Bit 6: CONSTANT_VOLT – Constant Voltage Mode Indication
0 = Constant Voltage Mode not enabled
1 = Constant Voltage Mode enabled
Bit 5: CC_TO_CV_INT – Constant Current Mode to Constant Voltage Mode latched status, cleared on read
0 = No transition from Constant Current to Constant Voltage detected
1 = Transition from Constant Current to Constant Voltage detected
Bit 4: CV_TO_CC_INT – Constant Voltage Mode to Constant Current Mode latched status, cleared on read
0 = No transition from Constant Voltage to Constant Current detected
1 = Transition from Constant Voltage to Constant Current detected
Bit 3: CC_TO_CP_INT – Constant Current Mode to Constant Power Mode latched status, cleared on read
0 = No transition from Constant Current to Constant Power detected
1 = Transition from Constant Current to Constant Power detected
Bit 2: CP_TO_CC_INT – Constant Power Mode to Constant Current Mode latched status, cleared on read
0 = No transition from Constant Power to Constant Current detected
1 = Transition from Constant Power to Constant Current detected
Bit 1: CP_TO_CV_INT – Constant Power Mode to Constant Voltage Mode latched status, cleared on read
0 = No transition from Constant Power to Constant Voltage detected
1 = Transition from Constant Power to Constant Voltage detected
Bit 0: CV_TO_CP_INT – Constant Voltage Mode to Constant Power Mode latched status, cleared on read
0 = No transition from Constant Voltage to Constant Power detected
1 = Transition from Constant Voltage to Constant Power detected

11.18 Cycle Adjustment Control Register (CYCADJCTRL)

Address 00020044

Bit Number	9:7	6:5
Bit Name	CYC_ADJ_GAIN	CYC_ADJ_SYNC
Access	R/W	R/W
Default	000	00

Bit Number	4:3	2:1	0
Bit Name	SECOND_SAMPLE_SEL	FIRST_SAMPLE_SEL	CYC_ADJ_EN
Access	R/W	R/W	R/W
Default	00	00	0

Bits 9-7: CYC_ADJ_GAIN – Configures gain of Cycle Adjustment calculation
- 0 = 1x gain (Default)
- 1 = 2x gain
- 2 = 4x gain
- 3 = 8x gain
- 4 = 16x gain
- 5 = 32x gain
- 6 = 64x gain
- 7 = 128x gain

Bits 6-5: CYC_ADJ_SYNC – Selects which DPWM A trigger synchronizes cycle adjustment calculation, first 2 samples after receipt of DPWM A trigger will be used for Cycle Adjustment Calculation.
- 0 = DPWM-1A trigger selected (Default)
- 1 = DPWM-2A trigger selected
- 2 = DPWM-3A trigger selected
- 3 = DPWM-4A trigger selected

Bits 4-3: SECOND_SAMPLE_SEL – Configures Front End Module Data used for Second Sample of Cycle Adjustment Calculation
- 0 = Front End Module 0 Error Data selected (Default)
- 1 = Front End Module 1 Error Data selected
- 2 = Front End Module 2 Error Data selected

Bits 2-1: FIRST_SAMPLE_SEL – Configures Front End Module Data used for First Sample of Cycle Adjustment Calculation
- 0 = Front End Module 0 Error Data selected (Default)
- 1 = Front End Module 1 Error Data selected
- 2 = Front End Module 2 Error Data selected

Bit 0: CYC_ADJ_EN – Cycle Adjustment Calculation Enable
- 0 = Cycle Adjustment Calculation disabled (Default)
- 1 = Cycle Adjustment Calculation enabled

11.19 Cycle Adjustment Limit Register (CYCADJLIM)

Address 00020048

Bit Number	28:16	15:13	12:0
Bit Name	CYC_ADJ_UPPER_LIMIT	RESERVED	CYC_ADJ_LOWER_LIM
Access	R/W	-	R/W
Default	0_0000_0000_0000	000	0_0000_0000_0000

Bits 28-16: CYC_ADJ_UPPER_LIMT – Cycle Adjustment Calculation signed upper limit value, output of Cycle Adjustment Calculation is clamped at the upper limit, if calculated

result exceeds the upper limit. LSB resolution equals High Frequency Oscillator period/16.
Bits 15-13: RESERVED – Unused Bits
Bits 12-0: CYC_ADJ_LOWER_LIMT – Cycle Adjustment Calculation signed lower limit value, output of Cycle Adjustment Calculation is clamped at the lower limit, if calculated result falls below the lower limit. LSB resolution equals High Frequency Oscillator period/16.

11.20 Cycle Adjustment Status Register (CYCADJSTAT)

Address 0002004C

Bit Number	28:16	15:10	9:0
Bit Name	CYC_ADJ_CALC	RESERVED	CYC_ADJ_ERROR
Access	R	-	R
Default	-	00_0000	-

Bits 28-16: CYC_ADJ_CALC – 13-bit signed value representing calculated Cycle Adjustment provided to DPWM module based on first 2 error samples
Bits 15-10: RESERVED – Unused Bits
Bits 9-0: CYC_ADJ_ERROR – 10-bit signed value representing calculated error of the first 2 error samples received

11.21 Global Enable Register (GLBEN)

Address 00020050

Bit Number	10	9	8	7:4
Bit Name	FE_CTRL2_EN	FE_CTRL1_EN	FE_CTRL0_EN	RESERVED
Access	R/W	R/W	R/W	-
Default	0	0	0	0000

Bit Number	3	2	1	0
Bit Name	DPWM3_EN	DPWM2_EN	DPWM1_EN	DPWM0_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 10: FE_CTRL2_EN – Global Firmware Enable for Front End Control 2 Module

0 = Front End Control 2 Module Disabled (Default)
1 = Front End Control 2 Module Enabled

Bit 9: FE_CTRL1_EN – Global Firmware Enable for Front End Control 1 Module
0 = Front End Control 1 Module Disabled (Default)
1 = Front End Control 1 Module Enabled

Bit 8: FE_CTRL0_EN – Global Firmware Enable for Front End Control 0 Module
0 = Front End Control 0 Module Disabled (Default)
1 = Front End Control 0 Module Enabled

Bits 7-4: RESERVED – Unused Bits

Bit 3: DPWM3_EN – Global Firmware Enable for DPWM 3 Module 0 = DPWM 3 Module Disabled (Default)
1 = DPWM 3 Module Enabled

Bit 2: DPWM2_EN – Global Firmware Enable for DPWM 2 Module 0 = DPWM 2 Module Disabled (Default)
1 = DPWM 2 Module Enabled

Bit 1: DPWM1_EN – Global Firmware Enable for DPWM 1 Module 0 = DPWM 1 Module Disabled (Default)
1 = DPWM 1 Module Enabled

Bit 0: DPWM0_EN – Global Firmware Enable for DPWM 0 Module 0 = DPWM 0 Module Disabled (Default)
1 = DPWM 0 Module Enabled

11.22 PWM Global Period Register (PWMGLBPRD)

Address 00020054

Bit Number	17:4	3:0
Bit Name	PRD	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bits 17-4: PRD – Global PWM Period value, overriding DPWM Period settings when global PWM period is selected within each DPWM module
Bits 3-0: RESERVED – Unused Bits

11.23 Sync Control Register (SYNCCTRL)

Address 00020058

Bit Number	5	4:2	1	0
Bit Name	SYNC_IN	SYNC_MUX_SEL	SYNC_OUT	SYNC_DIR
Access	R	R/W	R/W	R/W
Default	-	000	1	1

Bit 5: SYNC_IN – Value of Sync pin
0 = Logic level low present on Sync pin
1 = Logic level high present on Sync pin
Bits 4-2: SYNC_MUX_SEL – Selects which module controls Sync pin output
000 = DPWM 0 Sync Output (Default)
001 = DPWM 1 Sync Output
010 = DPWM 2 Sync Output
011 = DPWM 3 Sync Output
100 = Value from SYNC_OUT (Bit 1)
101 = Value from CLKOUT signal in TSAR Module (See Section 15.1)
110 = Low-Frequency Oscillator Clock Output
111 = Driven low
Bit 1: SYNC_OUT – Configure output value for Sync pin, if used as an output
0 = Sync pin driven low in output mode
1 = Sync pin driven high in output mode (Default)
Bit 0: SYNC_DIR – Configure direction of Sync pin
0 = Sync pin configured as an output pin
1 = Sync pin configured as an input pin (Default)

11.24 Light Load Control Register (LLCTRL)

Address 0002005C

Bit Number	25:8	7:4	3	2:1	0
Bit Name	DPWM_ON_TIME	RESERVED	CYCLE_CNT_EN	LL_FILTER_SEL	LL_EN
Access	R/W	-	R/W	R/W	R/W
Default	00_0000_0000_0000_0000	0000	0	00	0

Bits 25-8: DPWM_ON_TIME – DPWM pulse width used for EADC-based light load mode operation, when selected Filter data exceeds TURN_ON_THRESH value
Bits 7-3: RESERVED – Unused Bits
Bit 3: CYCLE_CNT_EN – Enables Switching Cycle Counter for enabling constant pulse widths when configured in Light Load operation
0 = Switching Cycle Counter disabled (Default)
1 = Switching Cycle Counter enabled
Bits 2-1: LL_FILTER_SEL – Configures source of filter data for Light Load comparisons
0 = Filter 0 data selected (Default)
1 = Filter 1 data selected
2 = Filter 2 data selected
Bit 0: LL_EN – EADC-based Light Load Mode Enable
0 = Light Load Mode disabled (Default)
1 = Light Load Mode enabled

11.25 Light Load Enable Threshold Register (LLENTHRESH)

Address 00020060

Bit Number	31:24	23:18	17:0
Bit Name	CYCLE_CNT_THRESH	RESERVED	TURN_ON_THRESH
Access	R/W	-	R/W
Default	0000_0000	0000_00	00_0000_0000_0000_0000

Bits 31-24: CYCLE_CNT_THRESH – Switching Cycle threshold where constant width DPWM pulses are enabled when number of switching cycles without pulses exceeds threshold
Bits 23-18: RESERVED – Unused Bits
Bits 17-0: TURN_ON_THRESH – Filter data threshold where constant width DPWM pulses are enabled when filter data exceeds threshold

11.26 Light Load Disable Threshold Register (LLDISTHRESH)

Address 00020064

Bit Number	17:0
Bit Name	TURN_OFF_THRESH
Access	R/W
Default	00_0000_0000_0000_0000

Bits 17-0: TURN_OFF_THRESH – Filter data threshold where constant width DPWM pulses are disabled when filter data falls below threshold

11.27 Peak Current Mode Control Register (PCMCTRL)

Address 00020068

Bit Number	5:4	3:0
Bit Name	PCM_FILTER_SEL	RESERVED
Access	R/W	-
Default	00	0000

Bits 5-4: PCM_FILTER_SEL – Selects source of Peak Current Slope Compensation Ramp Start

0 = Filter 0 data selected (Default)
1 = Filter 1 data selected
2 = Filter 2 data selected
3 = Constant Power/Constant Current data selected

Bits 3-0: Reserved

11.28 Analog Peak Current Mode Control Register (APCMCTRL)

Address 00020070

Bit Number	3	2:1	0
Bit Name	PCM_LATCH_EN	PCM_FE_SEL	PCM_EN
Access	R/W	R/W	R/W
Default	0	00	0

Bit 3: PCM_LATCH_EN – Enables latching of Peak Current Flag to end of frame

0 = PCM Flag is not latched to end of PCM Frame (Default)
1 = PCM Flag is latched to end of PCM Frame

Bits 2-1: PCM_FE_SEL – Selects source of Front End Comparator output for Analog Peak Current Mode Control

0 = Front End Control 0 Comparator output selected (Default)
1 = Front End Control 1 Comparator output selected
2 = Front End Control 2 Comparator output selected

Bit 0: PCM_EN – Analog Peak Current Mode Control Module Enable

0 = Analog Peak Current Mode Control Module disabled (Default)
1 = Analog Peak Current Mode Control Module enabled

11.29 Loop Mux Test Register (LOOPMUXTEST) (Test Use Only)

Address 00020074

Bit Number	18	17	16	15:10
Bit Name	BIST_COMP	BIST_EN	EADC_TRIM_TEST_EN	EADC_REF_TRIM
Access	R	R/W	R/W	R/W
Default	-	0	0	000000

Bit Number	9	8	7:2	1:0
Bit Name	EADC_REF_RESET	EADC_REF_EN	GAIN_TRIM	AFE_GAIN
Access	R/W	R/W	R/W	R/W
Default	1	0	0000_00	11

Bit 18: BIST_COMP – High-Speed Loop BIST Complete Status
0 = High-Speed Loop BIST not complete
1 = High-Speed Loop BIST completed
Bit 17: BIST_EN – High-Speed Loop BIST Enable
0 = High-Speed Loop BIST disabled (Default)
1 = High-Speed Loop BIST enabled
Bit 16: EADC_TRIM_TEST_EN – EADC Trim Test Mode Enable
0 = EADC Trim Test Mode disabled (Default)
1 = EADC Trim Test Mode enabled, bits 15:0 provided to all 3 Analog Front End modules
Bits 15-10: EADC_REF_TRIM – EADC Reference Trim Value. Bits will be programmed during test and should not be overwritten by firmware.
Bit 9: EADC_REF_RESET – EADC Reference Reset
0 = Reference not in reset
1 = Resets Reference (Default)
Bit 8: EADC_REF_EN – EADC Reference Enable
0 = Disables EADC Reference (Default)
1 = Enables EADC Reference
Bits 7-2: GAIN_TRIM – Sets trim for EADC Gain.
Bits 1-0: AFE_GAIN – AFE Front End Gain Setting
0 = 1x Gain, 8mV/LSB
1 = 2x Gain, 4mV/LSB
2 = 4x Gain, 2mV/LSB
3 = 8x Gain, 1mV/LSB (Default)

12 Fault Mux Registers Reference

12.1 Analog Comparator Control 0 Register (ACOMPCTRL0)

Address 00030000

Bit Number	30:24	23:22	21:19	18
Bit Name	ACOMP_B_THRESH	RESERVED	ACOMP_B_SEL	ACOMP_B_POL
Access	R/W	-	R/W	R/W
Default	000_0000	00	000	1

Bit Number	17	16:15	14:8	7:6
Bit Name	ACOMP_B_INT_EN	RESERVED	ACOMP_A_THRESH	RESERVED
Access	R/W	-	R/W	-
Default	0	00	000_0000	00

Bit Number	5:3	2	1	0
Bit Name	ACOMP_A_SEL	ACOMP_A_POL	ACOMP_A_INT_EN	ACOMP_EN
Access	R/W	R/W	R/W	R/W
Default	000	1	0	0

Bits 30-24: ACOMP_B_THRESH – Configures Analog Comparator B Threshold value
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V
Bits 23-22: RESERVED – Unused bits
Bits 21-19: ACOMP_B_SEL – Configures Analog Comparator B Threshold
0 = Analog Comparator B Threshold set by ACOMP_B_THRESH (Default)
1 = Analog Comparator B Threshold set by Comparator Ramp 0
2 = Analog Comparator B Threshold set by Filter 0 Output
3 = Analog Comparator B Threshold set by Filter 1 Output
4 = Analog Comparator B Threshold set by Filter 2 Output
Bit 18: ACOMP_B_POL – Analog Comparator B Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)
Bit 17: ACOMP_B_INT_EN – Analog Comparator B Interrupt Enable
0 = Disables Analog Comparator B Interrupt generation (Default)
1 = Enables Analog Comparator B Interrupt generation
Bits 16-15: RESERVED – Unused bits
Bits 14-8: ACOMP_A_THRESH – Configures Analog Comparator A Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V
Bits 7-6: RESERVED – Unused bits
Bits 5-3: ACOMP_A_SEL – Configures Analog Comparator A Threshold
0 = Analog Comparator A Threshold set by ACOMP_A_THRESH (Default)
1 = Analog Comparator A Threshold set by Comparator Ramp 0
2 = Analog Comparator A Threshold set by Filter 0 Output
3 = Analog Comparator A Threshold set by Filter 1 Output
4 = Analog Comparator A Threshold set by Filter 2 Output

Bit 2: ACOMP_A_POL – Analog Comparator A Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)
Bit 1: ACOMP_A_INT_EN – Analog Comparator A Interrupt Enable
0 = Disables Analog Comparator A Interrupt generation (Default)
1 = Enables Analog Comparator A Interrupt generation
Bit 0: ACOMP_EN – Analog Comparators Enable
0 = Analog Comparators Disabled (Default)
1 = Analog Comparators Enabled

12.2 Analog Comparator Control 1 Register (ACOMPCTRL1)

Address 00030004

Bit Number	30:24	23:22	21:19	18
Bit Name	ACOMP_D_THRESH	RESERVED	ACOMP_D_SEL	ACOMP_D_POL
Access	R/W	-	R/W	R/W
Default	000_0000	00	000	1

Bit Number	17	16	15	14:8
Bit Name	ACOMP_D_INT_EN	ACOMP_D_OUT_EN	RESERVED	ACOMP_C_THRESH
Access	R/W	R/W	-	R/W
Default	0	0	0	000_0000

Bit Number	7:6	5:3	2	1	0
Bit Name	RESERVED	ACOMP_C_SEL	ACOMP_C_POL	ACOMP_C_INT_EN	RESERVED
Access	-	R/W	R/W	R/W	-
Default	00	000	1	0	0

Bits 30-24: ACOMP_D_THRESH – Configures Analog Comparator D Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V
Bits 23-22: RESERVED – Unused bits
Bits 21-19: ACOMP_D_SEL – Configures Analog Comparator D Threshold
0 = Analog Comparator D Threshold set by ACOMP_D_THRESH (Default)
1 = Analog Comparator D Threshold set by Comparator Ramp 0
2 = Analog Comparator D Threshold set by Filter 0 Output
3 = Analog Comparator D Threshold set by Filter 1 Output
4 = Analog Comparator D Threshold set by Filter 2 Output
Bit 18: ACOMP_D_POL – Analog Comparator D Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)
Bit 17: ACOMP_D_INT_EN – Analog Comparator D Interrupt Enable
0 = Disables Analog Comparator D Interrupt generation (Default)
1 = Enables Analog Comparator D Interrupt generation
Bit 16: ACOMP_D_OUT_EN – Analog Comparator D DAC Output Enable
0 = Disables output of Comparator DAC D onto AD pin (Default)
1 = Enables output of Comparator DAC D onto AD pin
Bit 15: RESERVED – Unused bit
Bits 14-8: ACOMP_C_THRESH – Configures Analog Comparator C Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV

……..
127 = Comparator Reference of 2.5 V

Bits 7-6: RESERVED – Unused bits

Bits 5-3: ACOMP_C_SEL – Configures Analog Comparator C Threshold
0 = Analog Comparator C Threshold set by ACOMP_C_THRESH (Default)
1 = Analog Comparator C Threshold set by Comparator Ramp 0
2 = Analog Comparator C Threshold set by Filter 0 Output
3 = Analog Comparator C Threshold set by Filter 1 Output
4 = Analog Comparator C Threshold set by Filter 2 Output

Bit 2: ACOMP_C_POL – Analog Comparator C Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 1: ACOMP_C_INT_EN – Analog Comparator C Interrupt Enable
0 = Disables Analog Comparator C Interrupt generation (Default)
1 = Enables Analog Comparator C Interrupt generation

Bit 0: RESERVED – Unused bit

12.3 Analog Comparator Control 2 Register (ACOMPCTRL2)

Address 00030008

Bit Number	30:24	23	22	21:19
Bit Name	ACOMP_F_THRESH	RESERVED	ACOMP_F_REF_SEL	ACOMP_F_SEL
Access	R/W	-	R/W	R/W
Default	000_0000	0	0	000

Bit Number	18	17	16	15
Bit Name	ACOMP_F_POL	ACOMP_F_INT_EN	ACOMP_F_OUT_EN	RESERVED
Access	R/W	R/W	R/W	-
Default	1	0	0	0

Bit Number	14:8	7:6	5:3
Bit Name	ACOMP_E_THRESH	RESERVED	ACOMP_E_SEL
Access	R/W	-	R/W
Default	000_0000	00	000

Bit Number	2	1	0
Bit Name	ACOMP_E_POL	ACOMP_E_INT_EN	ACOMP_E_OUT_EN
Access	R/W	R/W	R/W
Default	1	0	0

Bits 30-24: ACOMP_F_THRESH – Configures Analog Comparator F Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V
Bit 23: RESERVED – Unused bit
Bit 22: ACOMP_F_REF_SEL – Analog Comparator F Reference Select
0 = Selects internal DAC reference (Default)
1 = Selects reference driven from AD-07 pin
Bits 21-19: ACOMP_F_SEL – Configures Analog Comparator F Threshold
0 = Analog Comparator F Threshold set by ACOMP_F_THRESH (Default)
1 = Analog Comparator F Threshold set by Comparator Ramp 0
2 = Analog Comparator F Threshold set by Filter 0 Output
3 = Analog Comparator F Threshold set by Filter 1 Output
4 = Analog Comparator F Threshold set by Filter 2 Output
Bit 18: ACOMP_F_POL – Analog Comparator F Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)
Bit 17: ACOMP_F_INT_EN – Analog Comparator F Interrupt Enable
0 = Disables Analog Comparator F Interrupt generation (Default)
1 = Enables Analog Comparator F Interrupt generation
Bit 16: ACOMP_F_OUT_EN – Analog Comparator F DAC Output Enable
0 = Disables output of Comparator DAC F onto AD pin (Default)
1 = Enables output of Comparator DAC F onto AD pin
Bit 15: RESERVED – Unused bit
Bits 14-8: ACOMP_E_THRESH – Configures Analog Comparator E Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV

……..
127 = Comparator Reference of 2.5 V

Bits 7-6: RESERVED – Unused bits

Bits 5-3: ACOMP_E_SEL – Configures Analog Comparator E Threshold
0 = Analog Comparator E Threshold set by ACOMP_E_THRESH (Default)
1 = Analog Comparator E Threshold set by Comparator Ramp 0
2 = Analog Comparator E Threshold set by Filter 0 Output
3 = Analog Comparator E Threshold set by Filter 1 Output
4 = Analog Comparator E Threshold set by Filter 2 Output

Bit 2: ACOMP_E_POL – Analog Comparator E Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 1: ACOMP_E_INT_EN – Analog Comparator E Interrupt Enable
0 = Disables Analog Comparator E Interrupt generation (Default)
1 = Enables Analog Comparator E Interrupt generation

Bit 0: ACOMP_E_OUT_EN – Analog Comparator E DAC Output Enable
0 = Disables output of Comparator DAC E onto AD pin (Default)
1 = Enables output of Comparator DAC E onto AD pin

12.4 Analog Comparator Control 3 Register (ACOMPCTRL3)

Address 0003000C

Bit Number	14:8	7:6	5:3
Bit Name	ACOMP_G_THRESH	RESERVED	ACOMP_G_SEL
Access	R/W	-	R/W
Default	000_0000	00	000

Bit Number	2	1	0
Bit Name	ACOMP_G_POL	ACOMP_G_INT_EN	ACOMP_G_OUT_EN
Access	R/W	R/W	R/W
Default	1	0	0

Bits 14-8: ACOMP_G_THRESH – Configures Analog Comparator G Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V

Bits 7-6: RESERVED – Unused bits

Bits 5-3: ACOMP_G_SEL – Configures Analog Comparator G Threshold
0 = Analog Comparator G Threshold set by ACOMP_G_THRESH (Default)
1 = Analog Comparator G Threshold set by Comparator Ramp 0
2 = Analog Comparator G Threshold set by Filter 0 Output
3 = Analog Comparator G Threshold set by Filter 1 Output
4 = Analog Comparator G Threshold set by Filter 2 Output

Bit 2: ACOMP_G_POL – Analog Comparator G Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 1: ACOMP_G_INT_EN – Analog Comparator G Interrupt Enable
0 = Disables Analog Comparator G Interrupt generation (Default)
1 = Enables Analog Comparator G Interrupt generation

Bit 0: ACOMP_G_OUT_EN – Analog Comparator G DAC Output Enable
0 = Disables output of Comparator DAC G onto AD pin (Default)
1 = Enables output of Comparator DAC G onto AD pin

12.5 External Fault Control Register (EXTFAULTCTRL)

Address 00030010

Bit Number	11	10	9	8
Bit Name	FAULT3_POL	FAULT2_POL	FAULT1_POL	FAULT0_POL
Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit Number	7	6	5	4
Bit Name	FAULT3_INT_EN	FAULT2_INT_EN	FAULT1_INT_EN	FAULT0_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	FAULT3_DET_EN	FAULT2_DET_EN	FAULT1_DET_EN	FAULT0_DET_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 11: FAULT3_POL – Polarity configuration for FAULT[3] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 10: FAULT2_POL – Polarity configuration for FAULT[2] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 9: FAULT1_POL – Polarity configuration for FAULT[1] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 8: FAULT0_POL – Polarity configuration for FAULT[0] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 7: FAULT3_INT_EN – FAULT[3] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 6: FAULT2_INT_EN – FAULT[2] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 5: FAULT1_INT_EN – FAULT[1] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 4: FAULT0_INT_EN – FAULT[0] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 3: FAULT3_DET_EN – FAULT[3] Pin Detection Enable
0 = Fault Detection Disabled (Default)
1 = Fault Detection Enabled
Bit 2: FAULT2_DET_EN – FAULT[2] Pin Detection Enable
0 = Fault Detection Disabled (Default)
1 = Fault Detection Enabled
Bit 1: FAULT1_DET_EN – FAULT[1] Pin Detection Enable
0 = Fault Detection Disabled (Default)
1 = Fault Detection Enabled
Bit 0: FAULT0_DET_EN – FAULT[0] Pin Detection Enable
0 = Fault Detection Disabled (Default)

1 = Fault Detection Enabled

12.6 Fault Mux Interrupt Status Register (FAULTMUXINTSTAT)

Address 00030014

Bit Number	16	15	14	13	12
Bit Name	DCOMP3	DCOMP2	DCOMP1	DCOMP0	LFO_FAIL
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit Number	11	10	9	8	7	6
Bit Name	FAULT3	FAULT2	FAULT1	FAULT0	DCM_DETECT	ACOMP_G
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit Number	5	4	3	2	1	0
Bit Name	ACOMP_F	ACOMP_E	ACOMP_D	ACOMP_C	ACOMP_B	ACOMP_A
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit 16: DCOMP3 – Digital Comparator 3 Interrupt Stat15us, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active
Bit 15: DCOMP2 – Digital Comparator 2 Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active
Bit 14: DCOMP1 – Digital Comparator 1 Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active
Bit 13: DCOMP0 – Digital Comparator 0 Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active
Bit 12: LFO_FAIL– Low Frequency Oscillator Failure Interrupt Status, cleared by read of status register
0 = Low Frequency Oscillator operational
1 = Low Frequency Oscillator failure detected
Bit 11: FAULT3 – External FAULT[2] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 10: FAULT2 – External FAULT[2] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 9: FAULT1 – External FAULT[1] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 8: FAULT0 – External FAULT[0] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 7: DCM_DETECT – Discontinuous Conduction Mode Interrupt Status, cleared by read of status register
0 = Discontinuous Conduction Mode detected
1 = Discontinuous Conduction Mode not detected
Bit 6: ACOMP_G – Analog Comparator G Interrupt Status, cleared by read of status register

0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active

Bit 5: ACOMP_F – Analog Comparator F Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active

Bit 4: ACOMP_E – Analog Comparator E Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active

Bit 3: ACOMP_D – Analog Comparator D Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active

Bit 2: ACOMP_C – Analog Comparator C Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active

Bit 1: ACOMP_B – Analog Comparator B Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active

Bit 0: ACOMP_A – Analog Comparator A Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt inactive
1 = Comparator threshold interrupt active

12.7 Fault Mux Raw Status Register (FAULTMUXRAWSTAT)

Address 00030018

Bit Number	16	15	14	13	12
Bit Name	DCOMP3	DCOMP2	DCOMP1	DCOMP0	LFO_FAIL
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit Number	11	10	9	8	7	6
Bit Name	FAULT3	FAULT2	FAULT1	FAULT0	DCM_DETECT	ACOMP_G
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit Number	5	4	3	2	1	0
Bit Name	ACOMP_F	ACOMP_E	ACOMP_D	ACOMP_C	ACOMP_B	ACOMP_A
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit 16: DCOMP3 – Digital Comparator 3 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 15: DCOMP2 – Digital Comparator 2 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 14: DCOMP1 – Digital Comparator 1 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 13: DCOMP0 – Digital Comparator 0 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 12: LFO_FAIL – Low Frequency Oscillator Failure Raw Status
0 = Low Frequency Oscillator operational

1 = Low Frequency Oscillator failure detected

Bit 11: FAULT3 – External Fault Detection on FAULT[3] pin
0 = No External FAULT[2] detection found
1 = External GPIO detection found

Bit 10: FAULT2 – External Fault Detection on FAULT[2] pin
0 = No External FAULT[2] detection found
1 = External GPIO detection found

Bit 9: FAULT1 – External Fault Detection on FAULT[1] pin
0 = No External FAULT[1] detection found
1 = External GPIO detection found

Bit 8: FAULT0 – External Fault Detection on FAULT[0] pin
0 = No External FAULT[0] detection found
1 = External GPIO detection found

Bit 7: DCM_DETECT – Discontinuous Conduction Mode Raw Status
0 = Discontinuous Conduction Mode detected
1 = Discontinuous Conduction Mode not detected

Bit 6: ACOMP_G – Analog Comparator G Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 5: ACOMP_F – Analog Comparator F Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 4: ACOMP_E – Analog Comparator E Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 3: ACOMP_D – Analog Comparator D Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 2: ACOMP_C – Analog Comparator C Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 1: ACOMP_B – Analog Comparator B Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 0: ACOMP_A – Analog Comparator A Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

12.8 Comparator Ramp Control 0 Register (COMPRAMP0)

Address 0003001C

Bit Number	31:28	27:10
Bit Name	START_VALUE_SEL	STEP_SIZE
Access	R/W	R/W
Default	0000	00_0000_0000_0000_0000

Bit Number	9:5	4	3
Bit Name	CLKS_PER_STEP	DPWM3_TRIG_EN	DPWM2_TRIG_EN
Access	R/W	R/W	R/W
Default	0_0000	0	00

Bit Number	2	1	0
Bit Name	DPWM1_TRIG_EN	DPWM0_TRIG_EN	RAMP_EN
Access	R/W	R/W	R/W
Default	00	00	0

Bits 31-28: START_VALUE_SEL – Configures comparator ramp starting value
0 = Filter 0 Output (Bits 17-11) (Default)
1 = Filter 1 Output (Bits 17-11)
2 = Filter 2 Output (Bits 17-11)
3 = Analog Comparator Threshold A Value
4 = Analog Comparator Threshold B Value
5 = Analog Comparator Threshold C Value
6 = Analog Comparator Threshold D Value
7 = Analog Comparator Threshold E Value
8 = Analog Comparator Threshold F Value
9 = Analog Comparator Threshold G Value

Bits 27-10: STEP_SIZE - Programmable 18-bit unsigned comparator step with Bits 27:24 representing the integer portion of the comparator step (0-15 Comparator steps of 19.5mV each) and Bits 23:10 representing the fractional portion of the comparator step

Bits 9-5: CLKS_PER_STEP – Selects number of MCLK (HFO_OSC/8) clock cycles per comparator step where number of subcycles can vary from 1 to 32
0 = 1 MCLK clock cycles per step (Default)
1 = 2 MCLK clock cycles per step
2 = 3 MCLK clock cycles per step
…….
31 = 32 MCLK clock cycles per step

Bit 4: DPWM3_TRIG_EN – Enables DPWM Trigger from DPWM 3 to Analog Comparator Ramp 0
0 = DPWM 3 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 3 trigger routed to Analog Comparator Ramp 0

Bit 3: DPWM2_TRIG_EN – Enables DPWM Trigger from DPWM 2 to Analog Comparator Ramp 0
0 = DPWM 2 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 2 trigger routed to Analog Comparator Ramp 0

Bit 2: DPWM1_TRIG_EN – Enables DPWM Trigger from DPWM 1 to Analog Comparator Ramp 0
0 = DPWM 1 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 1 trigger routed to Analog Comparator Ramp 0

Bit 1: DPWM0_TRIG_EN – Enables DPWM Trigger from DPWM 0 to Analog Comparator Ramp 0

0 = DPWM 0 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 0 trigger routed to Analog Comparator Ramp 0

Bit 0: RAMP_EN – Enable for Analog Comparator Ramp 0

0 = Analog Comparator Ramp disabled (Default)
1 = Analog Comparator Ramp enabled

12.9 Digital Comparator Control 0 Register (DCOMPCTRL0)

Address 0x00030020

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0
Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault

Bits 23-19: RESERVED – Unused bits

Bit 18: COMP_POL – Digital Comparator 0 Polarity

0 = Digital Comparator result asserted if value below threshold (Default)
1 = Digital Comparator result asserted if value above threshold

Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold

0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected

Bit 14: CNT_CLR – Comparator Detection Counter clear

0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault

Bit 13: CNT_CONFIG – Comparator Detection Counter configuration

0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold

Bit 12: INT_EN – Comparator Interrupt Enable

0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation

Bit 11: COMP_EN – Digital Comparator 0 Enable

0 = Disables Digital Comparator 0 (Default)
1 = Enables Digital Comparator 0

Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

12.10 Digital Comparator Control 1 Register (DCOMPCTRL1)

Address 0x00030024

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0
Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault
Bits 23-19: RESERVED – Unused bits
Bit 18: COMP_POL – Digital Comparator 1 Polarity
0 = Digital Comparator result asserted if value below threshold (Default)
1 = Digital Comparator result asserted if value above threshold
Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold
0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected
Bit 14: CNT_CLR – Comparator Detection Counter clear
0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault
Bit 13: CNT_CONFIG – Comparator Detection Counter configuration
0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
Bit 12: INT_EN – Comparator Interrupt Enable
0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation
Bit 11: COMP_EN – Digital Comparator 1 Enable
0 = Disables Digital Comparator 1 (Default)
1 = Enables Digital Comparator 1
Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

12.11 Digital Comparator Control 2 Register (DCOMPCTRL2)

Address 0x00030028

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0

Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault
Bits 23-19: RESERVED – Unused bits
Bit 18: COMP_POL – Digital Comparator 1 Polarity
0 = Digital Comparator result asserted if value below threshold (Default)
1 = Digital Comparator result asserted if value above threshold
Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold
0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected
Bit 14: CNT_CLR – Comparator Detection Counter clear
0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault
Bit 13: CNT_CONFIG – Comparator Detection Counter configuration
0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
Bit 12: INT_EN – Comparator Interrupt Enable
0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation
Bit 11: COMP_EN – Digital Comparator 2 Enable
0 = Disables Digital Comparator 2 (Default)
1 = Enables Digital Comparator 2
Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

12.12 Digital Comparator Control 3 Register (DCOMPCTRL3)

Address 0x0003002C

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0
Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault
Bits 23-19: RESERVED – Unused bits
Bit 18: COMP_POL – Digital Comparator 1 Polarity
0 = Digital Comparator result asserted if value below threshold (Default)

1 = Digital Comparator result asserted if value above threshold

Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold

0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected

Bit 14: CNT_CLR – Comparator Detection Counter clear

0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault

Bit 13: CNT_CONFIG – Comparator Detection Counter configuration

0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold

Bit 12: INT_EN – Comparator Interrupt Enable

0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation

Bit 11: COMP_EN – Digital Comparator 3 Enable

0 = Disables Digital Comparator 3 (Default)
1 = Enables Digital Comparator 3

Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

12.13 Digital Comparator Counter Status Register (DCOMPCNTSTAT)

Address 0x00030030

Bit Number	31:24	31:24	31:24	31:24
Bit Name	DCOMP3_CNT	DCOMP2_CNT	DCOMP1_CNT	DCOMP0_CNT
Access	R	R	R	R
Default	-	-	-	-

Bits 31-24: DCOMP3_CNT – Current value of Digital Comparator 3 detection counter
Bits 23-16: DCOMP2_CNT – Current value of Digital Comparator 2 detection counter
Bits 15-8: DCOMP1_CNT – Current value of Digital Comparator 1 detection counter
Bits 7-0: DCOMP0_CNT – Current value of Digital Comparator 0 detection counter

12.14 DPWM 0 Current Limit Control Register (DPWM0CLIM)

Address 0x00030034

Bit Number	16	15	14
Bit Name	ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	13	12	11	10	9
Bit Name	DCOMP1_EN	DCOMP0_EN	RESERVED	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	8	7	6	5	4

Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 16: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 0 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 15: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 14: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 13: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 12: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)

1 = Analog Comparator result enabled for current limit

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

12.15DPWM 0 Fault AB Detection Register (DPWM0FLTABDET)

Address 0x00030038

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection

Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection

Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection

Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection

Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 6: ACOMP_A_EN – Enables Analog Comparator G result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

12.16 DPWM 0 Fault Detection Register (DPWM0FAULTDET)

Address 0x0003003C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6

Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 15: RESERVED – Unused bit

Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 PWM-A Fault Detection

0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection

Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 PWM-A Fault Detection

0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection

Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 PWM-A Fault Detection

0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection

Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 PWM-A Fault Detection

0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection

Bit 10: PWMA_FAULT3_EN – Enables FAULT[3] pin for DPWM 0 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 0 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 0 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 0 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

12.17

DPWM 1 Current Limit Control Register (DPWM1CLIM)

Address 0x00030044

Bit Number	16	15	14
Bit Name	ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	13	12	11	10	9
Bit Name	DCOMP1_EN	DCOMP0_EN	RESERVED	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	8	7	6	5	4
Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 16: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 1 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 15: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 14: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 13: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 12: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 Current Limit

0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

12.18 DPWM 1 Fault AB Detection Register (DPWM1FLTABDET)

Address 0x00030048

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 Fault AB detection

0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

12.19DPWM 1 Fault Detection Register (DPWM1FAULTDET)

Address 0x0003004C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6

Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 15: RESERVED – Unused bit

Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection

Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection

Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection

Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection

Bit 10: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

12.20 DPWM 2 Current Limit Control Register (DPWM2CLIM)

Address 0x00030054

Bit Number	16	15	14
Bit Name	ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	13	12	11	10	9
Bit Name	DCOMP1_EN	DCOMP0_EN	RESERVED	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	8	7	6	5	4
Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 16: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 2 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 15: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 14: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 13: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 12: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit

Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

12.21 DPWM 2 Fault AB Detection Register (DPWM2FLTABDET)

Address 0x00030058

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 Fault AB detection

0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

12.22 DPWM 2 Fault Detection Register (DPWM2FAULTDET)

Address 0x0003005C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6

Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 15: RESERVED – Unused bit

Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 PWM-A Fault Detection

0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection

Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 PWM-A Fault Detection

0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection

Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 PWM-A Fault Detection

0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection

Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 PWM-A Fault Detection

0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection

Bit 10: PWMA_FAULT3_EN – Enables FAULT[3] pin for DPWM 2 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 2 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 2 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 2 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

12.23 DPWM 3 Current Limit Control Register (DPWM3CLIM)

Address 0x00030064

Bit Number	16	15	14
Bit Name	ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	13	12	11	10	9
Bit Name	DCOMP1_EN	DCOMP0_EN	RESERVED	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	8	7	6	5	4
Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 16: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 2 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 15: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 14: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 13: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 12: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit

Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

12.24 DPWM 3 Fault AB Detection Register (DPWM3FLTABDET)

Address 0x00030068

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 Fault AB detection

0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

12.25 DPWM 3 Fault Detection Register (DPWM3FAULTDET)

Address 0x0003006C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6

Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 15: RESERVED – Unused bit

Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 PWM-A Fault Detection

0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection

Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 PWM-A Fault Detection

0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection

Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 PWM-A Fault Detection

0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection

Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 PWM-A Fault Detection

0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection

Bit 10: PWMA_FAULT3_EN – Enables FAULT[3] pin for DPWM 3 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 3 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 3 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 3 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

12.26 HFO Fail Detect Register (HFOFAILDET)

Address 0x00030074

Bit Number	17:1	0
Bit Name	HFO_FAIL_THRESH	HFO_DETECT_EN
Access	R/W	R/W
Default	0_0000_0000_1111_1111	0

Bits 17-1: HFO_FAIL_THRESH – Configures threshold where a clear flag is used to clear a counter in the Low Frequency Oscillator domain (if LFO counter overflows, a reset will be generated), resolution of threshold equals High Frequency Oscillator period

Bit 0: HFO_DETECT_EN – Enables High Frequency Oscillator Failure Detection logic, device will be reset upon detection of an oscillator failure
0 = Disables High Frequency Oscillator Failure Detection (Default)
1 = Enables High Frequency Oscillator Failure Detection

12.27 LFO Fail Detect Register (LFOFAILDET)

Address 0x00030078

Bit Number	6:2	1	0
Bit Name	LFO_FAIL_THRESH	LFO_FAIL_INT_EN	LFO_DETECT_EN
Access	R/W	R/W	R/W
Default	0_0011	0	0

Bits 6-2: LFO_FAIL_THRESH – Configures threshold where a clear flag is used to clear a counter in the High Frequency Oscillator domain (if HFO counter overflows, a reset will be generated), resolution of threshold equals Low Frequency Oscillator period

Bit 1: LFO_FAIL_INT_EN – Low Frequency Oscillator Fail Interrupt Enable
0 = Disables Interrupt Generation upon LFO Failure Detection (Default)
1 = Enables Interrupt Generation upon LFO Failure Detection

Bit 0: LFO_DETECT_EN – Enables Low Frequency Oscillator Failure Detection logic, interrupt will be generated upon detection of an oscillator failure
0 = Disables Low Frequency Oscillator Failure Detection (Default)
1 = Enables Low Frequency Oscillator Failure Detection

12.28 IDE Control Register (IDECTRL)

Address 0003007C

Bit Number	31:24	23:16
Bit Name	DCM_LIMIT_H	DCM_LIMIT_L
Access	R/W	R/W
Default	0000_0000	0000_0000

Bit Number	15:14	13	12:0
Bit Name	RESERVED	DCM_INT_EN	IDE_KD
Access	-	R/W	R/W
Default	00	0	0_0000_0000_0000

Bits 31-24: DCM_LIMIT_H – Value added to 1-Da value to provide hysteresis for exiting DCM mode
Bits 23-16: DCM_LIMIT_L – Value subtracted from 1-Da value to provide hysteresis for entering DCM mode
Bit 15-14: RESERVED – Unused Bits
Bit 13: DCM_INT_EN – Enables Discontinuous Conduction Mode (DCM) interrupt generation based on selected Filter outputs

0 = Disables DCM Detection Interrupt (Default)
1 = Enables DCM Detection Interrupt

Bits 12-0: IDE_KD – 13-bit unsigned value used to calculate the DPWM B Pulse width when configured in IDE Mode. IDE_KD is configured in 4.9 format, with the integer portion of the KD value ranging from 0 to 15 and 9 fractional bits available for the pulse width calculation.

13 GIO – General Purpose Input/Output Module

GIO Registers have the following attributes:

- Addresses placed on word boundaries
- Byte, Half-word and Word Writes are permitted
- All Registers can be read in any mode
- All Registers are writeable

13.1 Fault IO Direction Register (FAULTDIR)

Address FFF7FA00

Bit Number	6	5	4	3	2	1	0
Bit Name	TMS_DIR	TDI_DIR	TDO_DIR	FLT3_DIR	FLT2_DIR	FLT1_DIR	FLT0_DIR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0

Bit 6: TMS_DIR – TMS Pin Configuration
0 = TMS pin configured as an input pin in GPIO mode (Default)
1 = TMS pin configured as an output pin in GPIO mode
Bit 5: TDI_DIR – TDI Pin Configuration
0 = TDI pin configured as an input pin in GPIO mode (Default)
1 = TDI pin configured as an output pin in GPIO mode
Bit 4: TDO_DIR – TDO Pin Configuration
0 = TDO pin configured as an input pin in GPIO mode (Default)
1 = TDO pin configured as an output pin in GPIO mode
Bit 3: FLT3_DIR – FAULT[3] Pin Configuration
0 = FAULT[3] pin configured as an input pin (Default)
1 = FAULT[3] pin configured as an output pin
Bit 2: FLT2_DIR – FAULT[2] Pin Configuration
0 = FAULT[2] pin configured as an input pin (Default)
1 = FAULT[2] pin configured as an output pin
Bit 1: FLT1_DIR – FAULT[1] Pin Configuration
0 = FAULT[1] pin configured as an input pin (Default)
1 = FAULT[1] pin configured as an output pin
Bit 0: FLT0_DIR – FAULT[0] Pin Configuration
0 = FAULT[0] pin configured as an input pin (Default)
1 = FAULT[0] pin configured as an output pin

13.2 Fault Input Register (FAULTIN)

Address FFF7FA04

Bit Number	6	5	4	3	2	1	0
Bit Name	TMS_IN	TDI_IN	TDO_IN	FLT3_IN	FLT2_IN	FLT1_IN	FLT0_IN
Access	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-

Bit 6: TMS_IN – Input Value of TMS Pin
0 = TMS pin driven low in GPIO mode
1 = TMS pin driven high in GPIO mode
Bit 5: TDI_IN – Input Value of TDI Pin
0 = TDI pin driven low in GPIO mode
1 = TDI pin driven high in GPIO mode
Bit 4: TDO_IN – Input Value of TDO Pin
0 = TDO pin driven low in GPIO mode
1 = TDO pin driven high in GPIO mode
Bit 3: FLT3_IN – Input Value of FAULT[3] Pin
0 = FAULT[3] pin driven low
1 = FAULT[3] pin driven high
Bit 2: FLT2_IN – Input Value of FAULT[2] Pin
0 = FAULT[2] pin driven low
1 = FAULT[2] pin driven high
Bit 1: FLT1_IN – Input Value of FAULT[1] Pin
0 = FAULT[1] pin driven low
1 = FAULT[1] pin driven high
Bit 0: FLT0_IN – Input Value of FAULT[0] Pin
0 = FAULT[0] pin driven low
1 = FAULT[0] pin driven high

13.3 Fault Output Register (FAULTOUT)

Address FFF7FA08

Bit Number	6	5	4	3
Bit Name	TMS_OUT	TDI_OUT	RESERVED	FLT3_OUT
Access	R/W	R/W	-	R/W
Default	0	0	0	0

Bit Number	2	1	0
Bit Name	FLT2_OUT	FLT1_OUT	FLT0_OUT
Access	R/W	R/W	R/W
Default	0	0	0

Bit 6: TMS_OUT – TMS Pin Output Value
0 = TMS pin driven low when configured as output in GPIO mode (Default)
1 = TMS pin driven high when configured as output in GPIO mode
Bit 5: TDI_OUT – TDI Pin Output Value
0 = TDI pin driven low when configured as output in GPIO mode (Default)
1 = TDI pin driven high when configured as output in GPIO mode
Bit 4: RESERVED – Unused Bit
Bit 3: FLT3_OUT – FAULT[3] Pin Output Value
0 = FAULT[3] pin driven low when configured as output (Default)

1 = FAULT[3] pin driven high when configured as output

Bit 2: FLT2_OUT – FAULT[2] Pin Output Value
0 = FAULT[2] pin driven low when configured as output (Default)
1 = FAULT[2] pin driven high when configured as output

Bit 1: FLT1_OUT – FAULT[1] Pin Output Value
0 = FAULT[1] pin driven low when configured as output (Default)
1 = FAULT[1] pin driven high when configured as output

Bit 0: FLT0_OUT – FAULT[0] Pin Output Value
0 = FAULT[0] pin driven low when configured as output (Default)
1 = FAULT[0] pin driven high when configured as output

13.4 Fault Interrupt Enable Register (FAULTINTENA)

Address FFF7FA14

Bit Number	6	5	4
Bit Name	TMS_INT_EN	TDI_INT_EN	TDO_INT_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_INT_EN	FLT2_INT_EN	FLT1_INT_EN	FLT0_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 6: TMS_INT_EN – TMS Interrupt Enable
0 = Interrupt disabled for TMS pin (Default)
1 = Interrupt enabled for TMS pin in GPIO mode

Bit 5: TDI_INT_EN – TDI Interrupt Enable
0 = Interrupt disabled for TDI pin (Default)
1 = Interrupt enabled for TDI pin in GPIO mode

Bit 4: TDO_INT_EN – TDO Interrupt Enable
0 = Interrupt disabled for TDO pin (Default)
1 = Interrupt enabled for TDO pin in GPIO mode

Bit 3: FLT3_INT_EN – FAULT[3] Interrupt Enable
0 = Interrupt disabled for FAULT[3] pin (Default)
1 = Interrupt enabled for FAULT[3] pin

Bit 2: FLT2_INT_EN – FAULT[2] Interrupt Enable
0 = Interrupt disabled for FAULT[2] pin (Default)
1 = Interrupt enabled for FAULT[2] pin

Bit 1: FLT1_INT_EN – FAULT[1] Interrupt Enable
0 = Interrupt disabled for FAULT[1] pin (Default)
1 = Interrupt enabled for FAULT[1] pin

Bit 0: FLT0_INT_EN – FAULT[0] Interrupt Enable
0 = Interrupt disabled for FAULT[0] pin (Default)
1 = Interrupt enabled for FAULT[0] pin

13.5 Fault Interrupt Polarity Register (FAULTINTPOL)

Address FFF7FA18

Bit Number	6	5	4
Bit Name	TMS_INT_POL	TDI_INT_POL	TDO_INT_POL
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_INT_POL	FLT2_INT_POL	FLT1_INT_POL	FLT0_INT_POL
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 6: TMS_INT_POL – TMS Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 5: TDI_INT_POL – TDI Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 4: TDO_INT_POL – TDO Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 3: FLT3_INT_POL – FAULT[3] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 2: FLT2_INT_POL – FAULT[2] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 1: FLT1_INT_POL – FAULT[1] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 0: FLT0_INT_POL – FAULT[0] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge

13.6 Fault Interrupt Pending Register (FAULTINTPEND)

Address FFF7FA1C

Bit Number	6	5	4
Bit Name	TMS_INT_PEND	TDI_INT_PEND	TDO_INT_PEND
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_INT_PEND	FLT2_INT_PEND	FLT1_INT_PEND	FLT0_INT_PEND
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 6: TMS_INT_PEND – TMS has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 5: TDI_INT_PEND – TDI has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 4: TDO_INT_PEND – TDO has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 3: FLT3_INT_PEND – FAULT[3] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 2: FLT2_INT_PEND – FAULT[2] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 1: FLT1_INT_PEND – FAULT[1] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 0: FLT0_INT_PEND – FAULT[0] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

13.7 External Interrupt Direction Register (EXTINTDIR)

Address FFF7FA20

Bit Number	0
Bit Name	EXT_INT_DIR
Access	R/W
Default	0

Bit 0: EXT_INT_DIR – EXT-INT Pin Configuration
0 = EXT-INT pin configured as an input pin (Default)
1 = EXT-INT pin configured as an output pin

13.8 External Interrupt Input Register (EXTINTIN)

Address FFF7FA24

Bit Number	0
Bit Name	EXT_INT_IN
Access	R
Default	-

Bit 0: EXT_INT_IN – Input Value of EXT-INT Pin
0 = EXT-INT pin driven low in GPIO mode
1 = EXT-INT pin driven high in GPIO mode

13.9 External Interrupt Output Register (EXTINTOUT)

Address FFF7FA28

Bit Number	0
Bit Name	EXT_INT_OUT
Access	R/W
Default	0

Bit 0: EXT_INT_OUT – EXT-INT Pin Output Value
0 = EXT-INT pin driven low (Default)
1 = EXT-INT pin driven high

13.10 External Interrupt Enable Register (EXTINTENA)

Address FFF7FA34

Bit Number	0
Bit Name	EXT_INT_EN
Access	R/W
Default	0

Bit 0: EXT_INT_EN – EXT-INT Interrupt Enable
0 = Interrupt disabled for EXT-INT pin (Default)
1 = Interrupt enabled for EXT-INT pin

13.11 External Interrupt Polarity Register (EXTTINTPOL)

Address FFF7FA38

Bit Number	0
Bit Name	EXT_INT_POL
Access	R/W
Default	0

Bit 0: EXT_INT_POL – EXT-INT Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge

13.12 External Interrupt Pending Register (EXTINTPEND)

Address FFF7FA3C

Bit Number	0
Bit Name	EXT_INT_PEND
Access	R/W
Default	0

Bit 0: EXT_INT_PEND – EXT-INT has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag.

References

1. UCD3138 ARM and Digital System Programmer's Manual (Literature Number: SLUU996)
2. UCD3138 ARM and Digital System Programmer's Manual (Literature Number: SLUU994)
3. UCD3138 Device Datasheet (Literature #: SLUSAP2)

Document Revision History

Version	Release Date	List of Changes
1p0	July 2012	Initial Document
2p0	April 2013	- Page 33: Added clarifications to CBC_PWM_EN description in "Section 2.15.3 Cycle by Cycle Current Limit Enable" - Page 34: Description and diagram added for negative dead times; Terminology corrected from "phase" to "duty" at multiple locations - Page 41: Corrected error in "Section: 2.16.13 Using DPWM Pins as General Purpose I/O" regarding description for bits PWM_A_OE and PWM_B_OE - Page 42: Added clarifications in "Section 2.17.3 Filter Duty Select" - Page 48: Updated Front End diagram to match UCD3138 datasheet. Clarified that Front End 2 is recommended for Peak Current Mode control - Page 63: Corrected picture in "Section 4.1.1 Filter Input and Branch Calculations" to show that there are only 6 limit comparators (limit 0 to limit 5) - Page 71: Added diagram in "Section 4.5 Coefficient Configuration Register" - Page 89: Added additional clarifications to explain IDE_KD connection to Filter and DPWMs in "Section 6.9 IDE /DCM Detection Control"

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