Tips to Achieve Balanced Design for Automotive LDO Application

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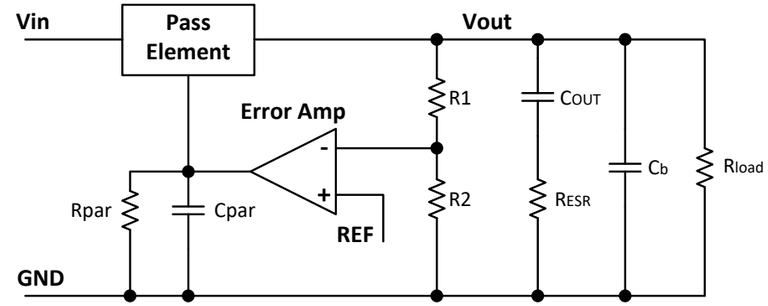
Summary

Training Summary:

This in-depth training will explain how to build a parallel LDO topology with balanced current and thermal distribution, in the meanwhile to analysis how to debug the LDO oscillation case and how to improve the transient performance. In addition, this training will also cover the key challenges of power solution for automotive off-board loads and the way to deal with them.

What you'll learn:

- Learn how to build a parallel LDO topology
- How to analysis the bode plot of LDO and how to use it for stability debug
- See the power solution for different automotive off-board loads



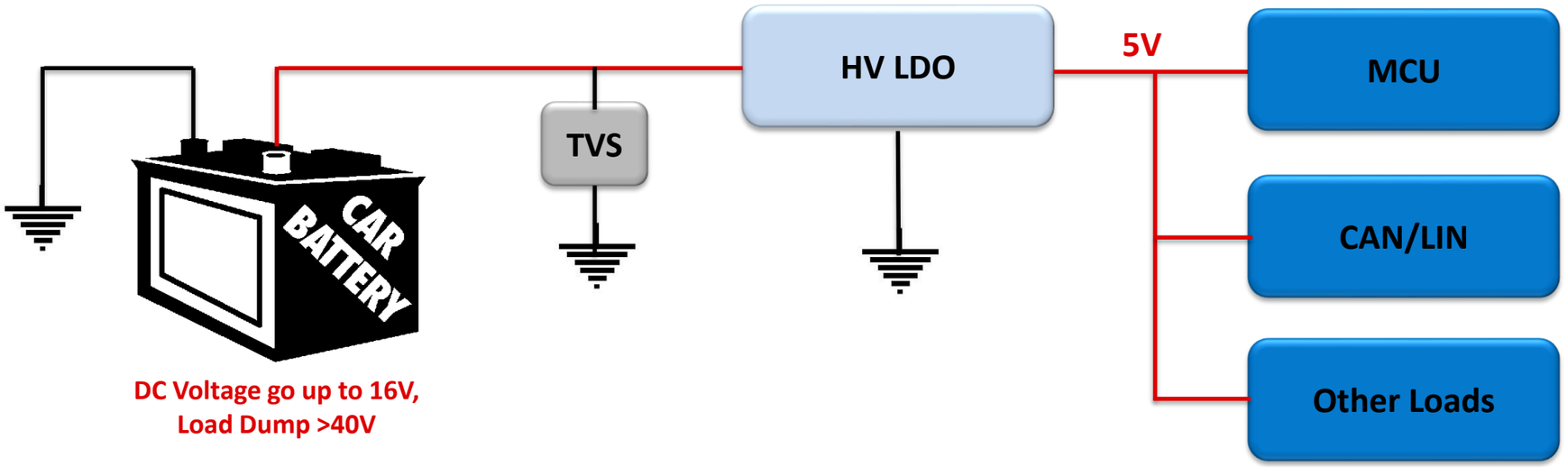
Link to the recorded training session can be found at ti.com/training

Agenda

- Parallel LDO Topology
- LDO Loop Stability and Transient Performance Analysis
  - LDO Bode Plot Analysis
  - How to debug LDO Oscillation
  - Loop Stable with Ceramic Capacitor
  - Fast Loop Insertion
  - Feed Forward Cap Add Phase Lead
  - How to Estimate Phase Margin
- Power Solution for Automotive Off-board Loads

Parallel LDO Topology

Off-Battery LDO Power Dissipation



The Power Dissipation of HV LDO can be calculated by below equation:

$$P_{LDO} = (Vin - Vout) * Iout + Vin * Iquiescent$$

For the worst case power estimation, usually 16V DC battery voltage is assumed, for many devices, quiescent current is uA level which could be neglected as well, so the maximum power dissipation could be estimated by below equation:

$$P_{Max} = (16V - 5V) * Iout\_max = 11 * Iout\_max$$

Off-Battery LDO Power Dissipation

For most automotive application, the ambient temperature could go up to 85C or even higher, so the maximum allowed temperature rise between device junction to ambient could be calculated per below:

$$Tja\_max = Tj - Ta = 150°C - 85°C = 65°C$$

Then the maximum allowed power dissipation could be calculated:

$$Pmax = \frac{Tja\_max}{\Theta ja} = \frac{65°C}{\Theta ja}$$

THERMAL METRIC[1]		TLE4275-Q1			UNIT
		KTT	KVU	PWP	
		5 PINS	5 PINS	20 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[2]	28.8	40.3	39.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	43.1	31.8	22.7	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	0.8	17.2	19.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	3.7	2.8	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	0.7	17.1	18.9	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	0.2	0.7	1.5	°C/W

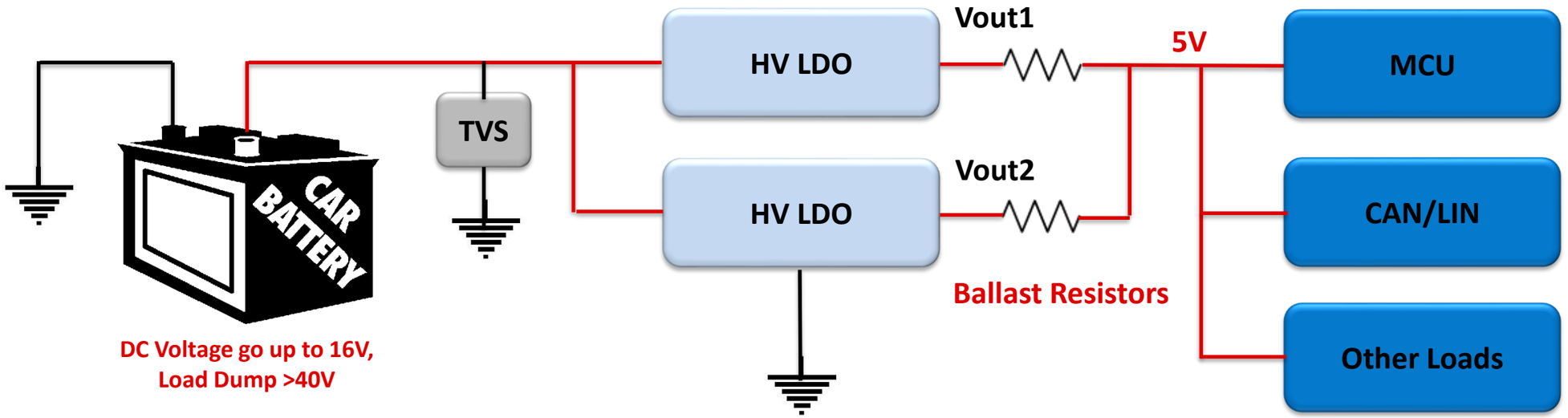
Good Copper Coverage and thermal vias

$$\Theta ja\_KTT = 20°C/W$$

Table 1. TLE4275 Thermal Data on JEDEC PCB

$$Pmax = \frac{Tja\_max}{\Theta ja\_KTT} = 3.25W \quad \Rightarrow \quad Iout\_max = \frac{Pmax}{11V} \approx \mathbf{300mA}$$

LDO Parallel Topology



The Maximum current difference between the two LDOs could be calculated by below:

$$\Delta Iout = \frac{Vout1 - Vout2}{R}$$

For most LDOs in the market, accuracy across temperature is ±2%, so in worst case:

$$\Delta Vout = Vout1_{max} - Vout2_{min} = 5V * (1 + 2\%) - 5V * (1 - 2\%) = 200mV$$

$R = 1\Omega \rightarrow \Delta Iout = 200mA$

$R = 10\Omega \rightarrow \Delta Iout = 20mA$

High Drop on Ballast Resistor

TPS7B4253: 300mA Low Dropout Tracking LDO

Features

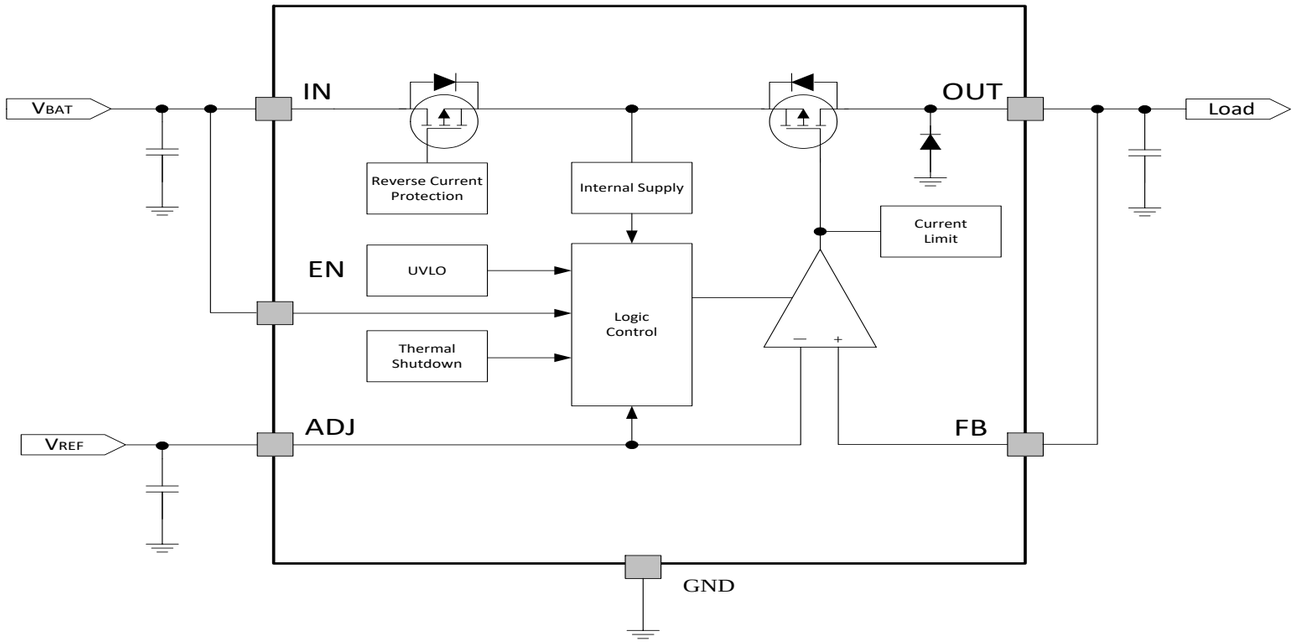
- -40V to 45V Wide Input Voltage Range (Maximum)
- Output Voltage Adjusts Down to:
  - 1.5 to 40V (HTSSOP-20)
  - 2 to 40V (HOSIC-8)
- Very Low Output Tracking Tolerance, ±4mV
- 320mV Low Dropout Voltage When IOUT=200mA
- 520mA Maximum Current Limit
- Low Quiescent Current (IQ):
  - < 4uA when EN=LOW
  - 60uA (Typical) at Light Loads
- Extremely Wide ESR Range.
  - Stable With 10 to 500uF Ceramic Output Capacitor, ESR 1mΩ to 20Ω
- Reverse Polarity Protection
- Current Limit and Thermal Shutdown Protection
- Output Short Circuit Proof to Ground and Supply
- Inductive Clamp at OUT Pin
- HTSSOP-20, HSOIC-8 Package

Applications

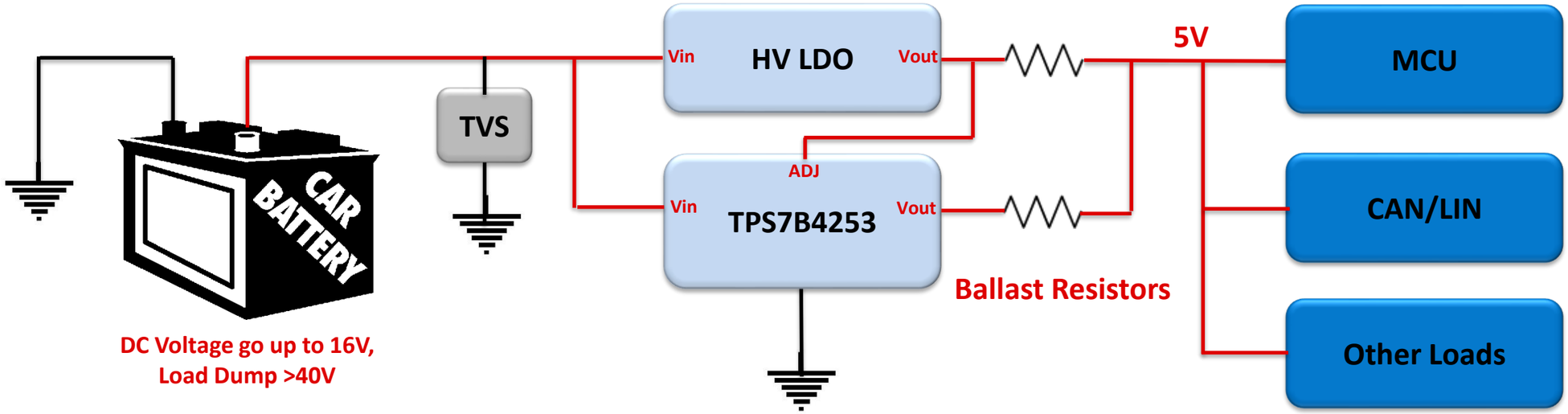
- Off-board Sensor Power Supply
- Parallel with Other LDOs
- Power Switch for Off-board Loads

Benefits

- 4mV Ultra Low Output Tracking Tolerance
- Wide Stable Region for Output Capacitor and ESR
- Wide Input and Output Voltage Operating Range, OUT pin with short to battery protection



LDO Parallel Topology with Tracker



The Maximum current difference between the two LDOs could be calculated by below:

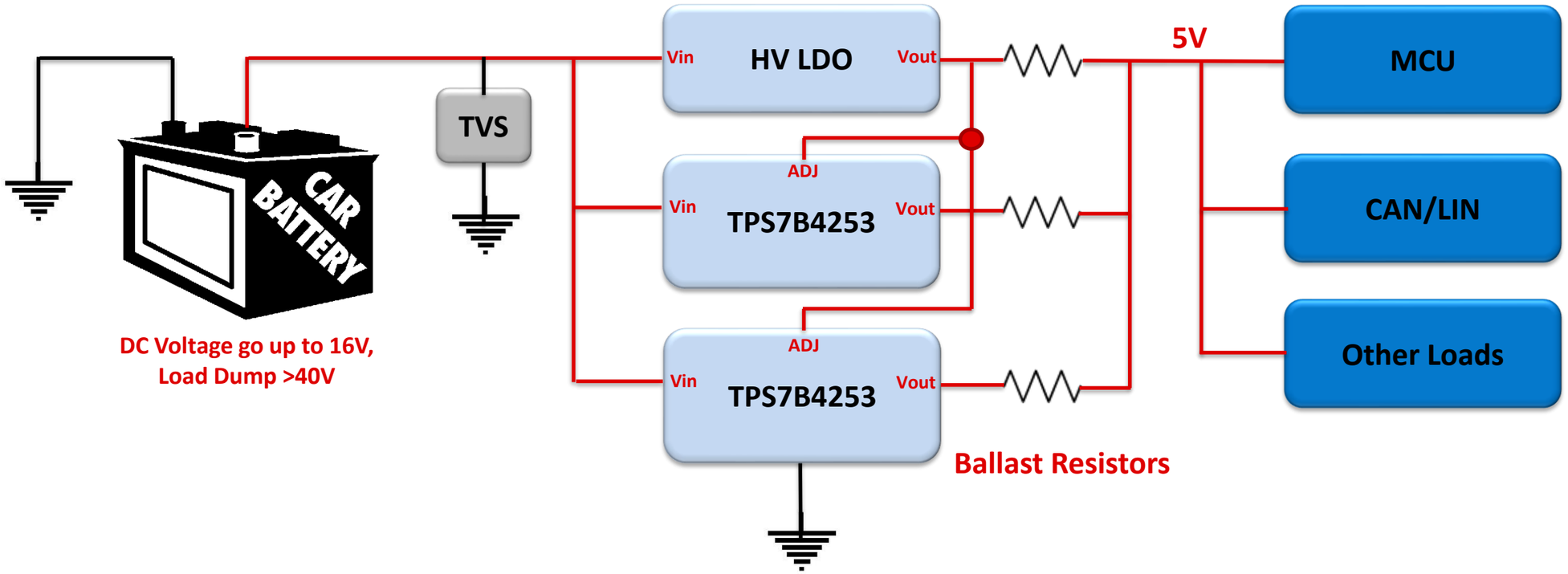
$$\Delta Iout = \frac{Vout1 - Vout2}{R}$$

The Maximum voltage difference between TPS7B4253 ADJ and Vout is shown below:

$$\Delta Vout = 4mV$$

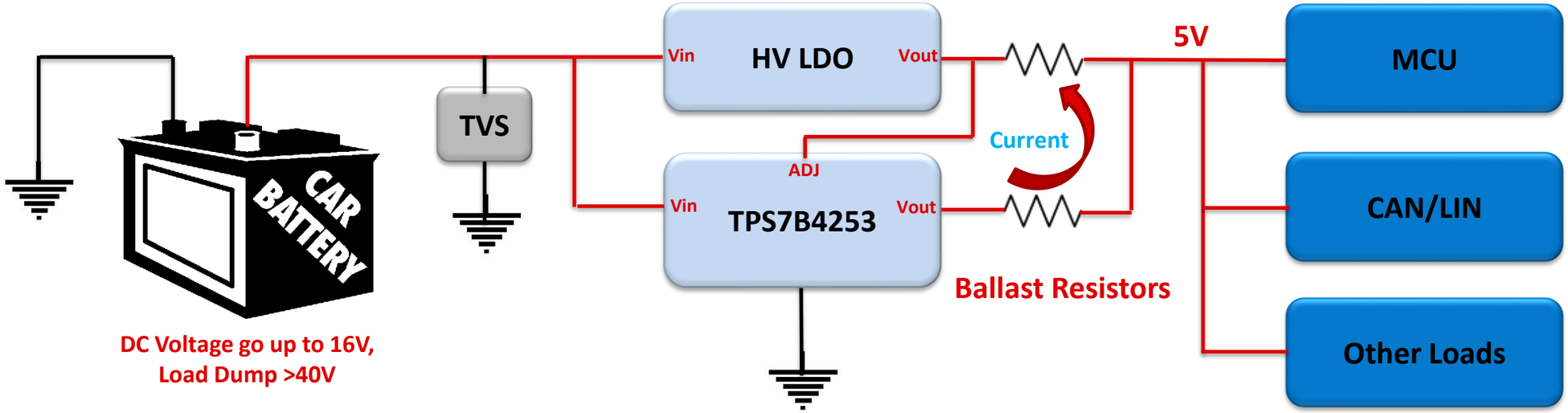
$R = 0.1\Omega$	$\Delta Iout = 40mA,$	$30mV\ Vdrop\ on\ ballast\ resistor\ under\ 600mA\ Load$
$R = 0.2\Omega$	$\Delta Iout = 20mA,$	$60mV\ Vdrop\ on\ ballast\ resistor\ under\ 600mA\ Load$

LDO Parallel Topology with Multiple Tracker



Multiple tracker could be paralleled with a single high voltage LDO.

Minimum Current for Tracker Parallel Topology



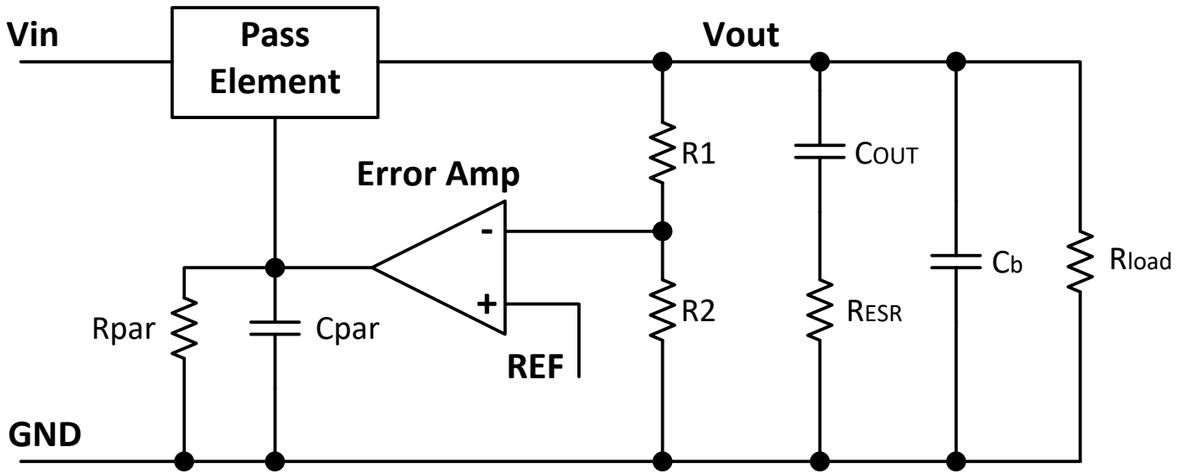
$R = 0.2\Omega$ → $\Delta Iout = 20mA,$ $60mV\ Vdrop\ on\ ballast\ resistor\ under\ 600mA\ Load$

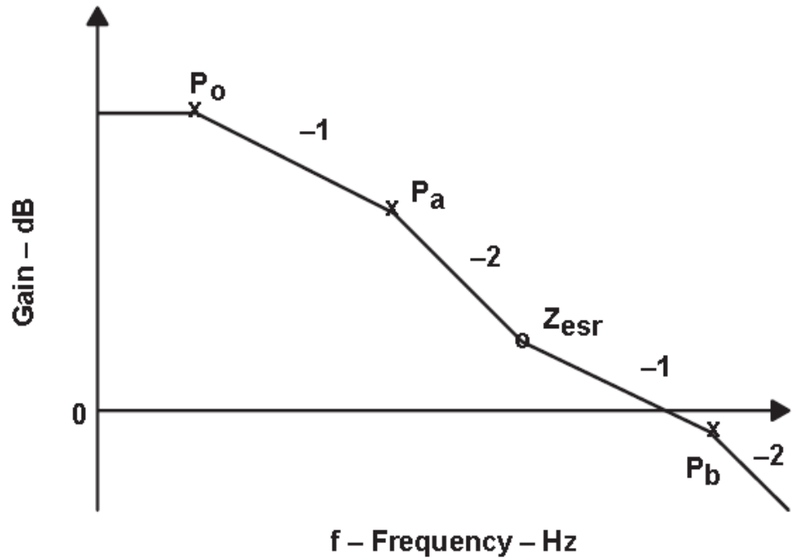
When $\mathrm{Iout} < \Delta Iout$, current will flow from TPS7B4253 Vout to HV LDO Vout which results to a positive feedback, 5V Vout could not be get in such case.

Minimum load current is required for this topology, or disable TPS7B4253 at light load.

LDO Loop Stability and Transient Performance Analysis

LDO Bode Plot Analysis





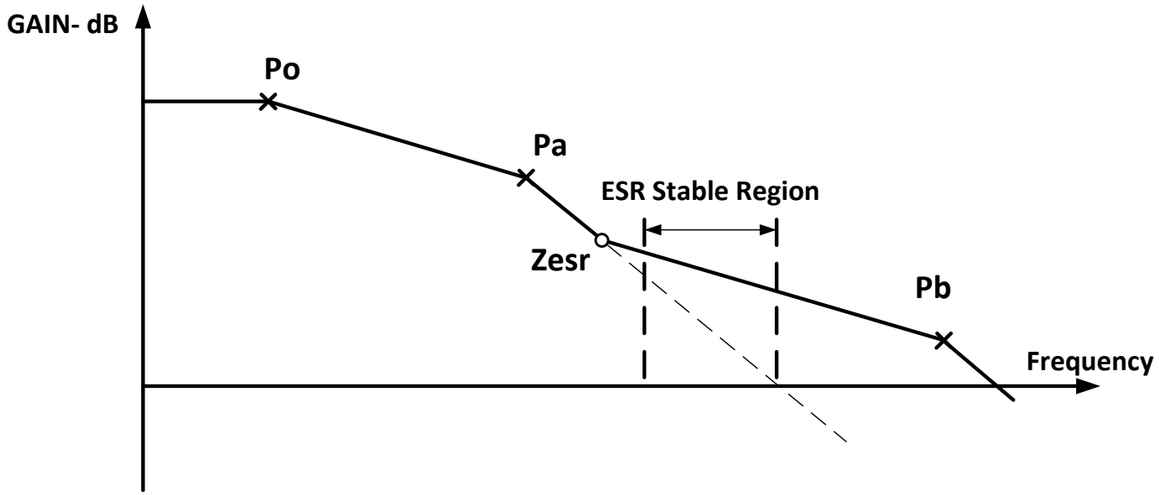
A capacitor in parallel with a resistor forms up a pole, so the poles could be calculated by below equation:

$$P_o = \frac{1}{2\pi * C_{OUT} * R_{OUT}} \qquad P_a = \frac{1}{2\pi * C_{par} * R_{par}} \qquad P_b = \frac{1}{2\pi * C_b * R_{ESR}}$$

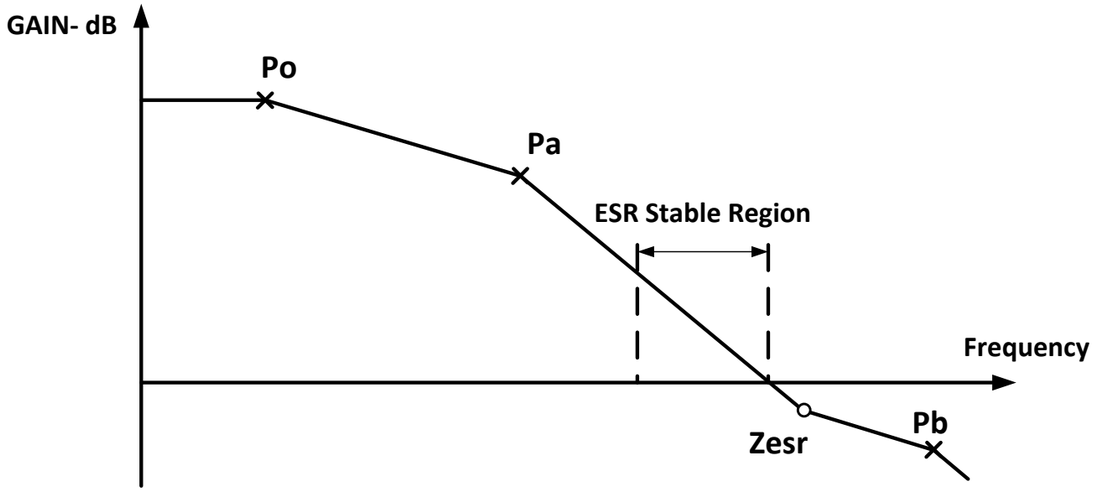
A capacitor in series with a resistor forms up a zero, the zero could be calculated by below equation:

$$Z_{ESR} = \frac{1}{2\pi * C_{OUT} * R_{ESR}}$$

ESR Range Requirement for Output Capacitor



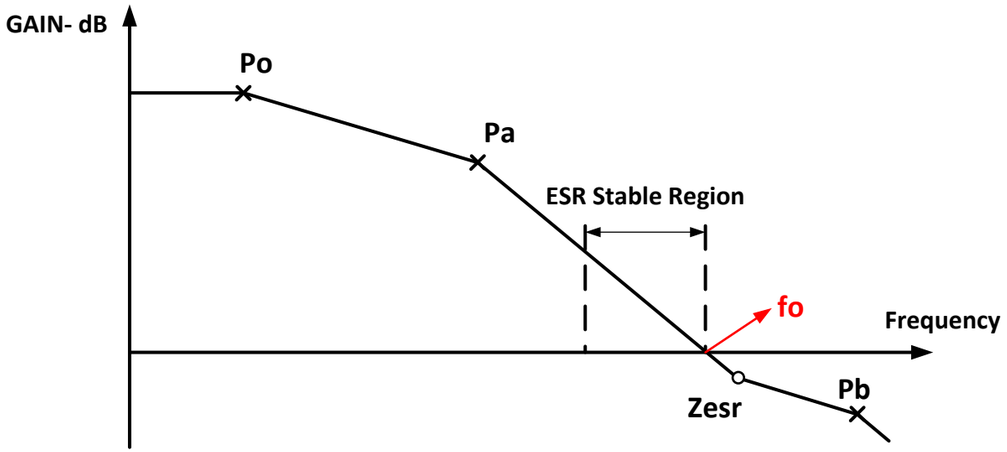
Unstable Frequency Response of LDO with too High ESR



Unstable Frequency Response of LDO with too Low ESR

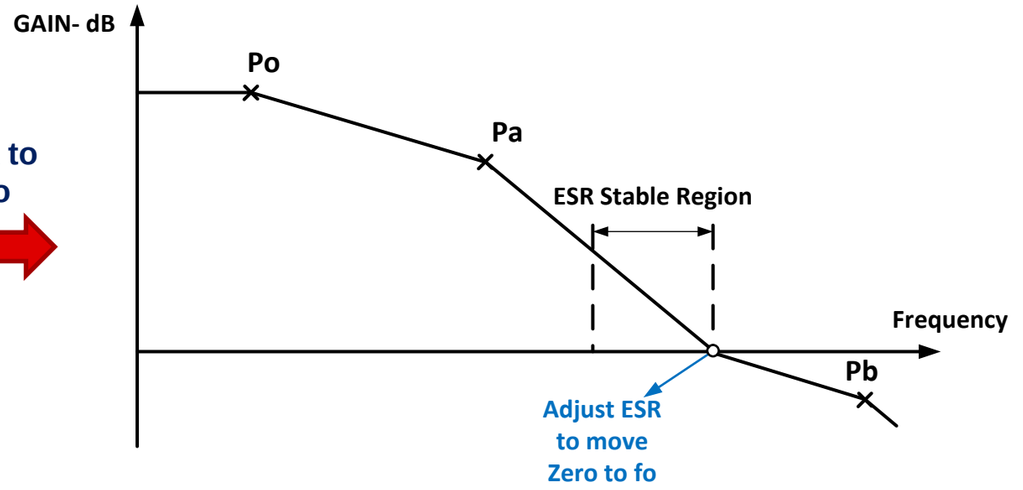
When the output cap selecting ESR range is out of the range specified in datasheet, oscillation will happen. Above two figures are examples, for both cases, the total phase shift at unity gain frequency is -180C.

How to debug LDO oscillation?



Unstable Frequency Response of LDO with too Low ESR

Adjust Cout ESR to move Zero to fo

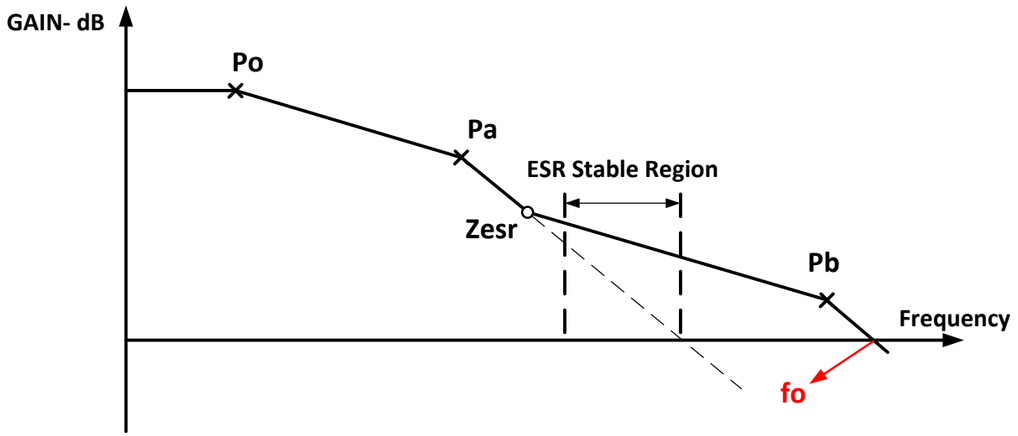


Adjust Output Capacitor ESR to move Zero frequency to fo

When LDO oscillation happens, the loop will oscillates at a frequency close to its bandwidth. In such case, we could adjust the ESR of the output capacitor to move the frequency of the zero formed by output capacitor to the oscillation frequency.

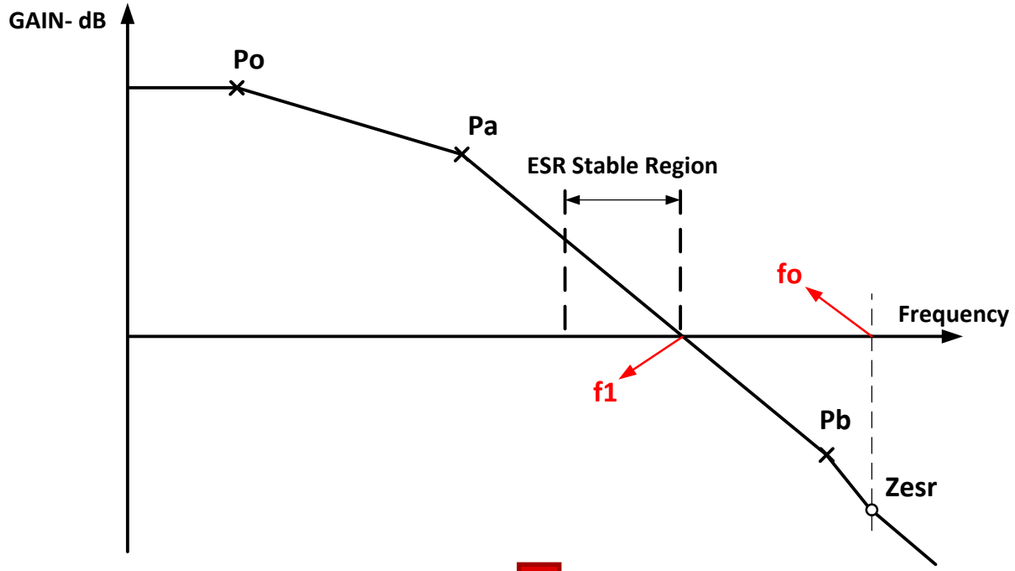
Above is an unstable frequency response of LDO with too low ESR, after the zero been removed to fo, the loop becomes stable again as ESR Zero creates more phase lead than the phase lag created by Pb.

How to debug LDO oscillation?

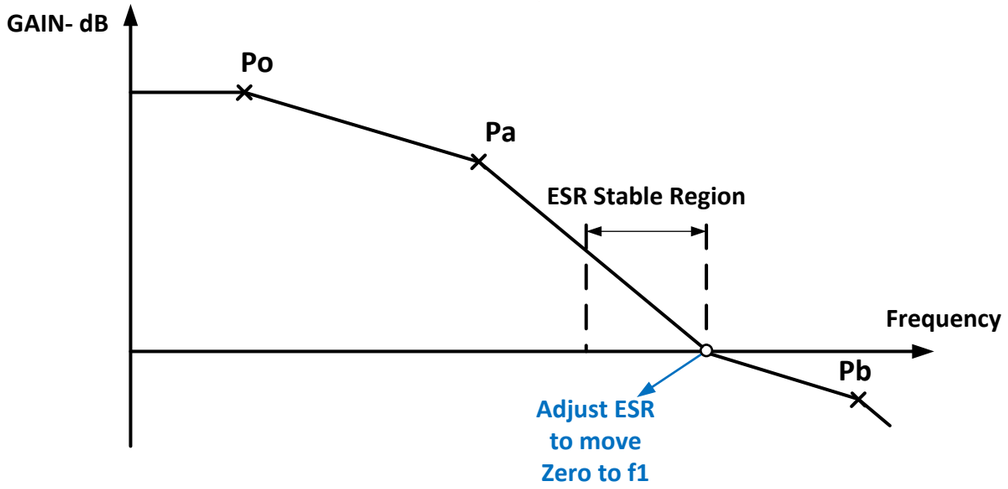


Unstable Frequency Response of LDO with too High ESR

Adjust Cout ESR to move Zero to fo

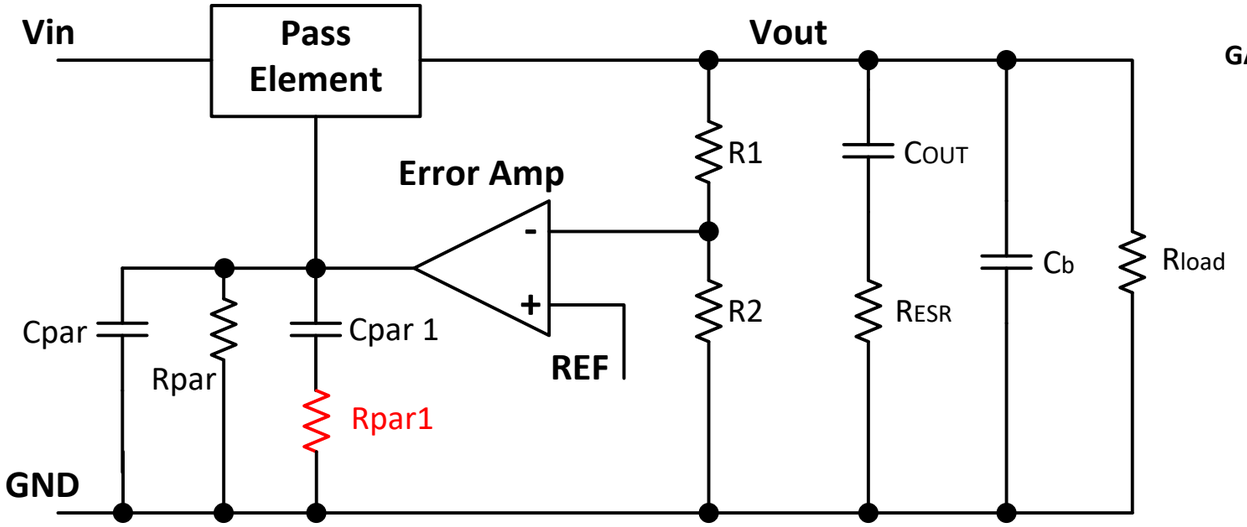


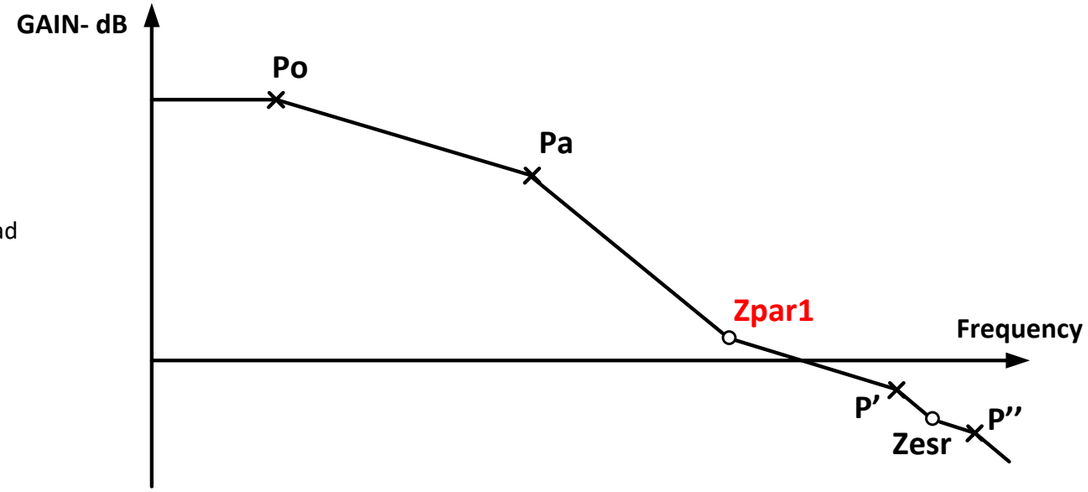
Adjust Cout ESR to move Zero to f1



For unstable frequency response of LDO with too high ESR, one more time adjustment is needed.

Loop Stable with Ceramic Capacitor



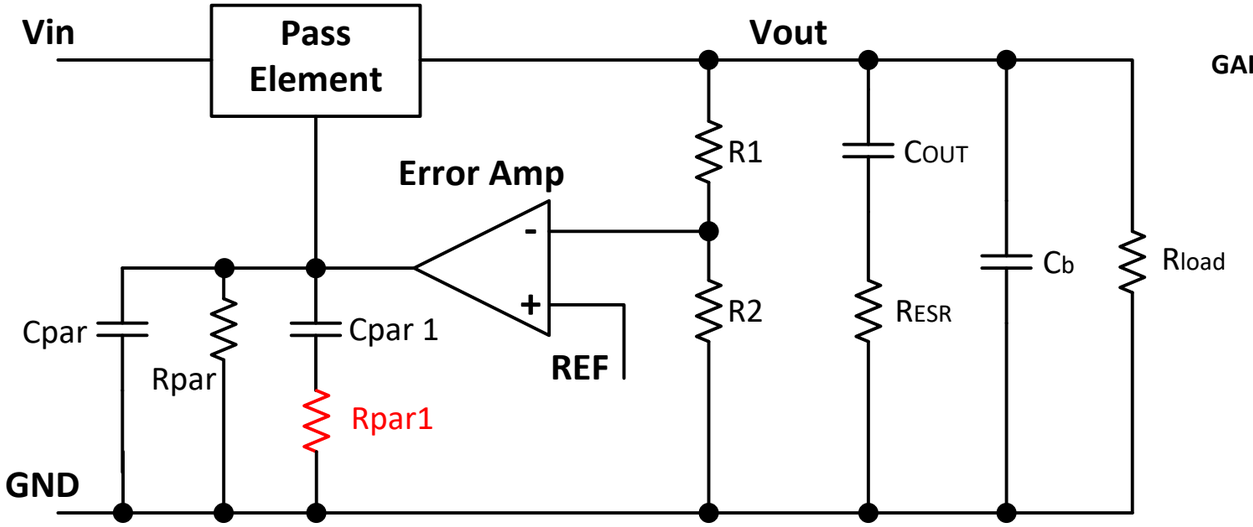


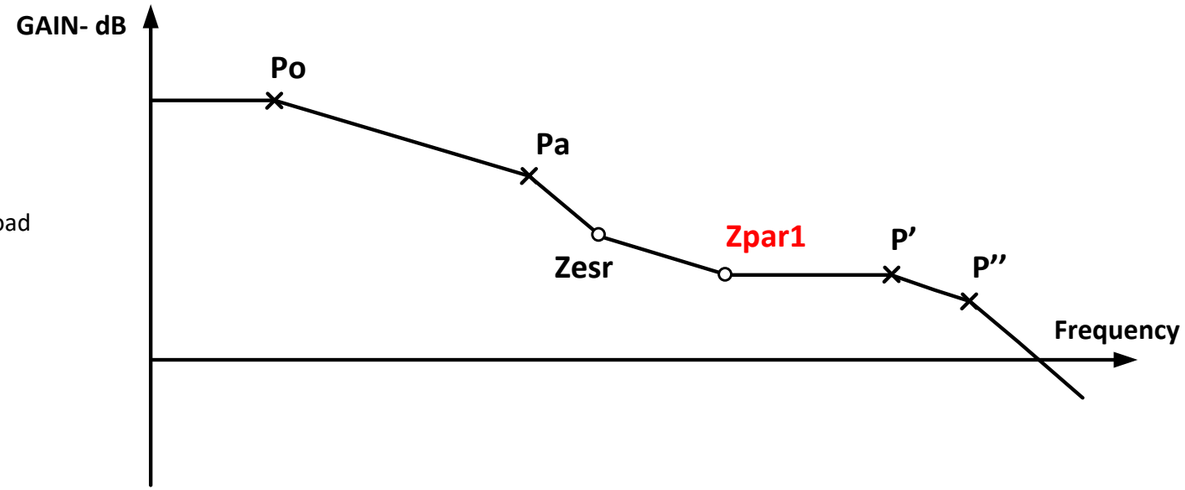
For a 10uF ceramic capacitor, the ESR is usually below 10mohm level:

$$Z_{ESR} = \frac{1}{2\pi * C_{OUT} * R_{ESR}} = \frac{1}{2\pi * 10uF * 10mohm} = 1.6MHz$$

1.6MHz frequency is too high for a LDO, the bandwidth is always lower than it. In order to stable the loop, a typical method is inserting a ZERO at amplifier output.

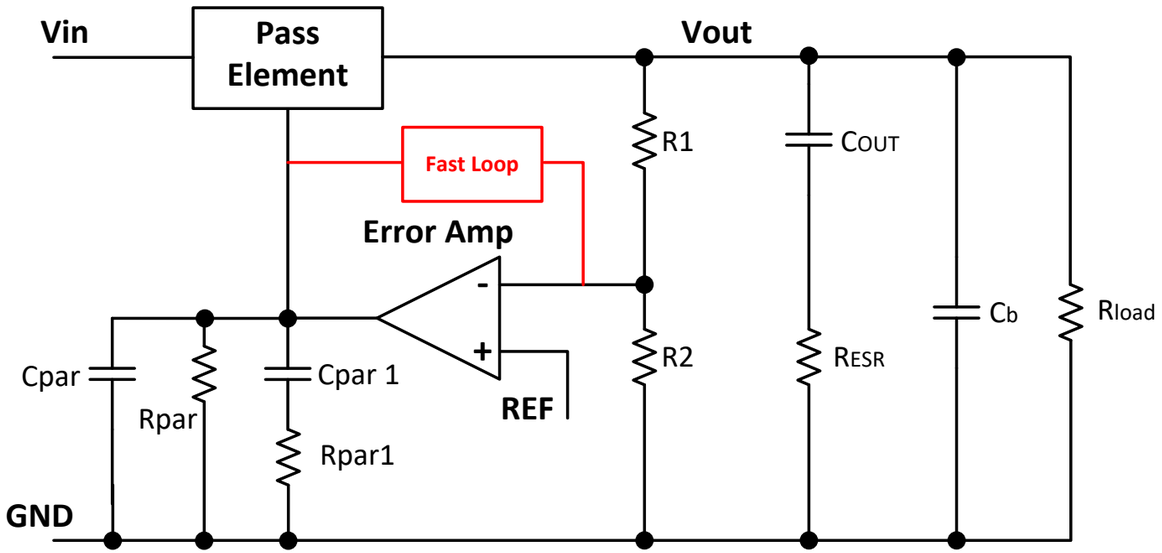
Problem for Loop Stable with Ceramic Capacitor

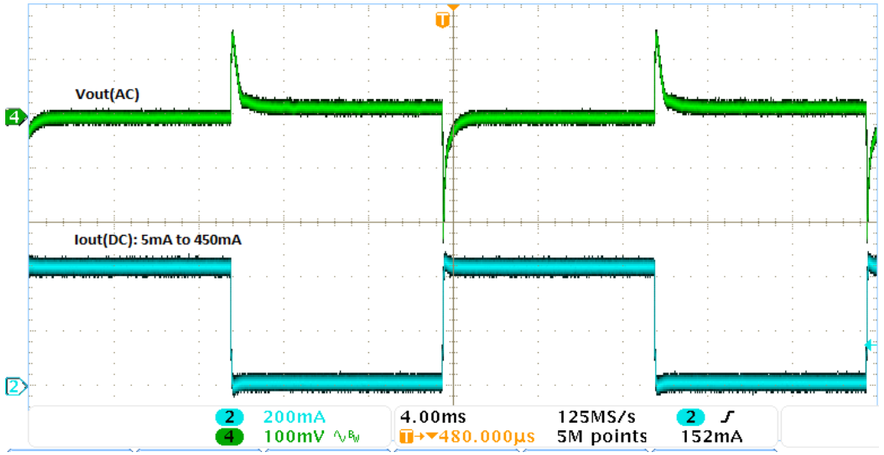




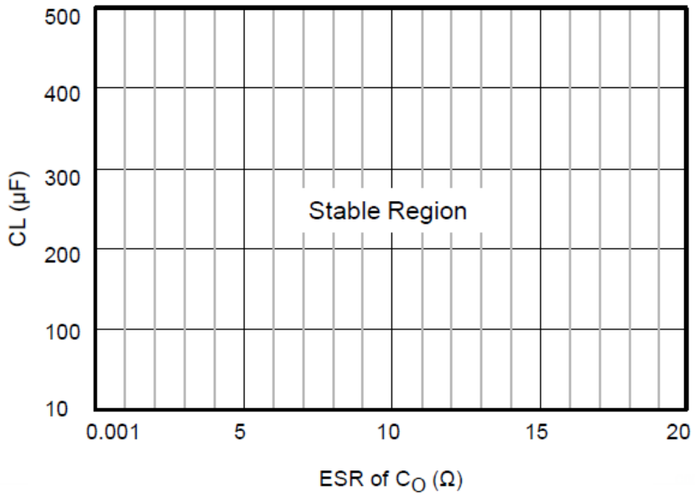
If electrolytic or tantalum capacitors are used, the Zero formed by output capacitor will move to low frequency, bandwidth would increase which might results to loop oscillation caused by high frequency poles.

Fast Loop Insertion to Achieve both Wide ESR range and Good Transient Performance





TPS7B6750-Q1, 5-450mA Load Step, 10uF Ceramic Output Capacitor



TPS7B6750-Q1 ESR Stable Region

In order to achieve both wide ESR range and good transient performance for a LDO, a fast loop could be inserted between FB and EA output.

TPS7B6750-Q1 is stable with 0.001-20ohm wide ESR range, still able to achieve a very good transient performance.

TPS7B67xx: 450mA 40-V LDO with Ultra Low Iq

Features

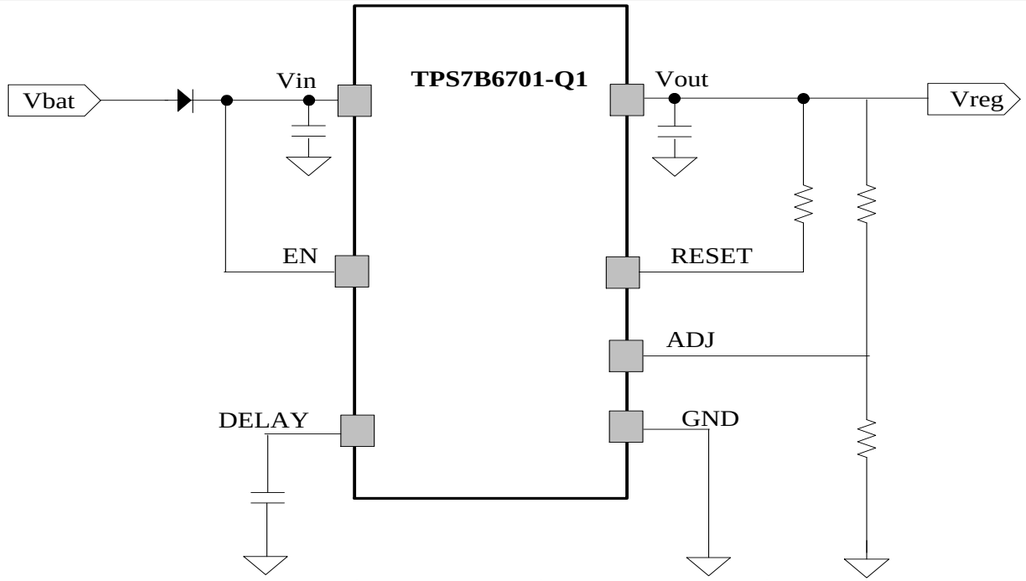
- Qualified for Automotive Applications
- 4 -V to 40-V Wide Vin Input Voltage Range
- With up to 45-V Transient
- Maximum Output current 450mA
- Low Quiescent Current Iq:
  - < 2uA when EN = low (shutdown mode)
  - 15uA typical at Light Loads
- Low ESR(0.001-20Ω) ceramic output stability capacitor (10uF-500uF)
- Maximum dropout Voltage 450mV at 400mA
- Adjustable 1.5V to 18V Output voltages
- Low Input Voltage Tracking to UVLO
- Integrated Power-On Reset
  - Programmable Reset Pulse Delay
  - Open drain Reset output
- Integrated Fault Protection
  - Thermal Shutdown
  - Short Circuit Protection
- Package: HTSSOP-20

Applications

- Cluster Power Supply
- Body Control Modules
- Always ON Battery Applications
  - Gateway Applications
  - Remote Keyless Entry Systems

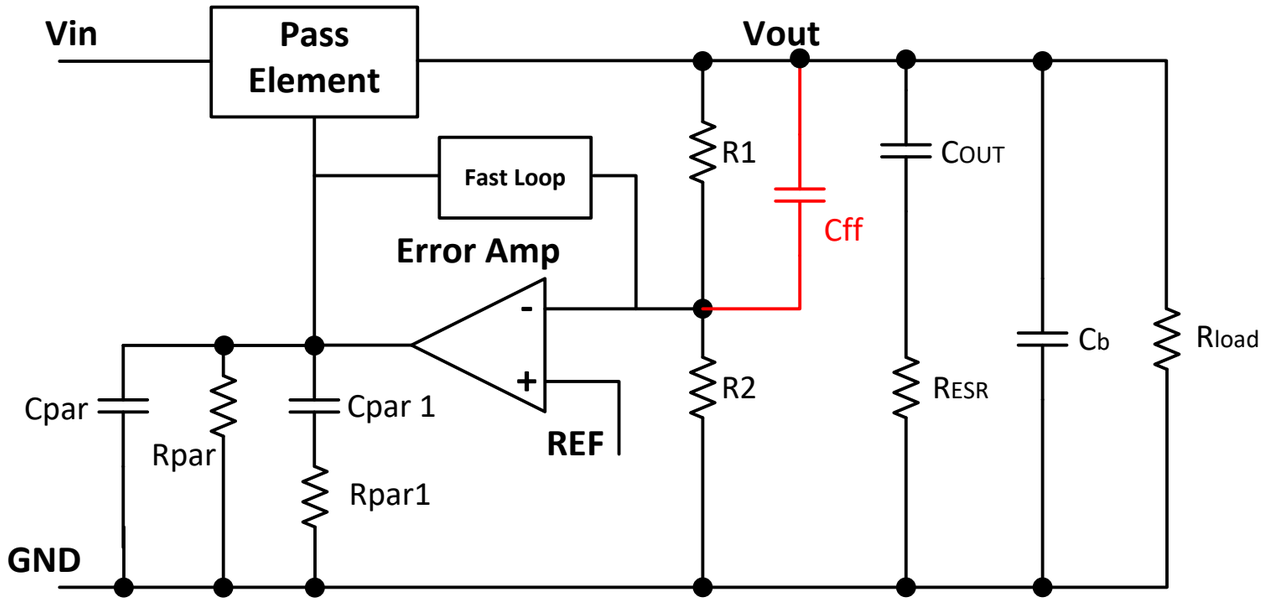
Benefits

- Low Quiescent Current Iq:
  - < 2uA when EN = low (shutdown mode)
  - 15uA typical at Light Loads
- Stable with wide output capacitor range (10uF-500uF) and wide ESR range ESR(0.001-20Ω)



TPS7B67xx Family	Vout (V)	Iq (typ) (uA)	Pin/Package
TPS7B6701-Q1	1.5 to 18	15	HTSSOP-20
TPS7B6733-Q1	3.3	15	HTSSOP-20
TPS7B6750-Q1	5	15	HTSSOP-20

Feedforward Capacitor Add Phase Lead



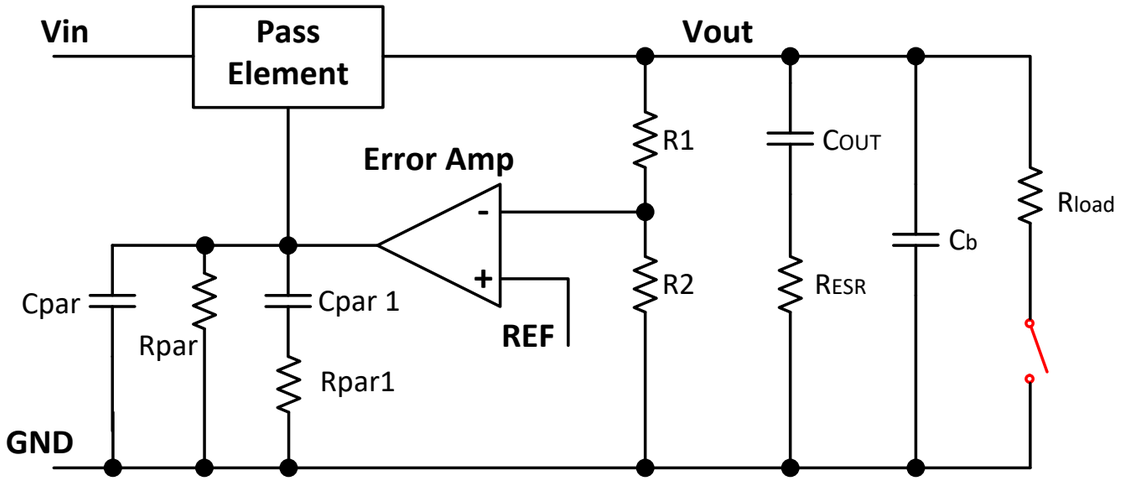
The Pole and Zero formed by feedforward capacitor Cff can be calculated by below:

$$P_{ff} = \frac{1}{2\pi * C_{ff} * \frac{R_1 * R_2}{R_1 + R_2}}$$

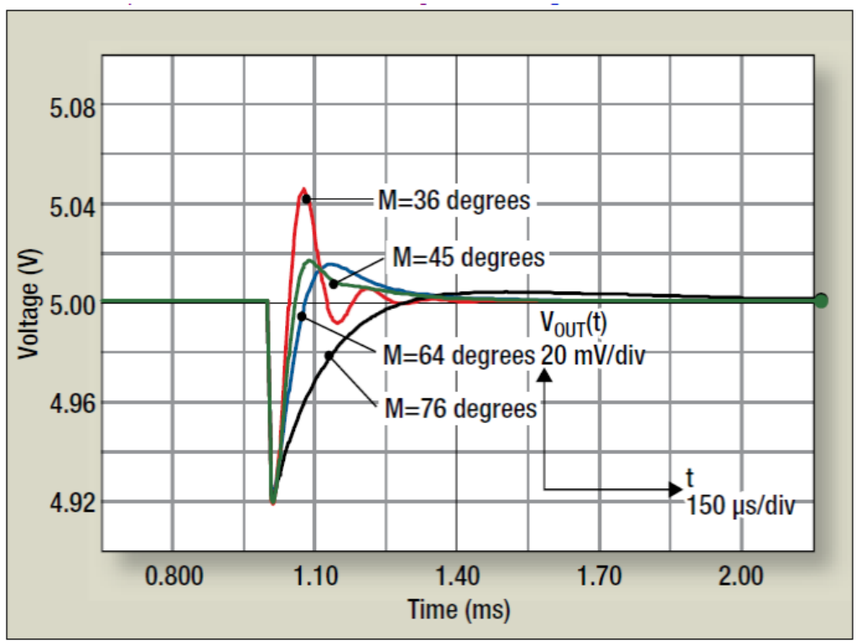
$$Z_{ff} = \frac{1}{2\pi * C_{ff} * R_1}$$

$$Z_{ff} < P_{ff}$$

Phase Margin Estimation



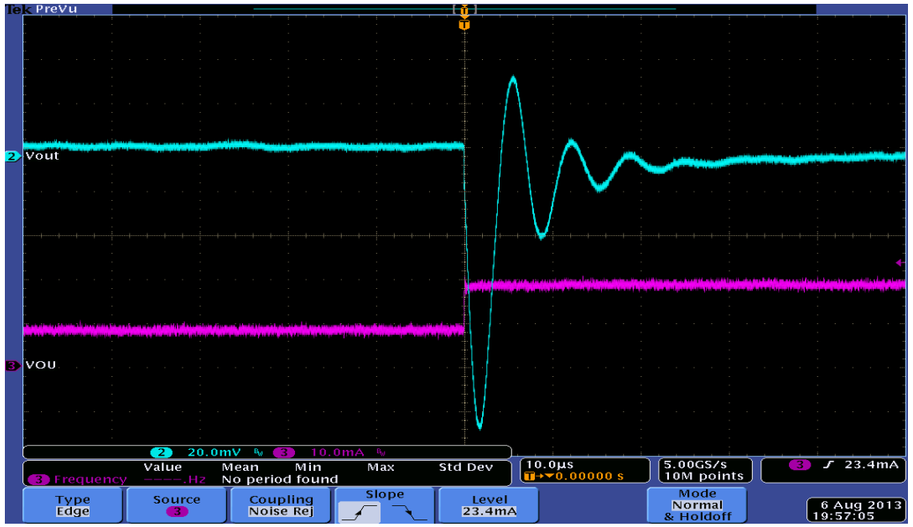
Phase Margin (Degrees)	Ringing (Bumps)
80.88	0
60.75	0
57.64	0
54.08	0
50.16	1
45.7	1.5
40.61	2
34.72	3
27.78	4
19.43	6
9.09	17



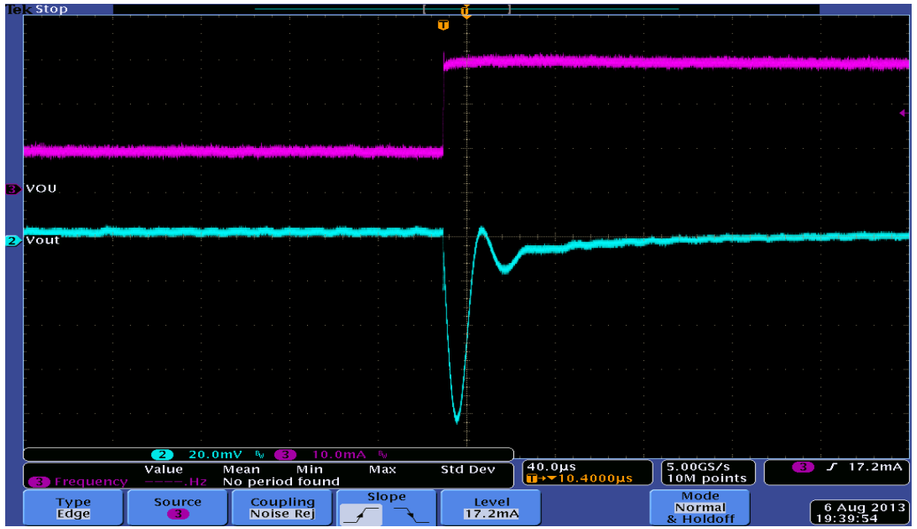
Phase Margin vs. Ringing

Phase margin is a measure of relative stability. Stability is a term referring to the ability of a controller to regain a constant or decaying output after an input or load step.

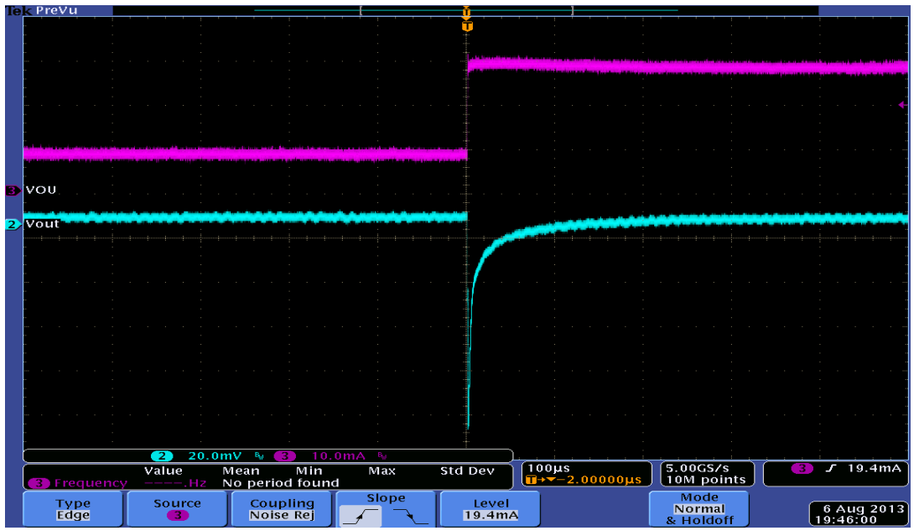
TPS7B4250 Phase Margin Estimation Margin Estimation



100nF Cout, 16° phase margin, 10-30mA load step



1uF Cout, 36° phase margin, 10-30mA load step



10uF Cout, >71° phase margin, 10-30mA load step

Above figures show the load transient responses under different phase margin by selecting different output capacitor, it can be seen that the ringing is related to the phase margin.

Power Solution for Automotive Off-board Loads

Off-board Sensor

Power Train

EPS

- Temperature Sensor
- Hall Sensor
- Pressure Sensor
- Position Sensor
- Lighting Sensor
- Urea Sensor

etc.…

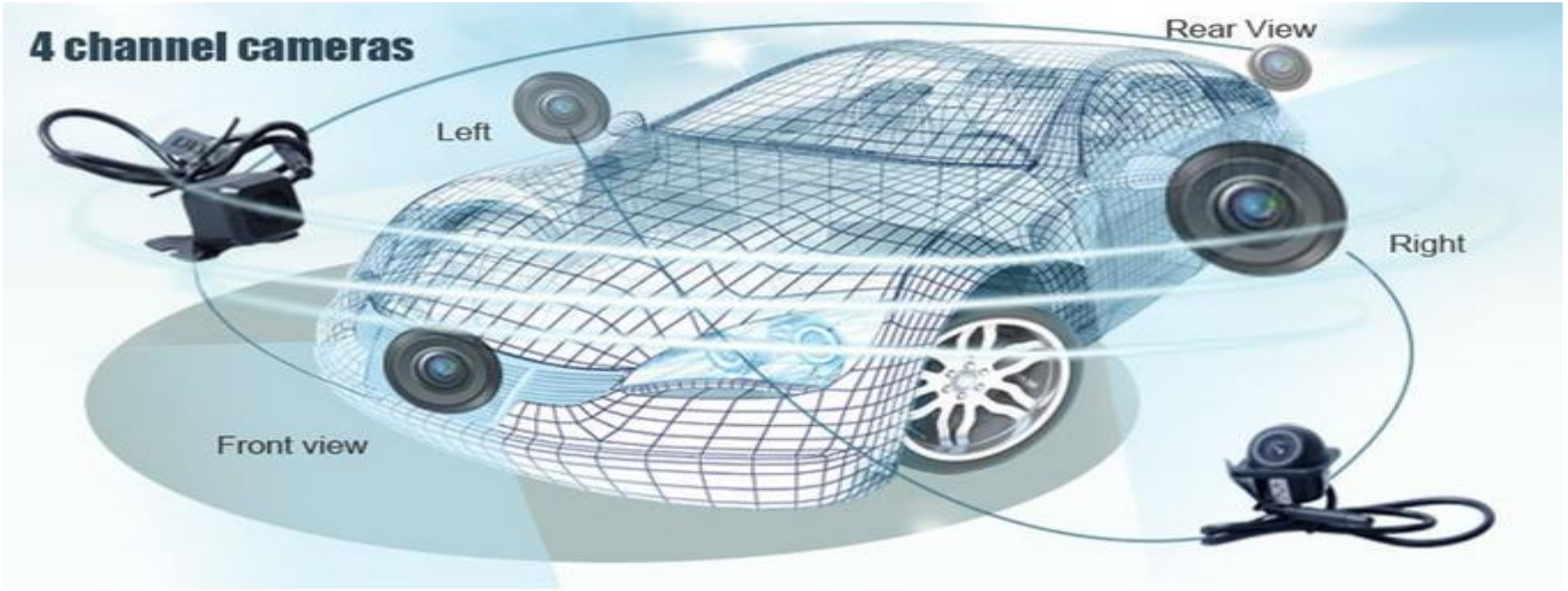
HVAC

BCM

Active Antenna

Estimated number of Antenna per car	Europe	North A.	China	Japan	S. Korea	India/ROW
AM/FM1	YES	YES	YES	YES	YES	YES
FM2	YES	YES	OPTIONAL	OPTIONAL	OPTIONAL	NO
DAB (Digital radio)	YES	OPTIONAL	NO	NO	YES	NO
GPS	OPTIONAL	OPTIONAL	OPTIONAL	YES	OPTIONAL	OPTIONAL
SDARS (Satelite radio, Sirius XM)	NO	YES	NO	NO	NO	NO
Minimum # of Antenna	3	3	1	2	2	1

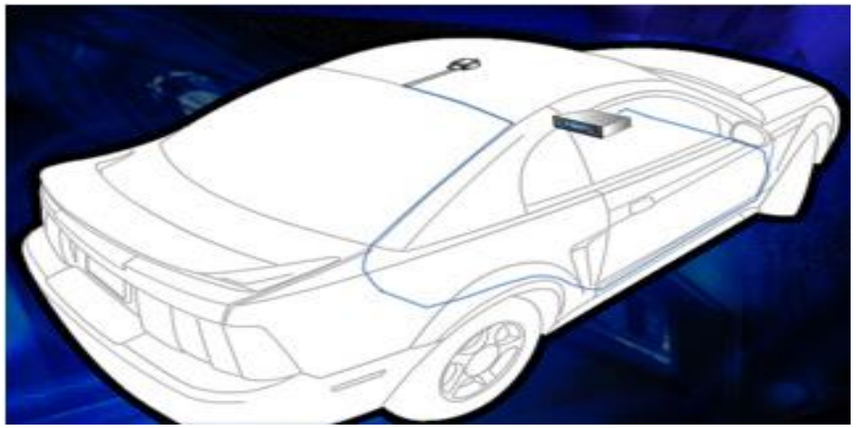
Surround View Camera



Automotive camera number trend, increasing!

Question

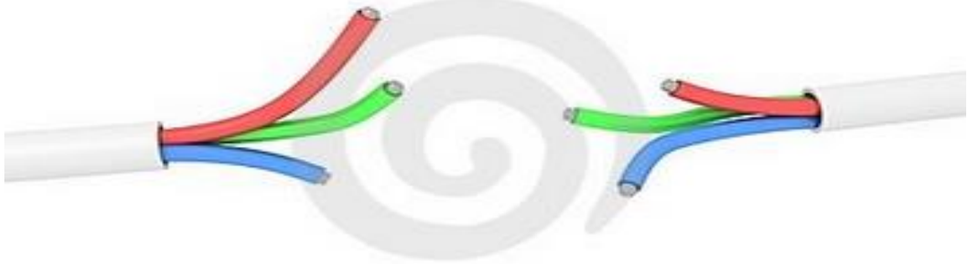
What is the common point of the off-board loads?

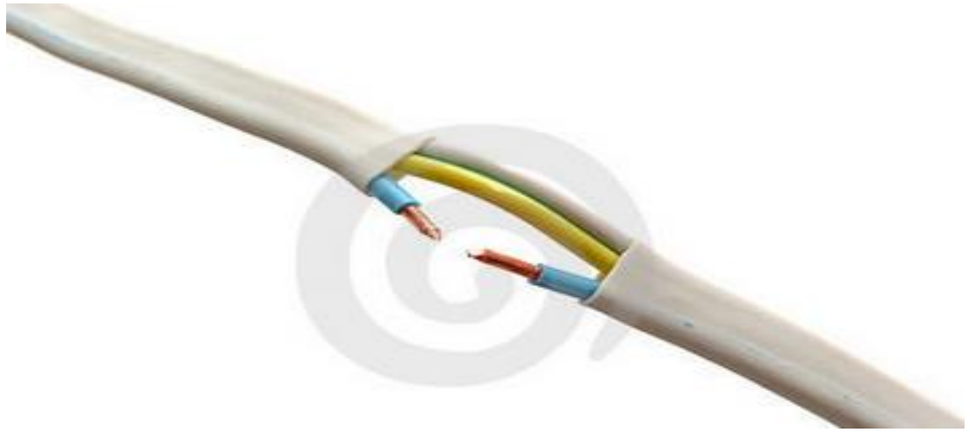


There is a cable connect between the main PCB and off-board load

Potential Issue

Cable Break

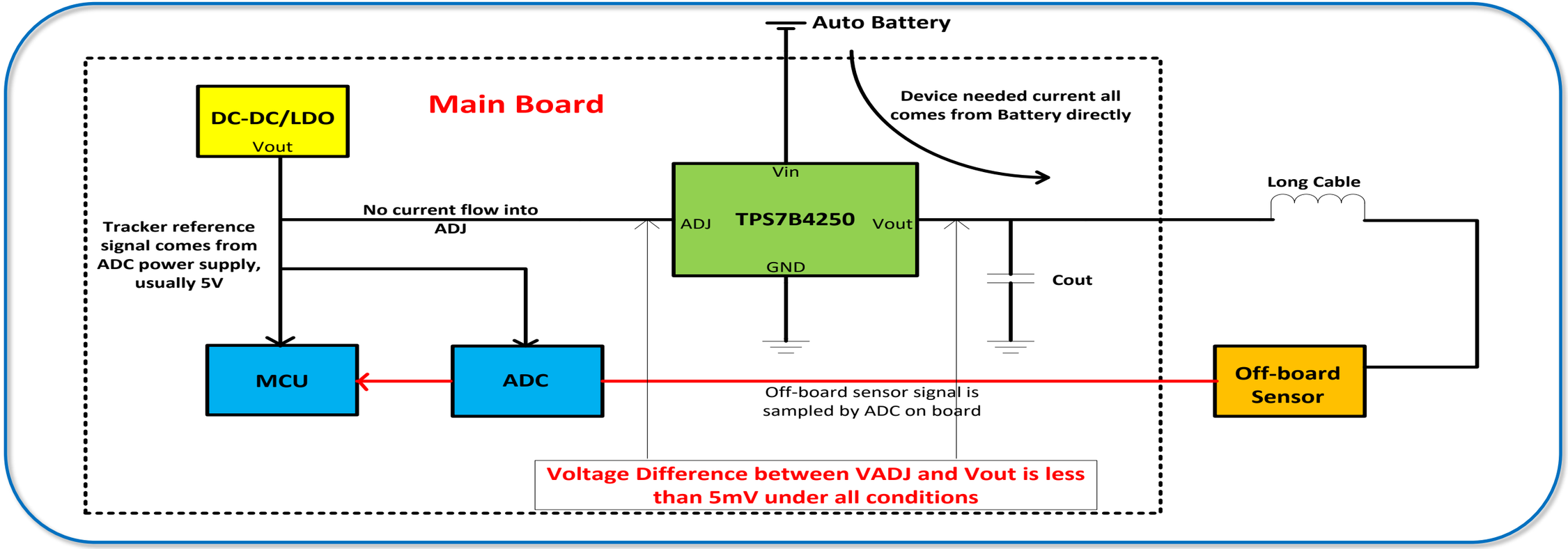




- Open
- Short to GND
- Short to Battery
- Reverse Polarity

Protection

Off-board Sensor Power supply



Application block diagram for off-board sensor power supply

Note: The long cable connect between off-board sensor and TPS7B4253 OUT might be broken during sever automotive conditions. TPS7B4253-Q1 is implemented with thermal shutdown, inductive clamp, over-load and short to battery protection, hence avoiding on-board components damage during harshness.

Tracking LDO Roadmap

Production | Sampling | Development | Concept

Output Current

TPS7B4253-Q1 (40V)

- Io = 300mA; Iq = 40uA; Rev. Polarity, inductive clamp
- ADJ pin for voltage tracking w/ ±4mV accuracy
- EN and FB pin to provide flexibility
- HTSSOP-20 in production
- HSOIC-8 Sample 3Q15, RTM 1Q16

TPS7B4254-Q1 (40V)

- Io = 150mA; Iq = 40uA; Rev. Polarity
- ADJ pin for voltage tracking w/ ±4mV accuracy
- Open Drain Status Output
- HSOIC-8

TPS7B4250-Q1 (40V)

- Io = 50mA; Iq = 40uA; Rev. Polarity
- ADJ pin for voltage tracking w/ ±5mV tolerance
- SOT23-5

Today **2016**

TPS7B4253: 300mA Low Dropout Tracking LDO

Features

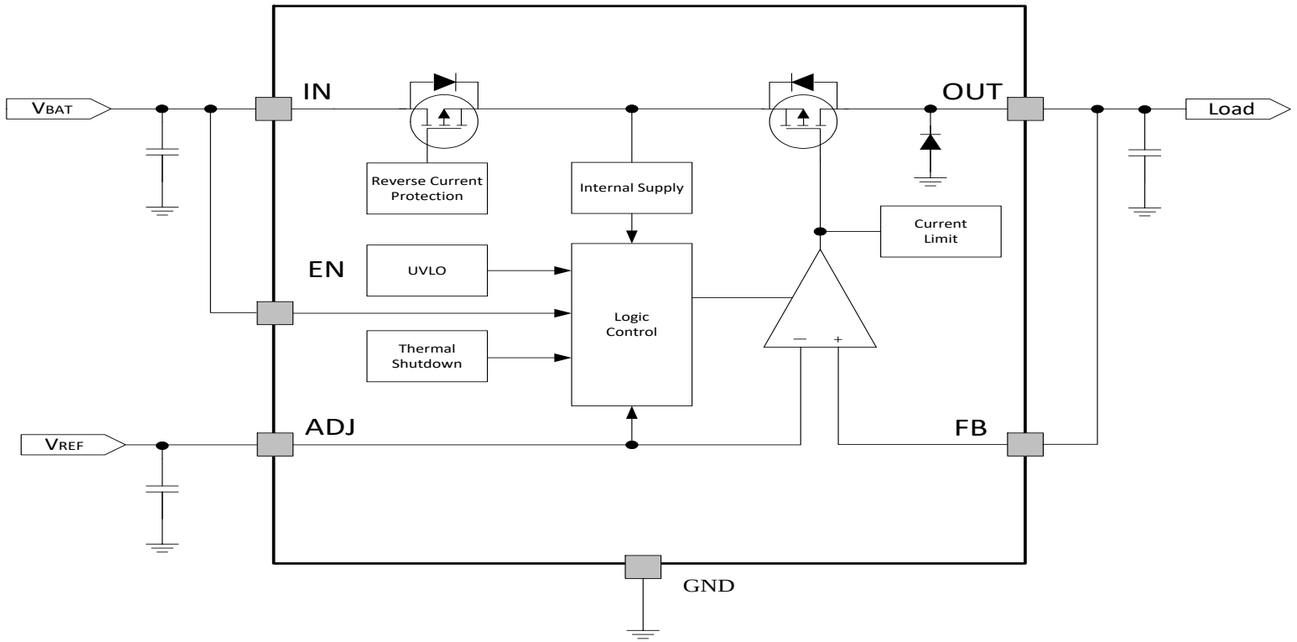
- -40V to 45V Wide Input Voltage Range (Maximum)
- Output Voltage Adjusts Down to:
  - 1.5 to 40V (HTSSOP-20)
  - 2 to 40V (HOSIC-8)
- Very Low Output Tracking Tolerance, ±4mV
- 320mV Low Dropout Voltage When IOUT=200mA
- 520mA Maximum Current Limit
- Low Quiescent Current (IQ):
  - < 4uA when EN=LOW
  - 60uA (Typical) at Light Loads
- Extremely Wide ESR Range.
  - Stable With 10 to 500uF Ceramic Output Capacitor, ESR 1mΩ to 20Ω
- Reverse Polarity Protection
- Current Limit and Thermal Shutdown Protection
- Output Short Circuit Proof to Ground and Supply
- Inductive Clamp at OUT Pin
- HTSSOP-20, HSOIC-8 Package

Applications

- Off-board Sensor Power Supply
- Parallel with Other LDOs
- Power Switch for Off-board Loads

Benefits

- 4mV Ultra Low Output Tracking Tolerance
- Wide Stable Region for Output Capacitor and ESR
- Wide Input and Output Voltage Operating Range, OUT pin with short to battery protection



Diagnose

Antenna LDO Roadmap

Production Sampling Development Concept

Output Current

TPS7B7702-Q1

- Io = 300mA dual channel
- High Current Sense Accuracy (±20% @ Io < 10mA)
- Output Configurable as Adjustable, Fixed and Power Switch
- Current Sense Multiplex to save ADC resource
- Full Diagnostic and Integrated Protection
- HTSSOP-16

TPS7B7701-Q1

- Io = 300mA single channel
- P2P w/ dual channel & same performance

Today 2016 2017

TPS7B77xx – Single and Dual-Channel Antenna Supply

Features

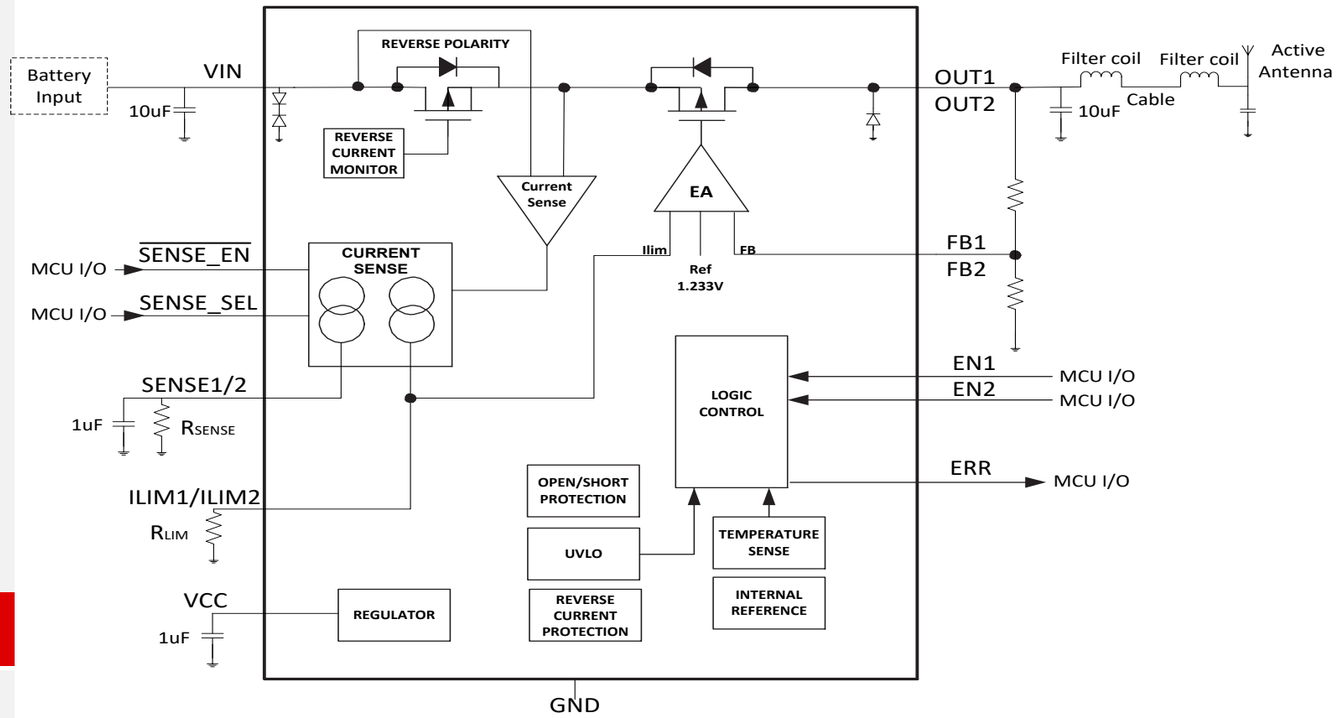
- Qualified for Automotive Applications
- Single and Dual-channel LDO in same package
- 4.5V to 40V wide Input Voltage Range, Load Dump 45V
- Adjustable Output Voltage 1.5 ~ 20V
- Adjustable Current Limit (50 ~ 300mA) with External Resistor
- High accuracy current sense to detect antenna open / normal / over current / short circuit conditions without further calibration at low current (±20% @ Io < 10mA)
- High Power Supply Rejection Ratio: typ. 73dB @ 100Hz
- Integrated Reverse Polarity Diode Protection, down to -40V
- Stable with Output Capacitor in 2.2 ~ 100uF (ESR 1mΩ to 5Ω)
- Full Diagnostic & Integrated Protection
  - ➢Thermal Shutdown
  - ➢Short Circuit Protection
  - ➢Reverse Battery Polarity Protection
  - ➢Reverse Current Protection
  - ➢Output Short to Battery Protection
  - ➢Output Inductive Load Clamp
  - ➢Multiplexing Current Sense between Channels and Device
  - ➢Ability to distinguish all faults with current sense
- Operating Ambient Temperature Range: -40°C to +125°C
- Thermally enhanced PWP package (HTSSOP - 16)

Applications

- Infotainment Active Antenna Power Supply
- Surround-View Camera Power Supply
- High-Side Power Switch For Small Current Applications

Benefits

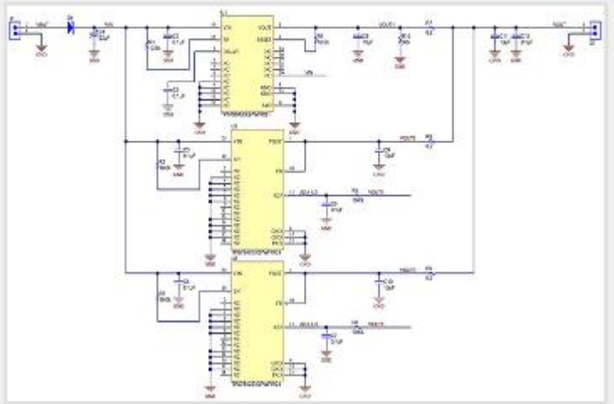
- High current sensing accuracy help to distinguish open and normal status without external calibration
- Complete protection and diagnose for off-board application
- Current sense multiplexing between device and channel help to save ADC resource

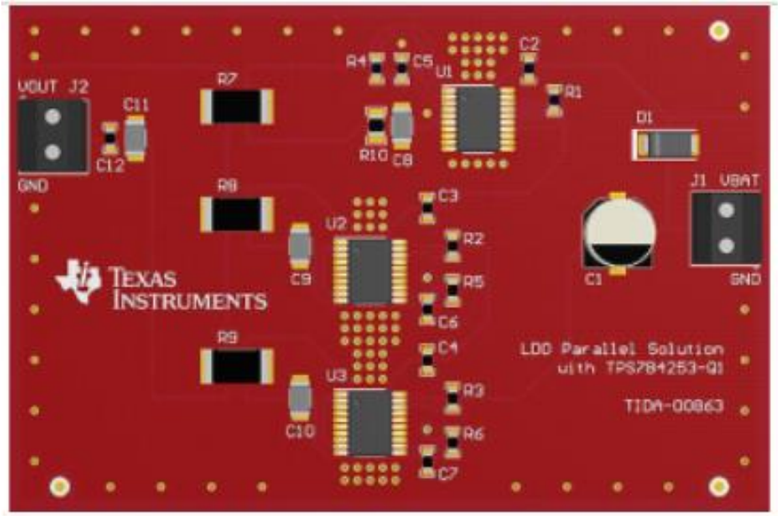


Additional Resources TI Designs

Schematic/Block Diagram

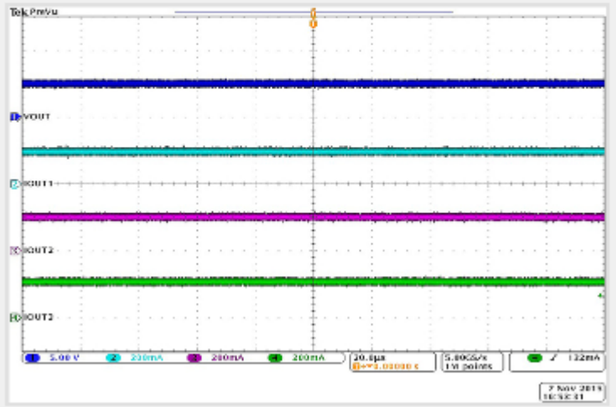
Quickly understand overall system functionality.





Test Data

Get results faster with test and simulation data that's been verified.



LDO Parallel Solution Reference Design with TPS7B4253-Q1

Thank you