Basics of Analog Multiplexers 2

TIPL 2602

TI Precision Labs – Op Amps

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Analog Multiplexer Parameters Summary

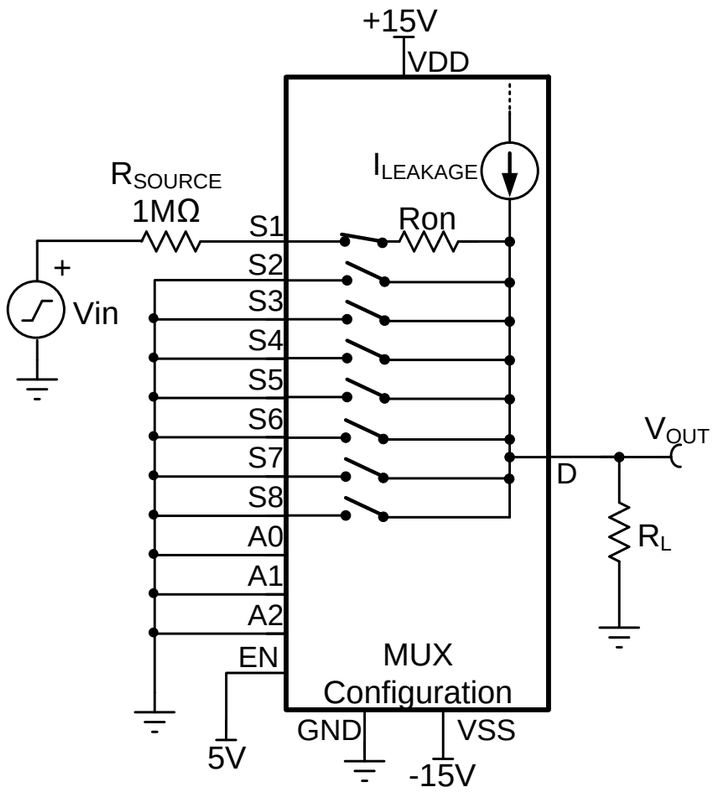
- Part 1: Understanding Performance parameters of Multiplexer

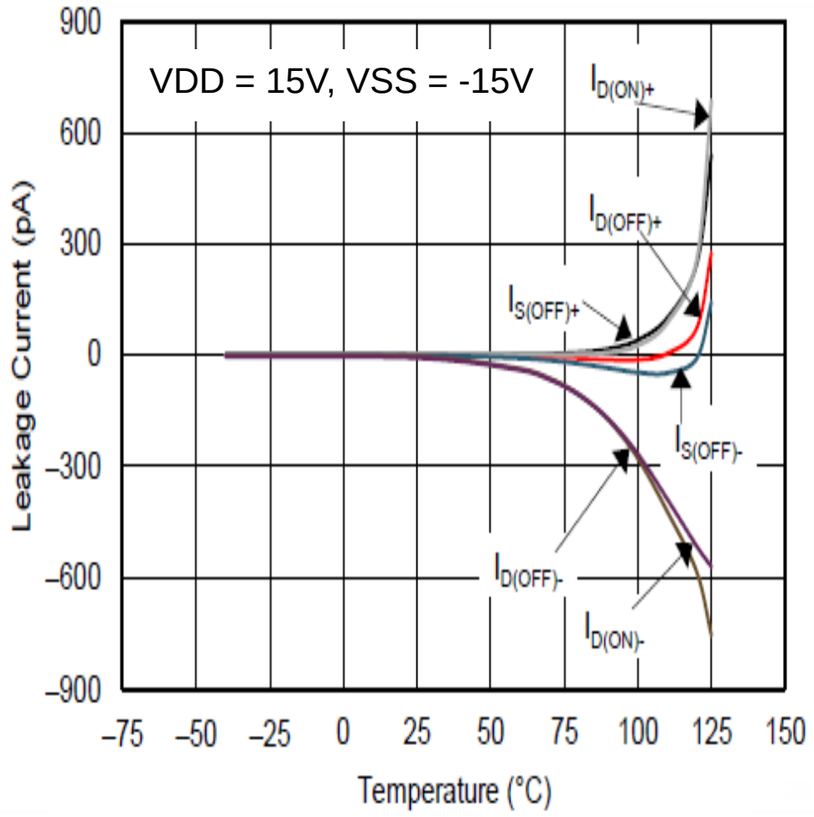
  1) Leakage Current
  - Types of Leakage Current
  - Offset issues Related to Leakage Current

  2) Charge Injection
  - Understanding Charge Injection Phenomenon
  - Effect of Charge Injection on Multiplexer Output Voltage Error

- Goals:
  - 1. To understand performance parameters of multiplexers
  - 2. Understand their importance while designing data acquisition system

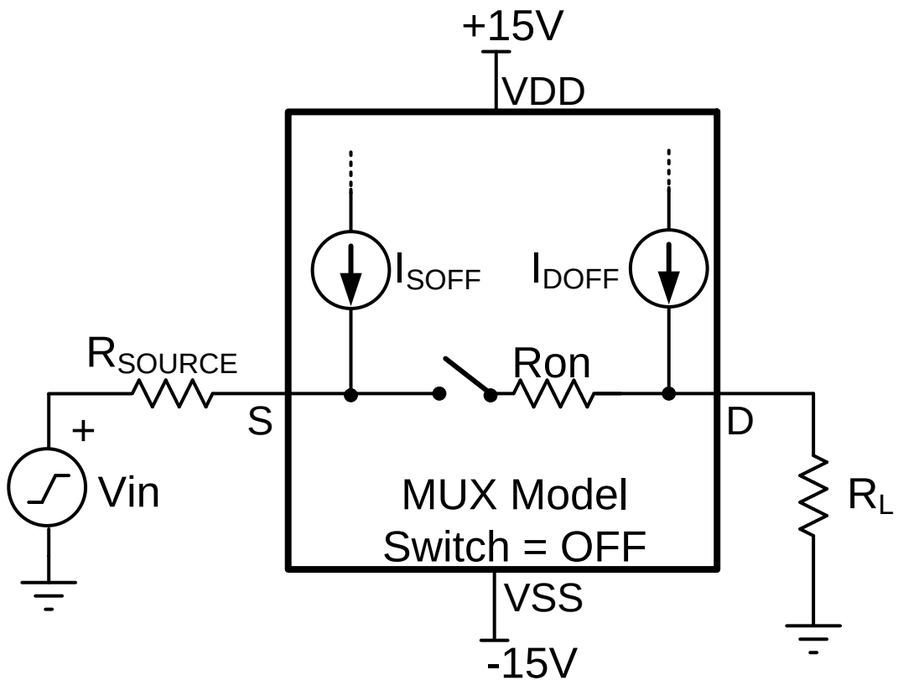
Leakage Current

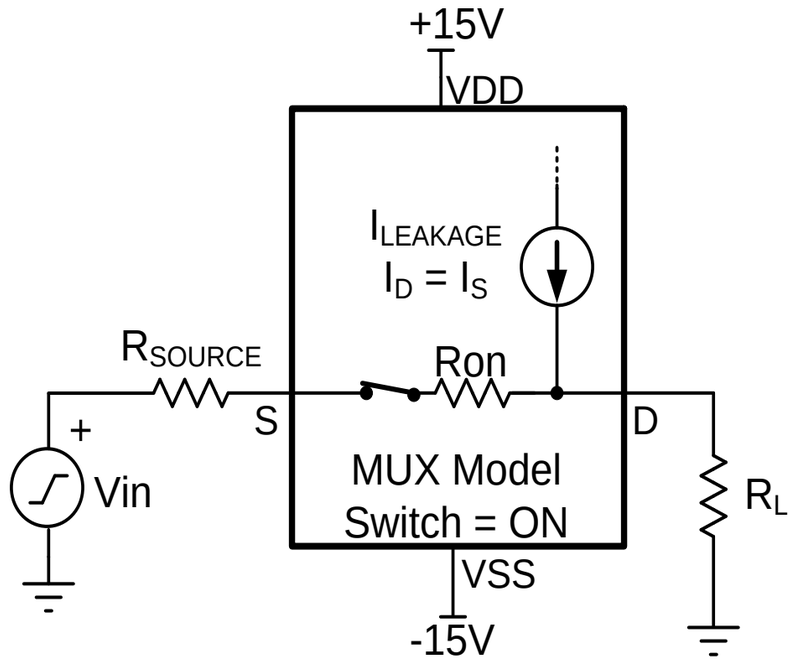




- **Leakage Current**: Current flowing out Source (S) and Drain (D) pins when MUX switch is ON or OFF
- **Switch = OFF**: Leakage current flows out Source pin and Drain pin, $I_{S(OFF)}$ and $I_{D(OFF)}$
- **Switch = ON:** Approximate leakage current out Source and Drain pin is $I_{S(ON)} = I_{D(ON)}$

Leakage Current

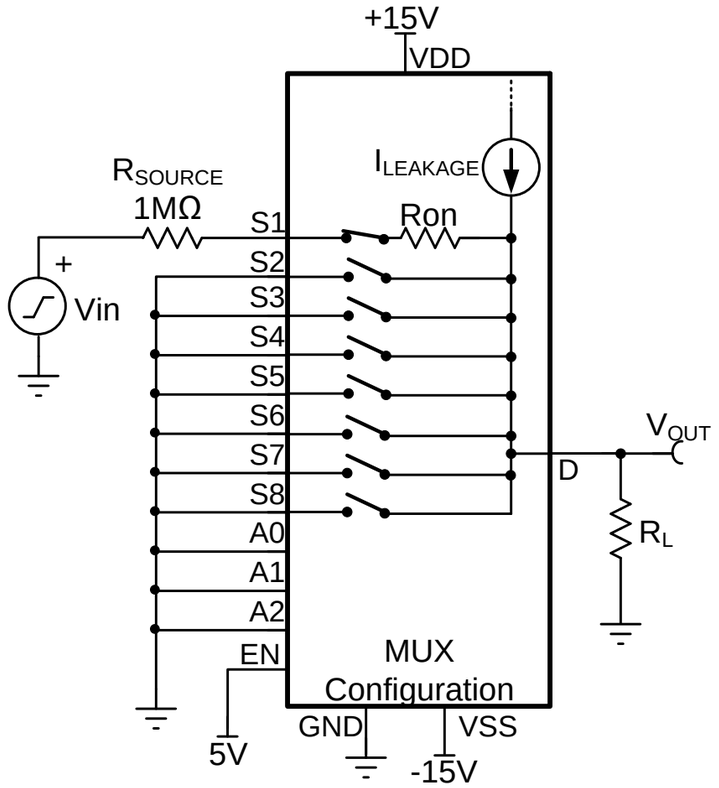




- **Switch = OFF:** $I_{S(OFF)}$ flows through R_{SOURCE} and $I_{D(OFF)}$ flows through R_L

- **Switch = ON:** Error introduced by leakage current: $V_{ERROR} = (R_{ON} + R_{SOURCE}) \times I_{D(ON)}$

Offset Error Introduced by Leakage Current



18-bit System Example Calculation

$$V_{ref} = 5V$$

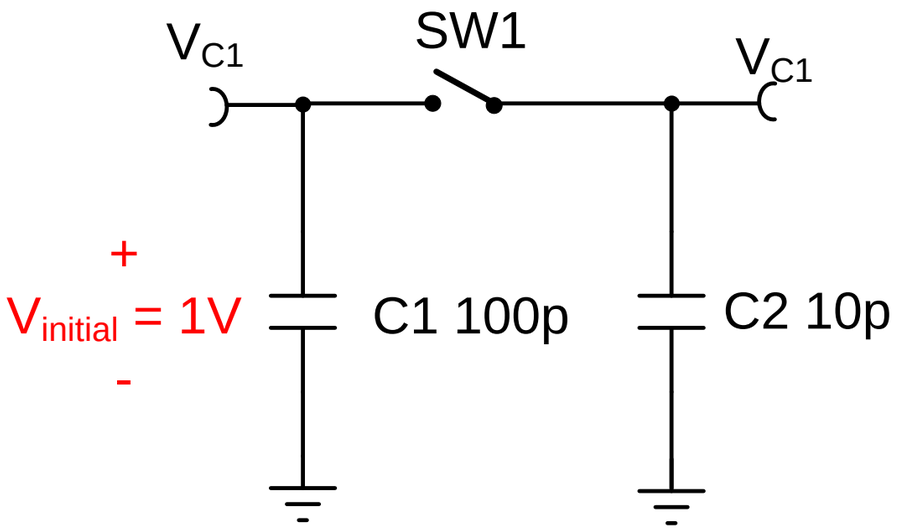
$$V_{LSB} = \frac{5V}{2^{18}} = 19.073\mu V$$

$$\text{OffsetError(V)} = I_{LEAKAGE} \cdot R_{SOURCE} = (100pA)(1M\Omega) = 100\mu V$$

$$\text{OffsetError(Bits)} = \frac{\text{OffsetError(V)}}{V_{LSB}} = \frac{100\mu V}{19.073\mu V} = 5.24\ codes$$

Multiplexer Examples	Multiplexer leakage current (25°C/85°C)	Offset error (25°C/85°C) ($I_{LEAKAGE}$ x R_{Source})	Offset Error 18 bit System (in bits)
MUX1 (Low Leakage)	10pA/50pA	10µV/50µV	0.52 / 2.62
MUX2 (High Leakage)	100pA/500pA	100µV/500µV	5.24 / 26.22

Review: Charge Equation



Charge Equation Example

Definition
Q = Charge in Coulombs
C = Capacitance in Farads
V = Voltage in Volts

$$Q = C \cdot V$$

Charge of C1,
Assuming initial 1V

$$Q = C_1 \cdot V_1 = (100pF) \cdot (1V) = 100pC$$

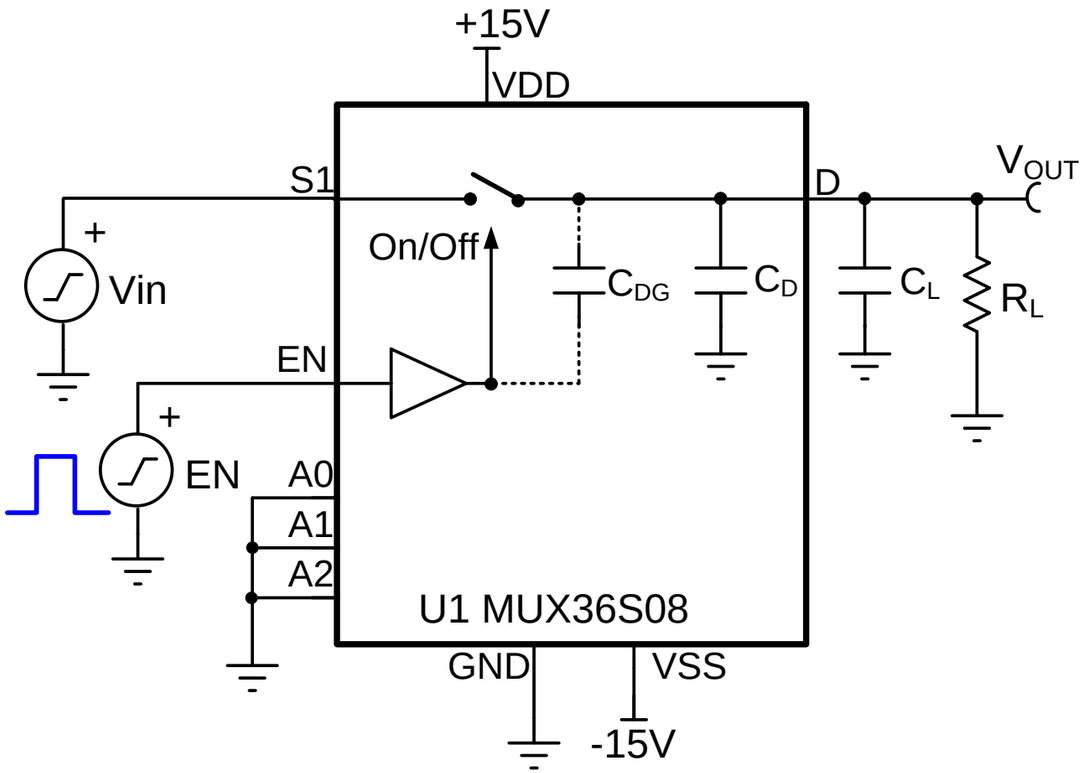
Close switch

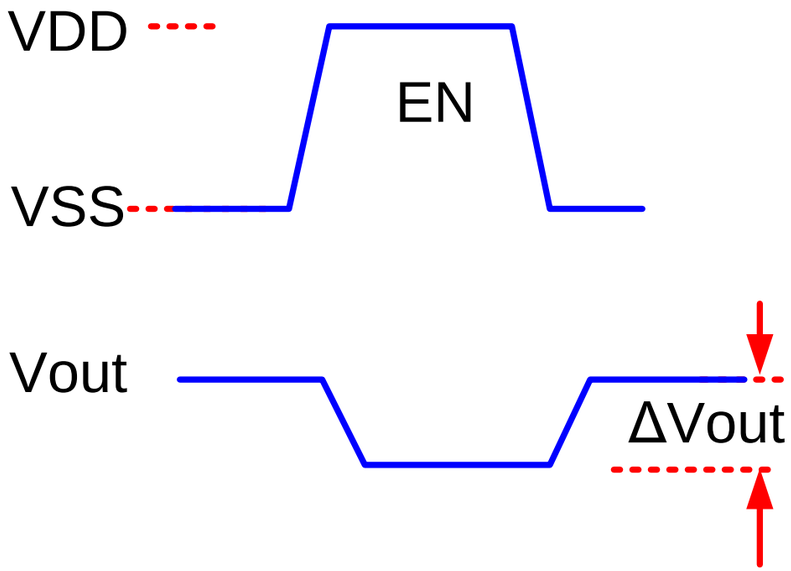
$$C_{total} = C_1 + C_2 = 110pF$$

New Voltage after charge redistribution

$$V_{final} = \frac{Q}{C_{total}} = \frac{100pC}{110pF} = 0.909V$$

Charge Injection (Q_{INJ})

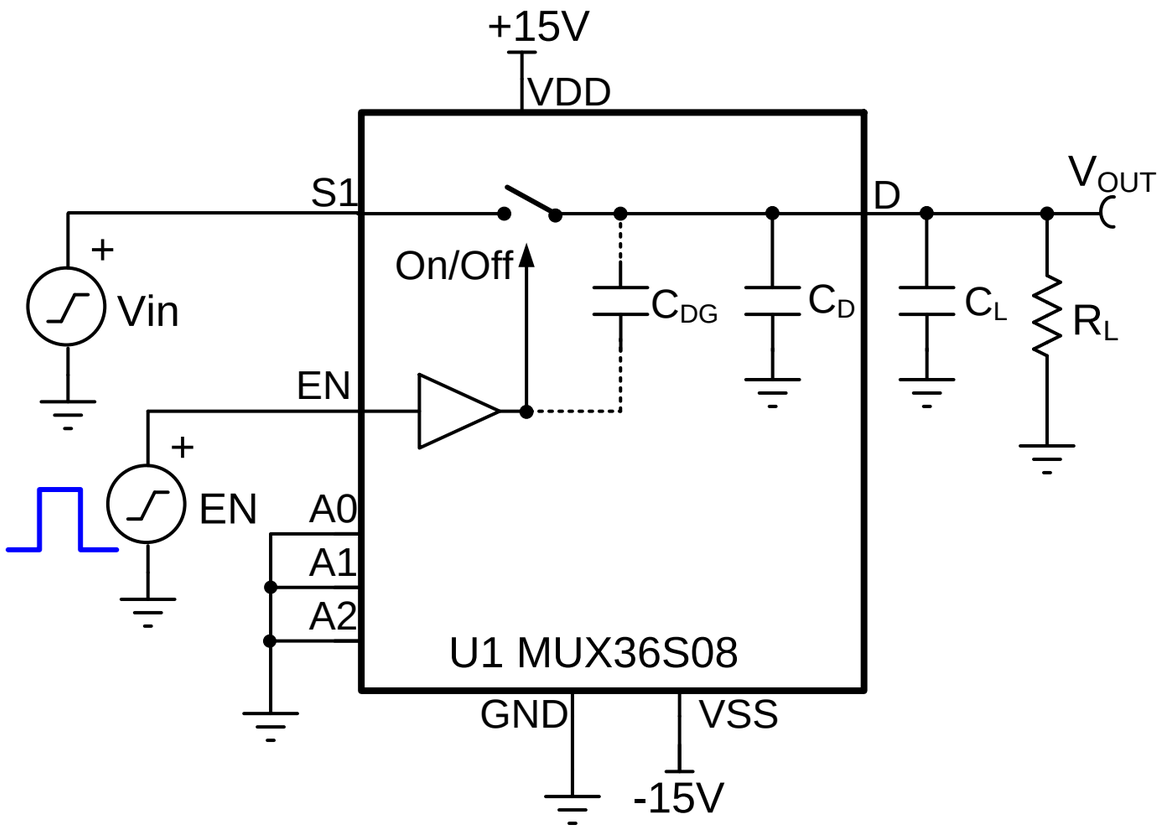


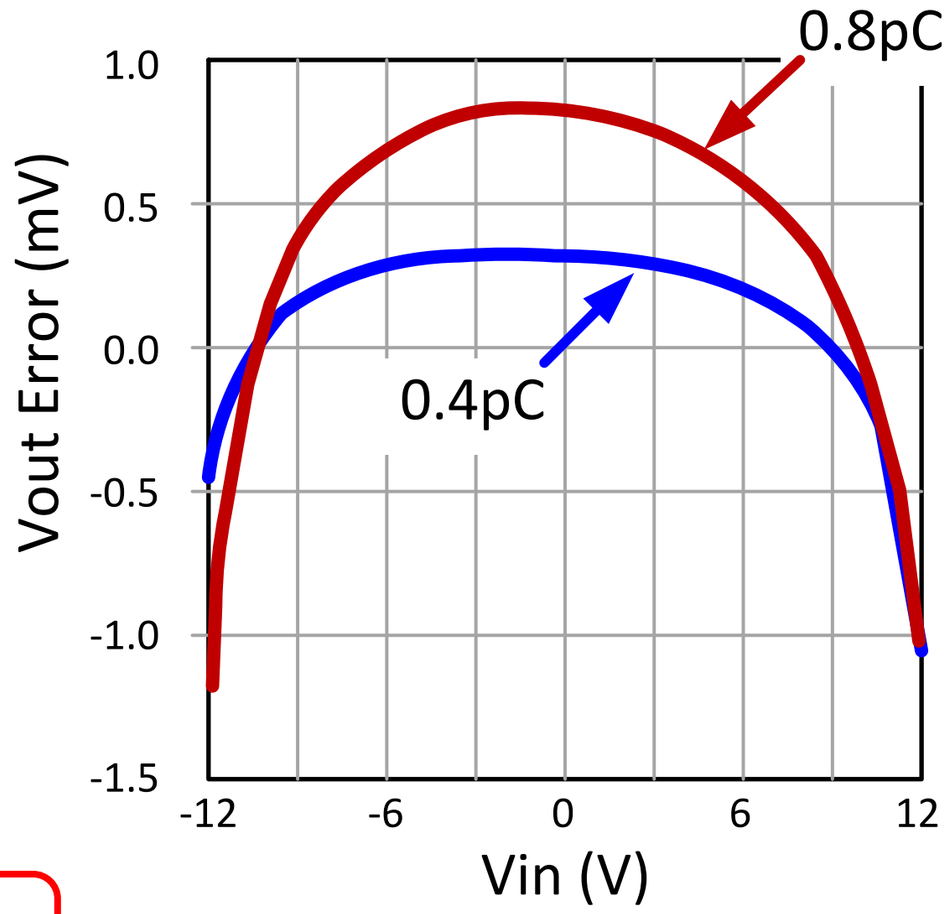


$$Q_{NJ} = (C_D + C_L) \cdot \Delta Vout$$

- **Charge injection Error**: Voltage change introduced at the output of switch when switch is turned ON or OFF
- Larger load capacitance minimizes the effect of charge Injection at the multiplexer output

Charge Injection Error vs. Input Voltage





Error = Q_{INJ} / C_L

Summary: MUX Leakage Current and Charge Injection

Leakage Current

- Introduces DC offset Error
- Varies with temperature and can introduces linearity errors too
- Important parameter for high input impedance data acquisition systems

Charge Injection

- Introduces output voltage error when control logic is switched
- Typically worse on multiplexers with large Con.
- Smaller the load capacitor higher the error introduced due to charge injection
- Important parameter for fast switching systems

Thanks for your time!
Please try the quiz.

Basics of Analog Multiplexers – 2

Multiple choice quiz
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Quiz: Basics of Analog Multiplexers – 2

1. Leakage current of a multiplexer

a. Introduces offset error

b. Varies with temperature

c. affects settling behavior of multiplexer

d. Both a and b

2. A multiplexer with a leakage current of 1nA interfaced with a 100k Ohm input impedance source can introduce

a. 10uV of offset error at input of the MUX

b. 100uV of error at input of the MUX

c. No offset error at input of the MUX

d. None of the above

Quiz: Basics of Analog Multiplexers – 2

3. Charge Injection effect is

a. Settling error introduced at the output of switch when switch is turned ON or OFF

b. Charge injected in power supply bypass capacitors when switch is turned ON or OFF

c. Amount of voltage change introduced at the output of switch when switch is turned ON or OFF

d. Both b and c

4. For a larger load capacitor at the output of a multiplexer,

a. More voltage error is introduced by charge injection

b. Less voltage error is introduced by charge injection

c. There is no relation with charge injection effect

d. None of the above

Quiz: Basics of Analog Multiplexers – 2

5. The charge injection parameter of a multiplexer can have one of the following units

a. Pico Coulomb

b. Pico Farad

c. Micro Volt

d. None of the above

6. A multiplexer with a charge injection of 1pC and a load capacitance of 50pF can introduce a voltage error of ____ when the switch is turned ON or OFF.

a. 20mV

b. 50mV

c. 5mV

d. None of the above

Quiz: Basics of Analog Multiplexers – 2

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Exercises

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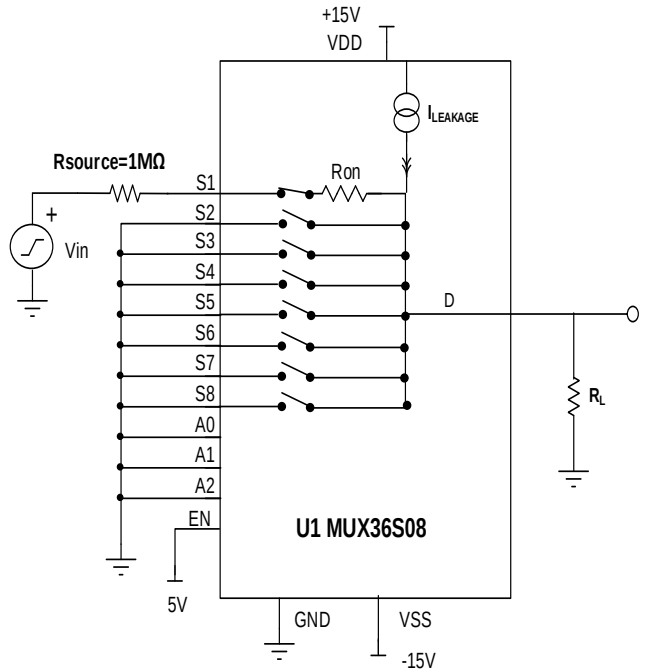
1. In the circuit below, the MUX36S08 input channel is interfaced with a high input impedance source (1MΩ). The MUX has an on leakage current specification of 8pA to 100pA over 25^0C to 85^0C temperature range. This multiplexer is used in a 18 bit data acquisition system referenced to 4.5V. It is required that offset error introduced due to MUX leakage should not exceed a 10 LSB specification. Does this multiplexer meet this condition?

Assume Rsource >> Ron



2. There is an option to select one of the two multiplexers (MUX1 and MUX2) for a given DAQ system. MUX1 and MUX2 have charge injection figures of 1pC and 4.7pC respectively. MUX1 has an output load capacitance of 47pF while MUX2 has a load capacitance of 100pF. Which multiplexer will have minimum voltage error due to charge injection at the output?

Basics of Analog Multiplexers – 2

Solution

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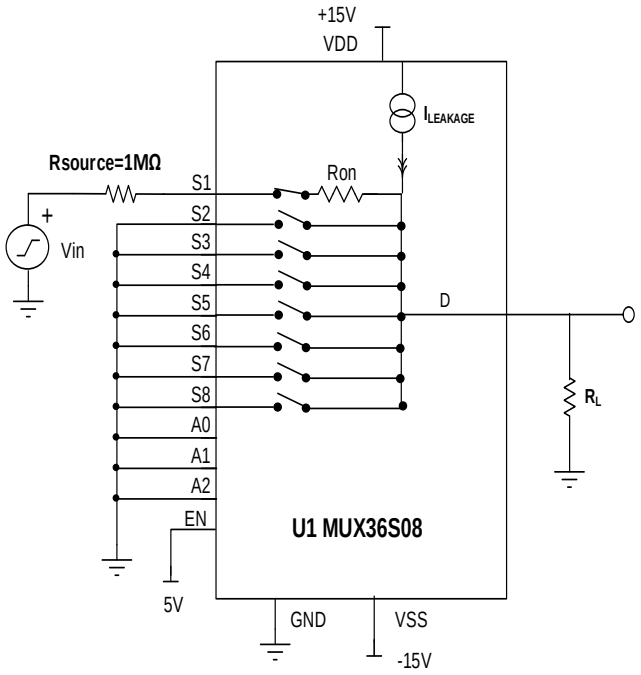
1. In the circuit below, the MUX36S08 input channel is interfaced with a high input impedance source (1MΩ). The MUX has an on leakage current specification of 8pA/100pA over 25^0C to 85^0C temperature range. This multiplexer is used in a 18 bit data acquisition system referenced to 4.5V. It is required that offset error introduced due to MUX leakage should not exceed a 10 LSB specification. Does this multiplexer meet this condition?



18-bit System Calculation

$$V_{ref} = 4.5V$$

$$V_{LSB} = \frac{4.5V}{2^{18}} = 17.16\mu V$$

$$\text{OffsetError}(V)_{25C} = I_{LEAKAGE} \cdot R_{SOURCE} = (8pA) * (1M\Omega) = 8\mu V$$

$$\text{OffsetError}(\text{Bits})_{25C} = \frac{\text{OffsetError}(V)}{V_{LSB}} = \frac{8\mu V}{17.16\mu V} = 0.46\ LSB$$

$$\text{OffsetError}(V)_{85C} = I_{LEAKAGE} \cdot R_{SOURCE} = (100pA) * (1M\Omega) = 100\mu V$$

$$\text{OffsetError}(\text{Bits})_{85C} = \frac{\text{OffsetError}(V)}{V_{LSB}} = \frac{100\mu V}{17.16\mu V} = 5.82\ LSB$$

1. In below circuit MUX36S08 input channel is interfaced with high input impedance source (1MΩ). MUX has on leakage current specification of 8pA/100pA over 25^0C to 85^0C temperature range. This multiplexer is used in 18 bit data acquisition system referenced to 4.5V. It is required that offset error introduced due to MUX leakage should not exceed 10 LSB specification. Does this multiplexer meet this condition?

Answer: From calculations shown in previous slide, we can see that the offset error introduced by the MUX36S08 across 25^0C to 85^0C is 0.46 LSBs to 5.82 LSBs which is less than the system offset requirement (10 LSBs). Thus, the MUX36S08 is suitable for this application.

2. There is an option to select one of the two multiplexers (MUX1 and MUX2) for a given DAQ system. MUX1 and MUX2 have charge injection figures of 1pC and 4.7pC respectively. MUX1 has an output load capacitance of 47pF while MUX2 has a load capacitance of 100pF. Which multiplexer will have minimum voltage error due to charge injection at the output?

Answer:

Output Error due to Charge Injection is given by

$$\text{Voltage Error} = Q_{INJ} / C_L$$

Where C_L is output load capacitance of MUX

2. There is an option to select one of the two multiplexers (MUX1 and MUX2) for a given DAQ system. MUX1 and MUX2 have charge injection figures of 1pC and 4.7pC respectively. MUX1 has an output load capacitance of 47pF while MUX2 has a load capacitance of 100pF. Which multiplexer will have minimum voltage error due to charge injection at the output?

Answer:

Output Error due to MUX1

$$\text{Voltage Error}_{\_MUX1} = Q_{INJ\_1} / C_{L1}$$
$$= 1pC / 47pF$$
$$= 21.27\ mV$$

Output Error due to MUX2

$$\text{Voltage Error}_{\_MUX2} = Q_{INJ\_2} / C_{L2}$$
$$= 4.7\ pC / 100\ pF$$
$$= 47\ mV$$

Thus, MUX1 will have less error due to charge injection at the output than MUX2.