

Closed-loop Delfino Control Systems: Multiple Industrial Protocol Support using the AMIC110 Sitara Processor

Part 2: Implementation of multiprotocol industrial communications solutions

Training series overview

AMIC110 Multiprotocol Industrial Interface for Closed-loop Delfino Control Systems:

- Part 1: Product solutions supported by the AMIC110 and Delfino system architecture
- **Part 2: Implementation of multiprotocol industrial communications solutions**
- Part 3: Industrial software and multiprotocol support

Training agenda

- Part 1: Product solutions supported by the AMIC110 and Delfino system architecture:
 - Solution space
 - The capabilities and advantages of this system solution
 - Applications of this systems solution
- **Part 2: Implementation of multiprotocol industrial communications solutions:**
 - **AMIC110 architecture**
 - **(TIDA-00299) AMIC110 ICE integration with dual-core MS320F2837x Delfino MCUs LaunchPad**
- Part 3: Industrial software and multi-protocol support:
 - Software architecture
 - Multi-protocol support
 - Simple Open Real-Time Ethernet (SORTE)

Implementation of multiprotocol industrial communications solutions

AMIC110 architecture

AMIC110

Benefits: PRU-ICSS provides a programmable solution for multiprotocol industrial communications.

Supporting:

- Factory automation & controls
- Motor drives
- Grid infrastructure

Software and development tools:

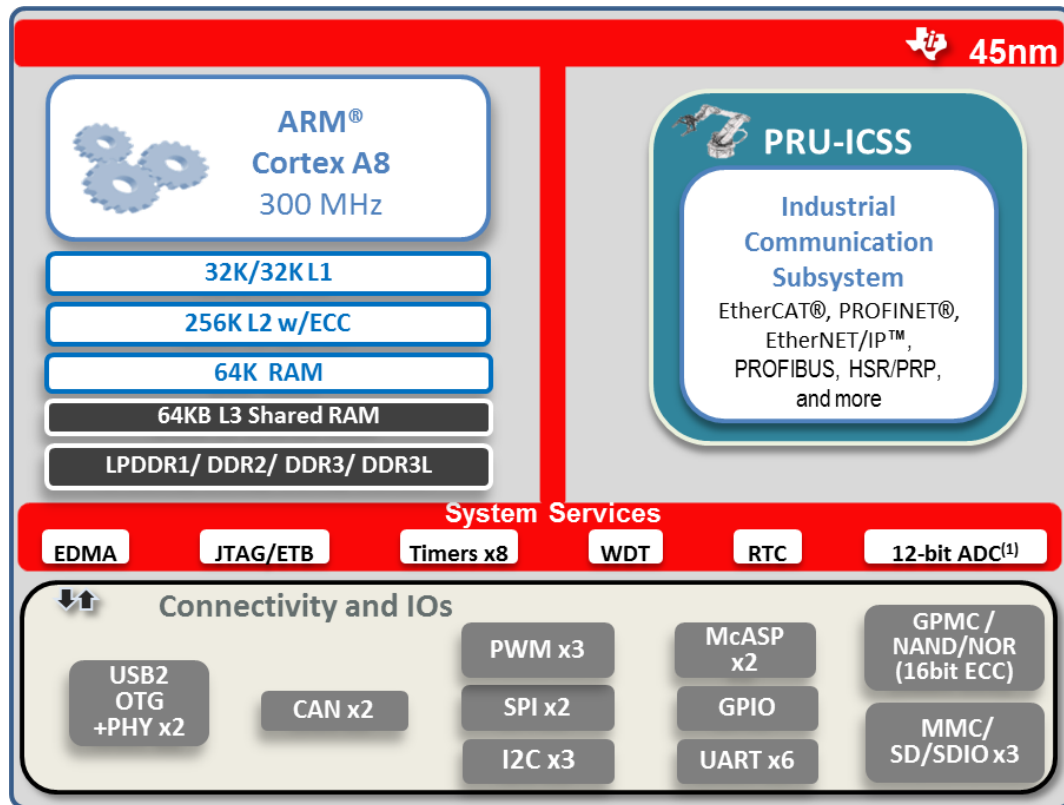
- Free TI-RTOS directly from TI
- Other RTOS from partners

Power estimates:

- Total power: 600mW-1000mW
- Standby power: ~25mW
- Deep sleep power: As low as 3mW

Schedule and packaging:

- | | |
|---|----------------|
| • Status: Production | Now |
| • AMIC110 ICE board: | Now |
| • EtherCAT | Now |
| • ET1100 emulation: | In a few weeks |
| • TI Design: | Now |
| • Other Protocols: | Q2-Q3 2017 |
| • Packaging: | 15x15, 0.8mm |
| • Extended Temp (-40C to 105C junction) | |



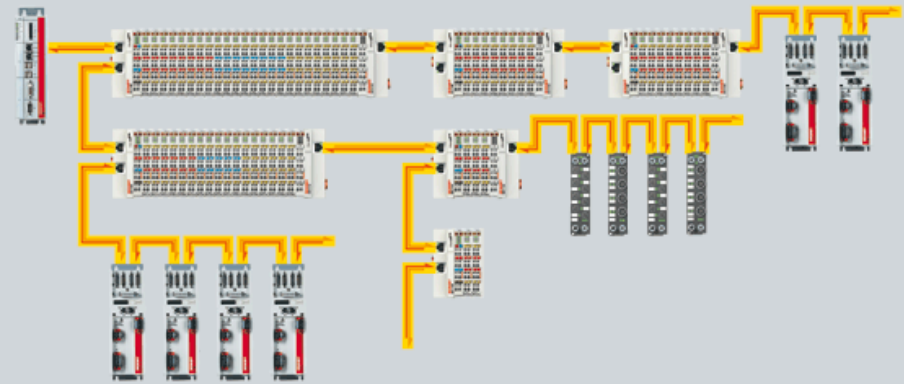
Features

- Origin: Beckhoff Automation, 2003
- User Organization: [EtherCAT Technology Group \(ETG\)](#)
- Topology: Line, ring, star network topology
- Network: 100Mbit, full duplex
- Specifics: Master generates frames; Slave performs on-the-fly frame processing; Slave port to port delay <math><1\mu\text{s}</math>
- Implementation:
 - Master: Store-and-forward frame processing; standard Ethernet MAC hardware with optional Time-Triggered Send (TTS)
 - Slave: On-the-fly frame processing
- Competition devices:
 - FPGA
 - ASIC

Benefits

- Fast process cycle times, low jitter, input/output synchronization
- EtherCAT slave license is available free of charge for ETG members; several 3rd party stacks available for purchase
- Supports higher level protocols such as TCP/IP encapsulated through Ethernet over EtherCAT

System Level View



EtherCAT Slave BoosterPack Plug-in Module with SPI Interface

Solution Features

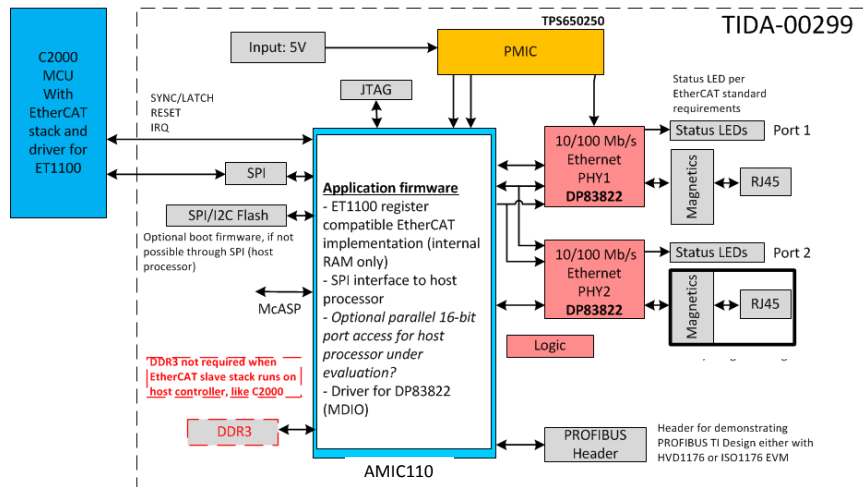
- EMC-compliant
- Hardware capable for extended temperature range up to 105C ambient
- 5-V input supply, single-chip Power Management IC (PMIC) TPS650250 to power entire board.
- AMIC110 configured to boot from SPI flash or option to boot through SPI for a host processor
- SPI slave interface (16MHz) to a host processor the runs the EtherCAT slave stack
- No external RAM required when EtherCAT slave stack runs on external host processor (TMS320F2837x)
- TI LaunchPad-compatible BoosterPack plug-in module format
- 3.3V SPI interface to C2000 LaunchPad
- Design Example - EtherCAT slave with Delfino TMS320F2837x MCU

Tools & Resources

- Applications: Industrial drives, industrial sensors, industrial automation
- Key devices: DP83822, AMIC110, TPS650250,

Solution Benefits

- Cost-optimized, dual-port EtherCAT slave that can multi-protocol Industrial Ethernets
- ET9300 register-compatible SPI interface
- A single cost-optimized Power Management IC (PMIC) to supply entire board
- Robust, low-latency DP83822 10/100 Mbps Ethernet PHY
- Designed to meet IEC 61000-4-2, 4-4, 4-5 EMC immunity

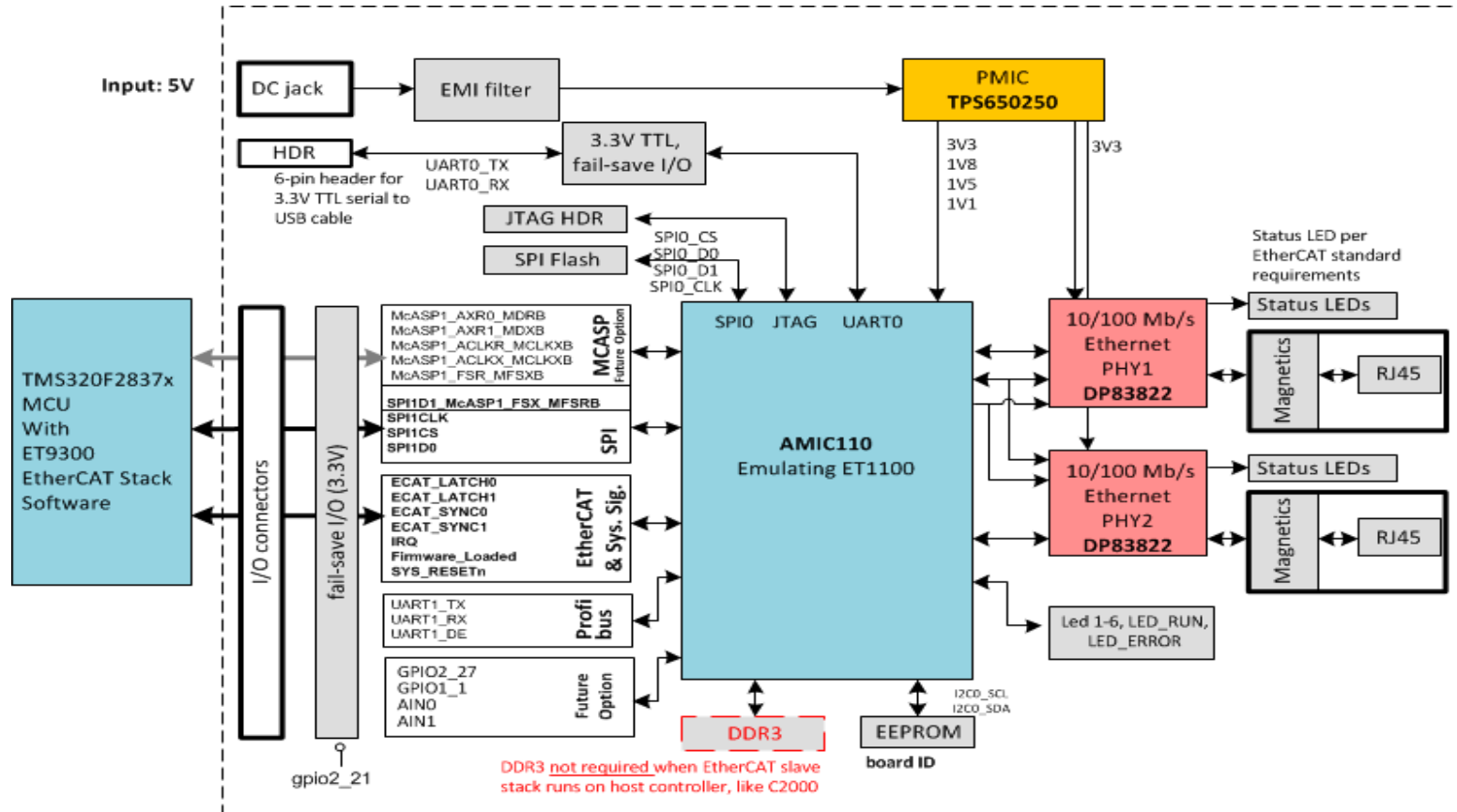


TMS320F2837x Dual-core Delfino Microcontroller

- The TMS320F2837x Delfino is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications:
 - Industrial drives and servo motor control
 - Solar inverters and converters
 - Digital power
 - Transportation
 - Power line communications.
- Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives.
- The Delfino MCU supports a new dual-core C28x architecture that significantly boosts system performance while integrated analog and control peripherals allow designers to consolidate control architectures and eliminate multiprocessor use in high-end systems.
- In the Delfino-AMIC110 design, the Delfino receives EtherCAT data from the AMIC110 through a serial (SPI) interface .

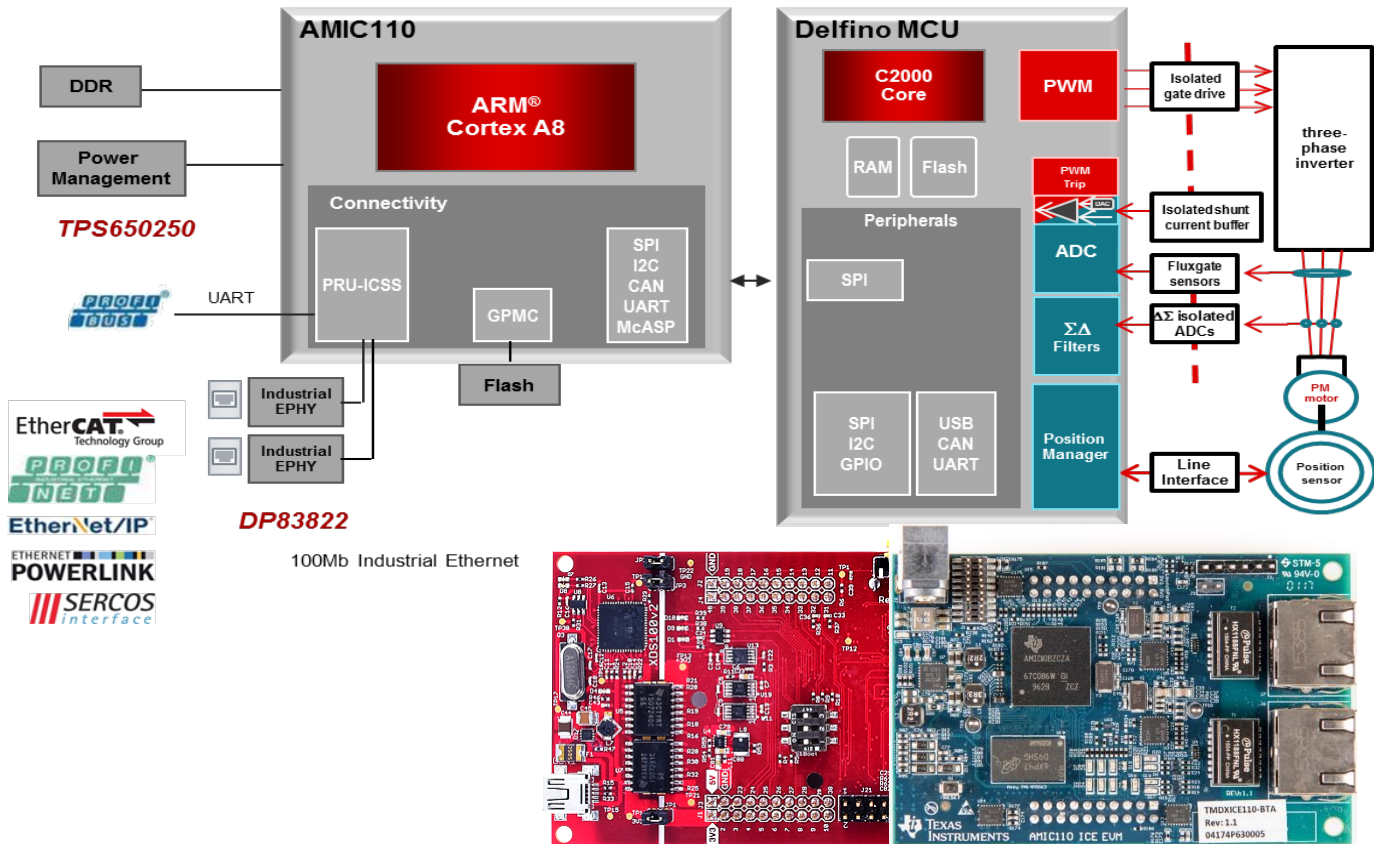
TIDA-00299/AMIC110 ICE Board with C2000 Delfino LaunchPad

Dual-port EtherCAT Slave BoosterPack plug-in module with C2000 LaunchPad



DDR3 not required when EtherCAT slave stack runs on host controller, like C2000

AMIC110 + Delfino-connected industrial drive



Associated Reference Designs
TIDA-00299
TIDA-00363

TI Products in this System
AMIC110
TMS320F2837xD
DP83822
TPS650250



Other devices on AMIC110 board

DP83822 10/100 Mbps Ethernet PHY Transceiver

Description:

- Low-power, single-port 10/100 Mbps Ethernet PHY
- Supports multiple industrial buses with fast link-down timing and auto-MDIX in forced modes
- QFN 32-pin 5.00-mm × 5.00-mm package

Features:

- ±16-kV HBM ESD protection
- ±8-kV IEC 61000-4-2 ESD protection
- Operating temperature: -40°C to 125°C
- I/O voltages: 3.3 V, 2.5 V and 1.8 V
- Cable diagnostics
- BIST (Built-in Self-Test)
- MDC/MDIO interface



TPS650250 PMIC for Li-Ion Powered Systems

- Integrated PMIC generating multiple power rails.
- Incorporates three highly efficient, step-down converters providing the core voltage, peripheral, I/O, and memory rails.
- QFN 32-pin 5.00-mm × 5.00-mm package



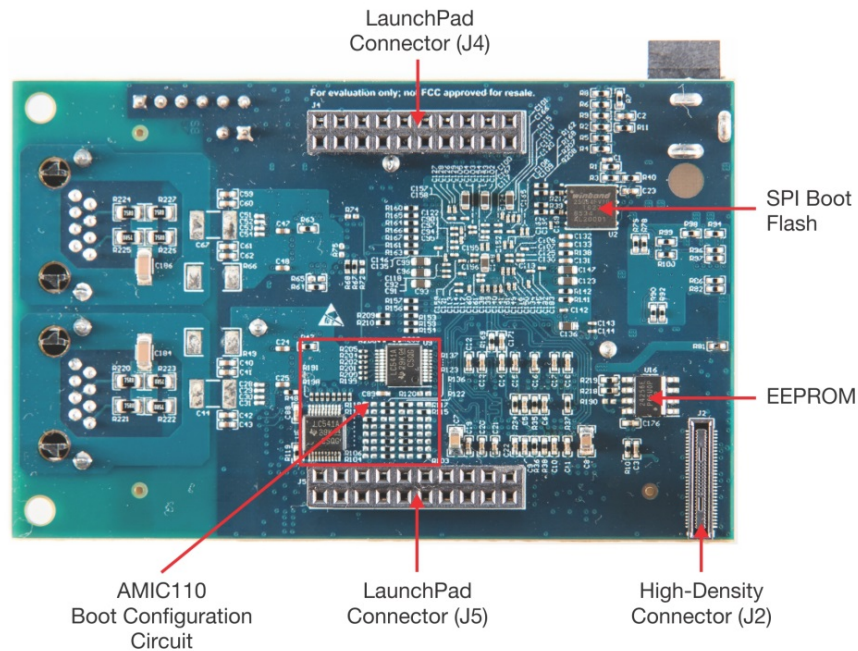
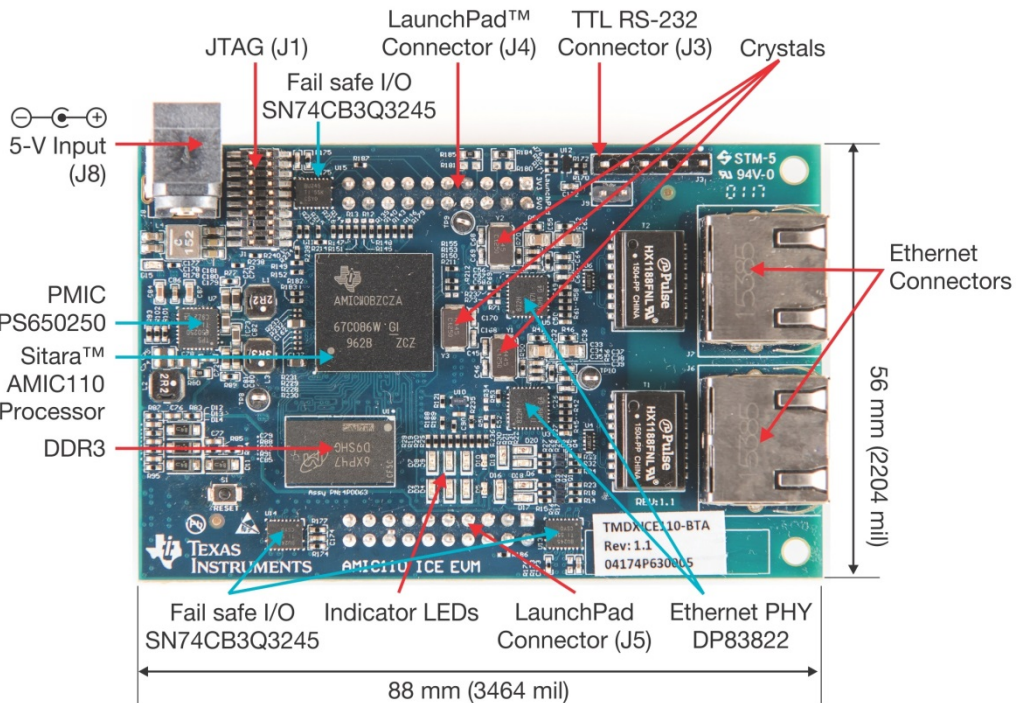
Board specifications

Parameter	Value	Description
DC input voltage	5V +/-5%	2.1mm ID/5.5mm ODM barrel DC jack. 5V input
DC input current	250mA (typical)	When EtherCAT slave is running connected to a EtherCAT master
Power consumption	1.25W (typical)	Total board consumption w/ EtherCAT slave example code on the 5V rail
Industrial Ethernet standard	EtherCAT Slave	Verified using EtherCAT Conformance Test Tool (CTT)
Indicator LEDs	Supporting industrial Ethernet standards	Hardware supports the requirements of each industrial Ethernet standard
I/O interface signaling voltage	3.3V	3.3V I/O with 5-V tolerant and fail-safe inputs. Compatible with TI LaunchPad.
Host processor SPI data rate	30MHz (master) 16MHz (slave)	
Temperature range	-40 to 85°C	Industrial temperature range -40 to 85. No heat sink required.
EtherCAT firmware storage	SPI flash	
Debugging interface	JTAG header	JTAG header for custom firmware development
Additional Information	www.ti.com/tool/tida-00299	Cost-optimized robust EtherCAT Slave and multiprotocol industrial Ethernet reference design

EtherCAT application interface to host MCU

Function	Signals	I/O [3.3V]	Description
Host Processor SPI interface	SPIDIN	Dig input	Data input for serial communication
	SPICS	Dig input	Chip-select signal; active low
	SPICLK	Dig input	Clock for serial communication, up to 16 MHz
	SPIDOUT	Dig output	Data output for serial communication
EtherCAT Clock synchronization	SYNC0	Dig output	EtherCAT Distributed Clock Sync0. Single shot and cyclic mode
	SYNC1	Dig output	EtherCAT Distributed Clock Sync1. Multiple of SYNC0 cycle time
EtherCAT Clock Latch	LATCH0	Dig input	EtherCAT Distributed Clock Latch0. Time stamp latch input0
	LATCH1	Dig input	EtherCAT Distributed Clock Latch1. Time stamp latch input1
EtherCAT Interrupt	IRQ	Dig output	EtherCAT interrupt signal
System Reset	Resetrn	Dig input	Host processor reset signal
Ready Signal	LOADED	Dig output	EtherCAT Ready signal

AMIC110 ICE



J4 & J5 EtherCAT signals

Function	Signals	I/O [3.3V]	Description
AMIC110 EtherCAT-specific signals	ECAT_LATCH0	Digital input	<ul style="list-style-type: none">• EtherCAT Distributed Clock Latch 0• Time stamp latch input0
	ECAT_LATCH1	Digital input	<ul style="list-style-type: none">• EtherCAT Distributed Clock Latch 1• Time stamp latch input1
	ECAT_SYNC0	Digital output	<ul style="list-style-type: none">• EtherCAT Distributed Clock Sync0 output• Single shot and cyclic mode supported
	ECAT_SYNC1	Digital output	<ul style="list-style-type: none">• EtherCAT Distributed Clock Sync1• Multiple of SYNC0 cycle time
	IRQ	Digital output	EtherCAT interrupt signal
	FIRMWARE_LOADED	Digital output	EtherCAT Operation Ready signal

J4 & J5 inter-processor communications and GPIO

Function	Signals	I/O [3.3V]	Description
AMIC110 Processor SPI interface	SPIx_D1 (I)	Digital input	Data input for serial communication
	SPIx_CS0n (I/O)	Digital input/output	Chip-select signal; active low
	SPIx_SCLK (I/O)	Digital input/output	Clock for serial communication
	SPIx_D0 (O)	Digital output	Data output for serial communication
AMIC110 UART1 interface	UART1_TX	Digital output	Future expansion such as PROFIBUS
	UART1_EN	Digital output	Future expansion such as PROFIBUS
	UART1_RX	Digital input	Future expansion such as PROFIBUS
Function	Signals	I/O [3.3V]	Description
AMIC110 GPIO signals	GPIO1_1	Digital input/output	GPIO for future expansion
	GPIO2_27	Digital input/output	GPIO for future expansion
AMIC110 Reset signal	SYS_RESETh	Digital input	Input to reset the AMIC110

J3 UART signals

Function	Signals	I/O [3.3V]	Description
AMIC110 UART0 interface	UART0_TX	Digital output	Serial port connection for virtual COM port
	UART0_RX	Digital input	Serial port connection for virtual COM port

For more information

- TI Designs:
 - EtherCAT Slave BoosterPack Plug-in Module with SPI Interface:
<http://www.ti.com/tool/TIDA-00299>
 - Simple Open Real-time Ethernet (SORTE) Device with PRU-ICSS Reference Design:
<http://www.ti.com/tool/TIDEP-0086>
- AMIC110 software: <http://processors.wiki.ti.com/index.php/AMIC110SW>
- Sitara Industrial FAQ: http://processors.wiki.ti.com/index.php/FAQ_Sitara_Industrial
- For questions about this training, refer to the TI E2E Community Sitara Processor Forum: https://e2e.ti.com/support/arm/sitara_arm/f/791



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