EtherCAT® Master on Sitara™ Processors

EtherCAT® Master on Sitara™ Processors Training Series [Part 2]

Acontis and CoDeSys EtherCAT Master Software Architectures

Training series agenda

Part 1:

- Overview of Training Series
- Sitara processors family in factory automation
- EtherCAT protocol technology review

Part 2:

- Acontis EtherCAT master software architecture on top of TI-RTOS and RT Linux
- CoDeSys EtherCAT master software architecture on top of RT Linux

Part 3:

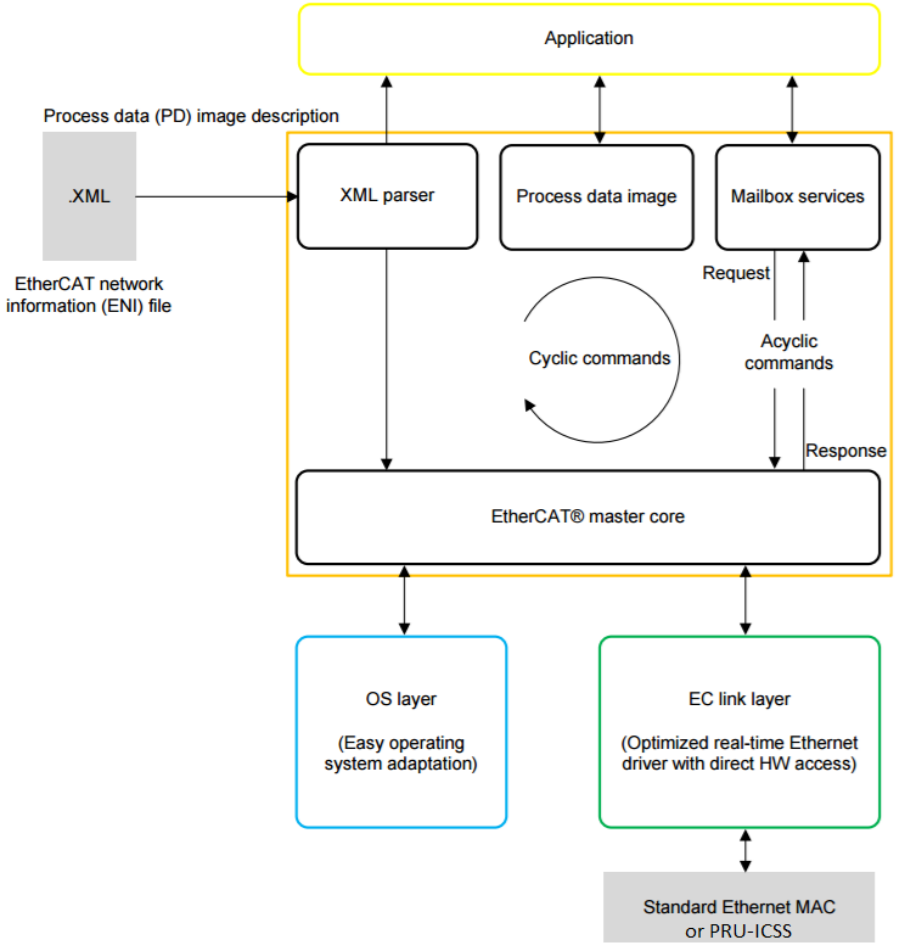
- EtherCAT master + time-triggered send (TTS)
- EtherCAT master on Sitara: A scalable and flexible solution

Acontis EtherCAT Master Software Architecture on TI-RTOS and RT Linux

Acontis EC-Master features

- EtherCAT master (EC-Master) Class A and Class B available
- Integrated diagnostics capabilities
- Optimized link layers for real-time systems
- Different OS are supported, among them TI-RTOS and Linux.
- Acontis offers EC-Engineer as a configuration and diagnostics tool, which can be used online or offline.

Acontis EC-Master Stack modules



EtherCAT Masters TI Designs

EtherCAT Master Reference Design on Sitara AM57x Gb Ethernet and PRU-ICSS with TTS:
http://www.ti.com/tool/tidep0079

Acontis EtherCAT Master Stack Reference Design:
http://www.ti.com/tool/tidep0043

TI Design: TIDEP0079

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Key Document

- TIDEP0079 Design Guide (Rev. B) (PDF 2490 KB)
  26 Oct 2016 1,980 views

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TIDEP0079 EtherCAT® Master Reference Design on Sitara AM57x Gb Ethernet and PRU-ICSS with Time Triggered Send Board Image

Description

The TIDEP0079 reference design demonstrates an EtherCAT® master interface running on the Sitara™ AM572x processor using the EC-Master stack from acontis. This EtherCAT master solution can be used for EtherCAT-based PLC or motion control applications. EtherCAT master is profiled on both the Ethernet switch and the PRU-ICSS Ethernet ports of the AM572x processor to give designers flexibility to use any of the two switch ports or four PRU-ICSS Ethernet ports on the device. The EtherCAT master implementation can achieve less than 100µs cycle times for both the switch and the PRU-ICSS Ethernet ports. Time-triggered send (TTS) can be enabled on the PRU-ICSS to reduce jitter, achieve shorter cycle times, and reduce latency in cases where distributed clocking is not used.

View available purchase options for designs kits, evaluation modules and/or the bill of materials.

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Key Document

- EtherCAT Master Stack for TI Sitara CPU Family Design Guide (Rev. A) (PDF 198 KB)
  19 Jul 2016 2,096 views

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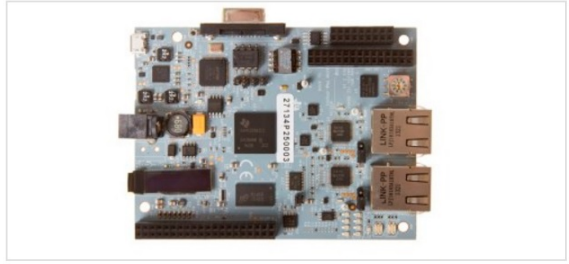


TIDEP0043 Acontis EtherCAT Master Stack Reference Design Board Image

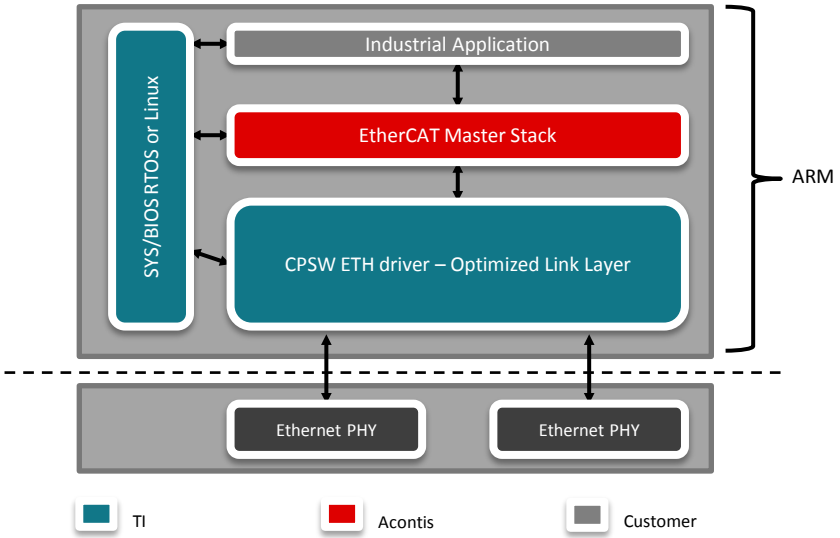
Fully assembled board (shown above) developed for testing and performance validation only, not available for sale.

Description

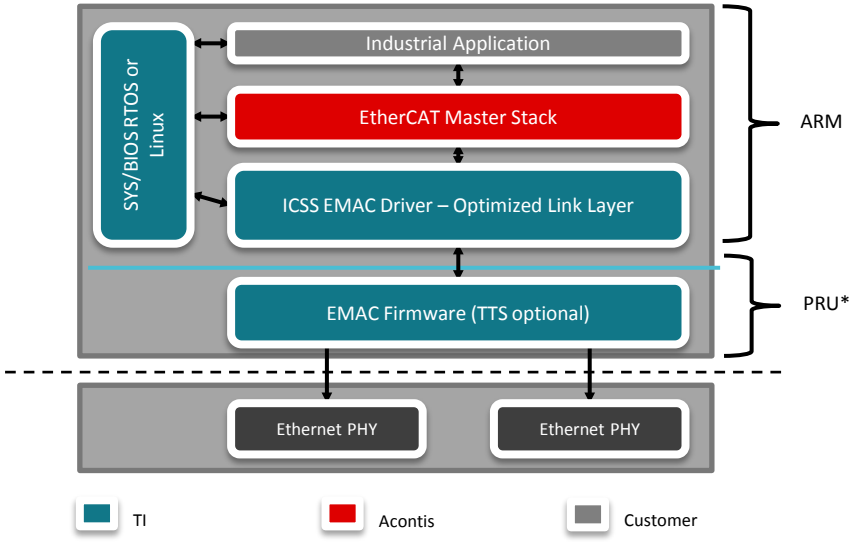
The acontis EC-Master EtherCAT Master stack is a highly portable software stack that can be used on various embedded platforms. The EC-Master supports the high performance TI Sitara MPUs, it provides a sophisticated EtherCAT Master solution which customers can use to implement EtherCAT communication interface boards, EtherCAT based PLC or motion control applications. The EC-Master architectural design does not require additional tasks to be scheduled, thus the full stack functionality is available even on an OS less platform such as TI Starterware suported on AM335x. Due to this architecture combined with the high speed Ethernet driver it is possible to implement EtherCAT master based applications on the Sitara platform with short cycle times of 100 microseconds or even below.

Acontis EC-Master software block diagrams

GMAC (CPSW)



PRU-ICSS

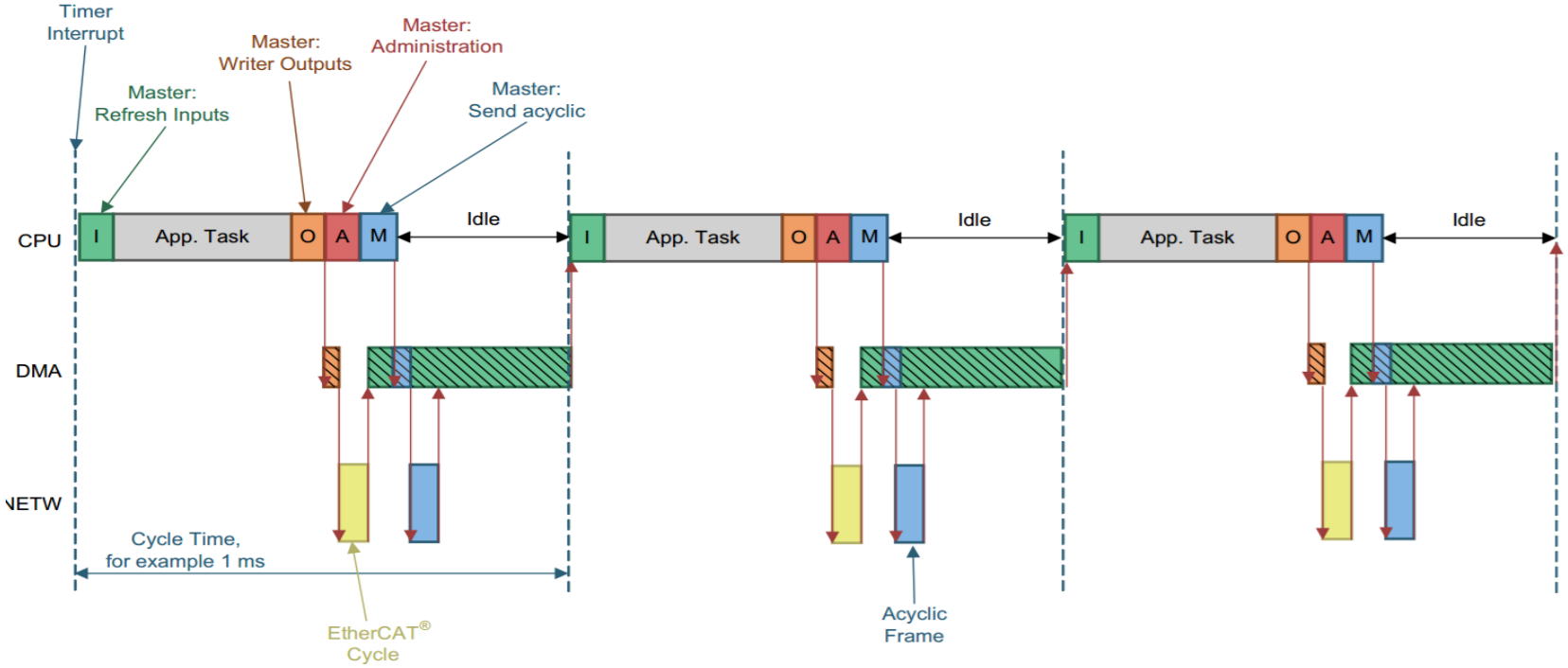


NOTE: EC-Master can run on PRU-ICSS Ethernet ports or GMAC ports when using AM57x IDK boards.

On AM335x, AM437x boards, EC-Master runs on CPSW ports.

EtherCAT Master: Bus timing diagram (CPU load)

CPU load measured in Inputs, Outputs, Administration, and Send Acyclic periods



Acontis EC-Master: CPU load benchmark

Table 1. AM572x EC-Master CPU Performance Operating on GMAC

Sitara AM572x 1000 MHz NIC: GMAC TI-RTOS (SYS/BIOS)		
NUMBER	**EC-MASTER JOB**	**AVERAGE µs**
1	I: Process Inputs	9
2	O: Send Outputs	5
3	A: Administration	4
4	M: Send Acyclic Frame	2
Total CPU Time		**20**

Table 2. AM572x EC-Master CPU Performance Operating on ICSS_PRU

Sitara AM572x 1000 MHz NIC: ICSS_PRU TI-RTOS (SYS/BIOS)		
NUMBER	**EC-MASTER JOB**	**AVERAGE µs**
1	I: Process Inputs	3
2	O: Send Outputs	15
3	A: Administration	5
4	M: Send Acyclic Frame	2
Total CPU Time		**25**

TI design link: http://www.ti.com/lit/ug/tidubz1b/tidubz1b.pdf

CoDeSys EtherCAT Master Software Architecture on RT Linux

CoDeSys development system

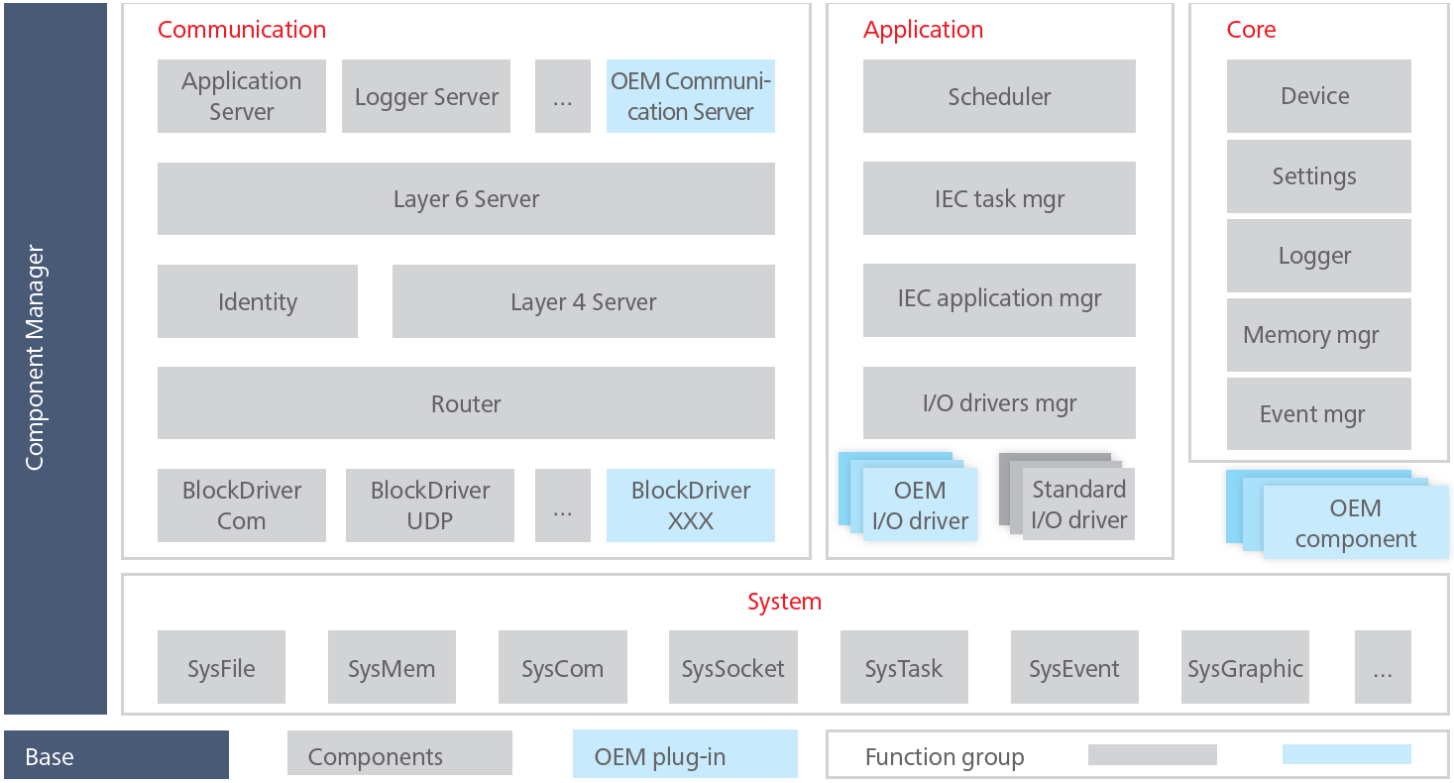
CoDeSys development system:

- A powerful IEC 61131-3 programming tool for programmable logic controllers
- Produces native machine code for different processors

Runtime features:

- CoDeSys runtime system architecture is based on components.
- Each component has a well-defined interface.
- Users can ‘pick’ the right modules for their application.

CoDeSys runtime modules

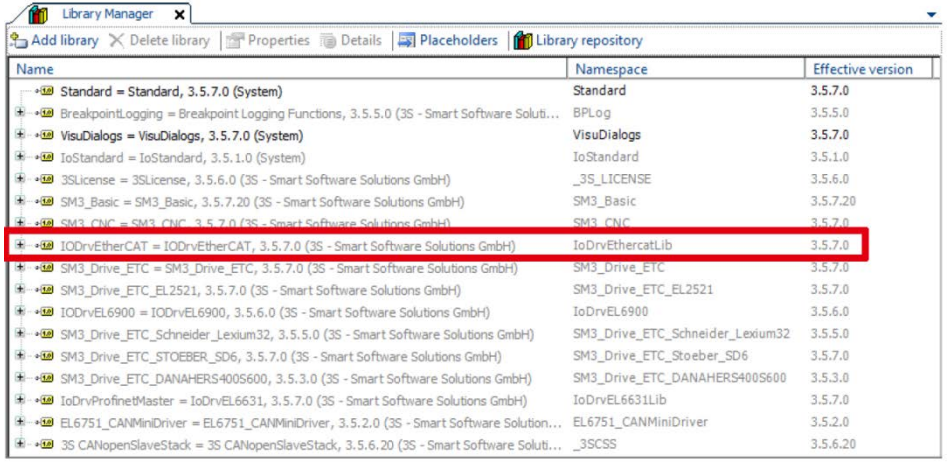


CoDeSys EtherCAT Master

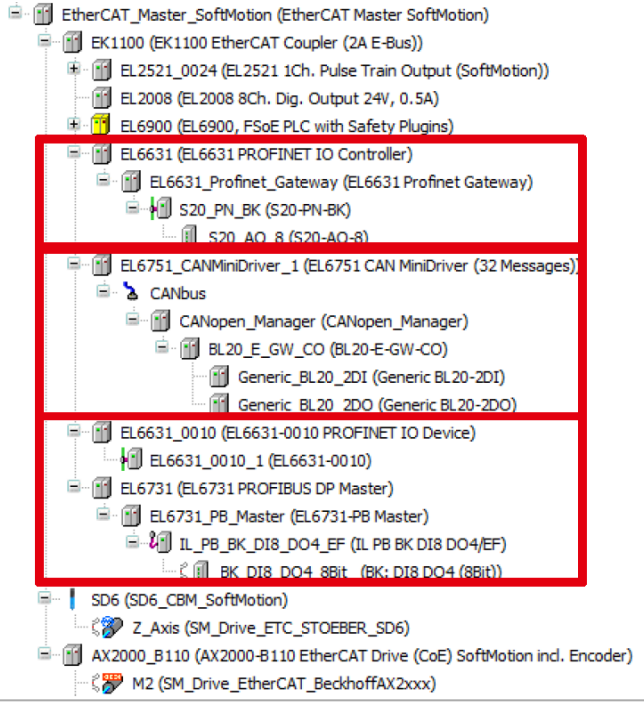
- EtherCAT Master protocol stack realized as CoDeSys library:
  - Compiled together with the application
  - Portable for different compatible platforms
- Support of multiple EtherCAT gateway clamps:
  - Integrated gateway functionality
  - Possible multiple fieldbuses
- Integrated diagnostics: Generic and EtherCAT-specific
- Integrated safety up to SIL3 with EtherCAT Safety Module
- Operating system for Sitara: RT Linux
- TI design coming soon

CoDeSys EtherCAT Master library

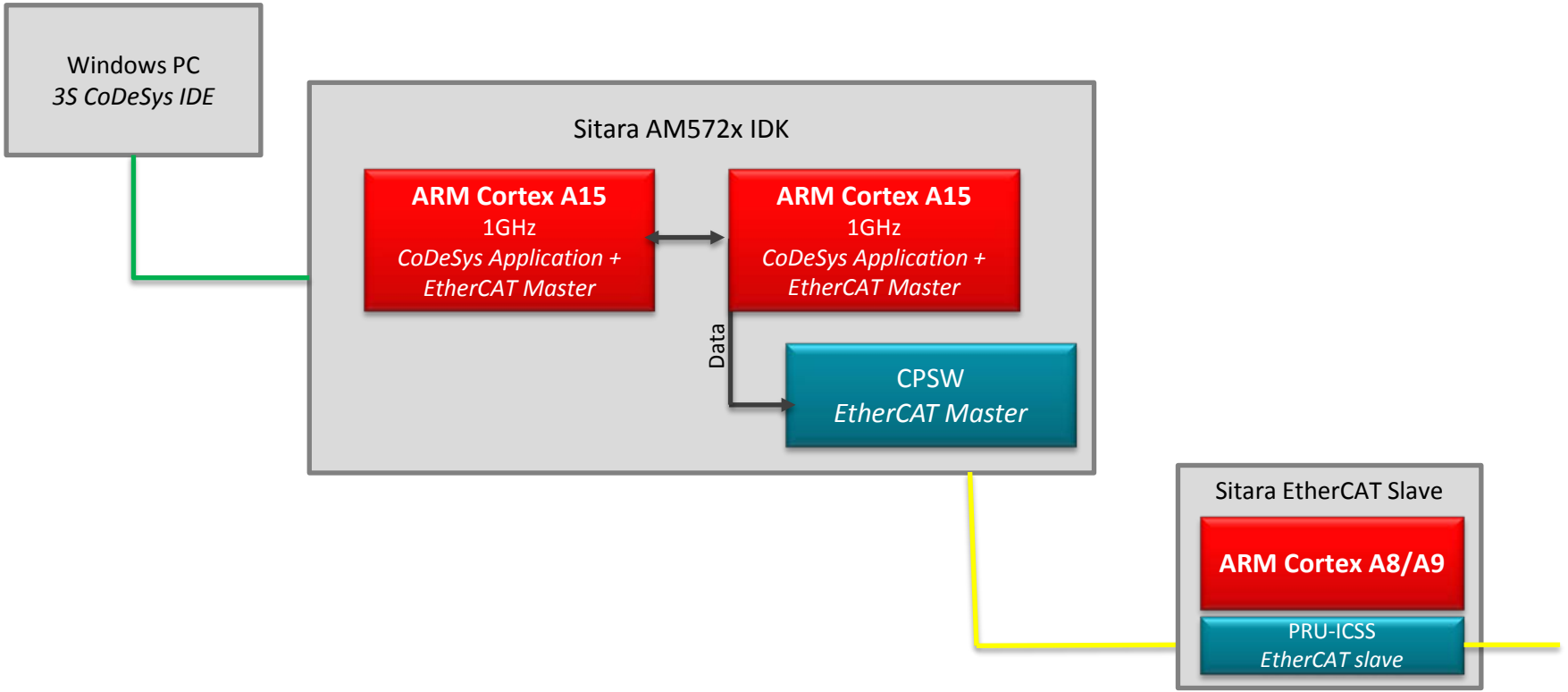
EtherCAT Master Lib



EtherCAT Master with other fieldbuses



CoDeSys system block diagram



For more information

- Sitara Processors Overview http://www.ti.com/sitara
- EtherCAT Masters TI Designs:
  - Acontis EtherCAT Master Stack Reference Design: http://www.ti.com/tool/tidep0043
  - EtherCAT Master Reference Design on Sitara AM57x Gb Ethernet and PRU-ICSS with TTS: http://www.ti.com/tool/tidep0079
- Online training:
  - Sitara AM57x Processors: https://training.ti.com/am57x-sitara-processors-training-series
  - Sitara AM437x Processors: https://training.ti.com/am437x
- CoDeSys EtherCAT Master: https://www.codesys.com/products/codesys-fieldbus/industrial-ethernet/ethercat.html
- Acontis EtherCAT Master for TI processors: http://www.acontis.com/eng/products/downloads/ethercat-for-ti-processors.html
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