Demonstrating The F28004x's Value Propositions in Real-Time Systems Solutions

Matthew Pate C2000

Training Summary

F28004x's Value Proposition per Systems Application:

Through the integration of various high-performance modules including: analog, controls and communications peripherals; C2000 has designed the F28004x family for multiple system solutions to help either reduce the total quantity of components (reduce hardware cost) or increase the efficiency in executing the core function of the system. Demonstrating to customers the value in the integration of these peripherals with respect to specific systems solutions can be a daunting task. This presentation will outline how to illustrate to the customer the value proposition in designing F28004x based systems solutions per a targeted subset of peripherals for multiple system applications.

This session will provide examples on how to demonstrate the value of F28004x in the following system applications:

- One Motor + PFC (3 PGAs/motor and 1 for PFC)
- Digital Power
- Industrial Drives

Training level: Intermediate

Course Details:
Audience: Digital, Systems

Matthew Pate

Product Marketing C2000 MCU

- **Career**
  - BS Engineering Physics Murray State University(2000)
  - Member of C2000 MCU team for 14 years involved in applications, test, and marketing teams

- **Expertise**
  - Multi-displinary background in both analog and digital modules
  - Involved in chip architecture and productization of 1st Piccolo devices 2802x/3x/6x
  - C2000 Digital Power Marketing

Detailed Agenda

- Piccolo 28004x Overview
  - General enhancements for all systems
- Digital Power Space
- Industrial Drives Space
- Motor Space

Piccolo™ F28004x

CS 1Q17 / RTM 1Q18 http://www.ti.com/product/TMS320F280049M

Differentiation

- 100MHz / 256KB flash / 100 KB SRAM
- 7 on-chip PGA(3/6/12/24) with post gain filtering and bypass option
- Next Generation CLA; support for continuous background task
- PMBUS HW support
- Addition of CW/CCW encoder support
- Under ½ power consumption of F2806x device
- Single Supply Support including on-chip DC/DC VREG
- 3 12-bit 3.5MSPS ADC with post processing threshold actions
- 7 Windowed Comparators + 2 12-bit output DACs
- 4 Sigma Delta Demodulation Channels
- CLB

Isolated Comms - FSI

- Communications speed across isolation barrier(hot/cold)
- 200Mbps capability with HW generated/embedded CRC
- HW skew control for isolation barrier compensation

F28004x

Temperatures: 105C | 125C | Q100

Sensing
- ADC1: 12-bit, 3.5 MSPS, 8ch
- ADC2: 12-bit, 3.5 MSPS, 8ch
- ADC3: 12-bit, 3.5 MSPS, 8ch
- 7x Windowed Comparators w/ Integrated 12-bit DAC
- 7x PGAs
- 4x Sigma Delta Channels (2x Filters per channel)
- Temperature Sensor
- 2x eQEP
- 7x eCAP (2x HRCAP)

Processing
- C28x™ DSP core 100 MHz
- FPU
- TMU
- VCU-I
- CLA core 100 MHz
- Floating Point Math
- 6ch DMA

Actuation
- 8x ePWM Modules 16x Outputs (16x High-Res)
- Fault Trip Zones
- 2x 12-bit DAC

Connectivity
- 3x UART(1 LIN)
- 2x I2C (1x true PMBus)
- 2x SPI
- 2x CAN 2.0B
- FSI

System Modules
- 3x 32-bit CPU Timers
- NMI Watchdog Timer
- 192 Interrupt PIE

Memory
- Up to 256 KB Flash +ECC
- Up to 100 KB SRAM +parity
- 2x 128-bit Security Zones
- Boot ROM
- InstaSPIN™ Motor ROM

Power & Clocking
- 2x 10 MHz 0-pin OSC
- 1.2V VREG
- 1.2V DCDC

Debug
- cJTAG / Real-time JTAG

Tools

F28004x Experimenter's Kit

Part Number: TMDXDOCK280049M
http://www.ti.com/tool/TMDSDOCK280049M

Software

TI RTOS

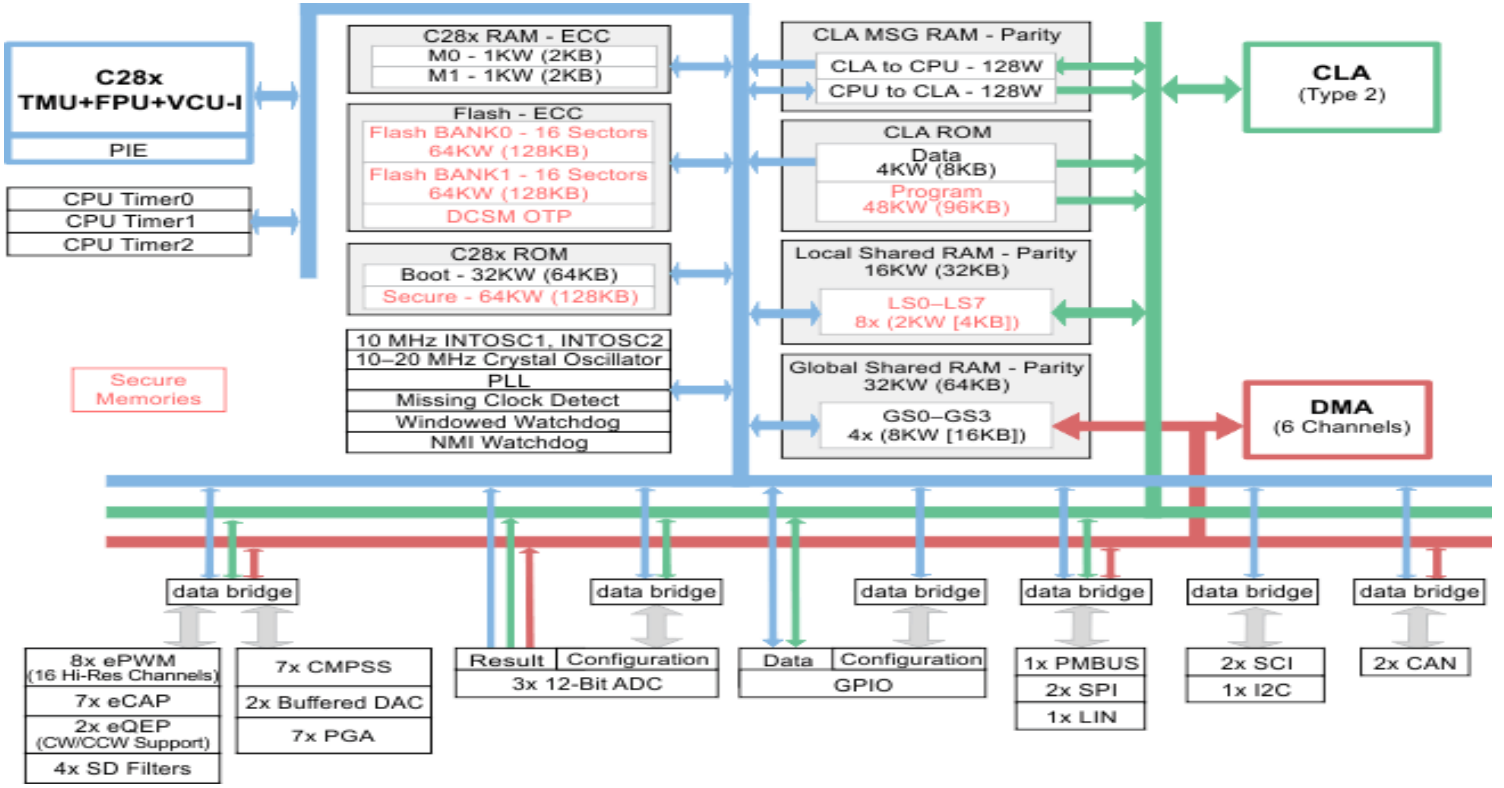
controlSUITE™ Software

Code Composer Studio (CCS) IDE

Packages

Package	Dimension
56-pin QFN (late avail)	7x7mm
64-pin LQFP	12x12mm
100-pin LQFP	16x16mm

Piccolo F28004x Block Diagram



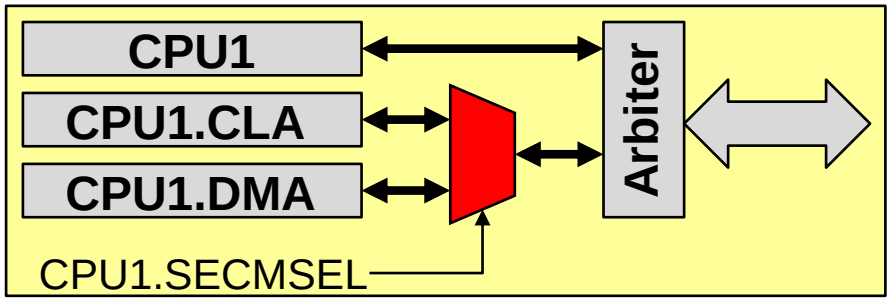
CLA Type 2 Enhancements

- Background Task
  - Option to run 8 tasks or 7 tasks and 1 background task
  - Task 8 can be used as background task
    - Runs continuously until disabled or device/soft reset
    - Can be triggered by a peripheral or software
    - Tasks 1 - 7 can interrupt background task in priority order (1-7)
    - Can make portions of background task uninterruptible, if needed
- Background Task Uses:
  - Continuous functions such as communications and clean-up routines
  - Used by InstaSPIN when running CLA code
- MDEBUGSTOP1
  - Used for software breakpoint (similar to C28x breakpoints)
  - Replaces instruction where execution must halt
  - Differs from MDEBUGSTOP
    - Flushes all instructions that have been fetched
    - On step or run free – will re-fetch same instruction it replaced
- Other
  - Two new hardware breakpoint and debug registers
    - Used by CCS to improve emulation capabilities

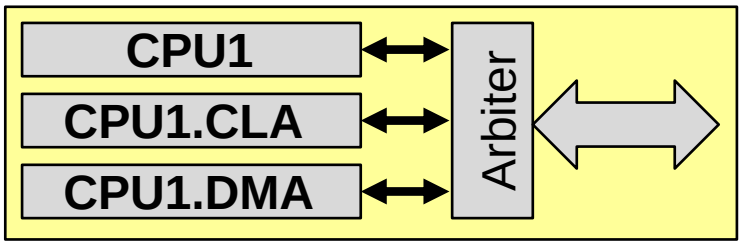
CPU / CLA / DMA Master Access

- CLA and DMA can now have simultaneous access with arbitration
- Peripheral master can have access without interference from other masters
  - Enables the CLA to utilize DMA transfers

F2807x



F28004x



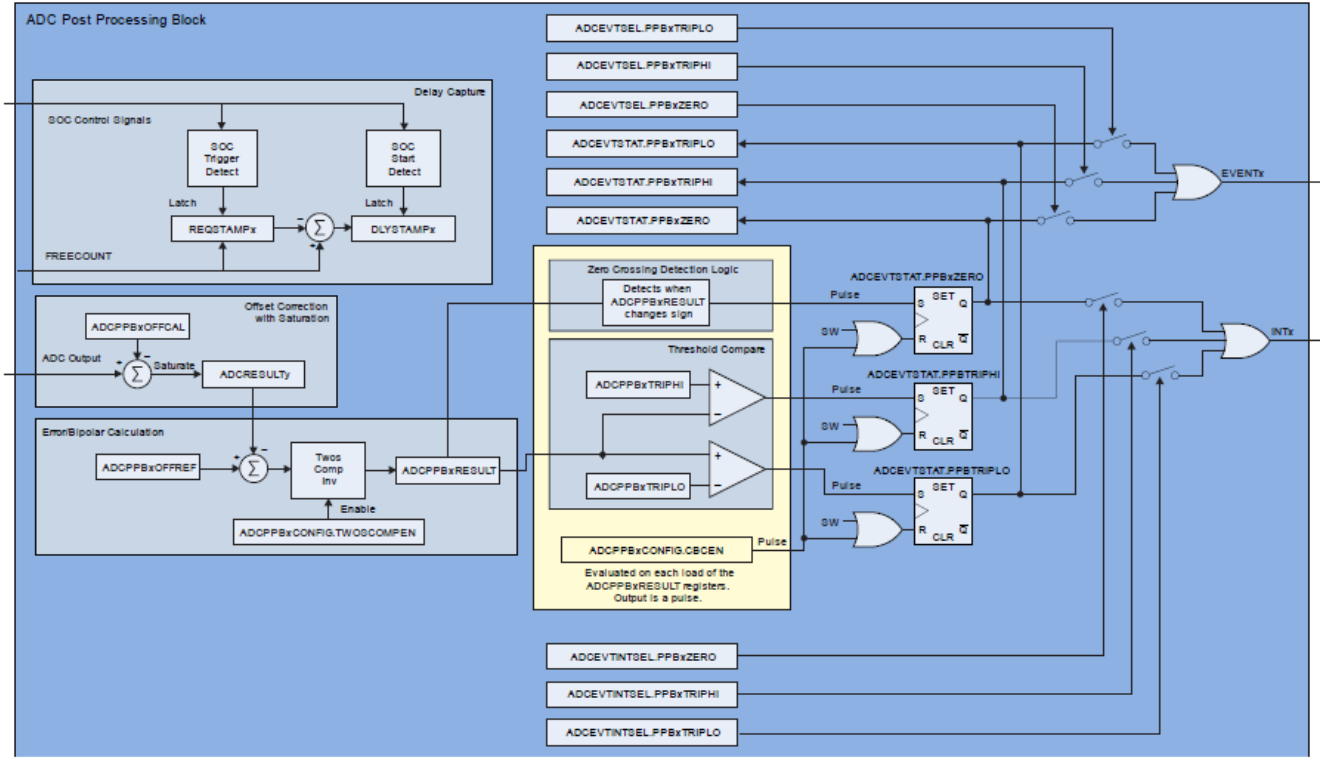
Memory Enhancements

- Flash is now separated into 2 128KB banks independent banks
  - Support for Live FW update, writing to one flash while reading/executing from other is supported
  - ECC syndrome added to flash for enhanced system reliability
    - 1 bit correct
    - 2 bit detect per 128 bit word
- For flash programmation now have HW state machine to control programming times/pulses
  - Previous Piccolo devices used C28x instructions limiting the CPU BW for application code/ISR service

HRCAP Type 0 vs. Type 1 Comparison

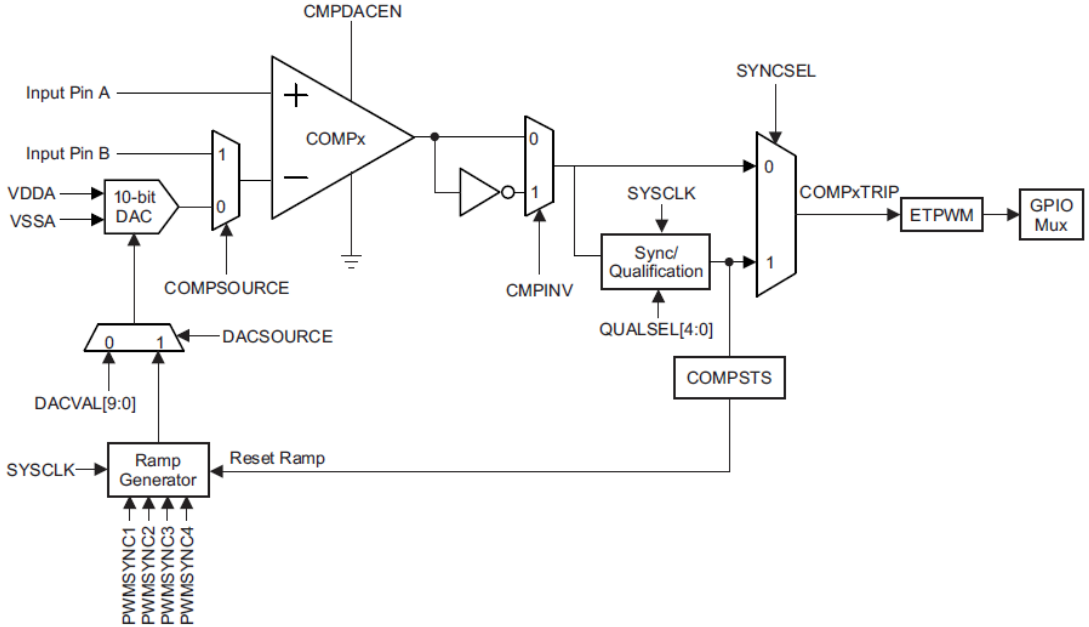
Type 0 HRCAP	Type 1 eCAP:HRCAP
• A separate module than eCAP	• eCAP extension (similar to PWM)
• No CLA and DMA access	• CLA and DMA access
• No support for one-shot operation	• One-shot operation
• HRCAP needs to be clocked at 98 MHz – 120 MHz	• No dependency on clock frequency
• Complex software intensive based calibration routine	• Hardware calibration
• No capture operation during calibration	• Capture operation during calibration
• Calibration must be run periodically → one dedicated HRPWM and HRCAP for calibration	• Continuous hardware calibration

ADC PostProcessing Block



- Offset Correction
- Reference Subtraction
- Threshold Compare
- Sample Delay Measurement

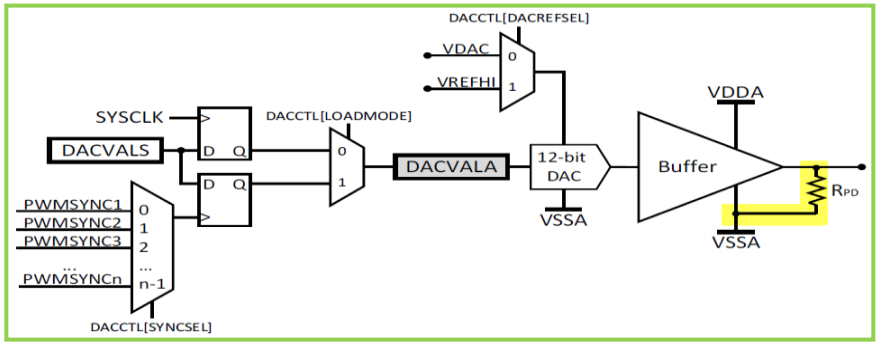
CMPSS Type 1 Enhancements / Changes



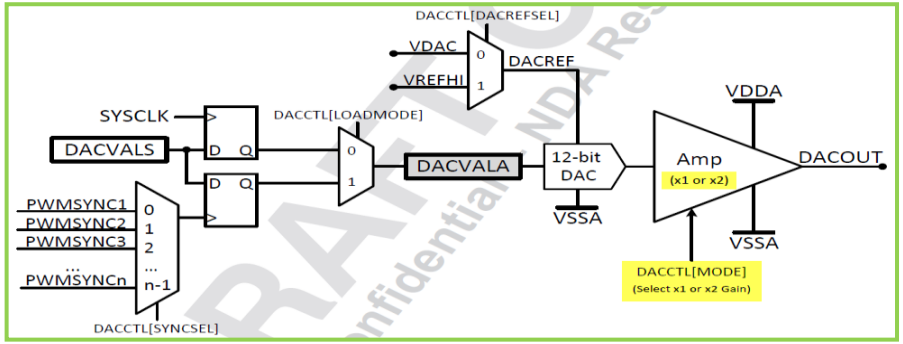
- Enhancements / C
  - Blanking capabi
    - Helps clear-an
  - Fixed trip vs clear-and-reset arbitration when Ramp Generator is used
    - Clear-and-reset is now higher priority than trip
  - CMPSS Comparator POS/NEG input signals are now independently selectable via an analog subsystem MUX scheme
    - Previously the POS/NEG pin input options were tightly coupled on Soprano between HIGH and LOW comparators

Buffered DAC Type 1 Changes

F2807x



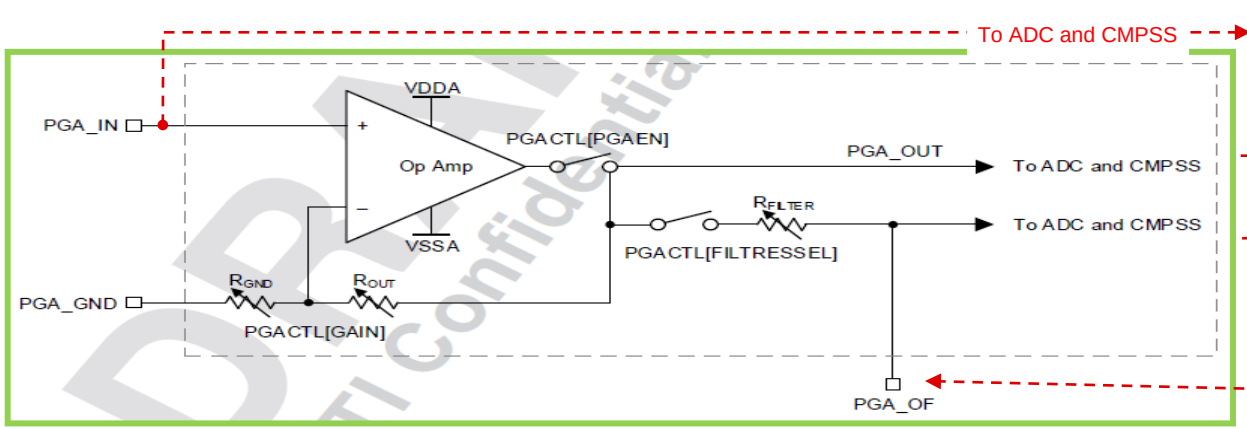
F28004x



- Enhancements / Changes
  - Pull-down resistor on output removed
  - 1x and 2x gain options
  - Increased load support
  - DAC internal reference – 2.5v and 3.3v option
    - 3.3v option outputs 1.65 and then use 2x mode on DAC
    - 2.5v option outputs 2.5v and then use 1x mode on DAC

Programmable Gain Amplifier (PGA)

- *Amplifies small input signals to increase the dynamic range of the downstream ADC and CMPSS modules*



PGA Input can be used as a regular ADC/CMPSS pin

Filtered and non-filtered paths to ADC and CMPSS

PGA Output Filter pin can be used as a regular ADC/CMPSS pin

- PGA Enhancements (over F2805x)
  - Additional gain mode of 24x
  - Support for low-pass filtering (by connecting an external capacitor to PGA_OF; cut-off frequency based on standard RC equation $f_C = \frac{1}{2\pi RC}$)
  - Hardware offset/gain trimming (instead of software post-processing)

Digital Power

Improvements for Digital Power

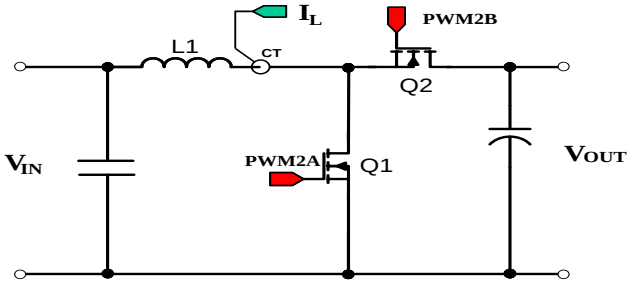
Key Enhancements (ePWM Type 4)

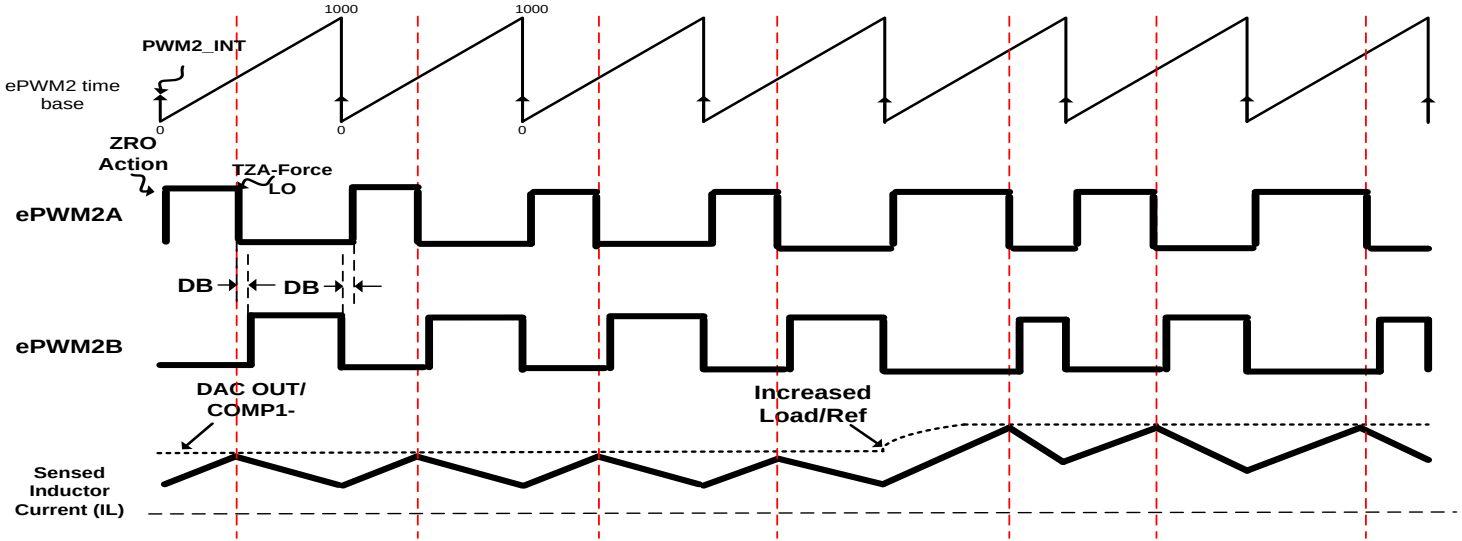
- **Delayed Trip Functionality:** Dead-band insertion capability on a trip event.
- **One Shot Reload:** One shot reload from shadow to active registers.
- **Global Reload:** Global reload of shadow to active registers with programmable pre-scale of load events.
- **Remapped Register Space:** Registers grouped by their functionality for better alignment and future expansion.
- **Support for Valley switching:** Ability to switch PWM output at the valley point for valley switching.

Delayed Trip Functionality

Peak Current Mode Control – Sync Boost

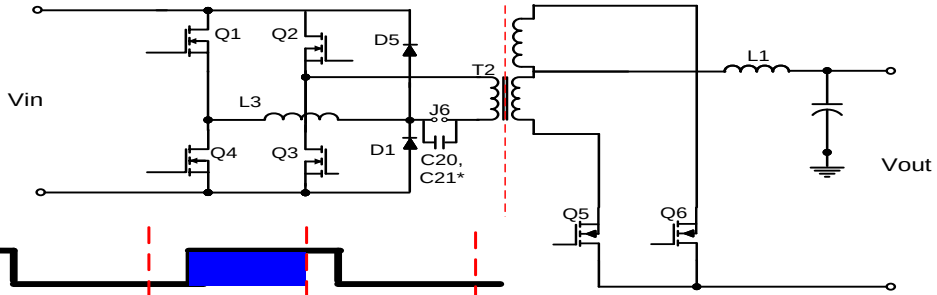
Peak current mode control of a synchronous DC-DC boost converter.

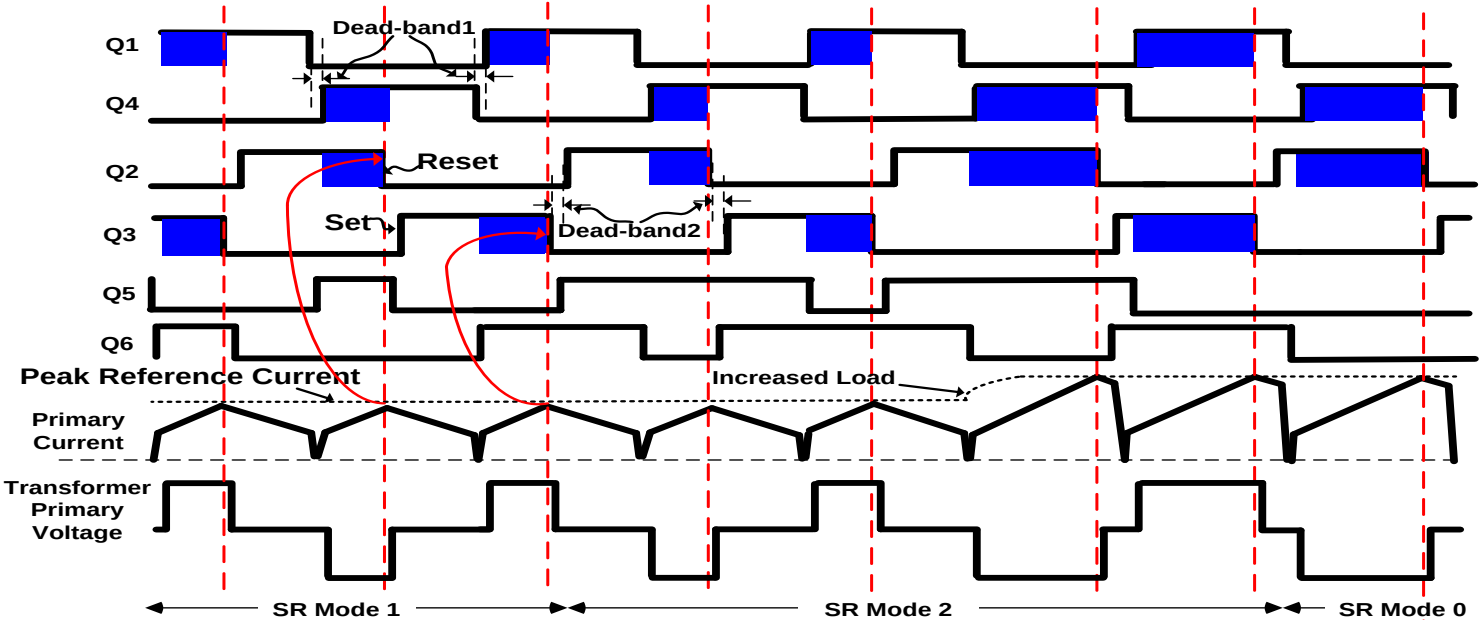




Peak Current Mode Control – PSFB

Peak current mode control of a Phase Shifted Full-Bridge (PSFB) DC-DC converter.



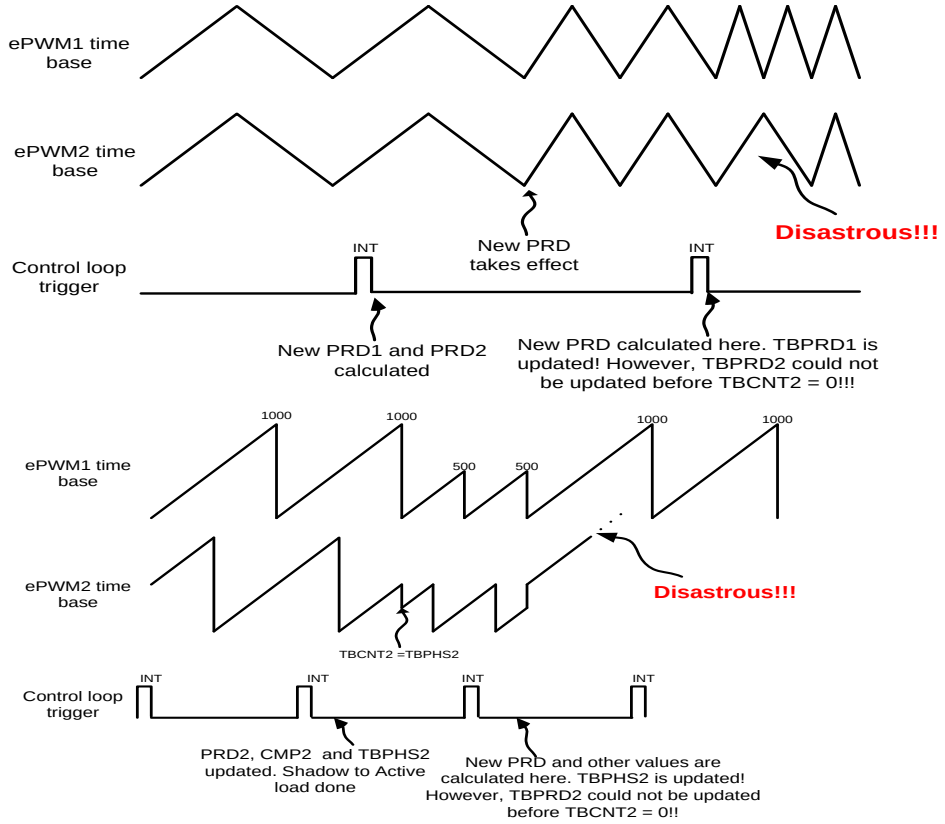


One Shot & Global Reload Capability

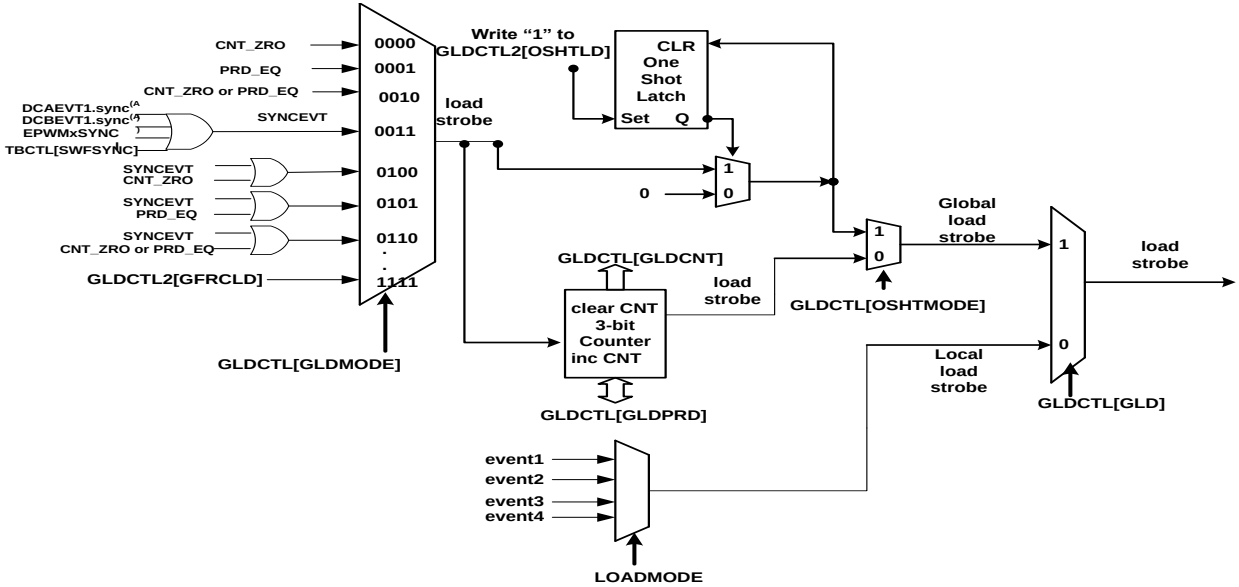
Shadow to Active Load of Registers

- Many enhancements already in place in Type-2
  - EPWM link, enables user to update all PWMs simultaneously
  - Reload on Sync, ensures that registers are loaded with the correct values

- What is missing on type-2?
  - INT can happen anytime during the update of multiple linked registers
  - Issue when all registers are not updated and Sync happens.

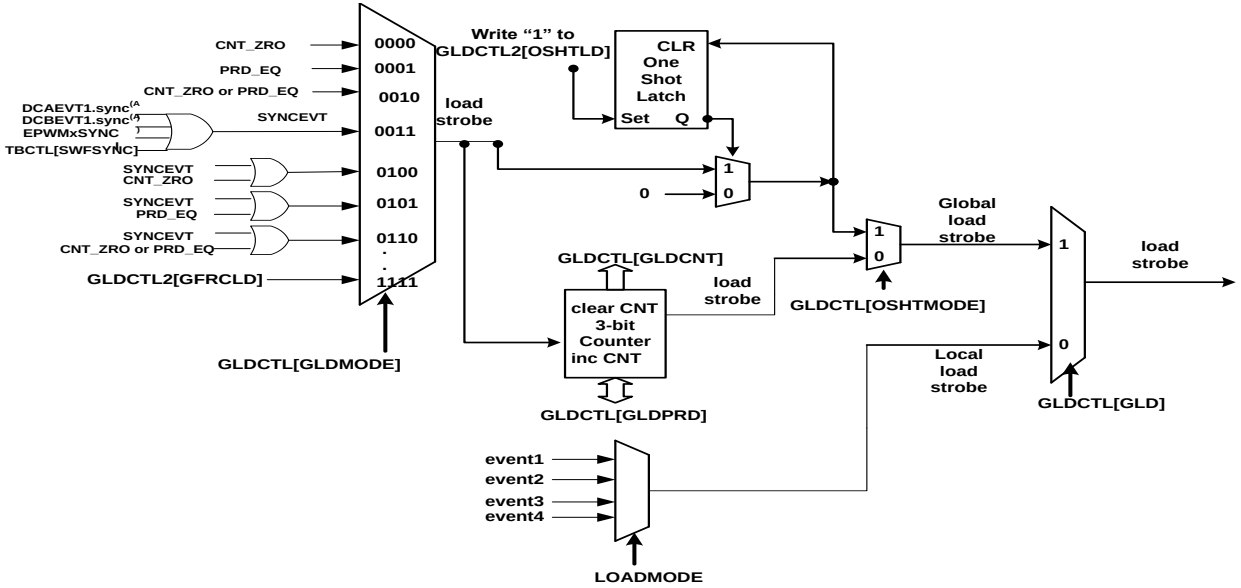


One Shot & Global Reload



- For all registers that have this mode enabled, shadow to active loads occur at the same event defined by GLDCTL[GLDMODE]
- Global reload pulse pre-scalar provides capability to choose transfers to happen once in 'N' occurrences of selected event

One Shot & Global Reload



One shot reload usage

Initialization

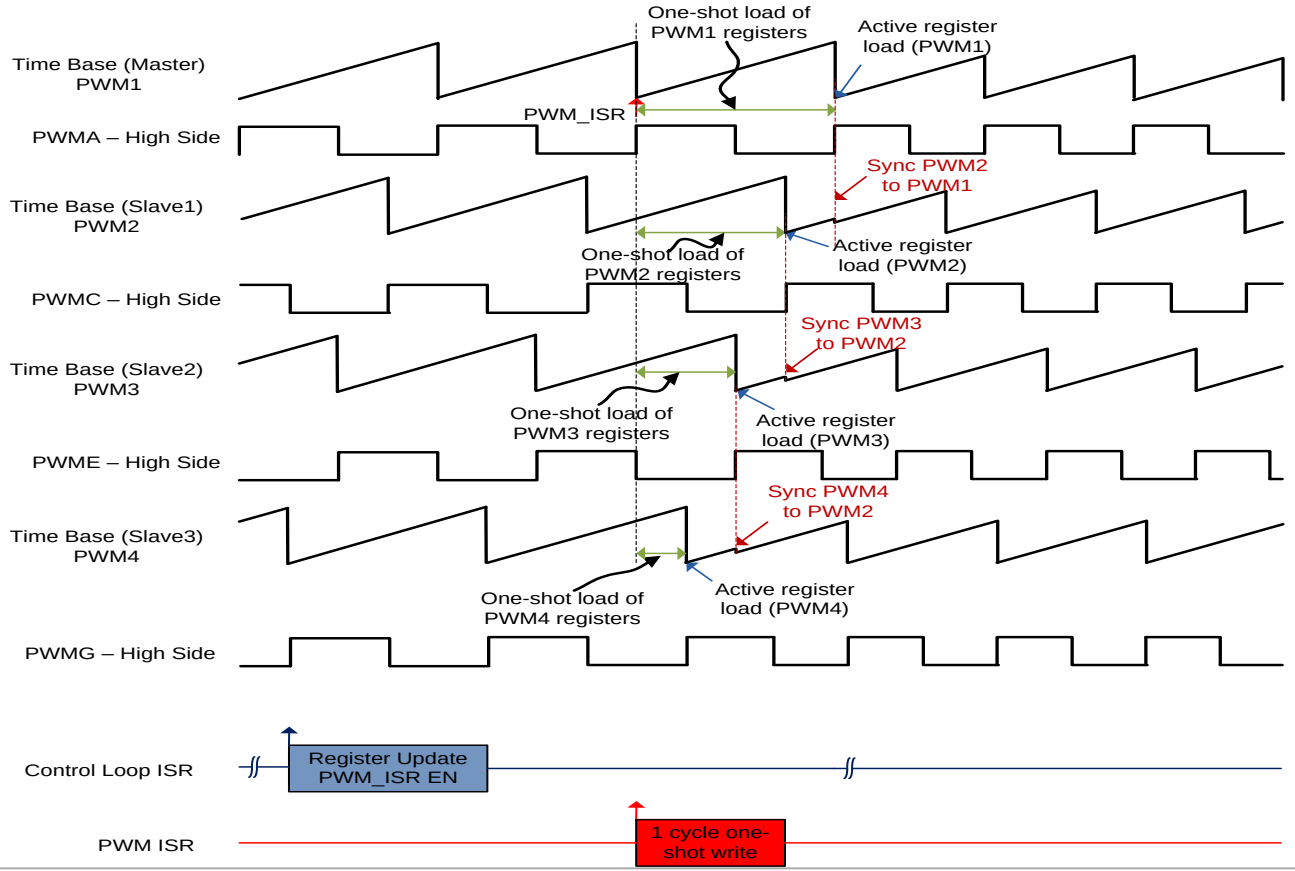
- Enable global reload
- Link GLDCTL2 registers

Run Time

- Update all registers
- Write '1' to GLDCTL2[OSHTLD]
- Write '1' to GLDCTL2[GFRCLD], if desired

- For all registers that have this mode enabled, shadow to active loads occur at the same event defined by GLDCTL[GLDMODE]
- Global reload pulse pre-scalar provides capability to choose transfers to happen once in 'N' occurrences of selected event

Example – Interleaved Resonant Converters



Remapped Register Space

Register Mapping

- PWM registers are spread over four data pages to allow future expansion
- Registers are grouped according to their functionality
- This reduces number of data page moves required, improving execution time

Support for Valley Switching

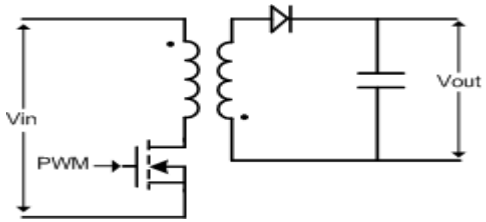
Valley Switching

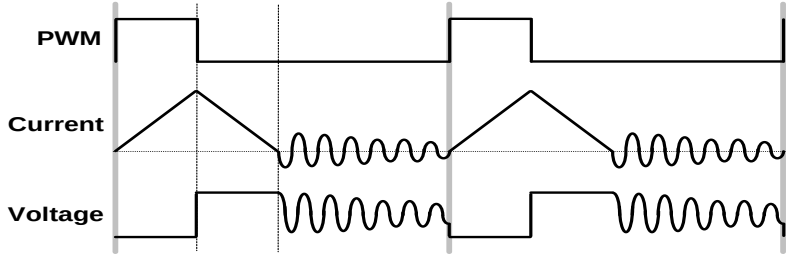
- Soft-switching technique that improves system efficiency and performance

- Switch should be turned ON at the valley point of the voltage across it

Challenges

- Resonant oscillations are highly dependent on circuit parasitics and on operating conditions – making it difficult to detect optimum valley point



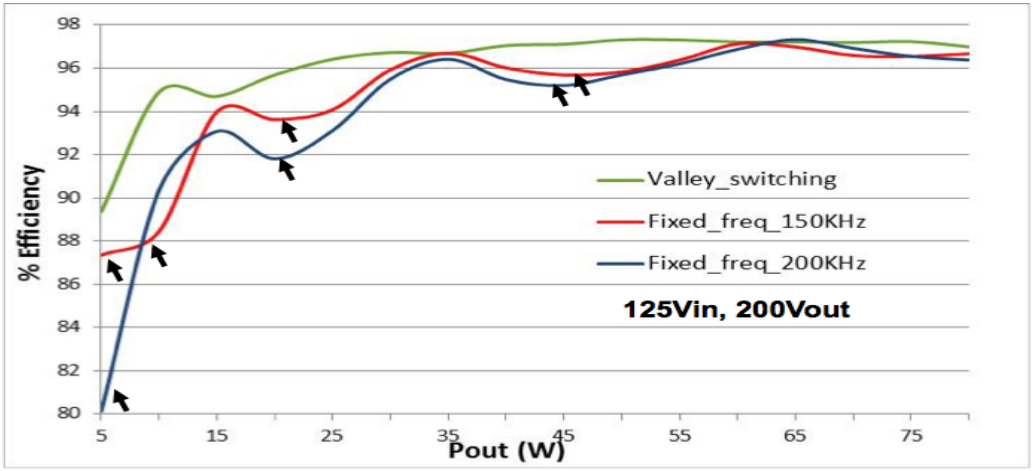


Valley Switching Enhancements

Highlights

- A hardware mechanism to precisely control PWM ON/OFF time instants to implement valley switching
- Captures time period of oscillations to accurately delay PWM switching instant
- Ability to add software programmable offset to captured delay
- Programmable number of edges before the delay takes effect
- Multiple choices of triggers and events
- Allows easy adaptability for optimum performance under changing system/operating conditions

Efficiency Results

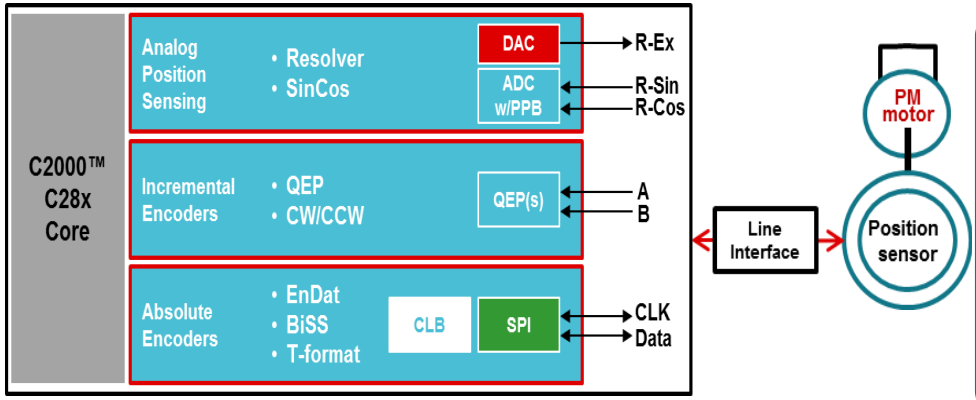


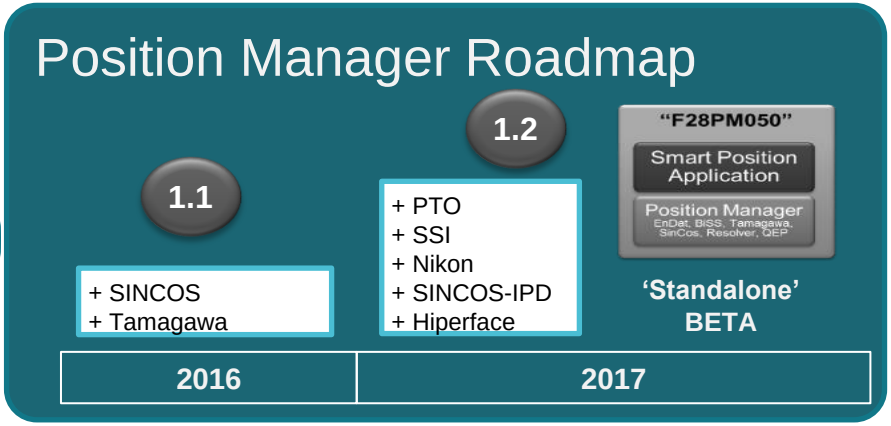
- Highlighted points in the fixed frequency curves correspond to the data where the MOSFET happens to turn ON at the peak of the drain-source voltage
- When valley switching is used the MOSFET is always turned ON at the valley of the drain-source voltage
- Biggest efficiency improvements are seen at the highlighted points

Industrial Drives

Improvements for Industrial Drives

Position Manager Technology





Sensor Type	Speed	Tested Length	Resolution	C2000 Supported Devices
Incremental	~ 12,000 rpm	N/A	Encoder dependent	'F2803x, 'F2806x,'F2807x, 'F2837xS, 'F2837xD, F28378S, 'F28378D, F28076, F280049
EnDat 2.2 / 2.1	8 MHz	100 m	Up to 35 bits	'F28379S, 'F28379D, F28378S, 'F28378D, F28076, F280049
BiSS-C	5 MHz	100 m	Up to 26 bits	'F28379S, 'F28379D, F28378S, 'F28378D, F28076, F280049
t-format (Tamagawa)	2.5 MHz	100m	Up to 24 bits	'F28379S, 'F28379D, F28378S, 'F28378D, F28076, F280049
SIN/COS	~ 12,000 rpm	70 m	+/- 4.5 arcsecs	'F2807x, 'F2837xS, 'F2837xD[1] , F28378S, 'F28378D, F28076, F280049
Resolver	> 3,000 rpm	~1 m	>13.47 ENOB	'F2802x, 'F2807x, 'F2837xS, 'F2837xD[1], F28378S, 'F28378D, F28076, F280049

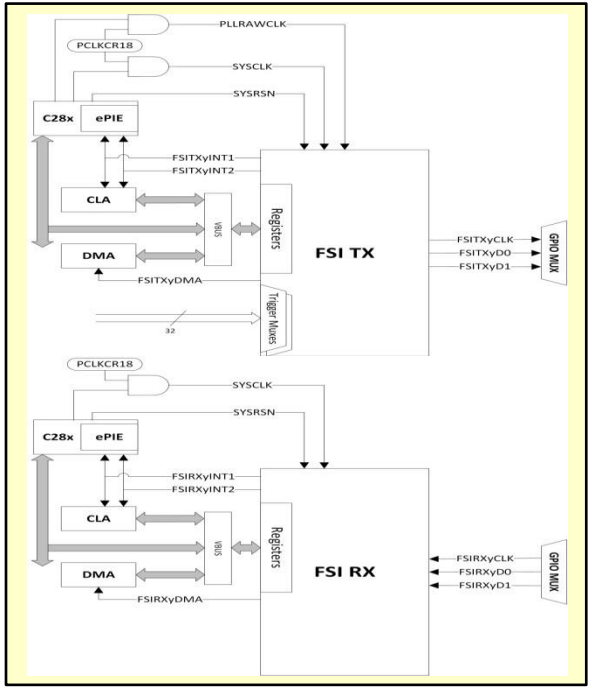
- Save at least 10% of the development effort when compared to custom solutions
- Reduce system cost by up to 10%
- Supports the leading analog and digital position sensors including resolver, SIN/COS, QEP, BiSS-C and EnDAT2.2
- Reference hardware, example is compliance tested and future-proof
- Compliance tested

* Devices in red coming soon….

Fast Serial Interface (FSI) – Type 0

- Motivation: trend/desire to move the control to the HOT side of a drive, but existing isolation technology is too slow or not safe
  - *FSI will provide high reliability, high speed transfers across isolation*

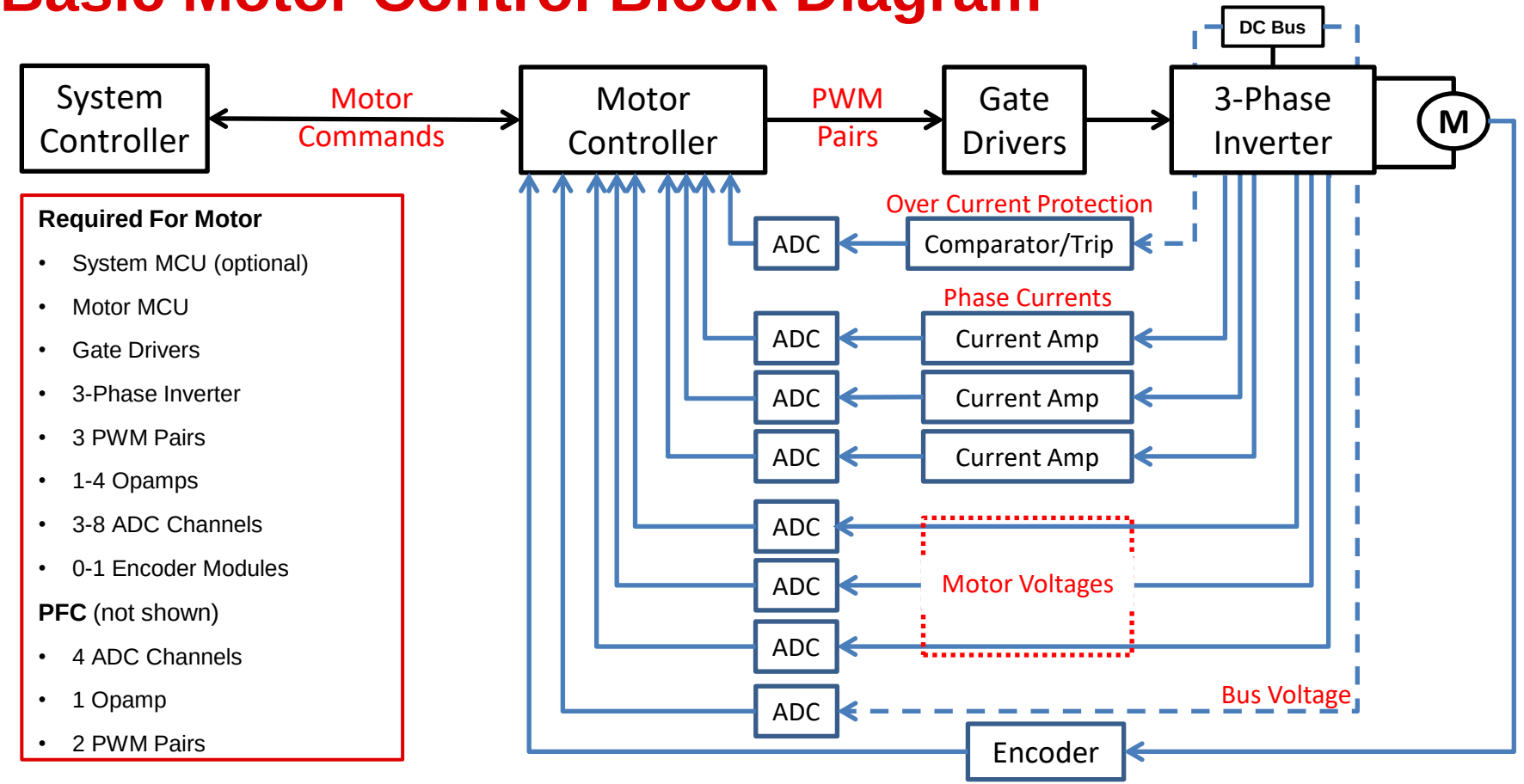
- **Features:**
  - Point-to-point (single master/single slave)
  - Fast transfer: 50 MHz (*Targeted*)
  - Double data rate (200Mbps @ 50MHz clock)
  - Single or dual data lines
  - Independent Transmit and Receive modules
  - 8-bit H/W CRC and checker
  - Skew compensation for signal delay due to isolation
  - Line break detection
  - Supports 5 kHz – 300 kHz PWM loops (single/multi)



PFC + Motor Control

Motors Application Example

Basic Motor Control Block Diagram



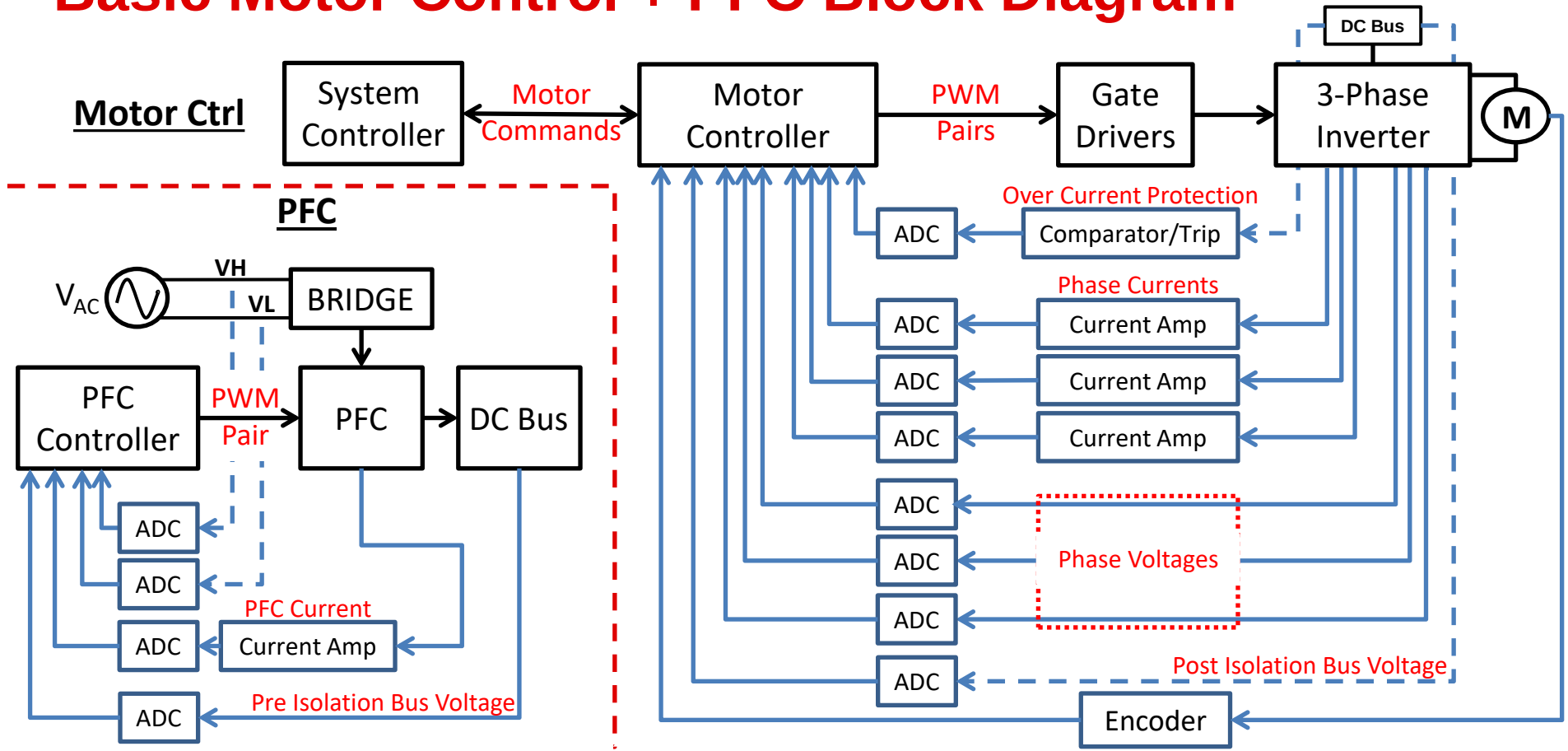
Required For Motor

- System MCU (optional)
- Motor MCU
- Gate Drivers
- 3-Phase Inverter
- 3 PWM Pairs
- 1-4 Opamps
- 3-8 ADC Channels
- 0-1 Encoder Modules

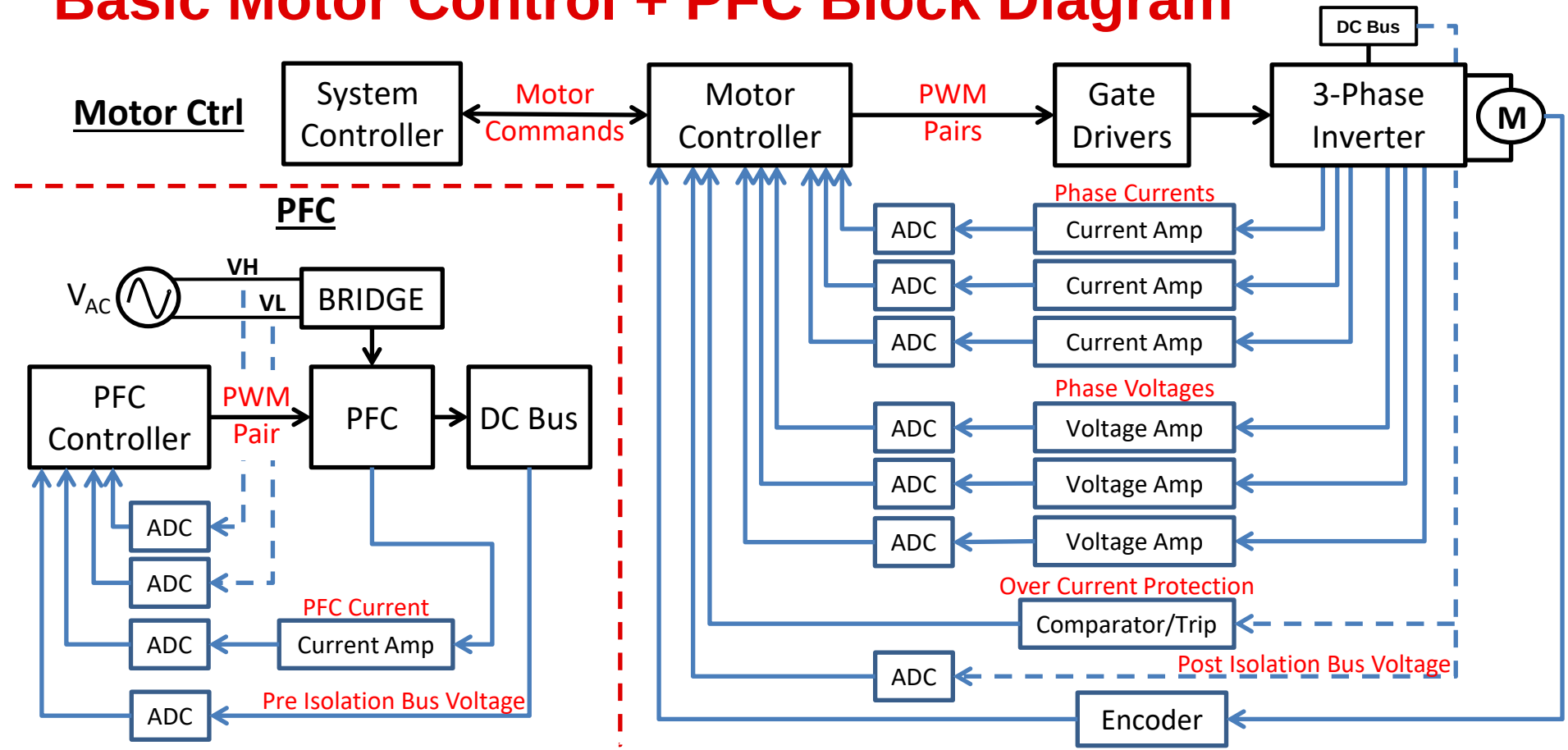
PFC (not shown)

- 4 ADC Channels
- 1 Opamp
- 2 PWM Pairs

Basic Motor Control + PFC Block Diagram



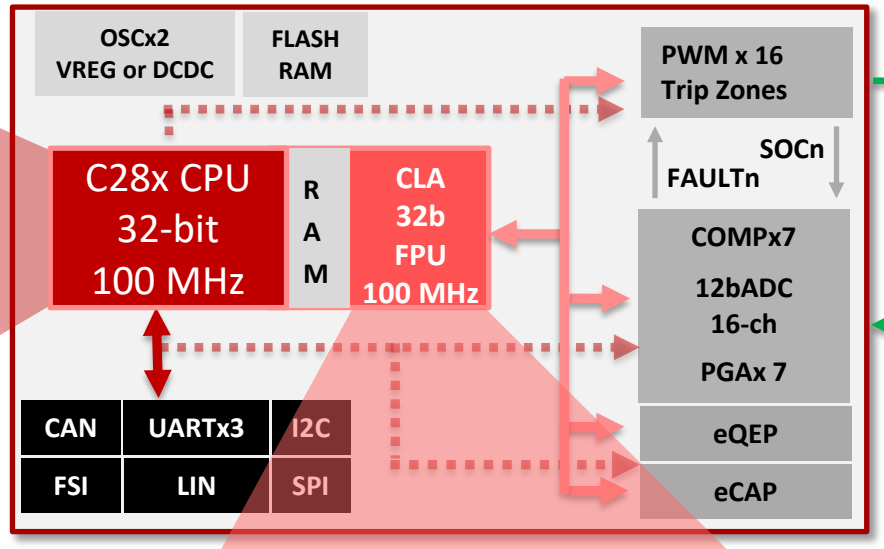
Basic Motor Control + PFC Block Diagram



Piccolo F28004x: Complete system integration: CLA + analog integration + motor library = *Flexible* motor engine

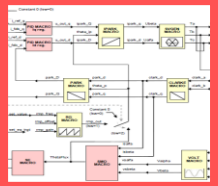
Speed, position, communications, supervisory, safety

- More efficient motor libraries



3PH-INV

Sensors optional



Independent FOC control

- C-programmable CLA doubles performance
- Flexible abstraction with available code blocks

Closing Remarks

TMS320F28004x targeted for real time control

- All EE improvements
  - Dual Bank Flash
  - CLA Type 2
  - Memory Subsystem
- Digital Power
  - Delay Trip
  - Global Load and One Shot Improvements
  - Valley Switching Support in HW
- Industrial Drives
  - Same encoder support as F28379D
  - Additional encoder standards coming
- Motor Control
  - InstaSPIN on CLA!