

Hello, and welcome to the TI Precision Labs video series discussing comparator applications. The comparator's job is to compare two analog input signals and produce a digital or logic level output based on that comparison. In this video we'll discuss the basic functionality of the analog comparator and some of its key specifications, including input offset voltage or VOS.



Let's begin by introducing the basic functionality of a comparator. Similar to a standard op amp, a comparator has two inputs, one output, and two power supply pins. From a schematic perspective it looks the same as an op amp, although its intended function is quite different.

A comparator gets its name because it **compares** the voltages applied to its inputs and sets its output voltage based on the input levels. One input is considered to be the primary input signal, or VIN, and the other input is considered to be the reference signal VREF. These inputs may have both dc and ac components. The output voltage Vout can be set to one of two levels; a high level or logic 1, or a low level or logic 0. VH, the output high level, approaches V+, the positive power supply voltage. VL, the output low level, approaches 0V or ground, or the negative supply in dual supply configurations.

The comparator shown on this slide is configured for non-inverting operation. In this condition, VIN, the input signal, is connected to the non-inverting input +IN, and VREF, the reference signal, is connected to the inverting input –IN. If VIN > VREF, the comparator output goes high. If VIN < VREF, the output goes low.



A comparator can also be used in an inverting configuration. In this condition, VIN, the input signal, is connected to the **inverting** input –IN, and VREF, the reference signal, is connected to the **non-inverting** input +IN. Because of the change in how we've defined our input signals, the output behavior can be considered inverted. Now if VIN > VREF, the comparator output goes **low**, and if VIN < VREF, the output goes **high**.



Let's take a look at a simplified internal design of a bipolar comparator, the LM139. The objective here is not to teach transistor theory or the detailed workings of a comparator design, but rather to give you a general idea of how a comparator works.

The input stage, outlined in the blue box, is comprised of a PNP differential amplifier. Each side of the differential stage uses Darlington PNP transistors. Using Darlington connected transistors increases the input impedance, lowers the input bias current, and allows the common-mode input voltage to extend down to zero volts. Each transistor in this stage has a current source in the emitter circuit that sets the emitter current.

The collectors of the transistors in the differential input stage are connected to NPN transistors that act as a dynamic load, as shown outlined in turquoise. Finally, the output of the dynamic load stage is coupled to an NPN driver and open collector output stage, as shown outlined in purple.

During normal operation of the comparator, the differential input signal [+IN – (-IN)] is amplified by the voltage gain of the input differential amplifier. The output of this differential stage is developed on T6 and is used to turn the output stage on or off depending on the input polarity.



To better understand the internal function, let's now apply some changing input signals to the comparator and see how the internal voltages change in the various states. In this example, we will be using the comparator in an inverting configuration, with VREF connected to +IN and VIN connected to –IN.

Let's first apply a 2.5V reference voltage to +IN and a 2.4V input signal to –IN, so we are comparing 2.4V against a 2.5V reference. The voltages are shown in red on each of the nodes, and the case with a 2.4V input is given on the bottom. Looking into –IN, the transistors connecting to that side of the differential

input pair connect to dynamic load transistor T6. The voltage at the collector of T6 is equal to 0.63V, clamped by the base-to-emitter voltage of transistor T7. Transistor T7 is now ON, which turns transistor T8 OFF by pulling down its base voltage. Since T8 is off, its collector looks like a high impedance, and the output voltage of the comparator is pulled high by the  $2k\Omega$  pull-up resistor connected to the positive power supply.

Now let's keep the 2.5V reference voltage on +IN but change the input signal on –IN to 2.6V. We are now comparing 2.6V against the 2.5V reference. Transistor T4 and T6 will be on and saturated, making the voltage across T6 very low. T7 now turns off, allowing T8 to fully turn on and drive the comparator output voltage down to approximately 0V or logic low.



Comparators are divided into two main types, based on the design of their output stage. These two types are called open-drain (or open-collector), and pushpull (also known as drain-drain, or collector-collector). Open-collector and collector-collector comparators are built with bipolar transistors, while open-drain and drain-drain comparators are built with FETs.

The comparator on the left and the LM139 example from the previous slide have an open-collector output, with an output stage consisting of a single NPN bipolar transistor. When this transistor is on, it actively sinks current from collector to emitter and pulls the output voltage Vo down very close to GND or OV. How close the output can swing to ground depends on the collector-to-emitter saturation voltage. When the transistor is off, its collector looks like high impedance and has essentially no effect on the output voltage. In this case, a small amount of current is sourced from V+ through the pull-up resistor and Vo rises to VOH, or logic 1. Without this pull-up resistor, Vo could float to an unknown state.

Push-pull comparators, on the other hand, have an output stage consisting of a pair of output transistors. Either the upper or lower transistor in the pair turns on and actively sources or sinks current in order to drive the output high or low as needed. In the example on the right, the P-channel upper FET turns on to source current and **push** the output high, while the N-channel lower FET turns on to sink current and **pull** the output low. No pull-up resistor is required for this type of comparator.



A commonly-desired function of comparators is to generate a logical **OR**, where an output is logic **LOW** when either of its two inputs is **ON**. This functional block is commonly implemented by wiring the outputs of two comparators together. However, care must be taken to use the right type of comparator, as we'll discuss.

Let's first consider the circuit on the left, with two push-pull devices whose outputs are tied together. Remember, a push-pull comparator actively sources or sinks current to push or pull its output voltage high or low. You may already see the problem with this circuit configuration, but let's analyze the different possibilities of its operation.

In the case where the outputs of both comparators are **high**, the **top** transistor in each push-pull output stage turns on and the output is driven **high**. Similarly, if both outputs are **low** then the **bottom** transistors in each comparator turn on and the output is driven **low**. The **problem** arises when the two comparators try to drive the output to different states – in this case, there is a conflict as each comparator tries to source or sink current to force the output to a different voltage. This creates a high current condition and drives the output to some indeterminate state which is neither high nor low. As you might imagine, this condition is undesirable and can even damage the devices. For this reason, push-pull comparators should never be connected together in this way.

On the other hand, open-collector or open-drain comparators work perfectly with this approach. Remember that the output stage of an open-collector or open-drain comparator is built with a single transistor that pulls the output low when it turns on, and looks like a high impedance when it turns off. Now, no matter which combination of high or low is present on each output, the output will safely be driven to a known state. If both outputs are low, both output transistors are **ON** and pull the overall output down to approximately OV. If both outputs are high, both transistors are **OFF** and act like a high impedance, allowing the output to be pulled up to logic high through the pullup resistors. If one output is high and one output is low, the low state will dominate as the transistor which is ON can sink much more current to pull the output low than the pull-up resistor can provide to drive the output high. You can check the truth table on the right for the logical behavior in all four possible input states. As you can see, this is equivalent to a logic OR function.

This implementation of a logical OR with comparators is commonly called the **wired-or configuration**.



We'll end this first video in the series with a discussion of comparator DC parameters, which should be very familiar to any one with knowledge of op amps. This diagram shows the basic comparator schematic along with many of the most common DC parameters, including:

Input offset voltage, or **VOS**, represented as a voltage source in series with the non-inverting input Input bias current, or **IB**, and input offset current, or **IOS**, represented as current sources flowing into or out of the comparator inputs Input common-mode voltage range, or **VCM**, the range of allowable input common-mode voltages before the input transistors will saturate or cut off, typically extending from one supply rail to the other on modern devices

Input differential voltage range, or **VDIFF**, the maximum allowable differential voltage across **+IN** and **-IN** 

Voltage output high from the rail, or **VOH**, the maximum logic high voltage relative to the positive power supply

Voltage output low from the rail, or **VOL**, the minimum logic low voltage relative to ground or the negative power supply

Output short-circuit current, or **ISC**, the maximum output current which can be sourced or sunk by the output stage transistors

Quiescent current, or **IQ**, the typical current consumption of the device when the output current is zero, and

Power supply voltage range, or **VS**, the range of allowable power supply voltages for specified operation

Other parameters may be specified, such as the open loop gain, voltage offset drift, common-mode rejection, and power supply rejection, but they are typically less critical to a comparator than the previous specifications and are considered less often.



One of the most critical DC specifications is the input offset voltage **VOS**. Since the VOS of a comparator creates an additional DC voltage in series with the non-inverting input, it has a major effect on the threshold at which the output of the comparator changes states. Let's analyze a non-inverting comparator circuit with three different VOS values to better understand the effect. Remember that for a non-inverting comparator, VOUT is **HIGH** if VIN > VREF, and VOUT is **LOW** if VIN < VREF.

In this example we will apply a reference voltage of 2.5V to the inverting input. The input signal is a slow-

moving ramp transitioning from 2.46V to 2.54V, as you can see in the dark blue waveform in the plot on the right. The offset voltage adds to the input signal to create a total effective input signal equal to **VIN + VOS**.

If VOS = 0, then the total input voltage is equal to VIN + 0, and circuit works as expected. When VIN > 2.5V, VOUT is high, and when VIN < 2.5V, VOUT is low, as you can see in the red waveform.

If VOS = +10mV, then the total input voltage is equal to VIN + 10mV. Now the output will transition at a lower voltage of VIN, because the added voltage from VOS allows the total input voltage to reach 2.5V earlier. You can see in the orange waveform that VOUT is high when VIN > 2.49V and VOUT is low when VIN < 2.49V.

Finally, if VOS = -10mV, then the total input voltage is equal to VIN – 10mV. Now the output will transition at a higher voltage of VIN because of the voltage which is subtracted by the negative VOS. You can see in the light blue waveform that VOUT is high when VIN > 2.51V, and VOUT is low when VIN < 2.51V. Keep in mind that not only does the **threshold voltage** change due to VOS, but the **timing** of the output waveform is also affected. For example, when VOS = +10mV, the output waveform is high for approximately 600 ms. When VOS = -10mV, the output waveform is high for less than 400 ms. This timing behavior may cause issues in certain designs, but the very slow-moving input signal in this example creates a worst-case scenario. To help prevent these types of errors, the frequency of the input signal can be increased.

Many engineers used to designing with modern op amps may be accustomed to offset voltages in the range of **microvolts** to a few **millivolts**. Comparators typically have offsets which are somewhat higher, ranging from about **±2mV** up to **±15mV**!



In some cases, the offset voltage of the comparator can completely change its output signal. Consider the circuit shown on the left, an inverting comparator with its input signal provided by a digital-to-analog converter. Digital to analog converters generate analog voltages (or currents) based on digital codes, so their output will often seem to step between different DC voltages over time.

Let's analyze the output of this circuit when we provide a reference voltage of 1.25V, and the offset voltage changes from +5mV, to 0 mV, to -5 mV. In this circuit, VOS is added to VREF, so the total effective reference voltage becomes VREF + VOS.

When VOS = +5mV, the total reference voltage is equal to 1.25V + 5mV, or 1.255 V. Because of the increased reference voltage, the comparator output only goes low twice during the input waveform, as shown in the blue plot on the top right. When VOS = 0 V, the total reference voltage is simply equal to 1.25V. The comparator output is shown in the red plot on the right.

When VOS = -5mV, the total reference voltage is equal to 1.25V – 5mV, or 1.245 V. The comparator output changes again, and is shown in the green plot on the bottom right.

The small input signal range of this example shows a worst-case scenario for errors due to VOS. To prevent these types of errors, increase the range of the input signal relative to the offset voltage. However, this type of behavior can still be encountered when the input signal fluctuates near the reference voltage. Make sure to watch the later videos in this series to learn simple, but powerful techniques that can help to prevent these kinds of errors!

### Thanks for your time! Please try the quiz.

That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.

🔱 Texas Instruments

# Comparator Applications 1 Quiz

TIPL 2101 TI Precision Labs – Op Amps





# **Question 1**

- Is the comparator circuit shown here in an inverting or non-inverting configuration?
- Fill in the  $V_{OUT}$  column of the table below for each input condition.

V <sub>IN</sub>	V <sub>REF</sub>	V <sub>OUT</sub>
1.3 V	1.25 V	
1.2 V	1.25 V	





### **Question 2**

- For the circuit shown below, draw Vout in the plot on the right when:
  - V1 = 1.65V, V2 = 40mVpp triangle wave, Vos = -10mV



# **Multiple Choice**

- When a comparator's open-collector output stage is OFF, it
  - Sinks current in order to pull the output voltage close to the negative power supply a.
  - Sources current in order to push the output voltage close to the positive power supply b.
  - Looks like a high impedance, allowing the output to be pulled high through a pull-up resistor C.
  - None of the above d.
- When a push-pull comparator's output is HIGH, the output stage will ullet

- Source current to drive the load to the required output voltage b.
- Sink current to drive the load to the required output voltage C.
- Float to an unknown state d.



Look like a high impedance a.

# **Multiple Choice**

- Push-pull comparators work well for wired-or applications.
  - a. True
  - b. False
- The maximum V<sub>OS</sub> of a comparator ranges from \_\_\_\_\_
  - a.  $\pm 1\mu V$  to  $\pm 10\mu V$
  - b.  $\pm 25\mu V$  to  $\pm 1mV$
  - c.  $\pm 2mV$  to  $\pm 15mV$
  - d.  $\pm 1\mu V$  to  $\pm 100mV$



Solutions



# **Question 1 – Solution**

- Is the comparator circuit shown here in an inverting or non-inverting configuration? Non-inverting
- Fill in the V<sub>OUT</sub> column of the table below for each input condition.

V <sub>IN</sub>	V <sub>REF</sub>	V <sub>OUT</sub>
1.3 V	1.25 V	HIGH (1)
1.2 V	1.25 V	LOW (0)



V+



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### **Question 2 – Solution**

- For the circuit shown below, draw Vout in the plot on the right when:
  - V1 = 1.65V, V2 = 40mVpp triangle wave, Vos = -10mV



### **Multiple Choice – Solutions**

- When a comparator's open-collector output stage is OFF, it
  - Sinks current in order to pull the output voltage close to the negative power supply a.
  - Sources current in order to push the output voltage close to the positive power supply b.
  - Looks like a high impedance, allowing the output to be pulled high through a pull-up resistor C.
  - None of the above d.
- When a push-pull comparator's output is HIGH, the output stage will ullet
  - Look like a high impedance a.
  - Source current to drive the load to the required output voltage b.
  - Sink current to drive the load to the required output voltage C.
  - Float to an unknown state d.



# **Multiple Choice – Solutions**

• Push-pull comparators work well for wired-or applications.

a. True

b. False

- The maximum V<sub>OS</sub> of a comparator ranges from \_\_\_\_\_
  - a.  $\pm 1\mu V$  to  $\pm 10\mu V$
  - b.  $\pm 25\mu V$  to  $\pm 1mV$
  - c.  $\pm 2mV$  to  $\pm 15mV$
  - d.  $\pm 1\mu V$  to  $\pm 100mV$

