

Optimizing Wide Vin Designs with LDOs

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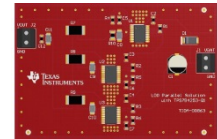
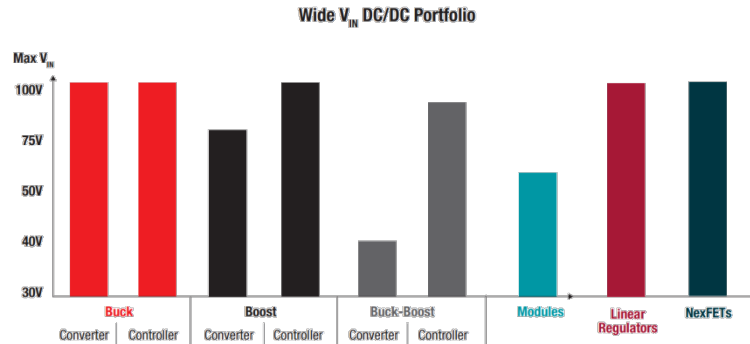


Agenda

- Common Design Requirements & Applications
- Design Challenges
- TI Solutions and Tools
- Summary
- Design Tools and Support

Why use wide V_{IN} LDOs?

Wide V_{IN} Capability	System Benefit
Increased robustness against input transients	Eliminates the need for external transient protection components, saves PCB area
Ability to convert high V_{IN} to low V_{OUT}	Eliminates two-stage conversions, saves PCB area
Low noise, low EMI solutions	Eliminates external filtering, improves quality of data signals
Stackable devices with current sharing	Enables re-use across multiple applications



Where do we need Wide V_{IN} LDOs?

Rugged Industrial Equipment

- 40V+ Wide V_{IN} operation for 24V backplanes
- Isolated bias power for PLCs and motor drives
- Low noise for precision circuits and sensing

Advanced Automotive Electronics

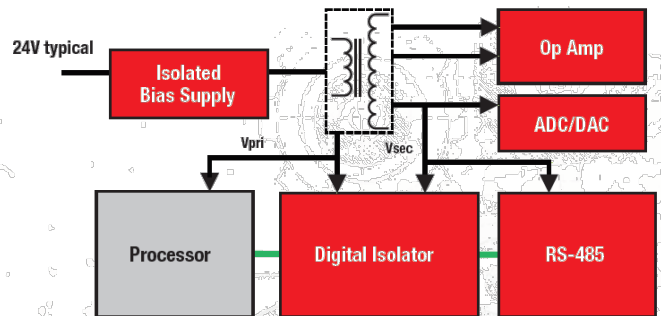
- 42V/60V Wide V_{IN} rating to survive load dump
- >2Mhz operation to reduce radio interference
- Low standby / shutdown I_Q to reduce batter drain
- Ultra-small IC packaging to reduce PCB footprint

Sensitive Communications Systems

- 75V/100V Wide V_{IN} operation for 48V backplanes
- High-performance/high-current power rails
- High PSRR and low-noise regulators for powering RF circuits

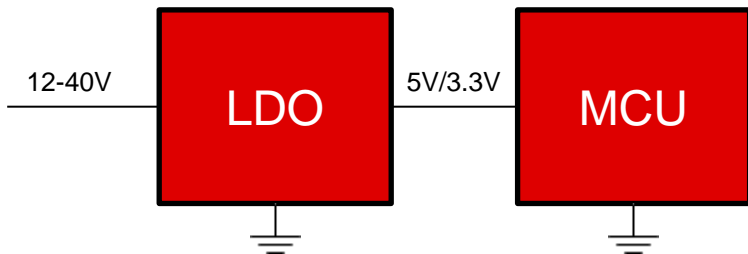


Isolated Signal and Power Path



Design Challenges

Design Challenges: Wide V_{IN}

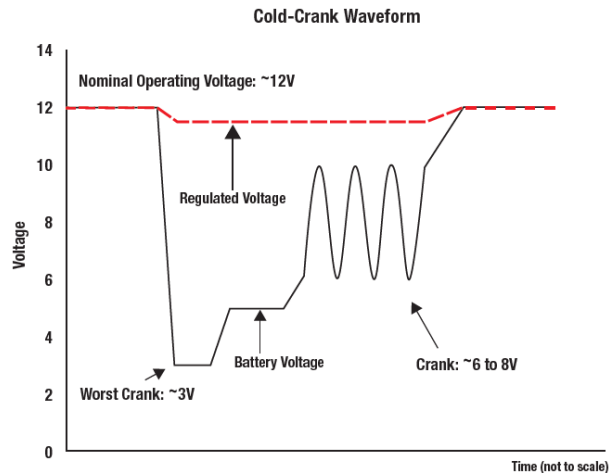


Voltage Spikes & Increases

- Voltage spikes may occur due to shorts between rails
- Variable power demand coming from inductive loads:

$$V = L \frac{\Delta I}{\Delta t}$$

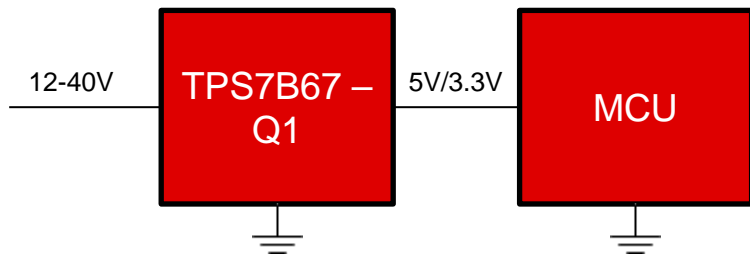
*See blog: [LDO Basics: Dropout](#)



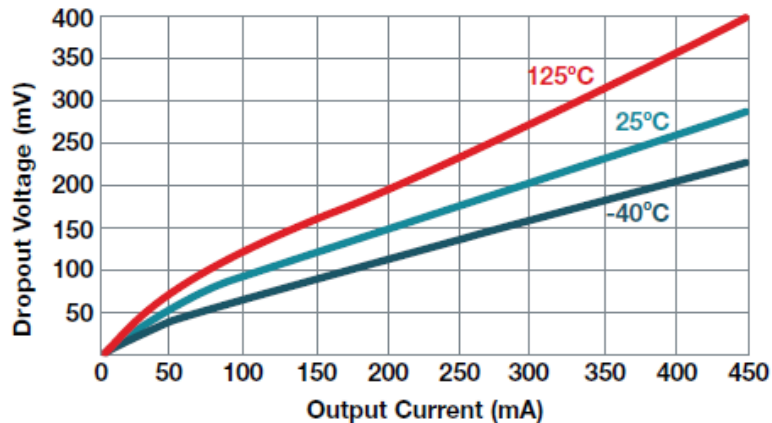
Cold-Crank and Battery Voltage

- Battery voltage drops significantly due to starter or high current pull
- Voltage drop may affect LDO regulation

Design Challenges: Adjusting for swings



Dropout Voltage vs. Output Current



Ensure V_{IN} is ideal for regulation

- Maintain a safe margin between $V_{(INMAX)}$ and $V_{IN(ABSMAX)}$
- Make sure V_{IN} is at least $V_{IN} + V_{DO(MAX)}$

Pick LDOs with very low V_{DO}

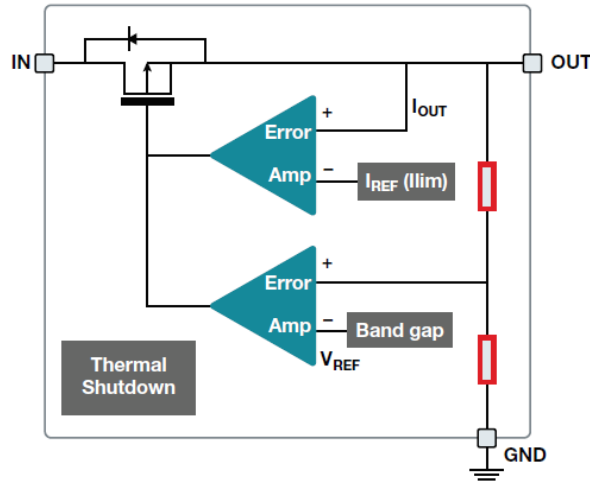
- Enables low-voltage regulation even in cold-crank conditions
- i.e. V_{IN} is 12V nominal, but can be 4V in cold-crank. TPS7B67-Q1 can still regulate to 3.3V

*See blog: [LDO Basics: Dropout](#)

Design Challenges: Current Limit

Current limit helps protect the LDO and sensitive electronics

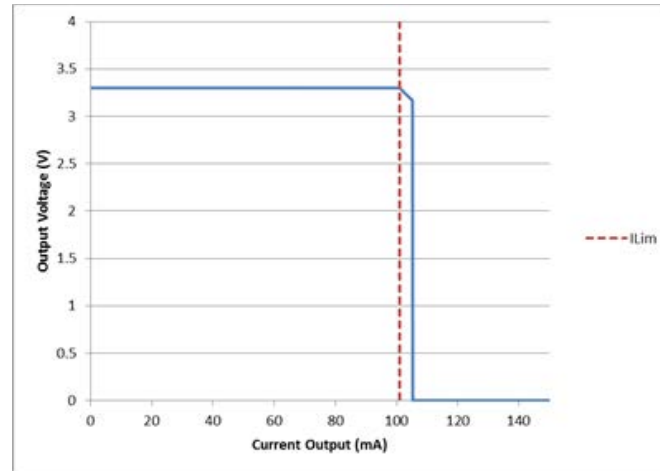
- Selecting an LDO with internal protection from short circuits and power surges



- LDOs feature internal current limits that range from low to high current
- The internal reference allows for a margin of operation, but it shuts down regulation whenever $I_{OUT} \geq I_{LIMIT}$
- LDOs are offered with two main current limit topologies: brick wall and fold-back current limiting

*See blog: [LDO Basics: Current Limit](#)

Design Challenges: Brick wall Current Limit



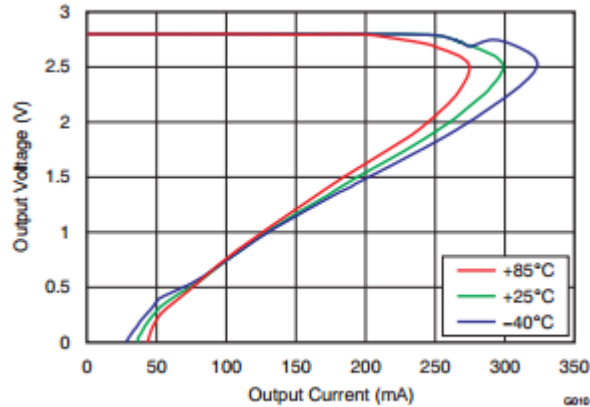
$$V_{OUT} = I_{LIMIT} \times R_{LOAD}$$

During brick wall current limiting

- The upper boundary is defined and the LDO supplies current incrementally until the limit current limit is reached
- Regulation will continue this operation and dissipate power, as long as the thermal resistance (θ_{JA}) allows for healthy power dissipation
- Once V_{OUT} goes too low and the thermal limit is reached, thermal shutdown will turn off the device in order to protect it from permanent damage

*See blog: [LDO Basics: Current Limit](#)

Design Challenges: Fold-back Current Limit



During fold-back current limiting

- the main goal of fold-back current is to limit the total power dissipation by reducing the output current limit linearly while V_{OUT} decreases and V_{IN} remains steady
- Additional protection is given to devices that are sensitive to temperature increases but can complicate the overall design

*See blog: [LDO Basics: Current Limit](#)

Design Challenges: Power Dissipation

Power Dissipation is high for wide V_{IN}

- LDOs dissipate power into heat proportional to the voltage drop from V_{IN} to V_{OUT}
- Heat is concentrated on the board triggering thermal shutdown for other devices

Low I_Q and EN can help reduce heat dissipation and improve efficiency

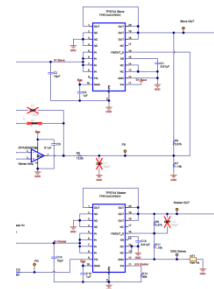
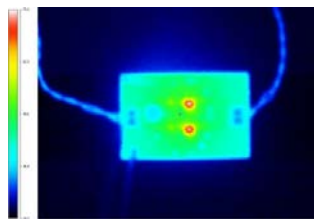
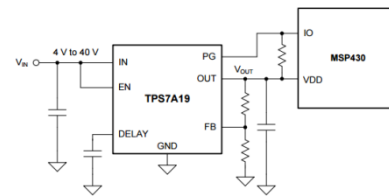
- During no-load conditions LDO power consumption becomes exponentially lower
- The LDO can also be used as a switch powering Ics only when needed

Load/Current sharing can help reduce board heat

- Using two LDOs in parallel can effectively split current and losses
- Heat is better distributed and dropout is lower

$$Total P_{LOSS} = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (I_Q \times V_{IN})$$

$$P_{LOSS} = I_{SHDN} \times V_{IN}$$



*See blog: [Double your current with current-sharing dual LDOs](#)

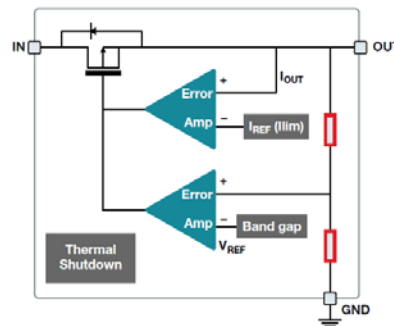
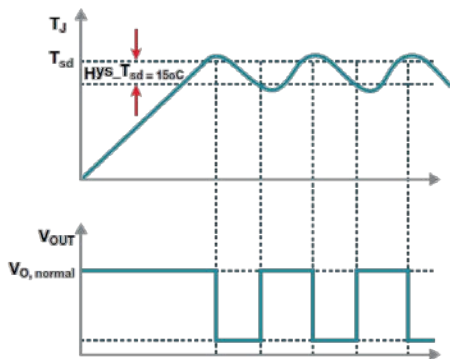
Design Challenges: Thermal Shutdown

Internal thermal protection saves the LDO

- Choosing an LDO with internal thermal protection helps disable outputs in unusually high demand conditions
- Thermal protection disables the output when the junction temperature rises to approximately 170°C
- When the device cools it will re-enable
- The junction temperature is dependent on the total effect of power dissipated & ambient temperature:

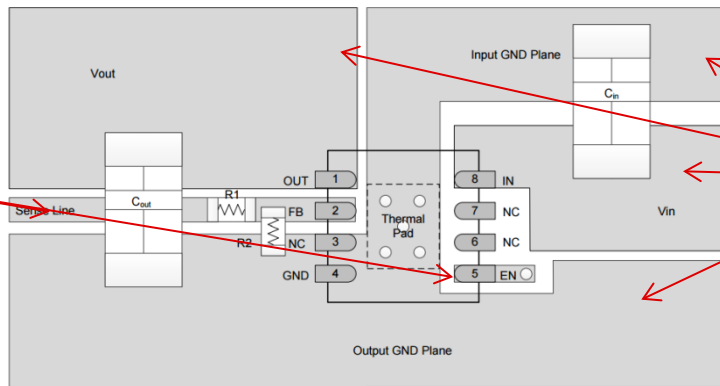
$$T_J = (\theta_{JA} \times PD) + T_A$$

- It is recommended to keep an additional margin to allow for thermal hysteresis to reduce any unwanted shutdowns



Design Challenges: Thermal Layout

Signal path
and logic paths
can handle
smaller traces



Add thick
traces for GND,
VIN and VOUT
planes

A proper layout will improve the LDOs heat, noise and PSRR performance

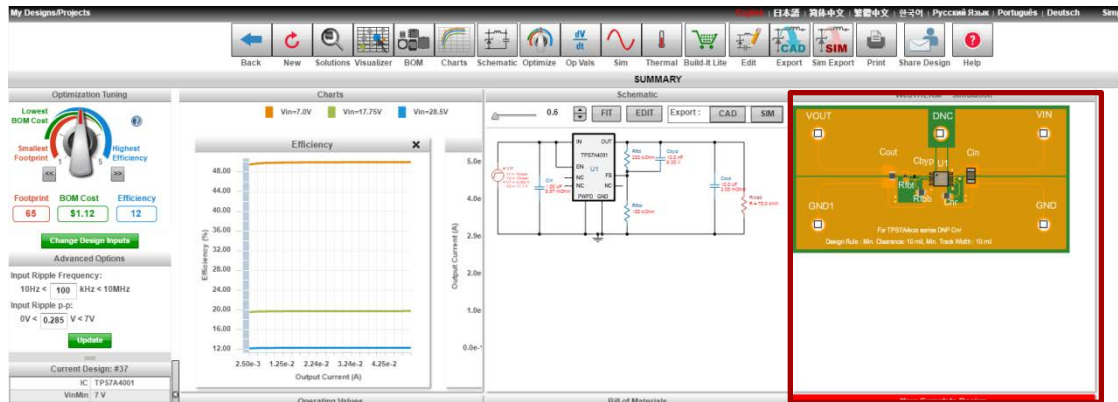
- It is recommended to separate ground planes for IN and OUT to improve noise, PSRR and transient response
- Save room between the LDO and other components to allow better heat dissipation
- Generate as large a GND plane as allowable on the top and bottom layers, especially right near the Package
- Gather the same functional pins together in die design, such as for GND, PVIN, POUT

*See app report: [A Guide to Board Layout for Best Thermal](#)

Design Tools: WEBENCH® Thermal Simulator

TI's WEBENCH® enables for quick and easy simulation!

- Design optimization
- Signal simulation
- BOM and schematic editing tools
- Thermal simulation



WEBENCH® Designer TPS7A4001

	Min	Max	Range
Vin	7.00 V	28.50 V	7.0 to 100.0V
Vout	3.50 V	90.0 V	1.17 to 90.0V
Iout	0.05 A	0.05 A	≤ 0.05A
Ambient Temp	30 °C	125 °C	-40 to 125°C

Lowest BOM Cost | Smallest Footprint | Highest Efficiency

Footprint: 86.0mm² | BOM Cost: \$1.19 | Efficiency: 12.0%

[Open Design](#) [Simulate Now](#)

WEBENCH®
Interactive design
[Preview design](#)

What are WEBENCH® tools?

Design Tools: WEBENCH® Thermal Simulator

Using the thermal Simulator:

- Default and key conditions
- Custom design and inputs

The screenshot displays the WEBENCH Thermal Simulator interface. At the top, the simulation ID is 0. The simulation name is 'Name This Simulation:' and the design ID is 'DesignID: 37, TP57A4001'. The comments field is empty. The 'Thermal Sim Parameters' section shows 'Operating Condition' with 'Vin: 28.50' and 'Iout: 0.05'. The 'Temperature Bar Scaling' section shows 'Min Colorbar Temp: 53' and 'Max Colorbar Temp: 125'. The 'Operating Temperatures' table is as follows:

Layer	Max T	PDiss.	Manufacturer	Part Number
PCB - Top	78°C			
IC - Top	82°C	1.25 W	Texas Instruments	TP57A4001DGNR
IC - Die	83°C	1.25 W	Texas Instruments	TP57A4001DGNR
PCB - Bottom	74°C			

The interface includes a toolbar with icons for Back, New, Solutions Visualizer, BOM, Charts, Schematic, Optimize, Op Vals, Sim (highlighted with a red box), Build-It Lite, Edit, Export, Sim Export, Print, Share Design, and Help. The 'SUMMARY' section shows the 'WebTHERM™ Simulation' results. The 'Optimization Tuning' section shows 'Lowest BOM Cost' at 65, 'Smallest Footprint' at 12, and 'Highest Efficiency' at 12. The 'Charts' section shows an 'Efficiency' graph with three data series for Vin=7.0V (orange), Vin=17.75V (green), and Vin=28.5V (blue). The 'Schematic' section shows a circuit diagram for the TP57A4001 converter. The 'WebTHERM™ Simulation' section shows a 3D model of the PCB and IC with temperature distribution. The 'Your Complete Design' section shows the design parameters: 'Current Design: #37', 'IC: TP57A4001', 'VinMin: 7 V', 'Orientation: Edge 3', 'Insulated OR: 30 °C'.

LDO Resources: TI.com, WEBENCH® and More

Find it all on the LDO landing page: ti.com/lido

Learn

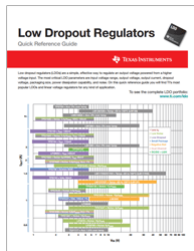
- [Read our LDO Basics blogs](#) to learn more about enhanced features of our LDOs
- Follow our upcoming [LDO training](#) modules for more information

Design

- Leverage our [WEBENCH®](#) designer tool, our TI Designs and app notes to improve your system

Select

- Download our latest selection guides and [Quick Reference Guide](#) to help you find our latest and greatest LDOs
- Go to our [featured products](#) tab where we showcase solutions for LDO design challenges and more



Evaluate & select

Linear Regulator (LDO)

TI LDOs address the power needs for applications requiring low IQ, low noise rails, wide input voltages, small form factors, fast transient responses, or low dropout.

Filter your search

Input Vin (V) Output Vout (V) Iout (A)

Output Options - Select One -

[View All 571 Products](#)

