Optimizing Wide Vin Designs with LDOs

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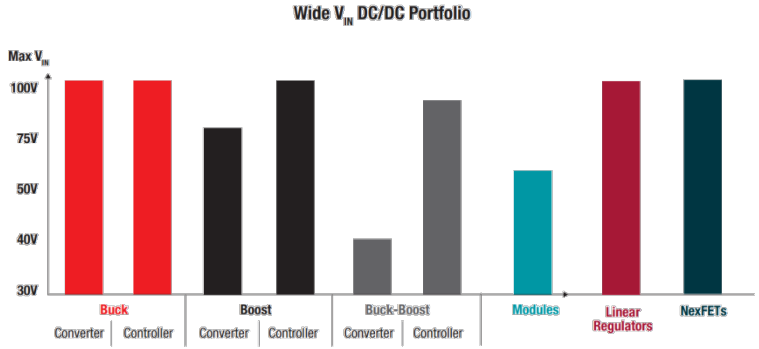
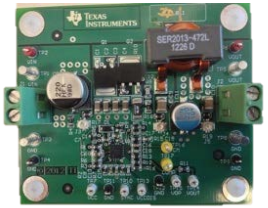
Agenda

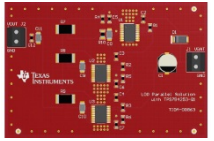
- Common Design Requirements & Applications
- Design Challenges
- TI Solutions and Tools
- Summary
- Design Tools and Support

Why use wide V_{IN} LDOs?

Wide V_{IN} Capability	System Benefit
Increased robustness against input transients	Eliminates the need for external transient protection components, saves PCB area
Ability to convert high VIN to low VOUT	Eliminates two-stage conversions, saves PCB area
Low noise, low EMI solutions	Eliminates external filtering, improves quality of data signals
Stackable devices with current sharing	Enables re-use across multiple applications





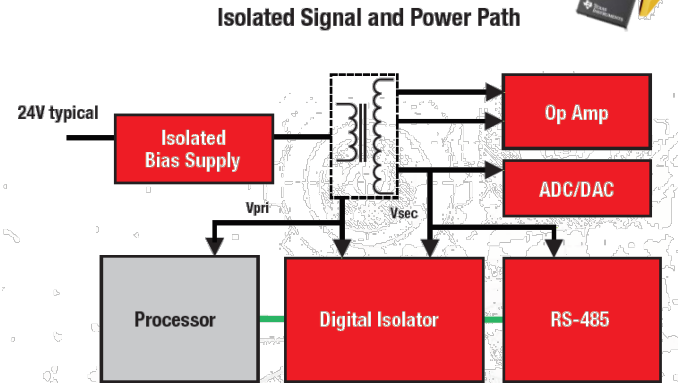


Where do we need Wide V_{IN} LDOs?

Rugged Industrial Equipment
- 40V+ Wide V_{IN} operation for 24V backplanes
- Isolated bias power for PLCs and motor drives
- Low noise for precision circuits and sensing

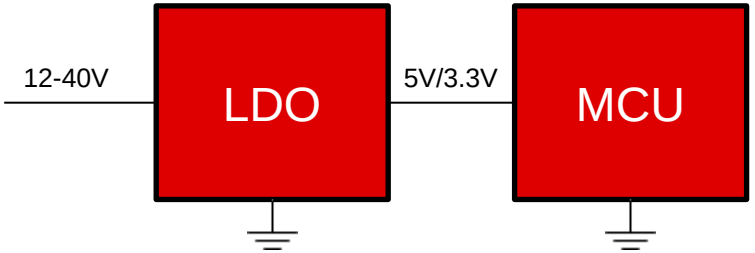
Advanced Automotive Electronics
- 42V/60V Wide V_{IN} rating to survive load dump
- >2Mhz operation to reduce radio interference
- Low standby / shutdown I_Q to reduce batter drain
- Ultra-small IC packaging to reduce PCB footprint

Sensitive Communications Systems
- 75V/100V Wide V_{IN} operation for 48V backplanes
- High-performance/high-current power rails
- High PSRR and low-noise regulators for powering RF circuits



Design Challenges

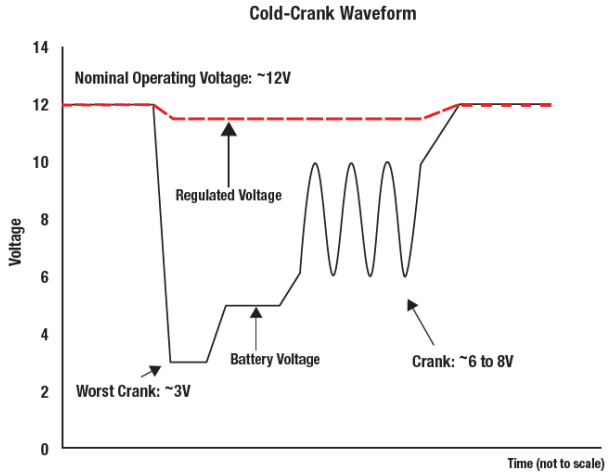
Design Challenges: Wide V_{IN}



Voltage Spikes & Increases

- Voltage spikes may occur due to shorts between rails
- Variable power demand coming from inductive loads:

$$V = L \frac{\Delta I}{\Delta t}$$

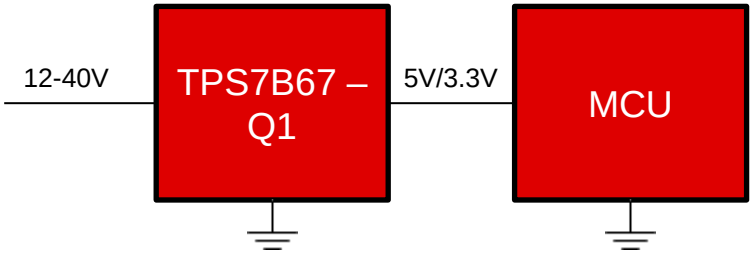


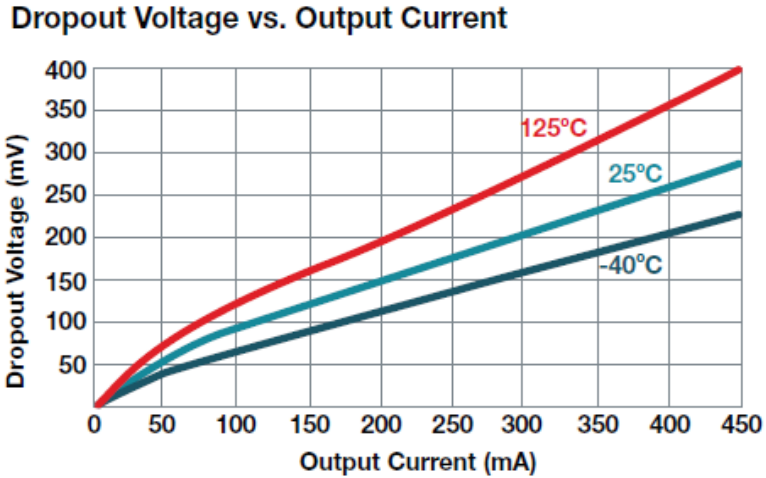
Cold-Crank and Battery Voltage

- Battery voltage drops significantly due to starter or high current pull
- Voltage drop may affect LDO regulation

*See blog: LDO Basics: Dropout

Design Challenges: Adjusting for swings





Ensure V_{IN} is ideal for regulation

- Maintain a safe margin between $V_{(INMAX)}$ and $V_{IN(ABSMAX)}$
- Make sure VIN is at least $V_{IN} + V_{DO(MAX)}$

Pick LDOs with very low V_{DO}

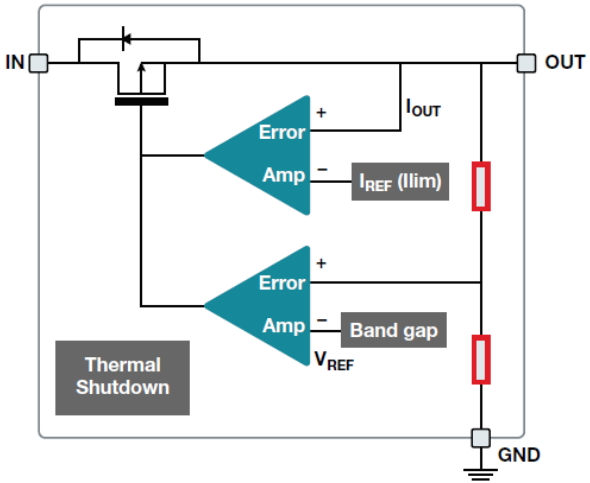
- Enables low-voltage regulation even in cold-crank conditions
- i.e. V_{IN} is 12V nominal, but can be 4V in cold-crank. TPS7B67-Q1 can still regulate to 3.3V

*See blog: LDO Basics: Dropout

Design Challenges: Current Limit

Current limit helps protect the LDO and sensitive electronics

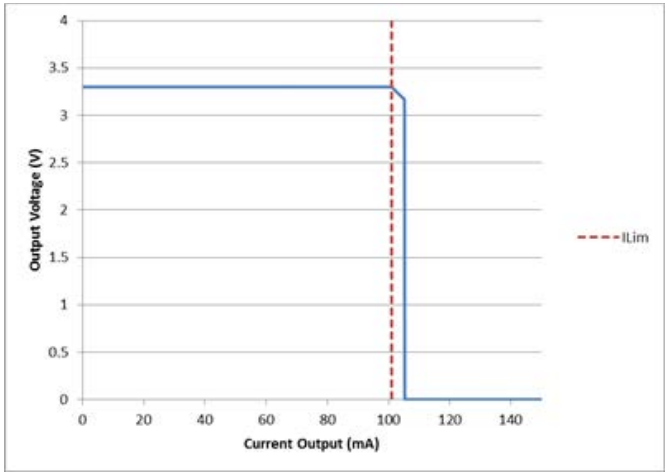
- Selecting an LDO with internal protection from short circuits and power surges



- LDOs feature internal current limits that range from low to high current
- The internal reference allows for a margin of operation, but it shuts down regulation whenever I_{OUT} >= I_{LIMIT}
- LDOs are offered with two main current limit topologies: brick wall and fold-back current limiting

*See blog: LDO Basics: Current Limit

Design Challenges: Brick wall Current Limit



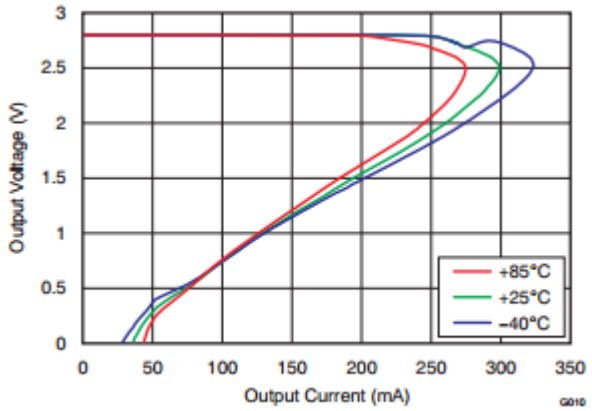
$$V_{OUT} = I_{LIMIT} \times R_{LOAD}$$

During brick wall current limiting

- The upper boundary is defined and the LDO supplies current incrementally until the limit current limit is reached
- Regulation will continue this operation and dissipate power, as long as the thermal resistance (θ_{JA}) allows for healthy power dissipation
- Once V_{OUT} goes too low and the thermal limit is reached, thermal shutdown will turn off the device in order to protect it from permanent damage

*See blog: LDO Basics: Current Limit

Design Challenges: Fold-back Current Limit



During fold-back current limiting

- the main goal of fold-back current is to limit the total power dissipation by reducing the output current limit linearly while V_{OUT} decreases and V_{IN} remains steady
- Additional protection is given to devices that are sensitive to temperature increases but can complicate the overall design

*See blog: LDO Basics: Current Limit

Design Challenges: Power Dissipation

Power Dissipation is high for wide V_{IN}

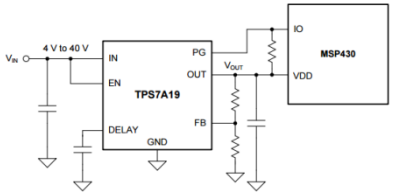
- LDOs dissipate power into heat proportional to the voltage drop from V_{IN} to V_{OUT}
- Heat is concentrated on the board triggering thermal shutdown for other devices

$$Total\ P_{Loss} = ((V_{IN} - V_{OUT}) x\ I_{OUT}) + (I_Q x V_{IN})$$

Low I_Q and EN can help reduce heat dissipation and improve efficiency

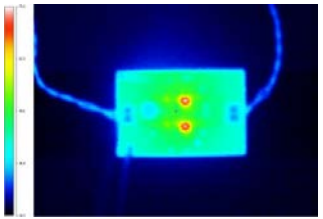
- During no-load conditions LDO power consumption becomes exponentially lower
- The LDO can also be used as a switch powering Ics only when needed

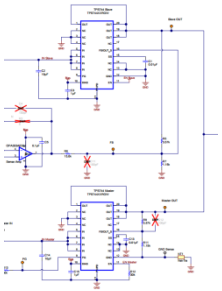
$$P_{LOSS} = I_{SHDN}\ x\ V_{IN}$$



Load/Current sharing can help reduce board heat

- Using two LDOs in parallel can effectively split current and losses
- Heat is better distributed and dropout is lower





*See blog: Double your current with current-sharing dual LDOs

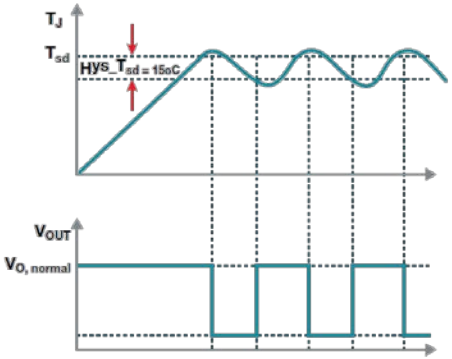
Design Challenges: Thermal Shutdown

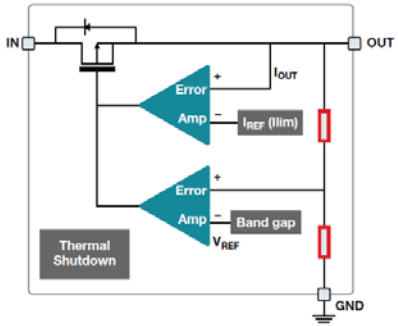
Internal thermal protection saves the LDO

- Choosing an LDO with internal thermal protection helps disable outputs in unusually high demand conditions
- Thermal protection disables the output when the junction temperature rises to approximately 170°C
- When the device cools it will re-enable
- The junction temperature is dependent on the total effect of power dissipated & ambient temperature:

$$T_J = (\emptyset_{JA}\, x\, PD) + TA$$

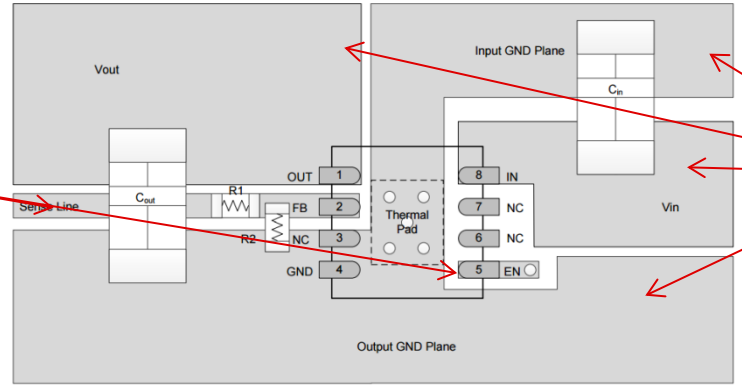
- It is recommended to keep an additional margin to allow for thermal hysteresis to reduce any unwanted shutdowns





Design Challenges: Thermal Layout

Signal path and logic paths can handle smaller traces



Add thick traces for GND, VIN and VOUT planes

A proper layout will improve the LDOs heat, noise and PSRR performance

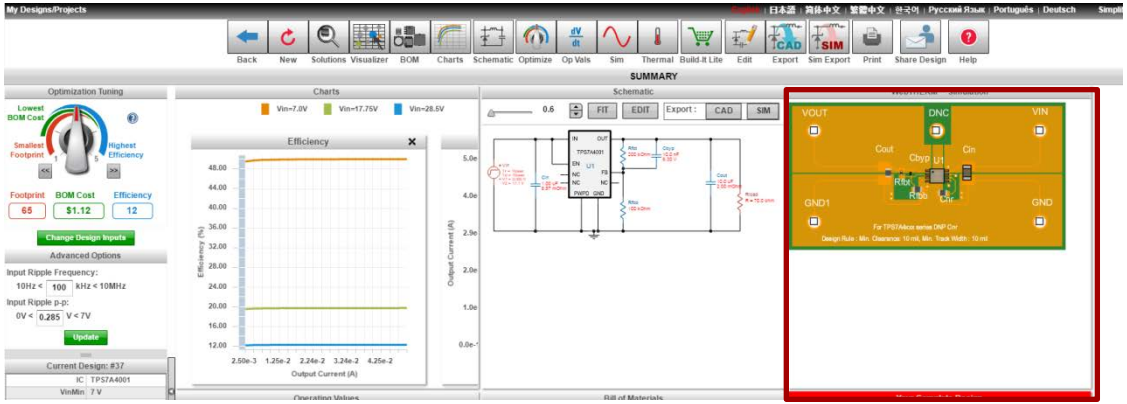
- It is recommended to separate ground planes for IN and OUT to improve noise, PSRR and transient response
- Save room between the LDO and other components to allow better heat dissipation
- Generate as large a GND plane as allowable on the top and bottom layers, especially right near the
- Package
- Gather the same functional pins together in die design, such as for GND, PVIN, POUT

*See app report: A Guide to Board Layout for Best Thermal

Design Tools: WEBENCH® Thermal Simulator

TI's WEBENCH® enables for quick and easy simulation!

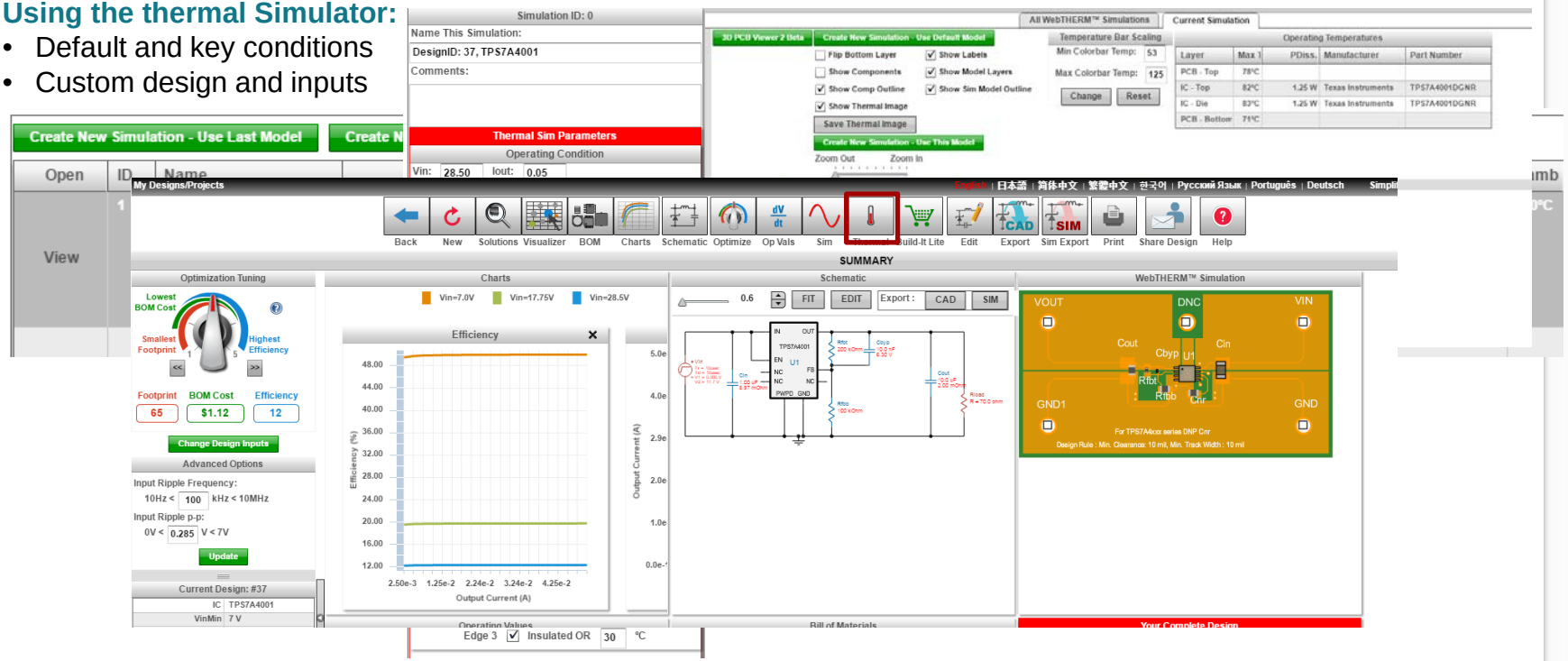
- Design optimization
- Signal simulation
- BOM and schematic editing tools
- Thermal simulation



Design Tools: WEBENCH® Thermal Simulator

Using the thermal Simulator:

- Default and key conditions
- Custom design and inputs



LDO Resources: TI.com, WEBENCH® and More

Find it all on the LDO landing page: ti.com/ldo

Learn

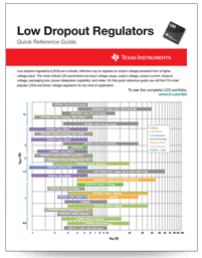
- *Read our LDO Basics blogs to learn more about enhanced features of our LDOs*
- Follow our upcoming LDO training modules for more information

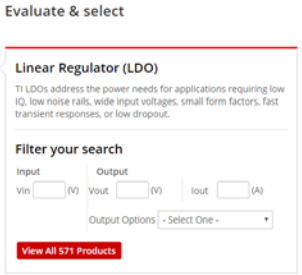
Design

- Leverage our WEBENCH® designer tool, our TI Designs and app notes to improve your system

Select

- Download our latest selection guides and Quick Reference Guide to help you find our latest and greatest LDOs
- Go to our featured products tab where we showcase solutions for LDO design challenges and more





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