

High **VOLT** Interactive

Where power supply design meets collaboration

GaN: the path to high power density

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What will I get out of this session?

- Purpose:

Advantages of LMG3410 Self-Protected GaN Power Stage

A tutorial on PCB layout when using GaN Power Stages to achieve best performance and reliability.

GaN-based CCM Totem-Pole PFC design with 2X power density.

GaN-based 1MHz LLC isolated DC/DC converter design with integrated transformer and 97.6% peak efficiency

- Part numbers mentioned:

- LMG3410
- UCD3138, UCD7138
- UCC28740, UCC27714

- Reference designs mentioned:

- PMP20873
- PMP20637

- Relevant End Equipment:

- Industrial/Telecom/Server

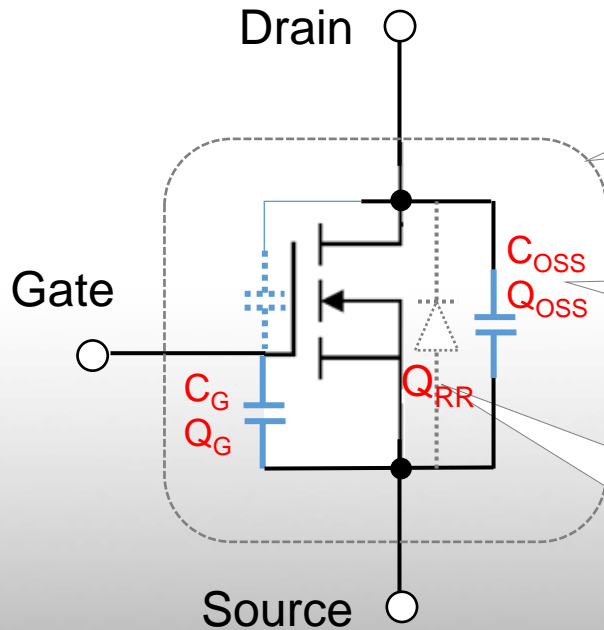
Question #1: Why is GaN so exciting?

- A) It enables 2x Power density of Silicon
- B) It's reliable
- C) You can make your magnetics 6x smaller
- D) All of the above

Agenda

- GaN technology
 - Advantages of GaN FET
 - Why GaN Power Stage?
- System design of LMG3410 half-bridge daughter card
 - Layout and thermal design and trade-offs
- System design of 1kW CCM totem-pole PFC
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 - Magnetics design considerations

GaN FET Advantages



C_G, Q_G Low gate capacitance/charge:

- ✓ faster turn-on and turn-off, higher switching speed
- ✓ reduced gate drive losses

C_{OSS}, Q_{OSS} Low output capacitance/charge:

- ✓ faster switching, high switching frequencies
- ✓ reduced switching losses

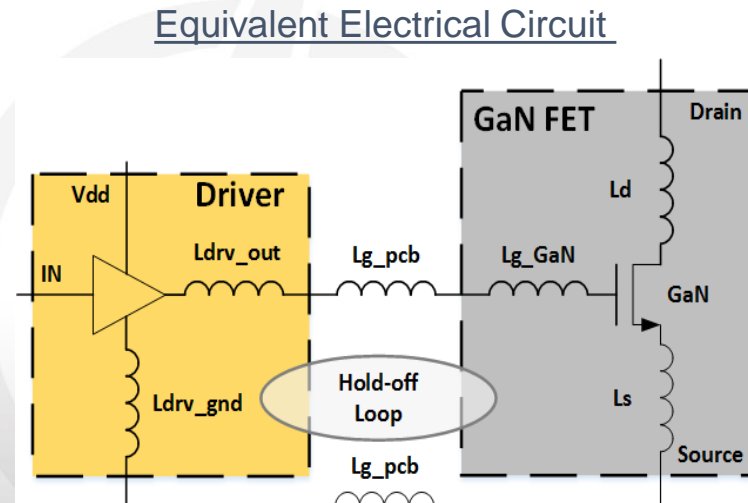
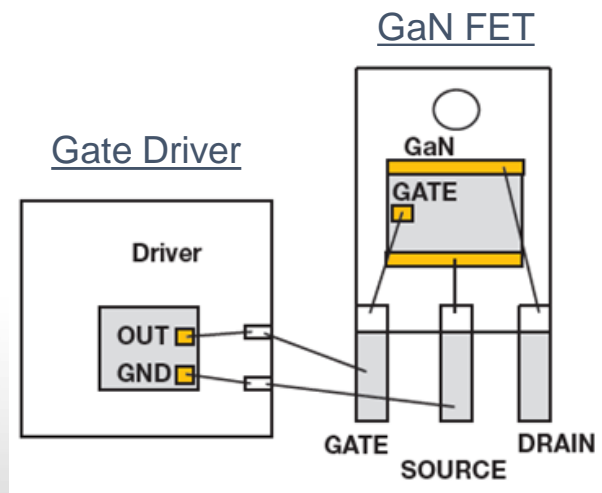
Very fast turn-on/turn-off and low R_{DSON} enables

- ✓ very short dead time, which yields low output voltage distortions
- ✓ lower switching losses

Zero Q_{RR} No 'body diode', zero reverse recovery:

- ✓ Almost eliminate over-/under-shoot and ringing on switch node and hence reduce EMI
- ✓ Smaller over-/under-shoot and ringing increase device reliability

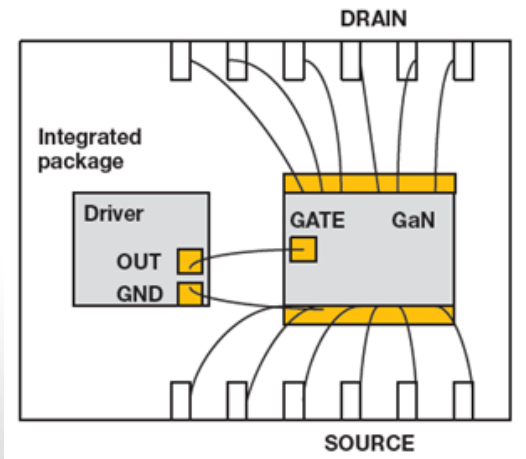
Discrete GaN: Limits System Performance



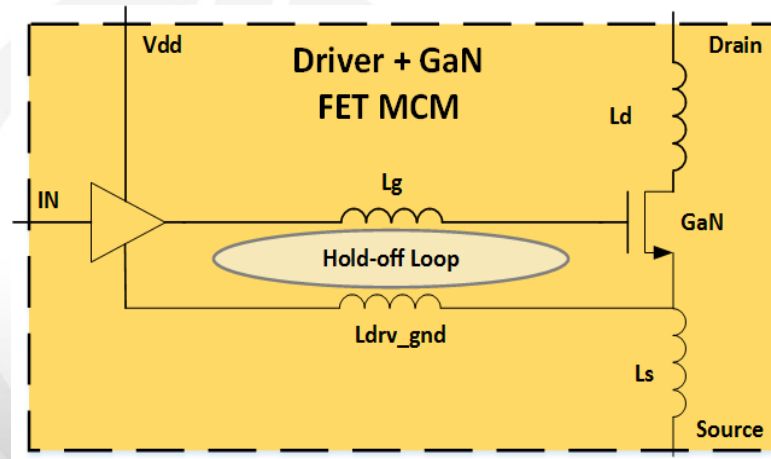
- Parasitic inductances cause switching loss, ringing and reliability issues, especially at higher frequencies
- Why use a solution that limits your system performance?

Integrated Driver: For Best Total Solution

GaN FET/Driver Integrated Package



Equivalent Electrical Circuit



- Integrating the driver eliminates common-source inductance and significantly reduces the inductance between the driver output and GaN gate, as well as the inductance in driver grounding.

TI-GaN Power Stage: LMG3410

Slew rate control by one external resistor: 30 V/ns to 100 V/ns

Digital PWM input

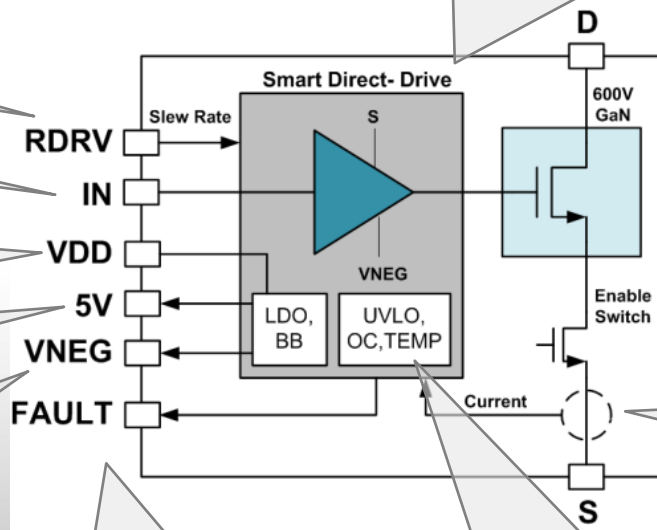
Only +12V unregulated supply needed

Built-in 5V LDO to power external digital Isolator

Integrated gate drive bias supply for reliable GaN switching

Fault feedback to system controller

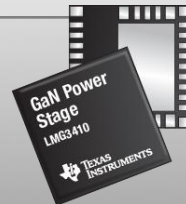
Integrated direct gate driver with zero common source inductance



70mΩ-600V GaN for 12A continuous operation

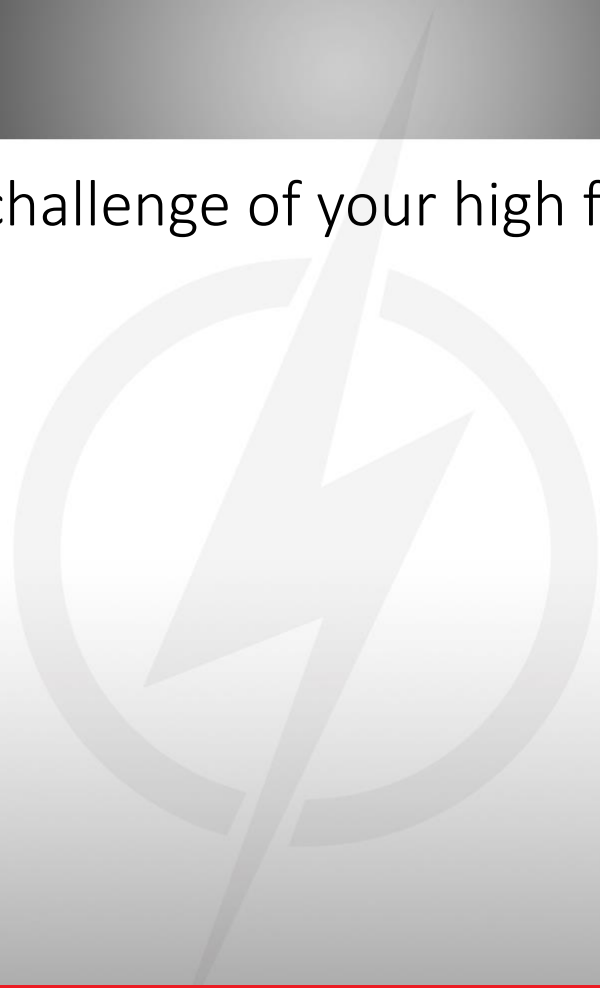
High speed over current protection with 100ns response time

Integrated temperature protection and UVLO



Question #2: What's the biggest challenge of your high frequency power supply design ?

- A) Layout
- B) Magnetics
- C) EMI
- D) Other

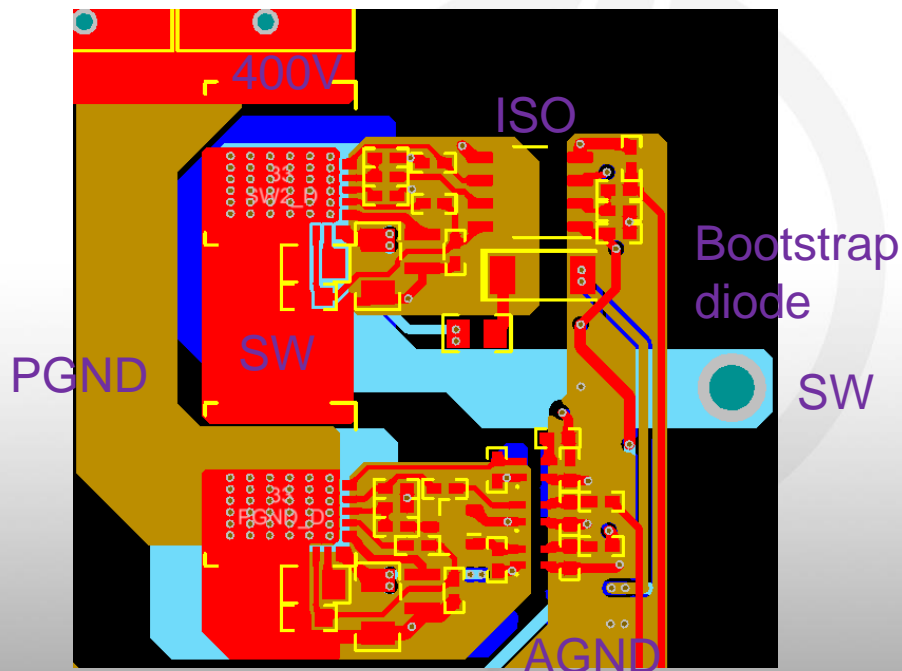


Agenda

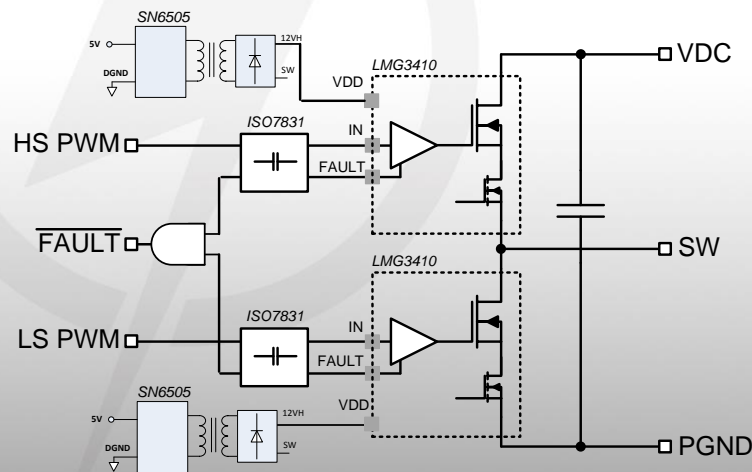
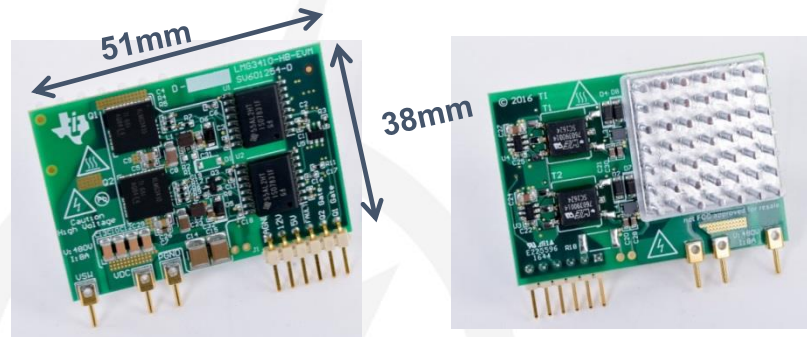
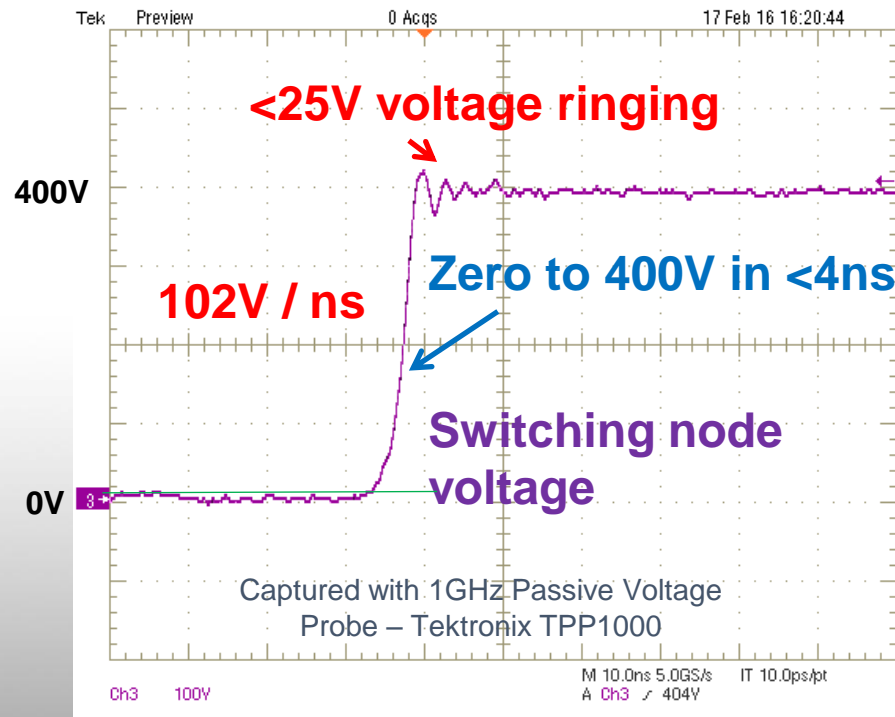
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Question #3: How many places in the layout can be improved?

- A) 2
- B) 3
- C) 4
- D) >4



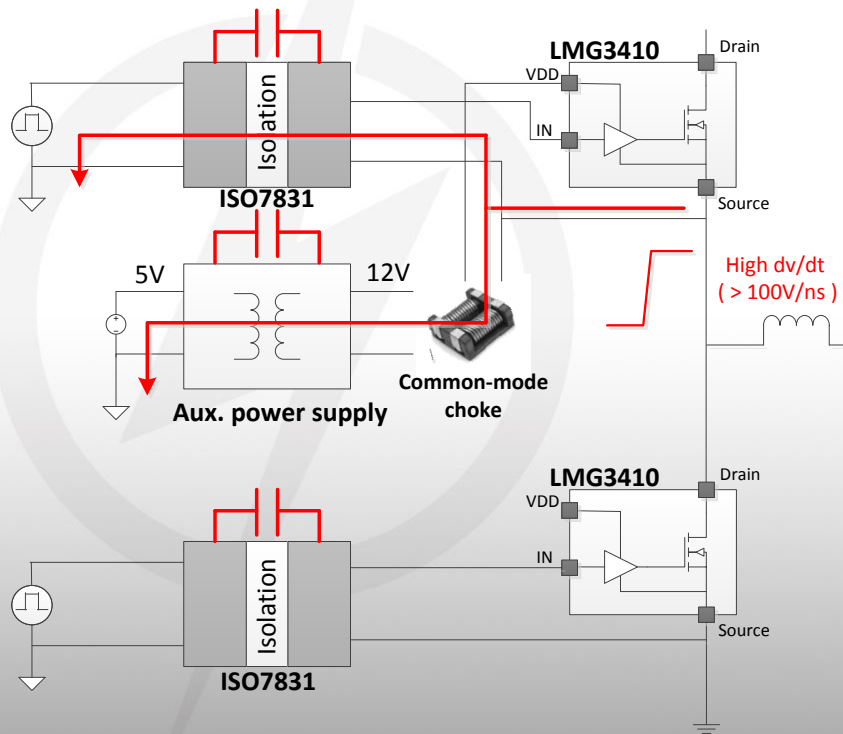
TI-GaN LMG3410-HB-EVM



High Side Level and Power Shifting

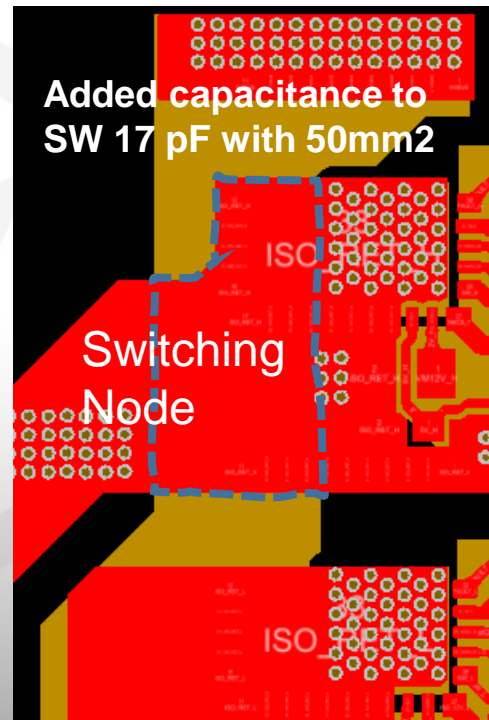
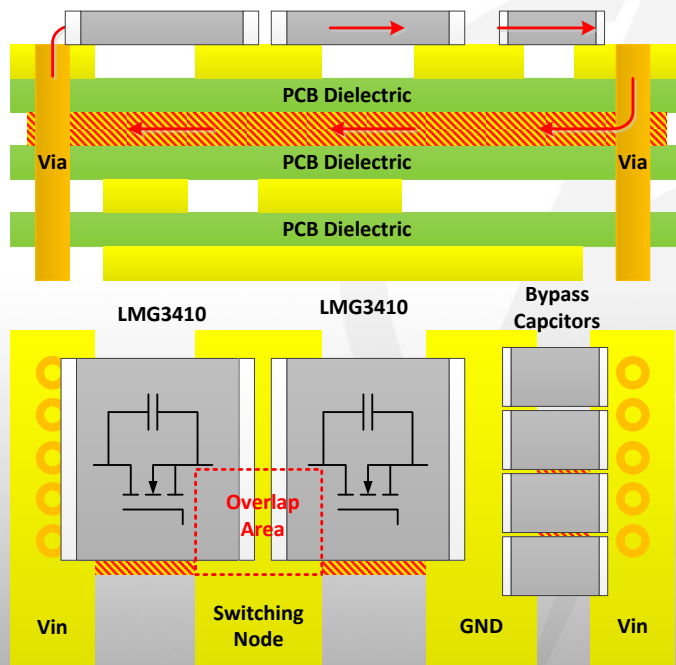
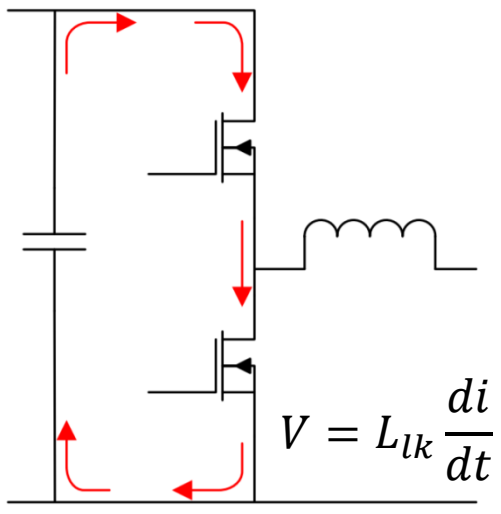
High side device level and power shifting are critical due to high dv/dt ($>100V/ns$)

- Signal level shifting: isolator with high common mode transient immunity (CMTI) are required. ISO7831 is recommended
- High side Aux. power supply: low intra-winding capacitance transformer and extra common-mode choke are recommend to minimize dv/dt noise to digital ground
- Optimize layout to reduce switching node to controller ground capacitive coupling
- Bootstrap: Fast recovery or SiC diode is recommended



Minimize power loop impedance and parasitic capacitance

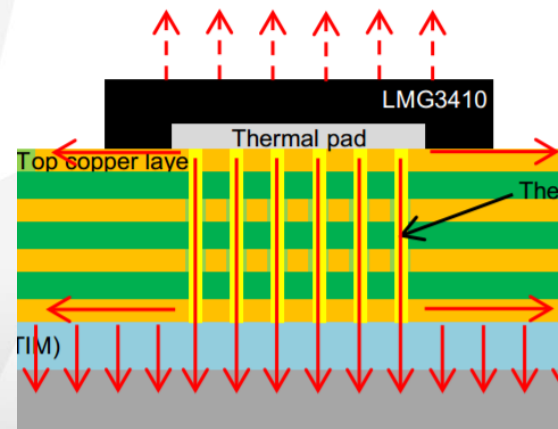
Small Return Path
Minimizes Power Loop
Impedance



Thermal design

- Increase copper thickness (2-3 oz copper)
- Reduced FR4 thickness (5 mil)
- Increase thermal vias numbers and optimized pattern
- Filled thermal vias for better thermal conduction

TIM NAME	MATERIAL	THERMAL PERFORMANCE	ELECTRICAL ISOLATION	ASSEMBLY
Thermal Grease	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in silicone or non-silicone matrix	High	No	Moderate
Phase Change Material	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in phase-change polymer (polyolefin, epoxy, polyesters, or acrylics) Can be laminated on carriers (Al foil, polyimide, or fiberglass) for mechanical or dielectric strength	High	Yes	Difficult
Thermal Gel	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in silicone or non-silicone matrix	Medium	No	Moderate
Adhesive Tape	High-thermal conductivity particles dispersed in silicone or non-silicone matrix and reinforced by glass fiber carrier or PET liner	Low	Yes	Easy
Filled Polymer Pad	High-thermal conductivity particles (Al_2O_3 or BN) dispersed in silicone or non-silicone matrix Reinforced by glass fiber or polyimide film for improved mechanical and dielectric strength	Medium	Yes	Moderate



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Half-bridge hard switching loss calculation

- GaN FET driver losses (high & low-side):

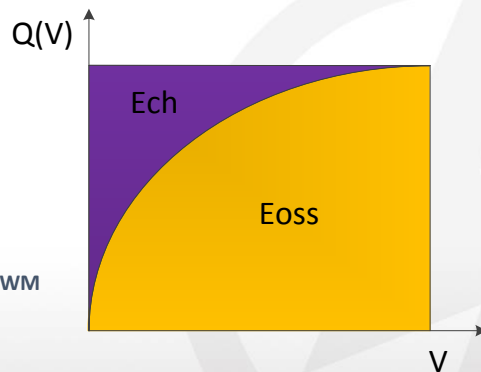
$$P_{GATE} \sim 2 \times Q_G \times V_{DD} \times f_{PWM}$$

- GaN FET (high & low-side)

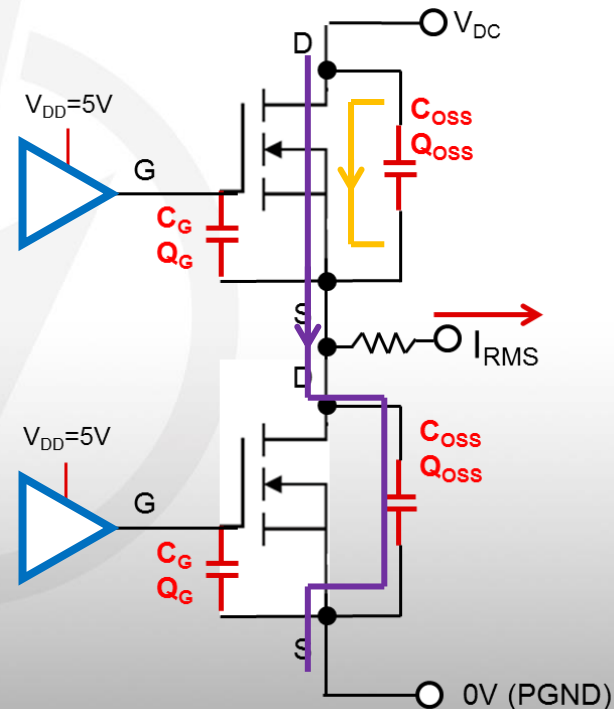
- Conduction losses: $P_{COND} = I_{RMS}^2 \times R_{DSON}$
- Dead time losses: $P_{DB} \sim I_{RMS} \times V_{3Q} \times (t_{DBR} + t_{DBF}) \times f_{PWM}$
- Switching losses: $P_{SW} \sim (I_{RMS} \times V_{DC} \times t_{SW} \times f_{PWM})/2$

$$+ (V_{DC} \times Q_{OSS} \times f_{PWM})$$

$$+ (V_{DC} \times Q_{rr} \times f_{PWM})$$



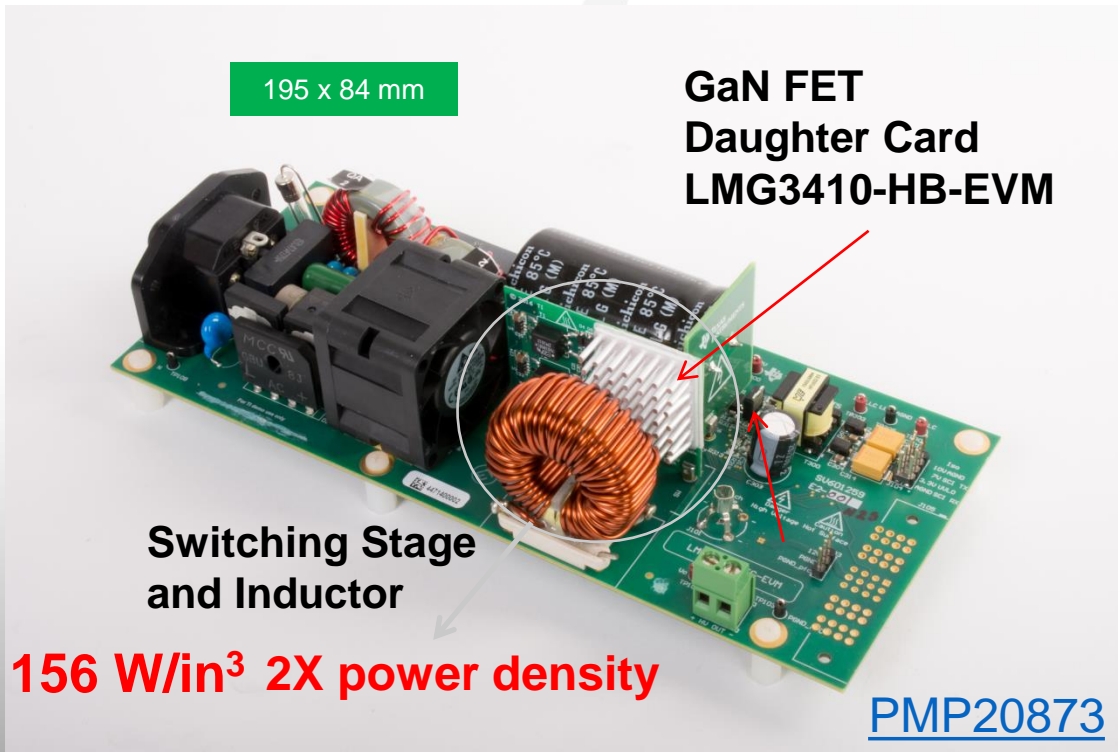
$$E_{OSS} \times f_{PWM} + E_{ch} \times f_{PWM} = V_{DC} \times Q_{OSS} \times f_{PWM}$$



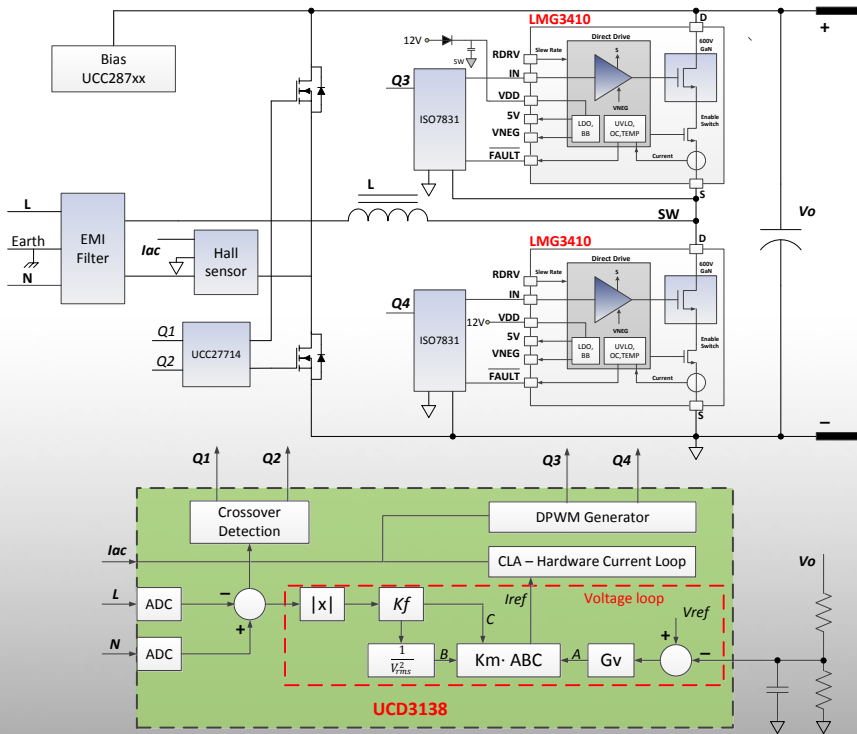
Typical Si FET, Q_{rr} = 2 uC 2 uC * 400V* 100kHz = 80W !

1kW GaN-based Totem-Pole CCM PFC

Parameter	Value
Input Voltage	85 – 265 V _{AC}
Input Frequency	50 – 60 Hz
Output Voltage	385 V _{DC}
Output Power	1 kW
Input Inductance	481 μH
Switching Frequency	100 kHz / 140 kHz
HL Efficiency	99%



Block diagram



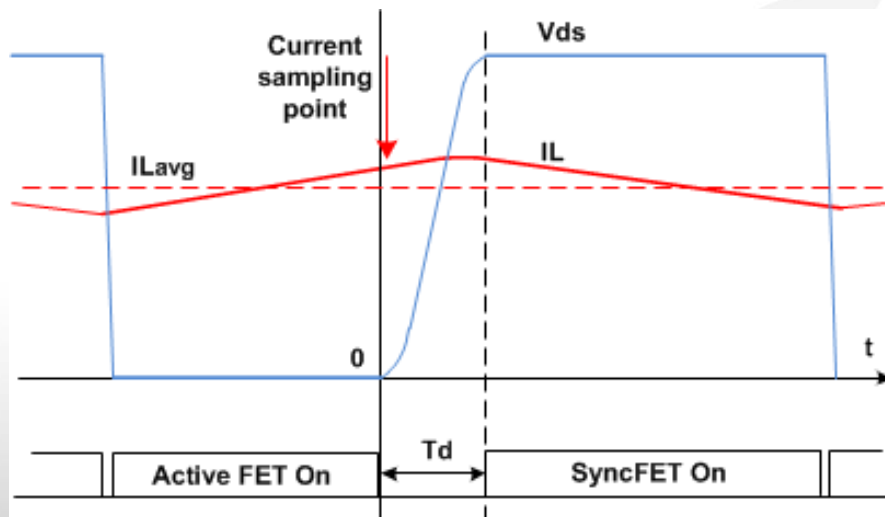
Specifications

- Universal AC line input
- High voltage DC bus output
- 1 kW output across universal input
- Continuous conduction mode

Features

- LMG3410 GaN FET implemented with LMG3410-HB-EVM
- Controlled with UCD3138
 - Highly integrated digital solution offering superior performance
 - Advanced control algorithm
 - Adaptive dead time control
 - Excellent THD and PF

Adaptive Dead-Time Control for SyncFET to Turn On



$$T_d = \frac{2C_{sw} \times V_o}{I_{L_{peak}}}$$

Switching node capacitance = top and bottom device C_{oss_tr} + PCB, heatsink, inductor coupling capacitance
 C_{oss_tr} is equivalent charge-related C_{oss} when V_{ds} changes between 0V and V_o

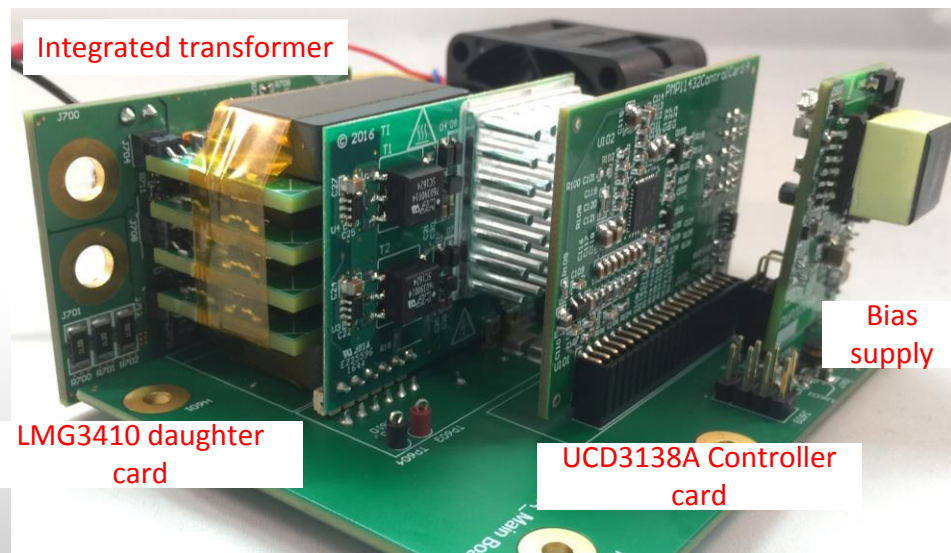
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GaN – A Superior Solution for LLC

- **Reduced Switching Losses**
 - GaN superior switching characteristics significantly reduce gate driver loss and turn-off loss for LLC application
- **Reduced Output Capacitance**
 - Low C_{OSS} reduces dead-time, increasing the time when current delivered to the output
 - Low C_{OSS} allows larger magnetizing inductance and lower circulating current losses as well as transformer fringe-field losses
- **System Optimization**
 - GaN enables higher switching frequency to reduce magnetic components significantly
 - GaN enables LLC converter with higher efficiency and higher power density

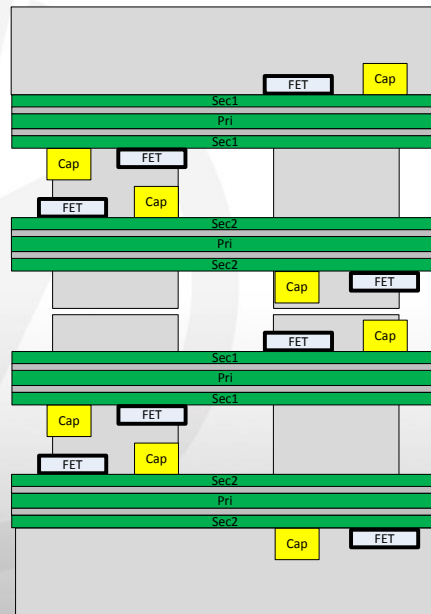
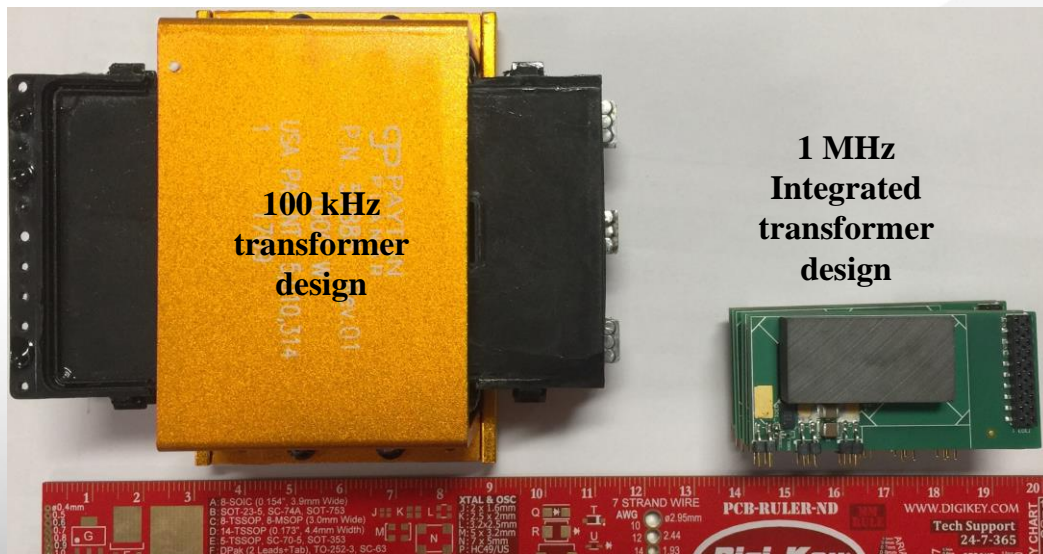
LLC Solution: 1MHz Isolated DCDC Converter



[PMP20637](#)

	Specification
Input voltage (V)	380 ~ 400
Output voltage (V)	48V Nom unregulated
Power (W)	1000
Size (in)	2 x 2.1 x 1.7
Power density (W/in ³)	140 1.5X power density
Peak Efficiency	>97.5% High Efficiency
Switching freq	1 MHz

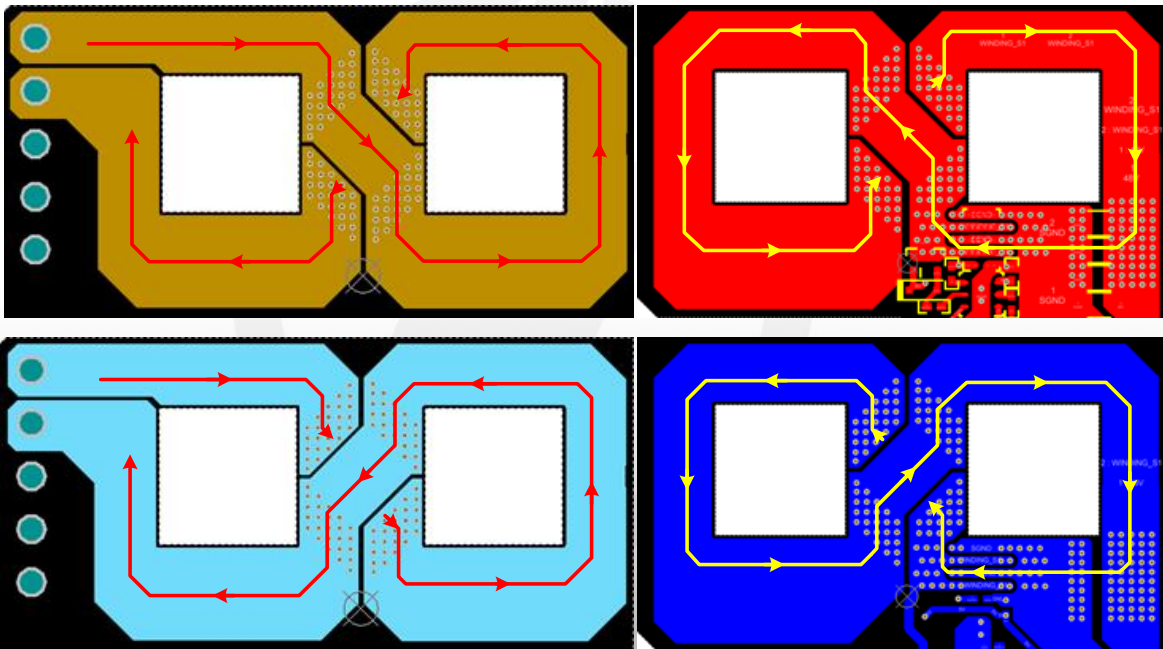
LLC: 1MHz Frequency Shrinks Magnetics

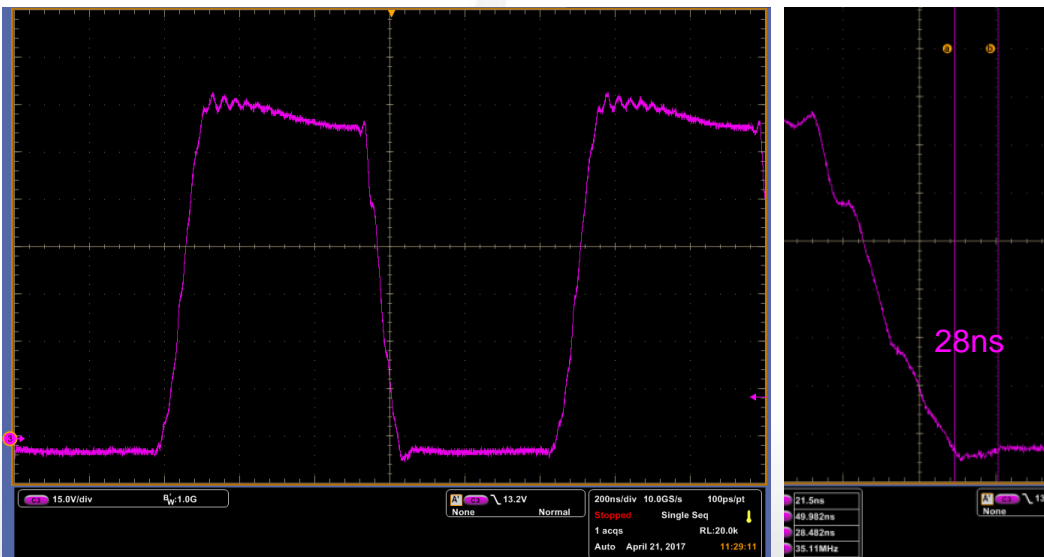
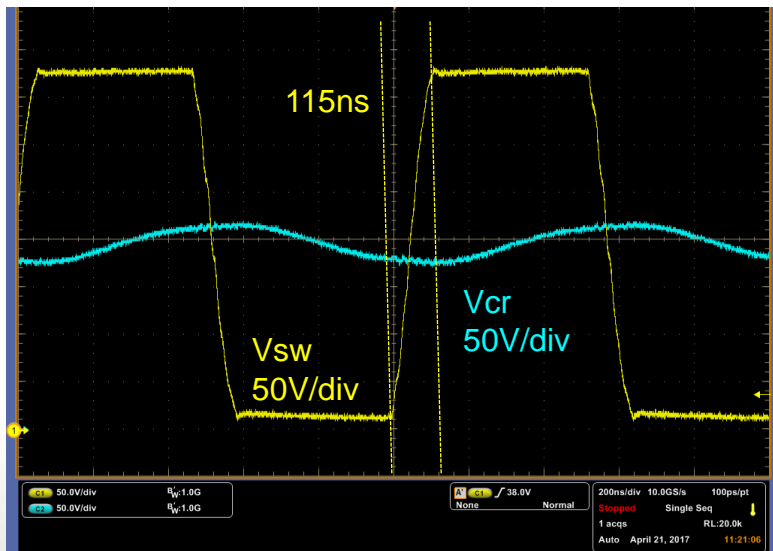


Compared with 100kHz LLC design, the integrated transformer is **6X** smaller

1MHz LLC: Integrated transformer Design Details

- PCB windings integrated with SR FETs & output capacitors for low interconnect and leakage loss
- Interleaved structure for lower winding loss
- “∞” shaped winding structure to achieve high power density
- Better thermal performance





Primary Deadtime for ZVS is small with GaN
3rd quadrant conduction time is minimized by digital controller

SR FET Body diode conduction time is minimized by UCD7138 with UCD3138A

Thank you for your attention!

References for more information:

- 1) Texas Instruments, Gallium Nitride (GaN) Solutions, www.ti.com/gan
- 2) Texas Instruments, LMG3410, 600-V 12-A Single Channel GaN Power Stage, <http://www.ti.com/product/LMG3410>
- 3) Texas Instruments, High Voltage Half Bridge Design Guide for LMG3410, Smart GaN FET, Application Report (SNOA946)
- 4) Texas Instruments, Using the LMG3410-HB-EVM Half-Bridge and LMG34XXBB-EVM Breakout Board EVM, User Guide (SNOU140A)
- 5) Texas Instruments, Optimizing GaN Performance with an Integrated Driver, White Paper (SLYY085)
- 6) Texas Instruments, GaN FET Module Performance Advantage over Silicon, White Paper (SLYY071)
- 7) Texas Instruments, 99% Efficient 1kW GaN-based CCM Totem-pole Power Factor Correction (PFC) Converter Reference Design, TI design (PMP20873)
- 8) Texas Instruments, High Efficiency and High Power Density 1kW Resonant Converter Reference Design with TI HV GaN FET, TI design (PMP20637)



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