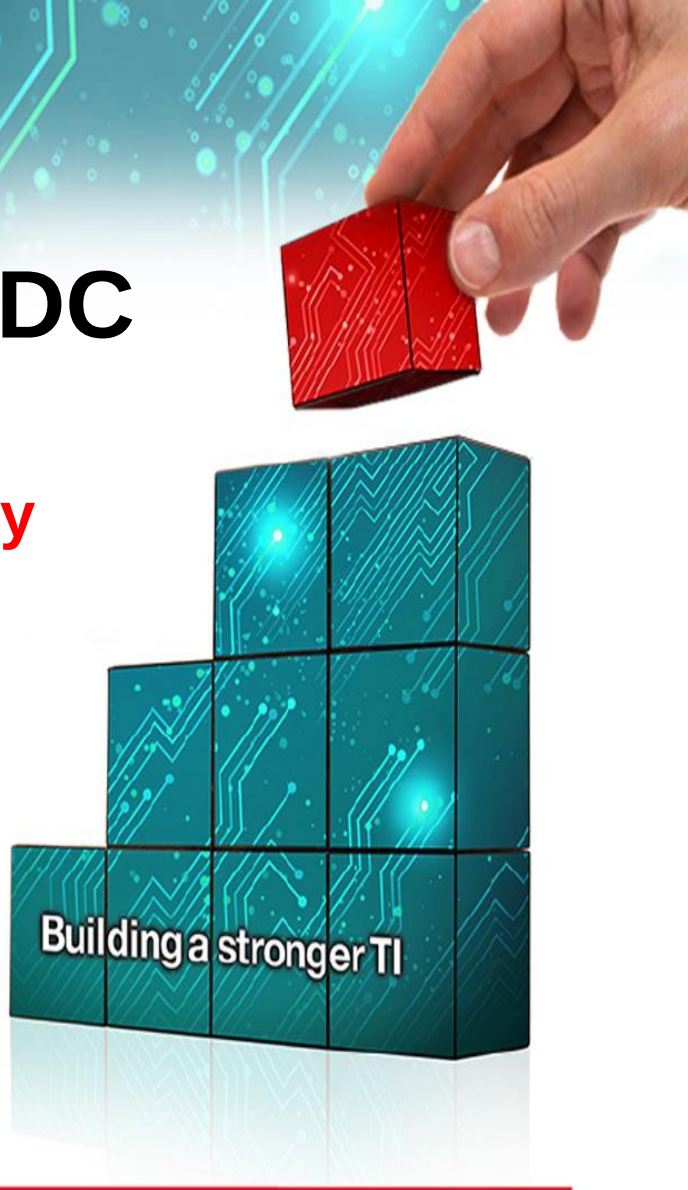
4V-16V/40A Stackable DC/DC Converter TPS543C20

Internal Compensation Fixed Frequency Converter



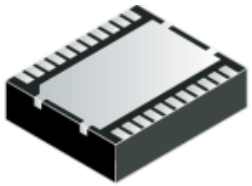
Texas Instruments

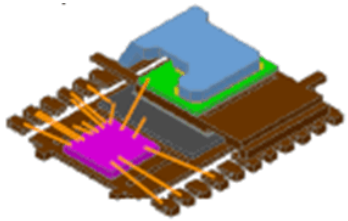
Contents

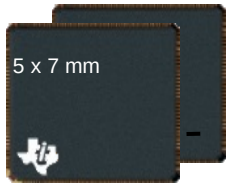
- TPS543C20/B20 Overview
- Integrated Stacked High Current MOSFETs
- Efficiency and Thermal performance
- 2-Phase Stackable Configuration
- Control scheme and loop stability
- Transient performance and Body breaking feature
- Design configuration
- Vout Regulation
- Protection Features

TPS543C20 Stackable DC/DC Converter

Features	Benefits
• Stackable DC/DC Converter • Output Voltage Range 0.6V to 5.5V • ACM Fixed Frequency with CLK Sync	• Power ASICs and System Rails • No External Compensation
• Fully Differential Remote Voltage Sense	• +/-0.5% 1Vref accuracy over temp
• Fsw: 300KHz to 2MHz (1Ph) 300KHz to 1MHz (2--Ph) • 10 Vref choices: 0.6V to 1.1V • 10 SS choices: 0.5, 1, 2, 4, 5, 8, 12, 16, 24, 32ms	• Easy to optimize for efficiency and BOM size • Flexible Design for multiple Vouts • Flexible Design for startup timing option
• High accuracy Over Current Limit (Hiccup Ilim)	• +/-10% Ilim Accuracy over temp & process • Option to better manage undershoot/ overshoot
• Asynchronous Pulse Injection (API)/ Body Braking Features • 5x7x1.5mm, 0.5mm pitch 40Ld Stacked Clip QFN • Stackable DC/DC Converter	• High density & Easy Layout w/ single GND pad

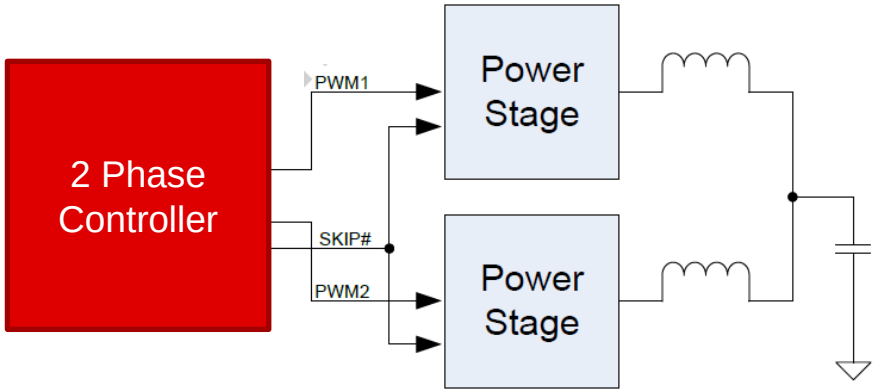




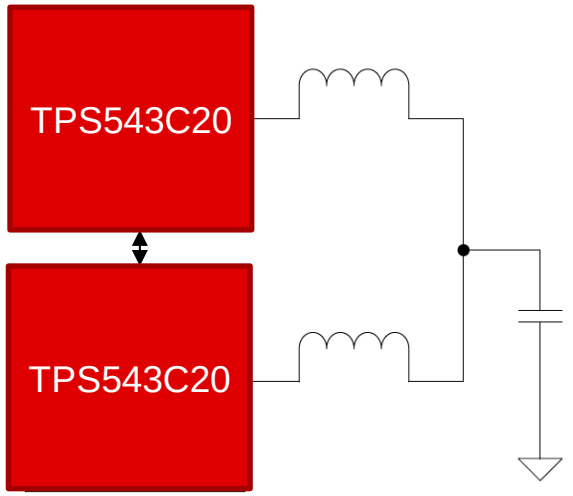


2-Phase Stackable: 2x the output current

Traditional 2-Phase DC/DC

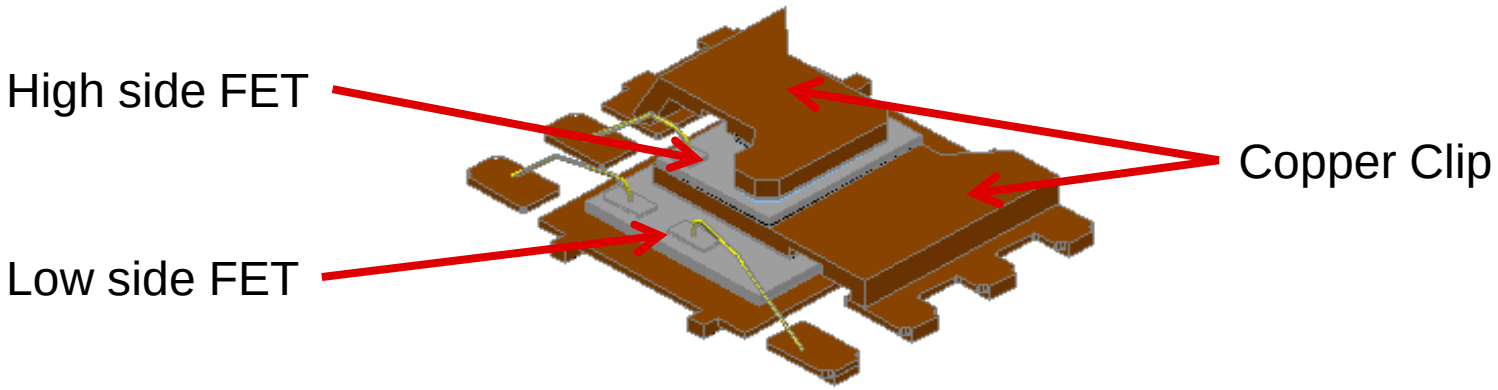


Advanced 2-Phase stackable DC/DC

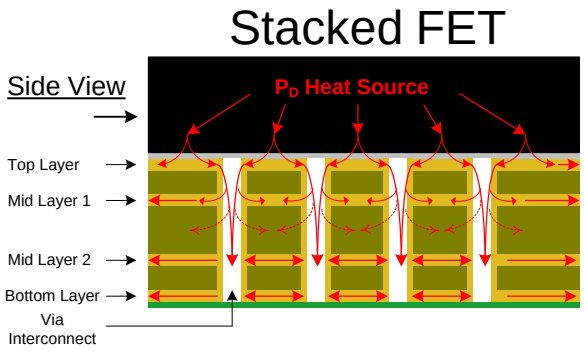


Integrated Stacked High Current MOSFETs

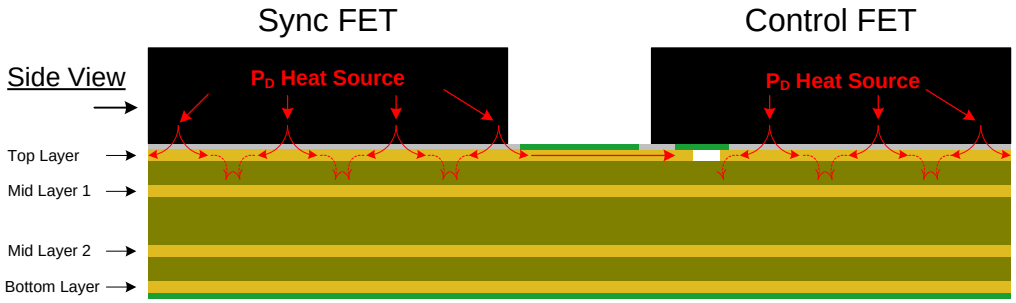
Device	Output Current	Vin Range	Rdson	Stackable
TPS543C20	40A	4V to 16V	UF: 3mΩ LF: 0.9mΩ Included Clip metal 20V FET	Yes-2PH
TPS543B20	25A	4V to 19V	UF: 4.1mΩ LF: 1.9mΩ Included Clip metal 25V FET	No



Grounded Thermal Advantage



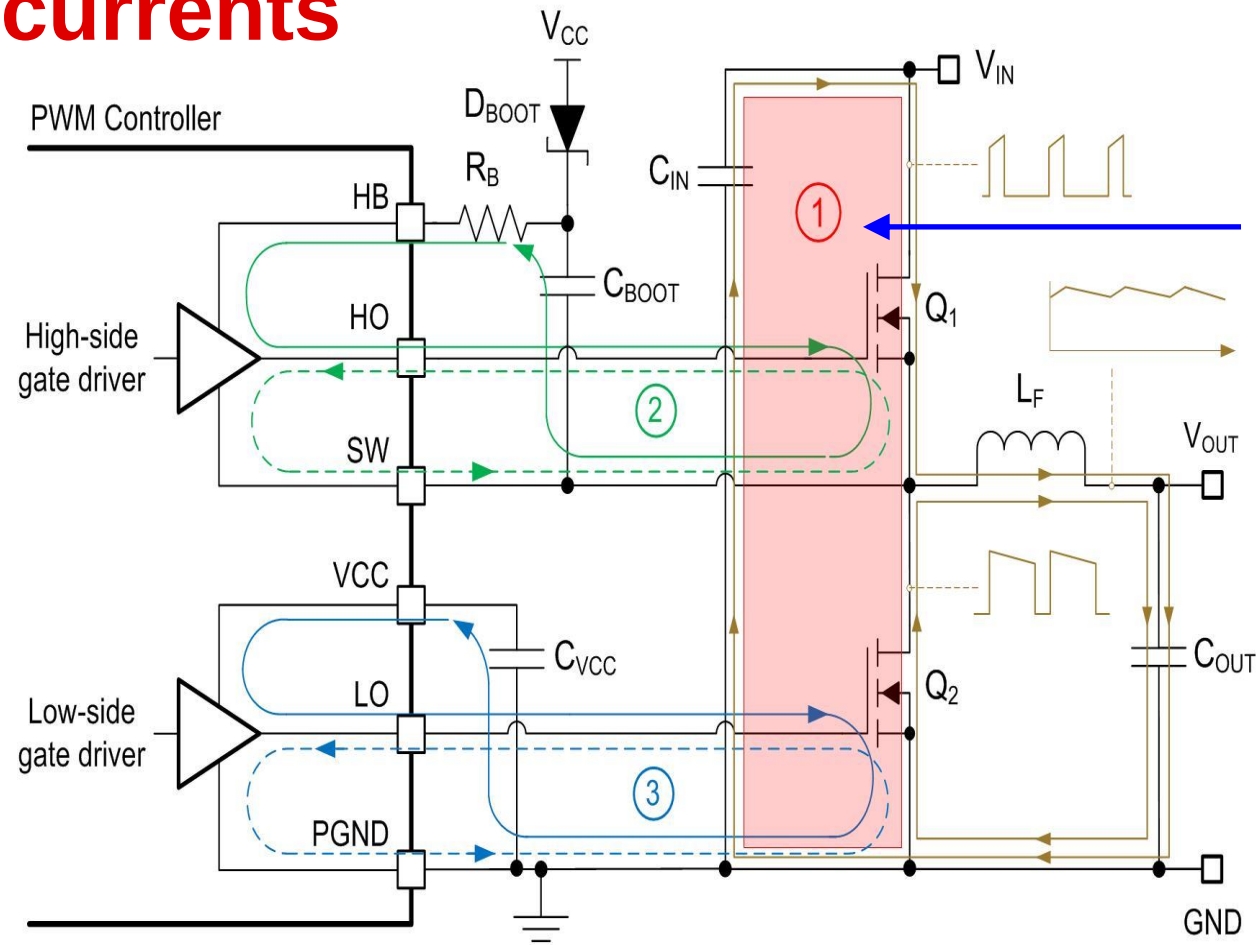
Abundant GND layers typical in all systems. PCB surface area helps dissipate heat.



Discrete & DrMOS solutions create localized hot spots!
DrMOS is Like Co-Packaged /Smaller Discrete Design

TI Can Use Ground Planes to Dissipate Heat More Effectively and Run Cooler Even if there is Similar Power Loss

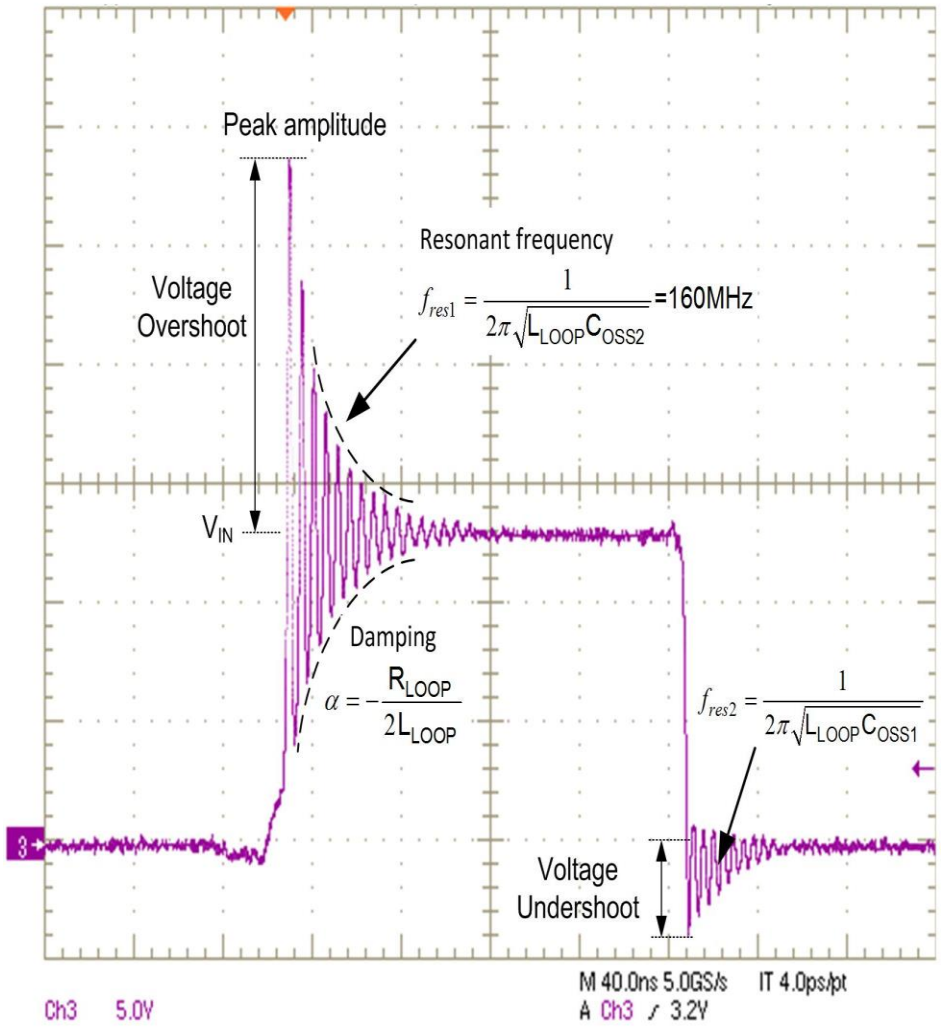
Identify critical loops with high di/dt currents



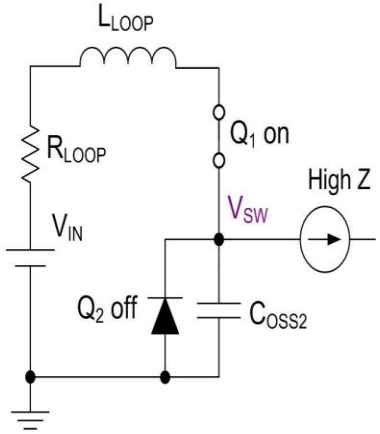
High frequency "power loop"
…critical path area reduction

In translating a converter schematic to a board layout, it's essential to pinpoint the high slew-rate current (**high di/dt**) **loops** to recognize the layout-induced **parasitic or stray inductances** that cause excessive **noise, overshoot, ringing and ground bounce**

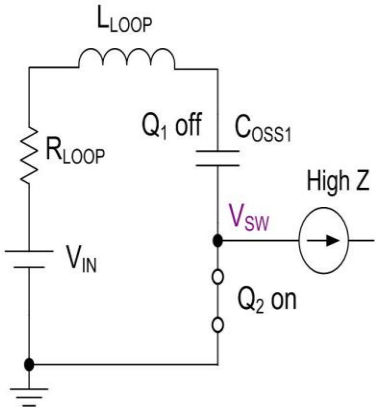
Equivalent RLC circuits for SW node ringing – buck



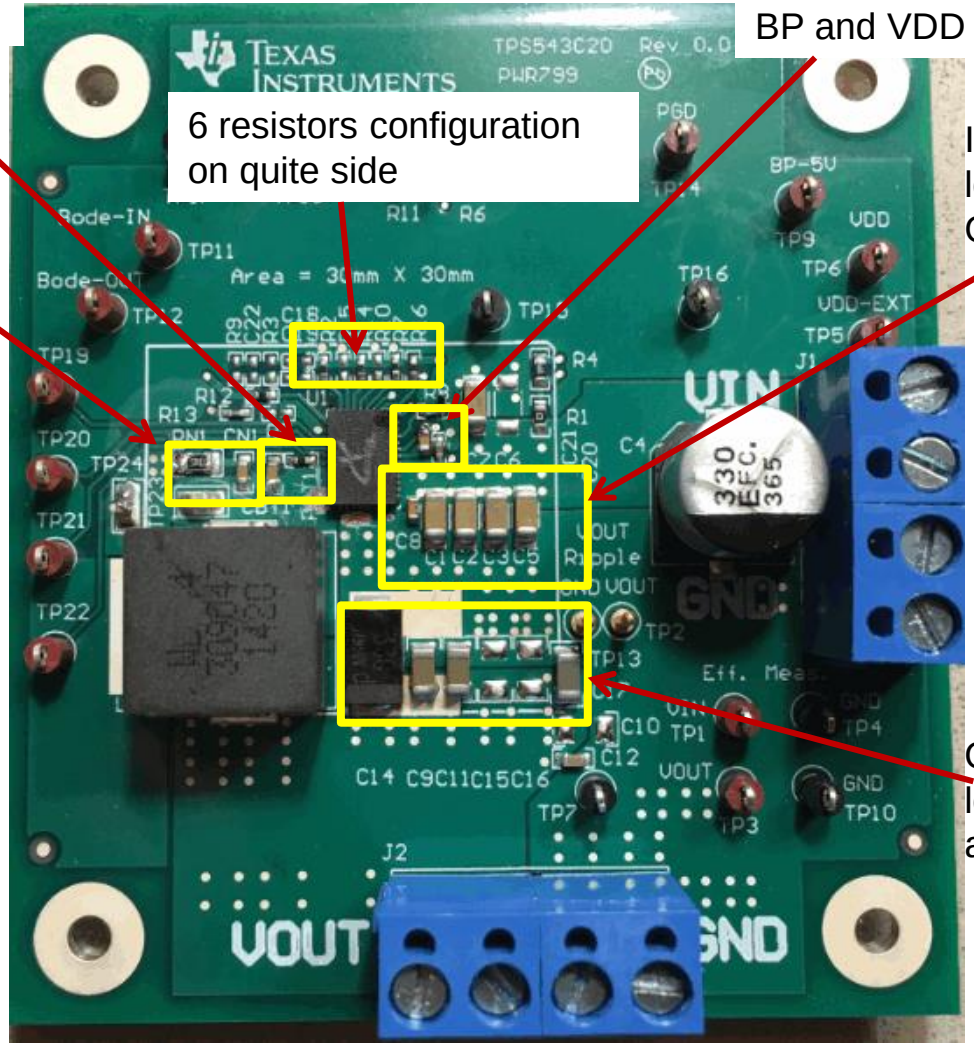
Equivalent RLC circuit after Q_1 turns **ON**



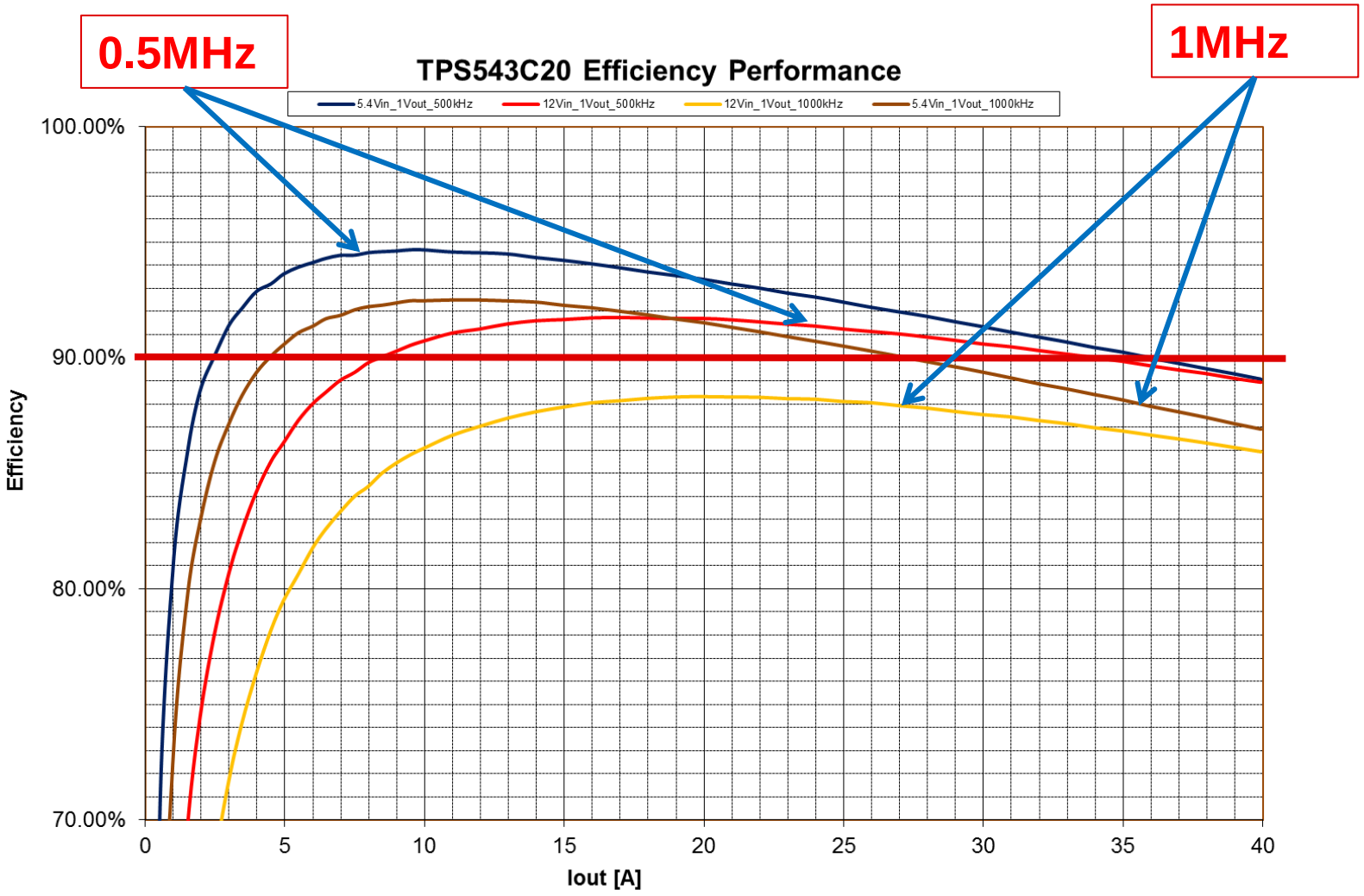
Equivalent RLC circuit after Q_1 turns **OFF**



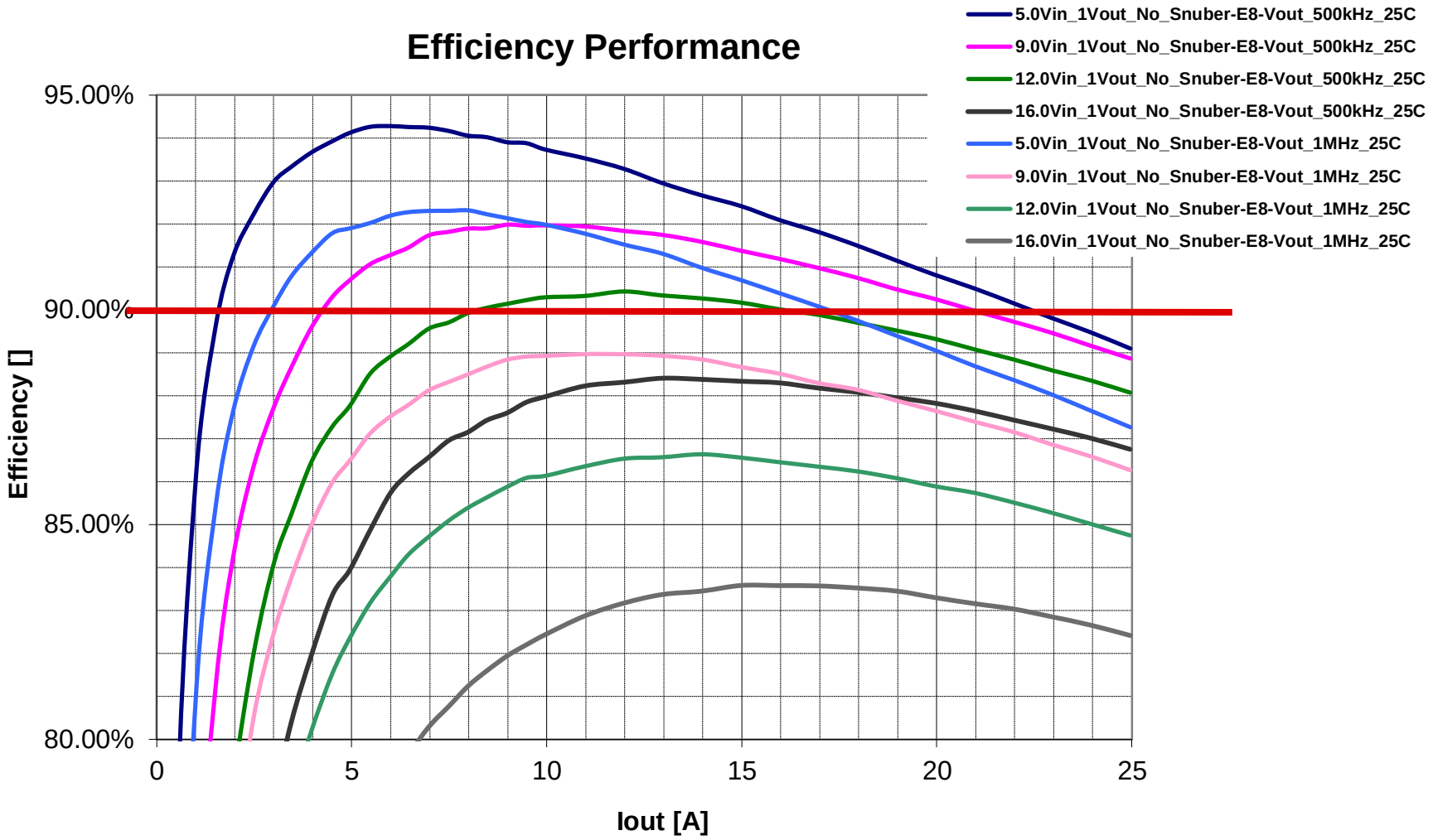
Total Solution Area: 30 x 30mm



TPS543C20 Efficiency: 1Vout@ 5.4-12Vin

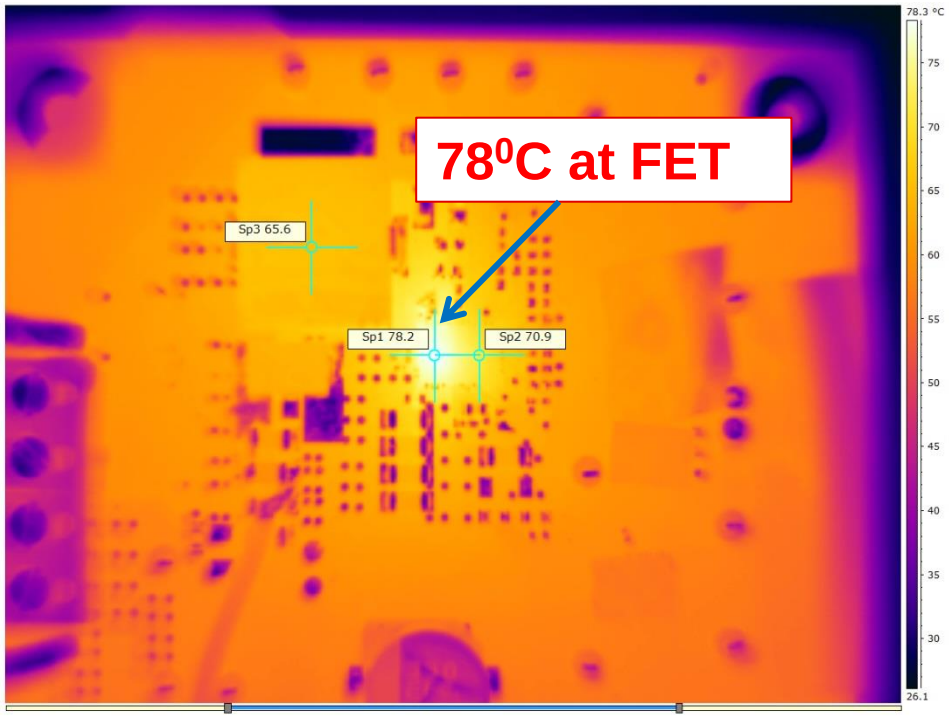


TPS543B20 Efficiency: 1Vout@ 5.0-16Vin with Fsw at 0.5MHz and 1MHz



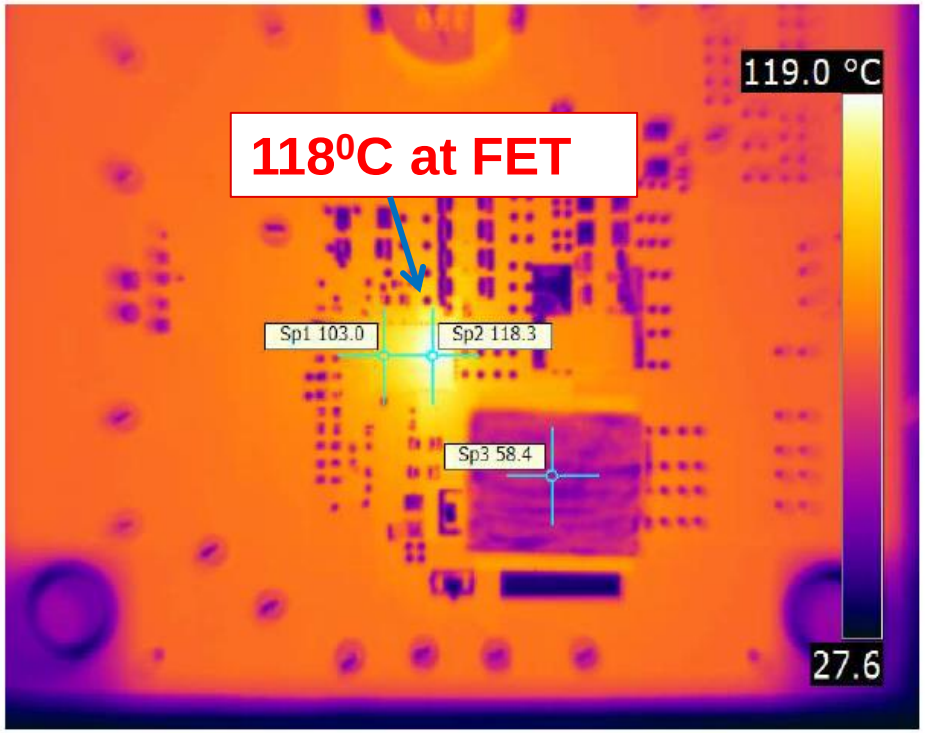
TPS543C20 Thermal Performance

IOUT = 40A



VIN = 12V, Vout=0.9V, Fsw=500kHz,

IOUT = 40A

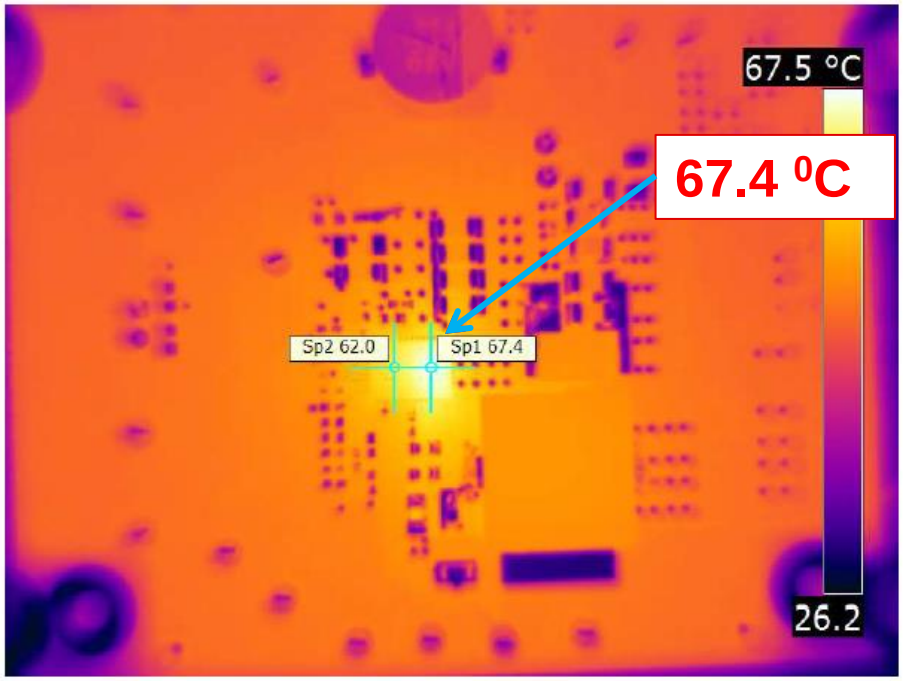


VIN = 12V, Vout=5V, Fsw=500kHz,

Thermal Equilibrium: 10 mins

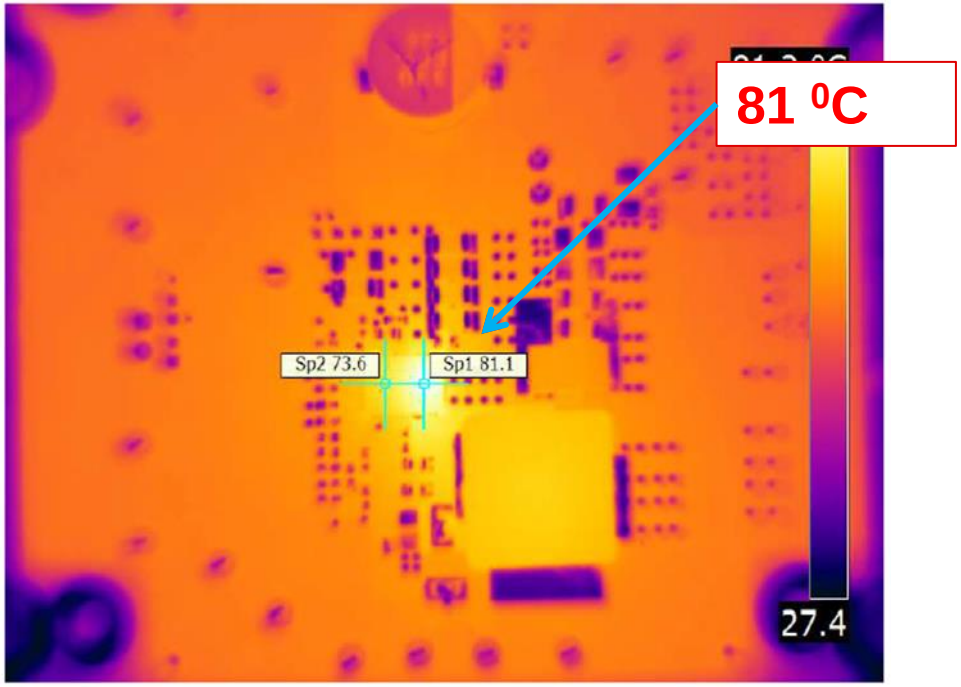
TPS543B20 Thermal Performance

IOUT = 25A



VIN = 12V, Vout=1V, fsw=500kHz

IOUT = 25A

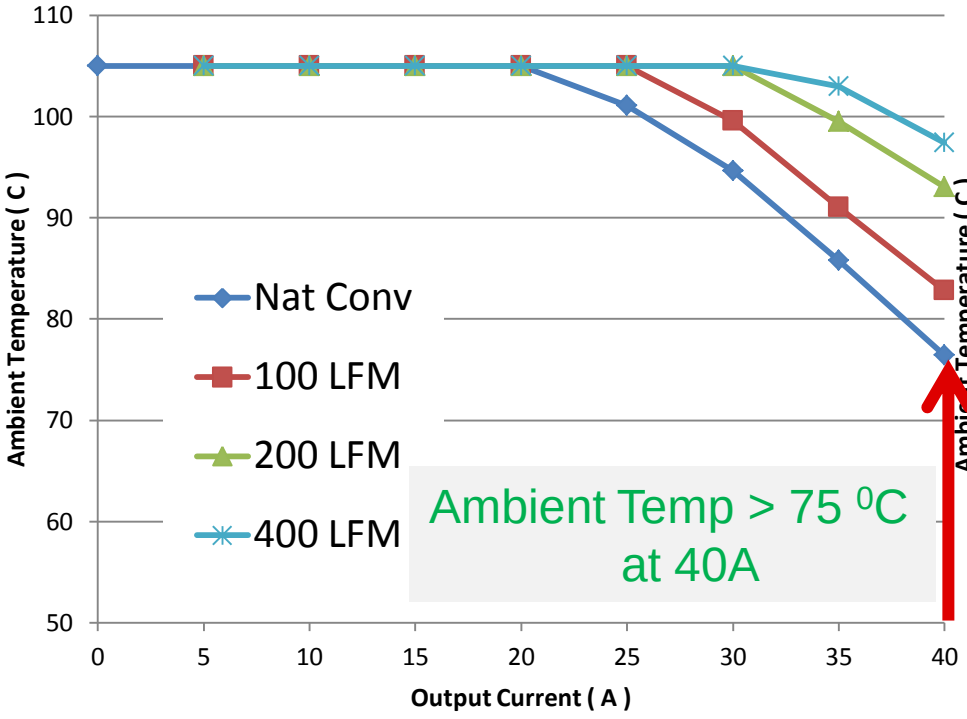


VIN = 12V, Vout=5V, fsw=500kHz

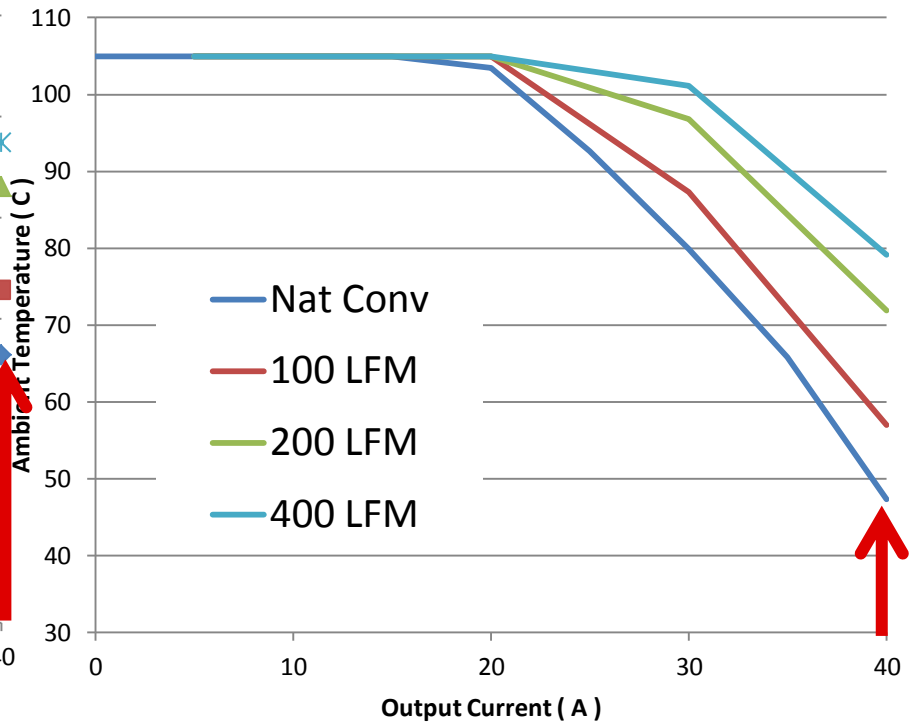
Thermal Equilibrium: 10 mins

Safe Operating Area: TPS543C20

TPS543C20 SOA: 12Vin, 1.0Vout, 500kHz



TPS543C20 SOA: 12Vin, 5.0Vout, 500kHz

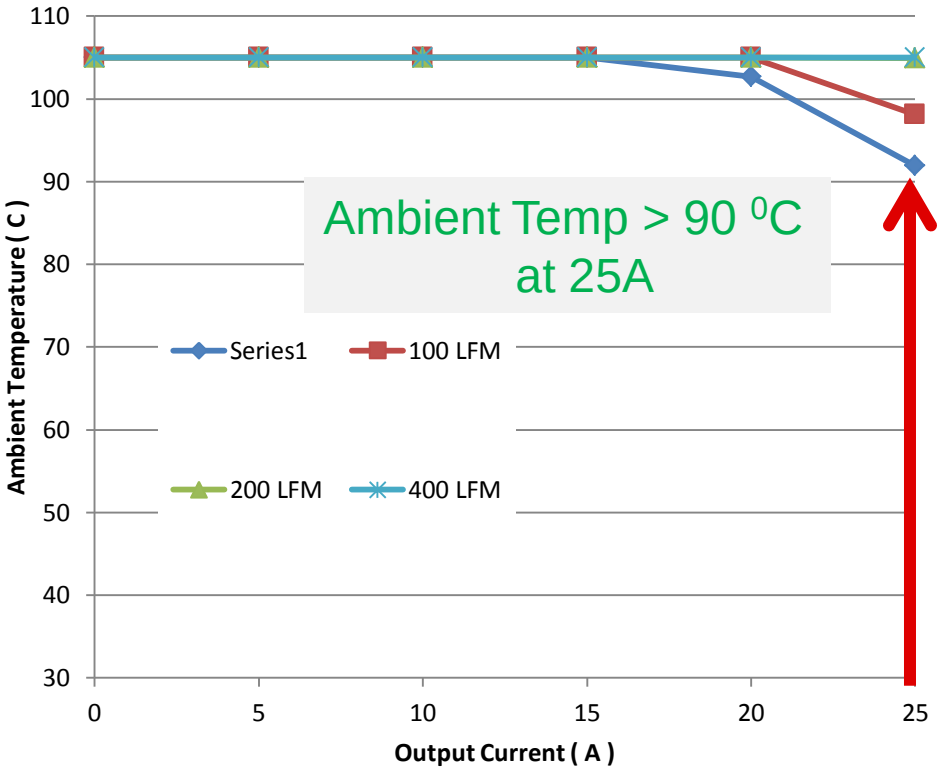


Note: The Tj = 125 ^{0}C for all data point
For more information of SOA:
http://www.ti.com/lit/an/slva766/slva766.pdf

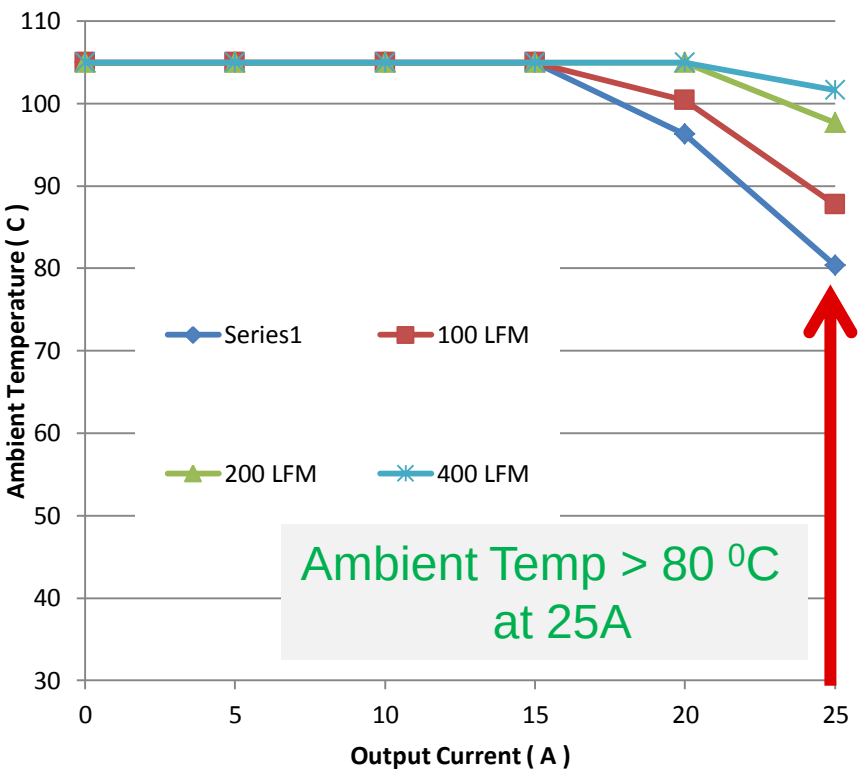
Ambient Temp > 47 ^{0}C
at 40A

Safe Operating Area: TPS543B20

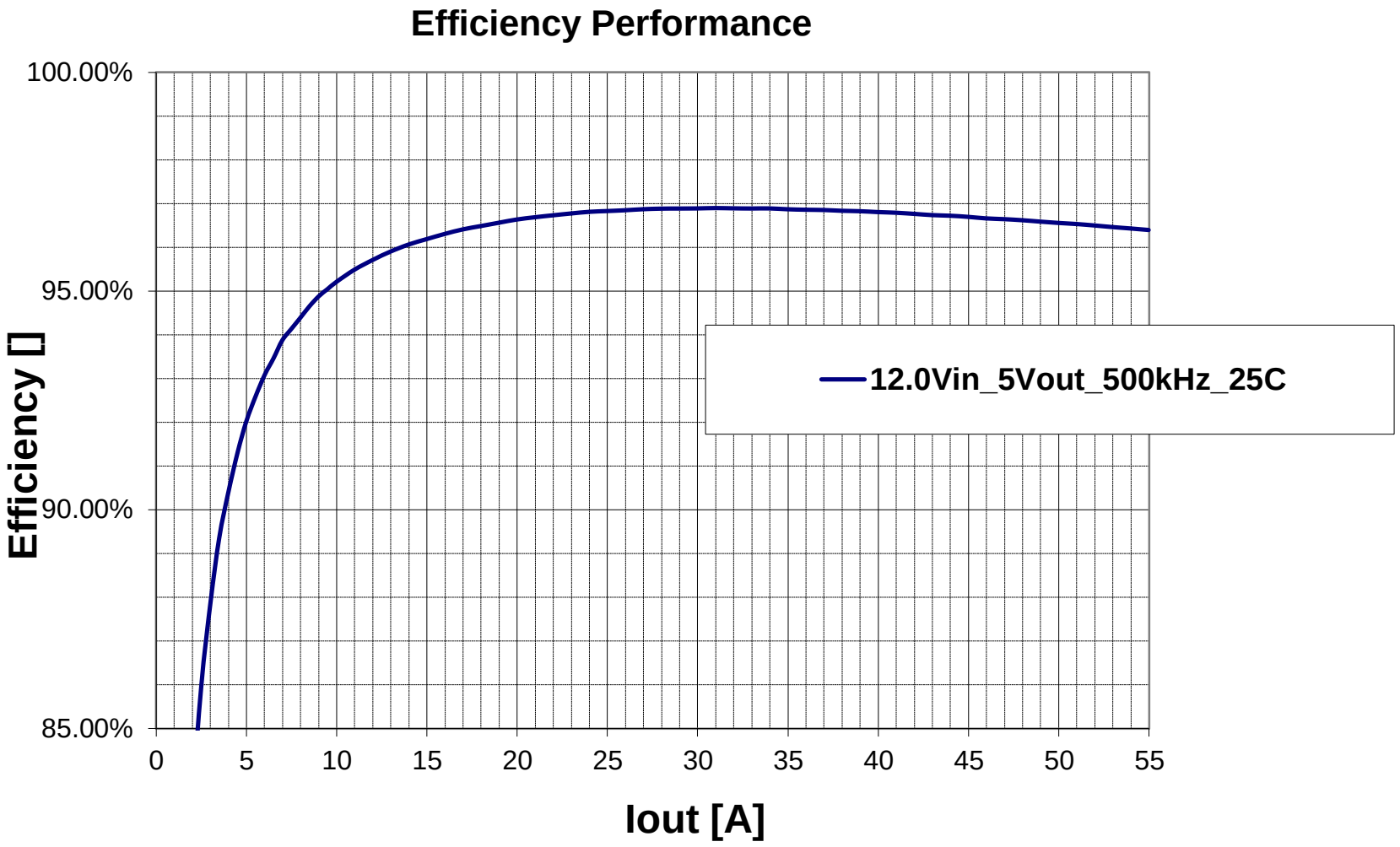
TPS543B20 SOA: 12Vin, 1.0Vout, 500kHz



TPS543B20 SOA: 12Vin, 5.0Vout, 500kHz



2-Phase Stackable Efficiency: 275Watts Output



2-Phase Stackable Thermal: 275Watts Output

76.9 ^{0} C

78.4 ^{0} C

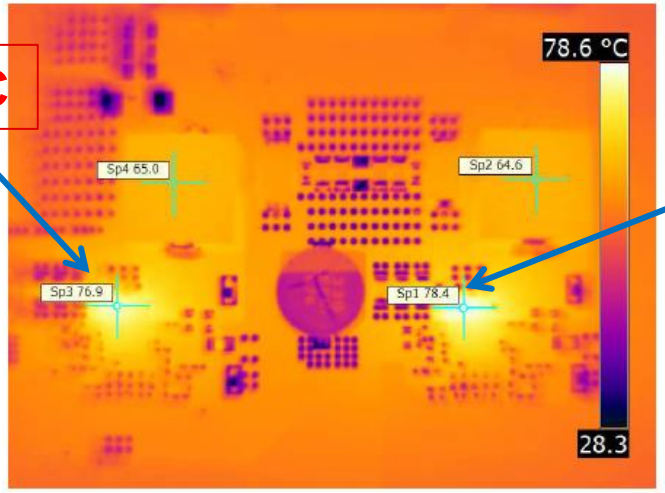


Image and Object Parameters	
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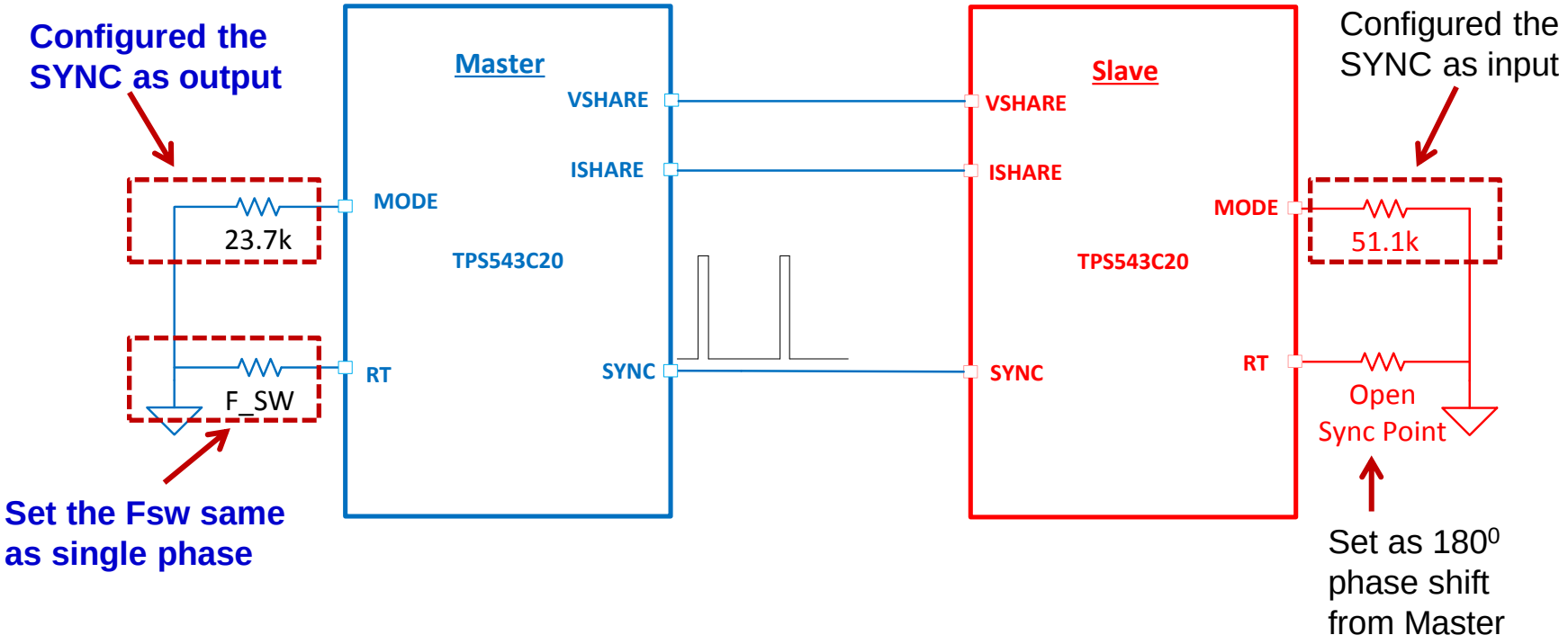
Image Date	11/9/2016 11:35:06 PM
Image Name	IR_0208.jpg
Emissivity	0.95
Reflected apparent temperature	20.0 °C
Object Distance	1.0 ft

Text Comments	
Sp1=IC1	78.4C
Sp2=Inductor1	64.6C
Sp3=IC2	76.9C
Sp4=Inductor2	65C

Description
Vin=12V, Vout=5V, Iout=55A, Fsw=500kHz, Ta=room

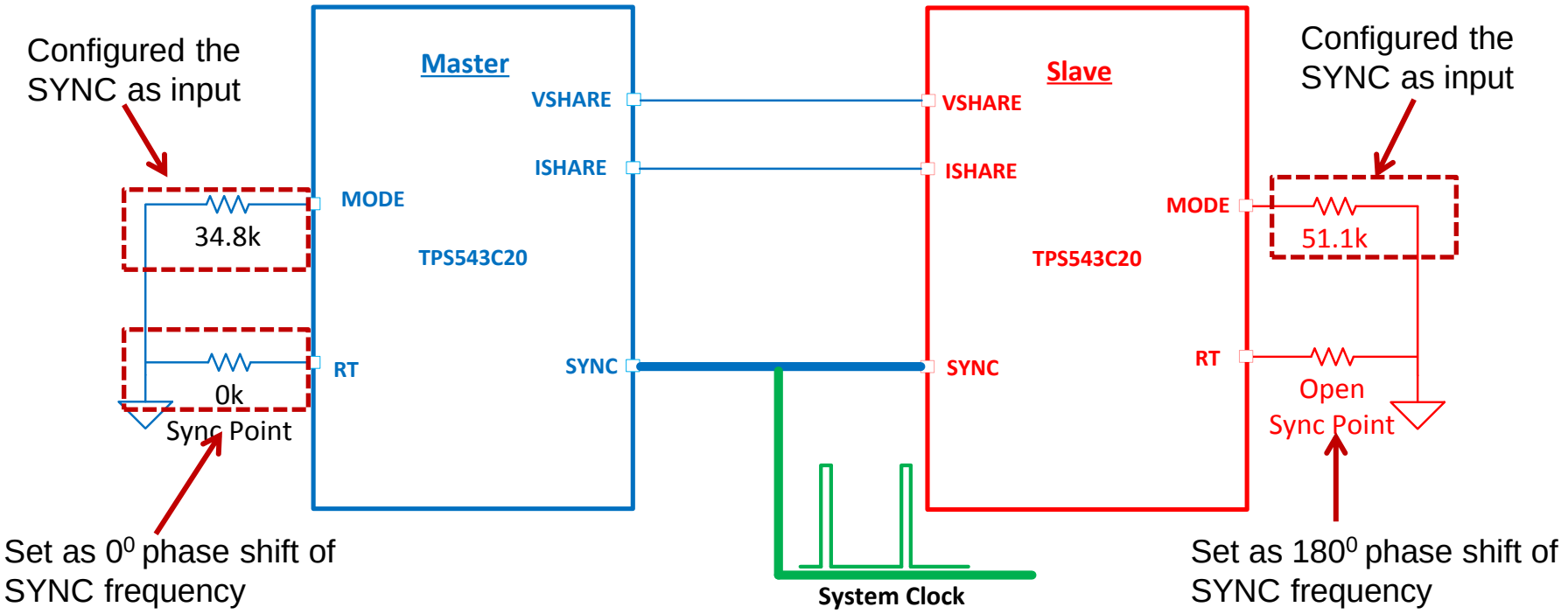
Stackable Operation 1:

- Direct SYNC, VSHARE and ISHARE connections between Master and Slave.
- Switching frequency is set by RT pin of Master, and pass to slave through SYNC pin. SYNC pin of master will be configured as sync out by it's MODE pin.
- Slave receives clock from SYNC pin. It's RT pin determines the sync point for clock phase shift.

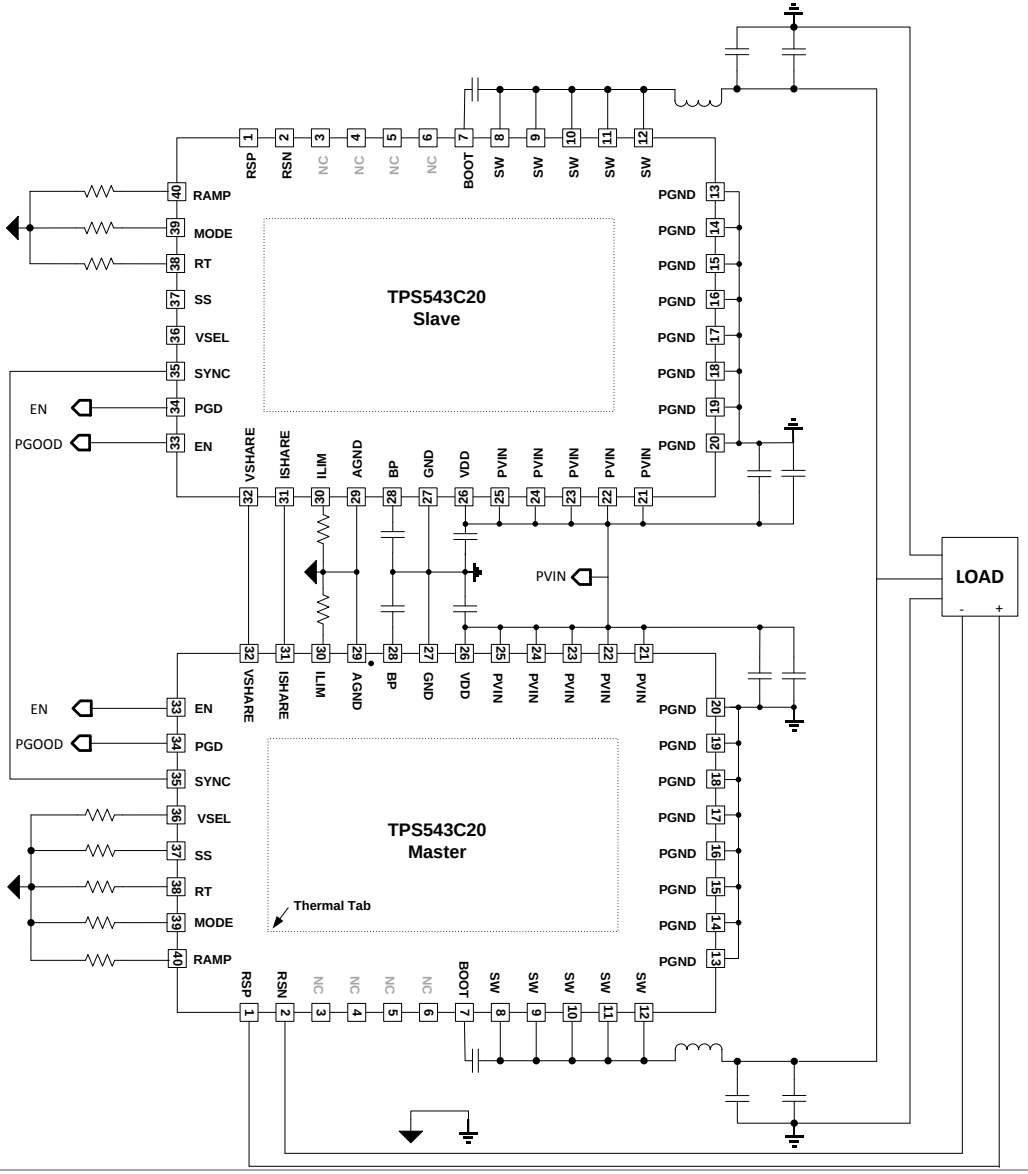


Stackable Operation 2

- Direct connection between external clock and SYNC pin of Master and Slave.
- Direct VSHARE and ISHARE connections between Master and Slave.
- SYNC pin of master will be configured as sync in by it's MODE pin.
- Master and Slave receive external system clock from SYNC pin. Their RT pin determine the sync point for clock phase shift.

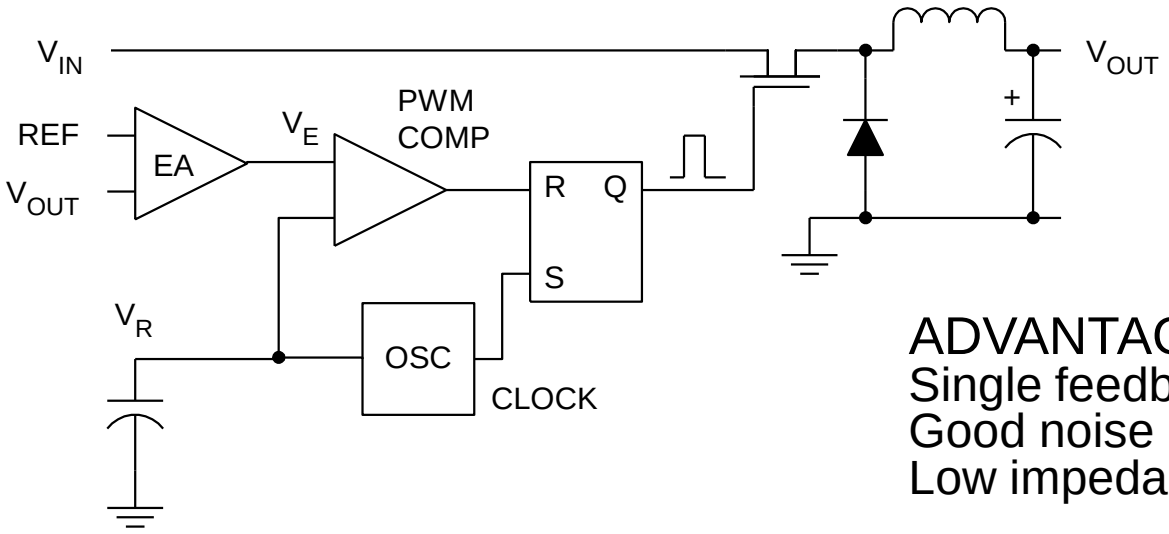


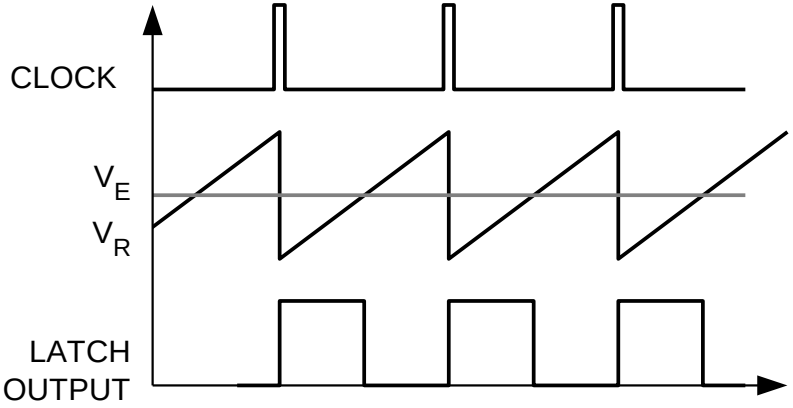
2-Phase Stackable DC/DC schematic



Control Loop Topologies

Voltage Mode



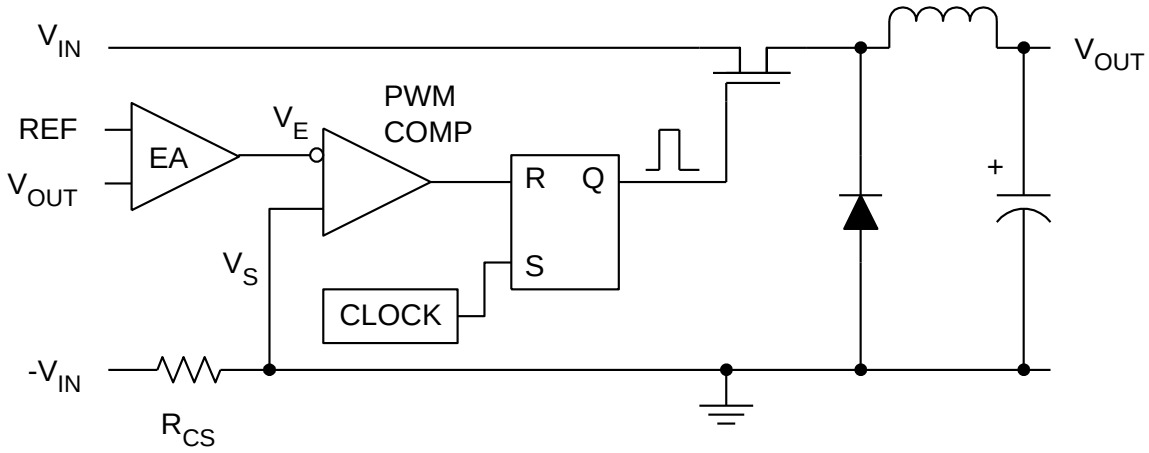


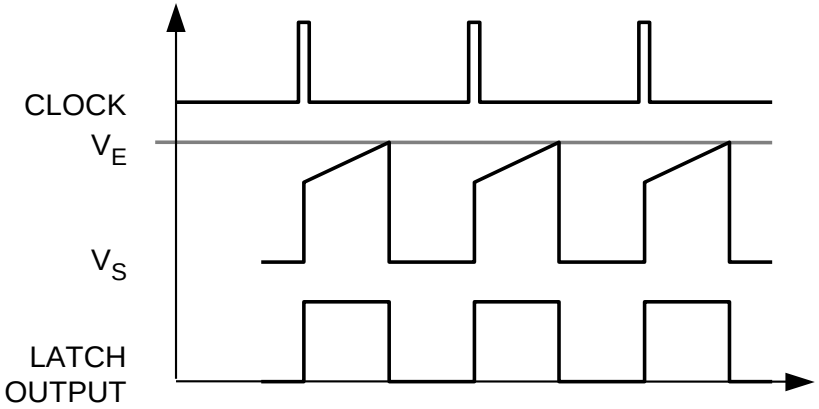
ADVANTAGES
Single feedback loop
Good noise margin
Low impedance output

DISADVANTAGES
Slow dynamic response
Double-pole compensation
Output caps affect comp
V_{IN} affects loop gain

Control Loop Topologies

Current - Mode



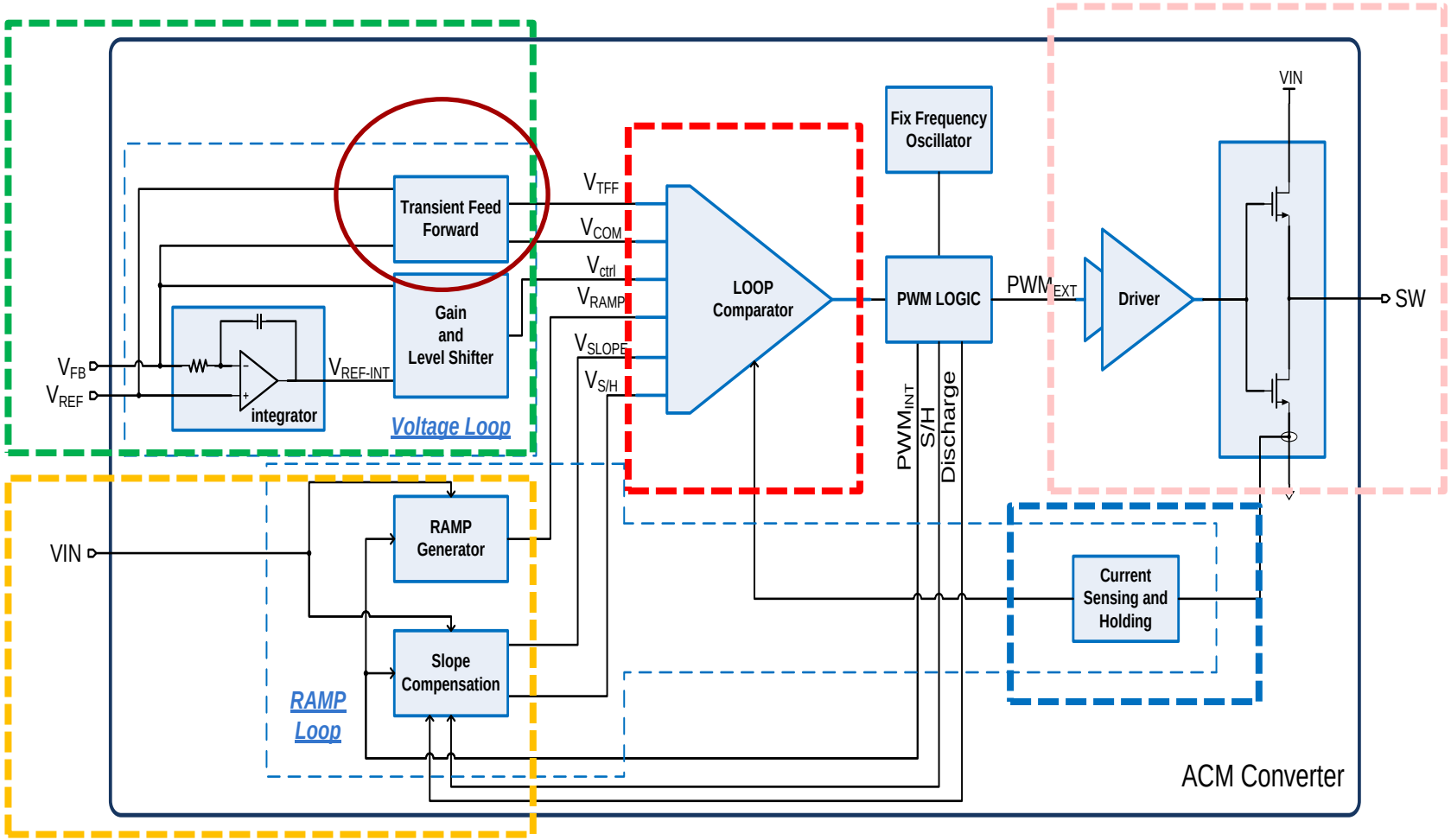


ADVANTAGES
- Fast response to input voltage changes
- Single-pole compensation
- Inherent current limiting
- Parallelability with load sharing

DISADVANTAGES
- Noise sensitivity to current spikes
- Two feedback loops
- Need for slope compensation
- Current limit “tail”

ACM(Advanced Current Mode)-True Fixed Frequency with Internal Compensation

- Inside the converter



Advanced DART Control

DART : Directly Amplified Ripple Tracking control topology

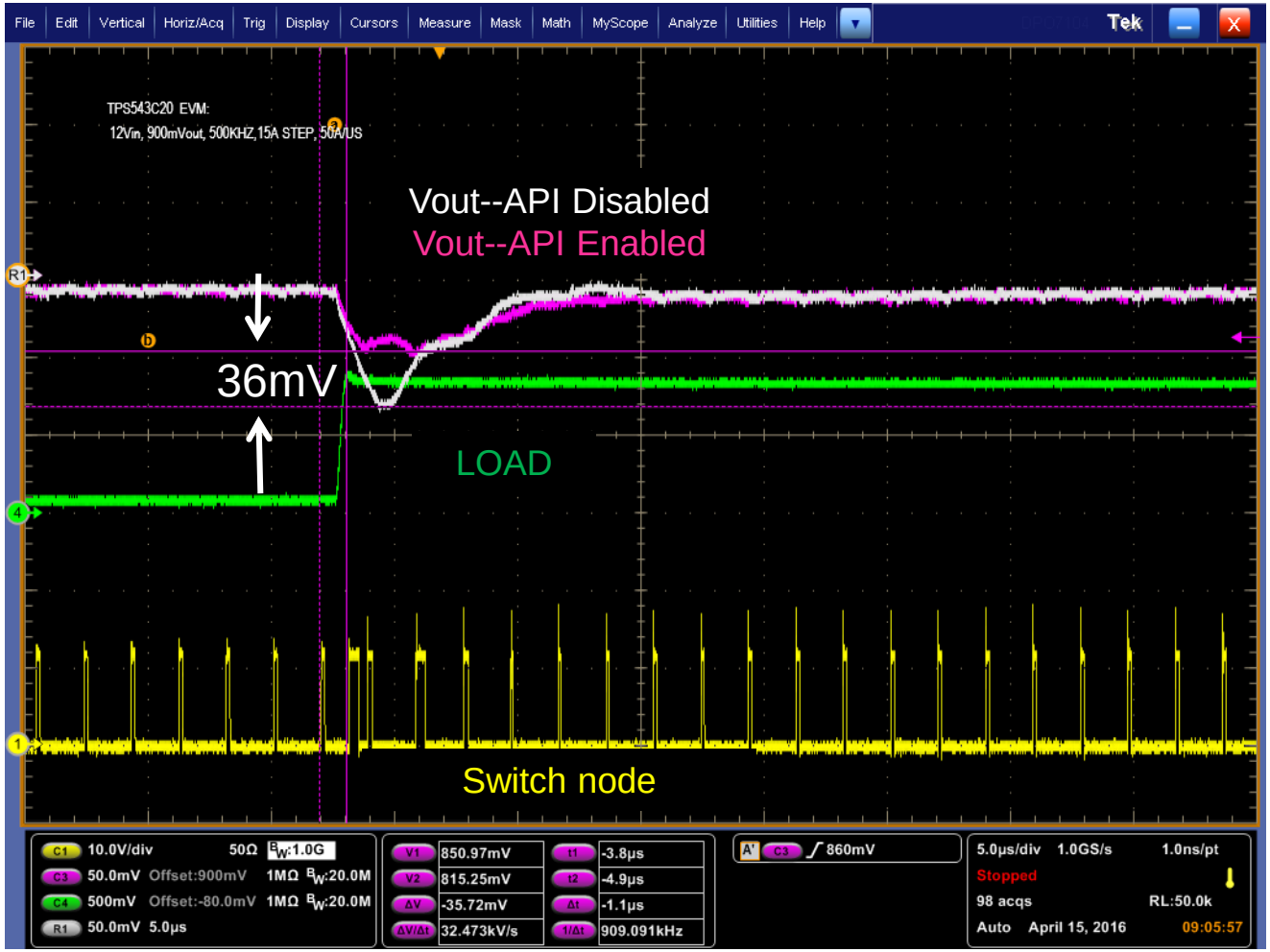
- TPS543C20 is a true fixed-frequency, non-comp IFET converter
  - Fast loop response
  - Wide LC stability range
  - High Signal to noise ratio. Good jitter performance
  - Ease of design

- DART Control can achieve
  - True fixed frequency modulator
  - No external compensation needed, ease of design
    - One resistor to GND for control loop optimization
  - "Constant phase" for over a decade
    - Wide stability range to support large design parameter variation
  - Supports very high frequency, low duty operation with small Jitter

Fast Transient Response and No External Compensation with DART Control

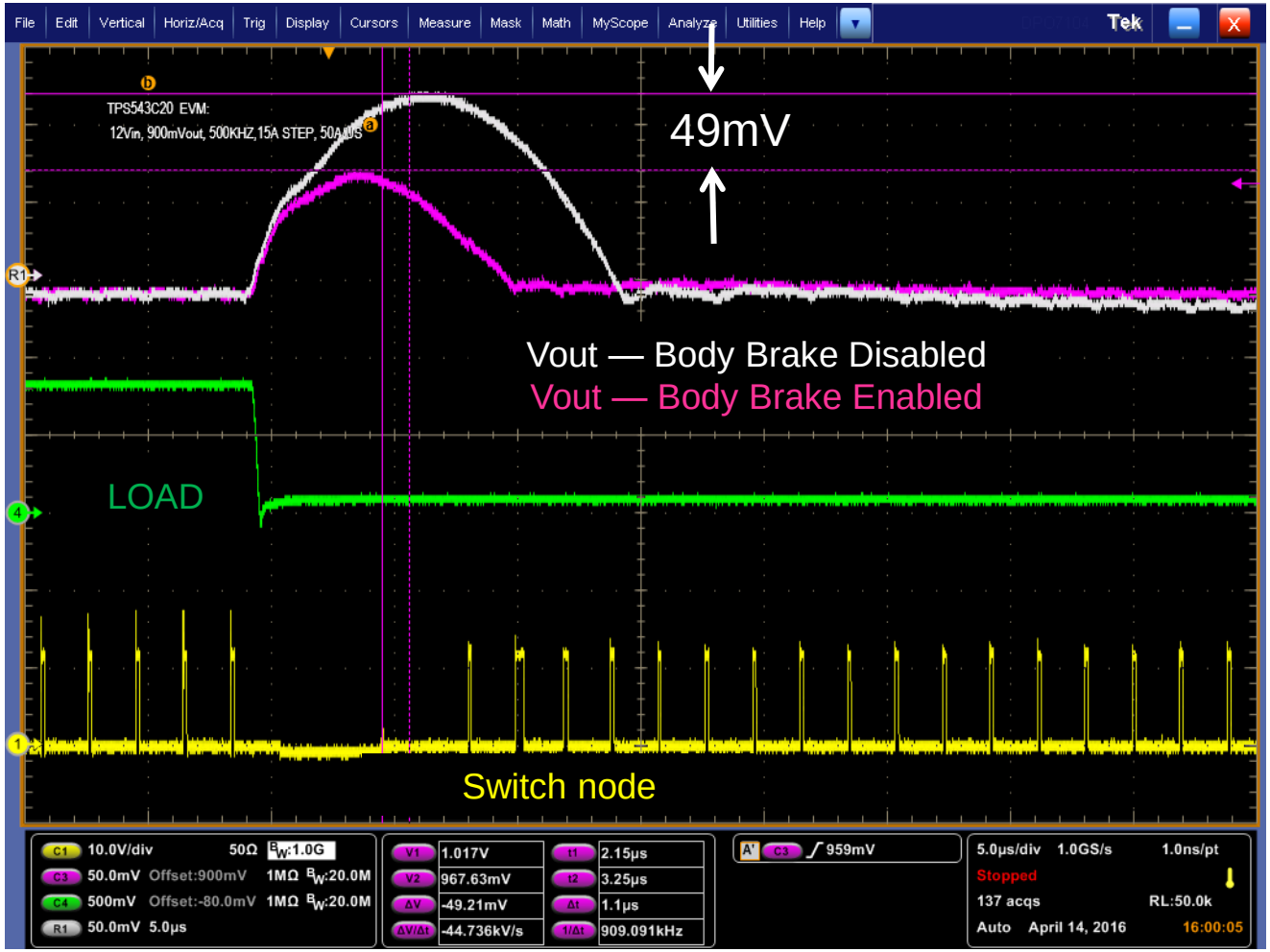
API - Asynchronous Pulse Injection

Further Reducing Transient Undershoot



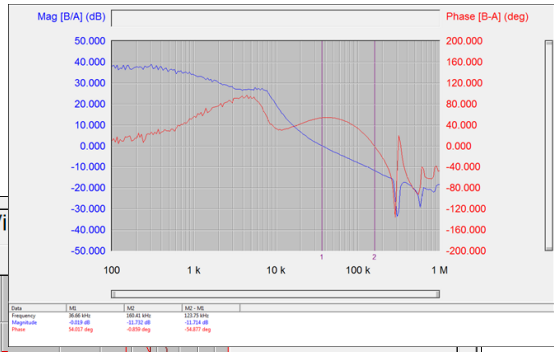
Body Brake

Further Reducing Transient Undershoot

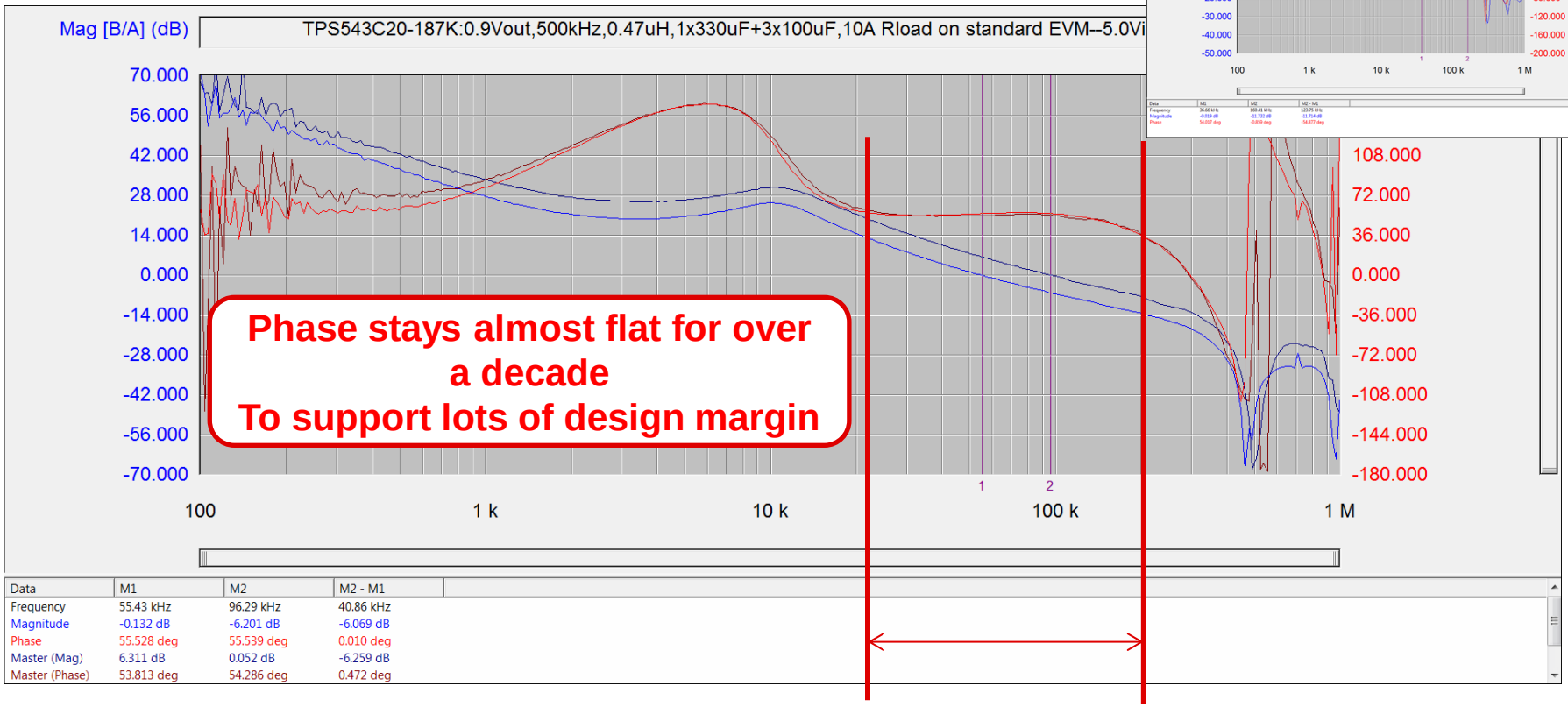


ACM Constant Phase Character

VM control



0.9V, 500kHz, 10A Load and Vin = 5V vs. 12V



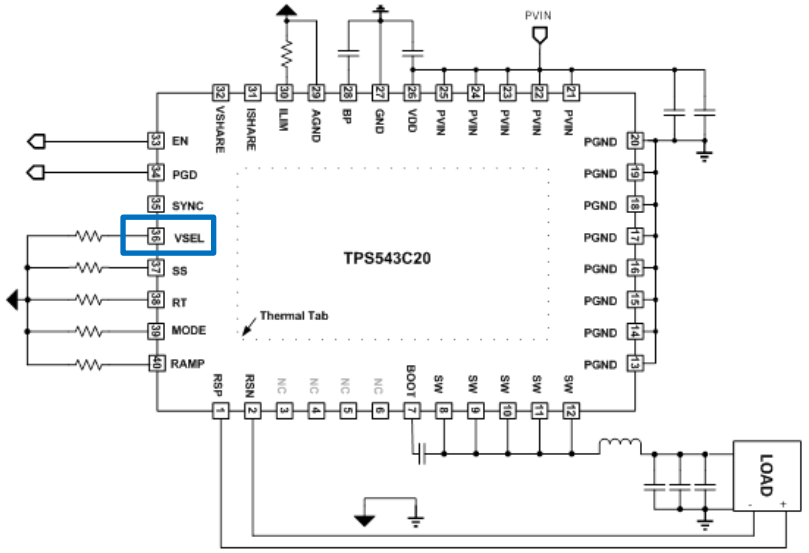
Single Phase Configuration—6 Pins to Setup:
Reference voltage or Vout

VSEL pin (36): Set the Vref and RSP/RSN directly to Vout < 1.1V

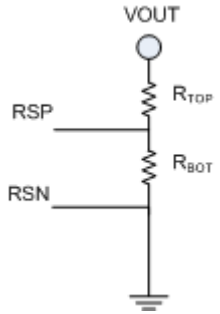
Table 2. VSEL Pin Configuration

DEFAULT Vref (V)	RESISTOR VALUE (kΩ)(1)
0.6	0
0.7	8.66
0.75	15.4
0.8	23.7
0.85	34.8
0.9	51.1
0.95	78.7
1.0	OPEN
1.05	121
1.1	187

(1) The E48 series resistors with no worse than 1% tolerance are recommended



VSEL pin (36): Set the Vref and RSP/RSN directly to resistor divider Vout > 1.1V



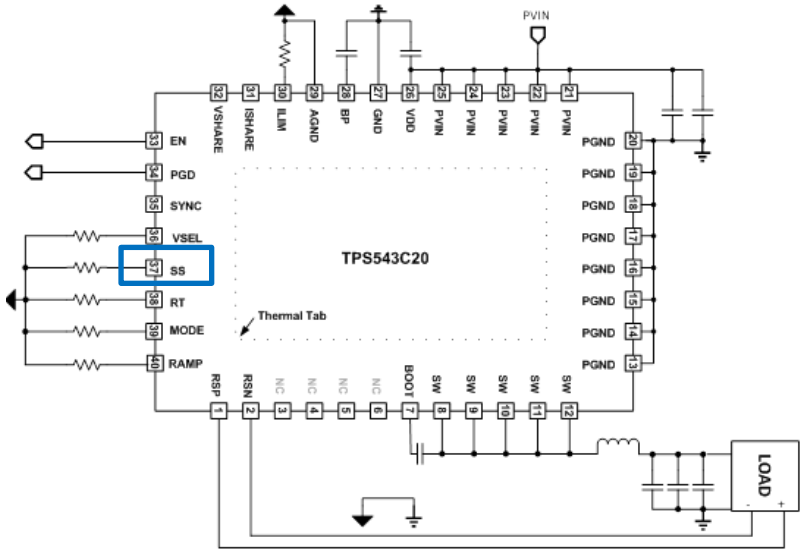
Single Phase Configuration—6 Pins to Setup: Soft-Start

SS pin (37): 10 options to choose from table 1.

Table 1. SS Pin Configuration

SS TIME (ms)	RESISTOR VALUE (kΩ)(1)
0.5	0
1	8.66
2	15.4
5	23.7
4	OPEN
8	34.8
12	51.1
16	78.7
24	121
32	187

(1) The E48 series resistors with no more than 1% tolerance are recommended.



Single Phase Configuration—6 Pins to Setup: Switching Frequency

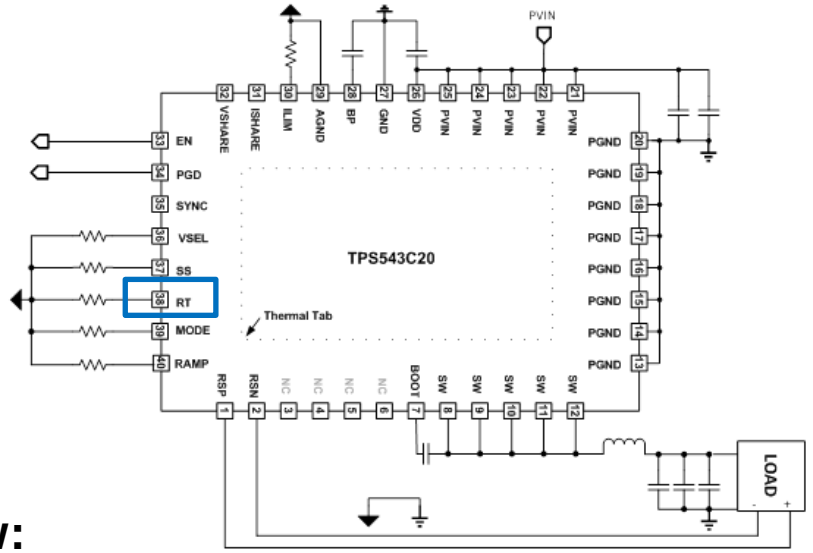
RT pin (38): 300kHz to 2MHz calculation from equation 1.

Resistor R_{RT} sets the continuous switching frequence selection by

$$R_{RT} = \frac{20 \times 10^9}{f_{SW}} - \frac{f_{SW} \times 2}{2000}$$

where

- R is the resistor from RT pin to GND, in Ω
- f_{SW} is the desired switching frequency, in Hz



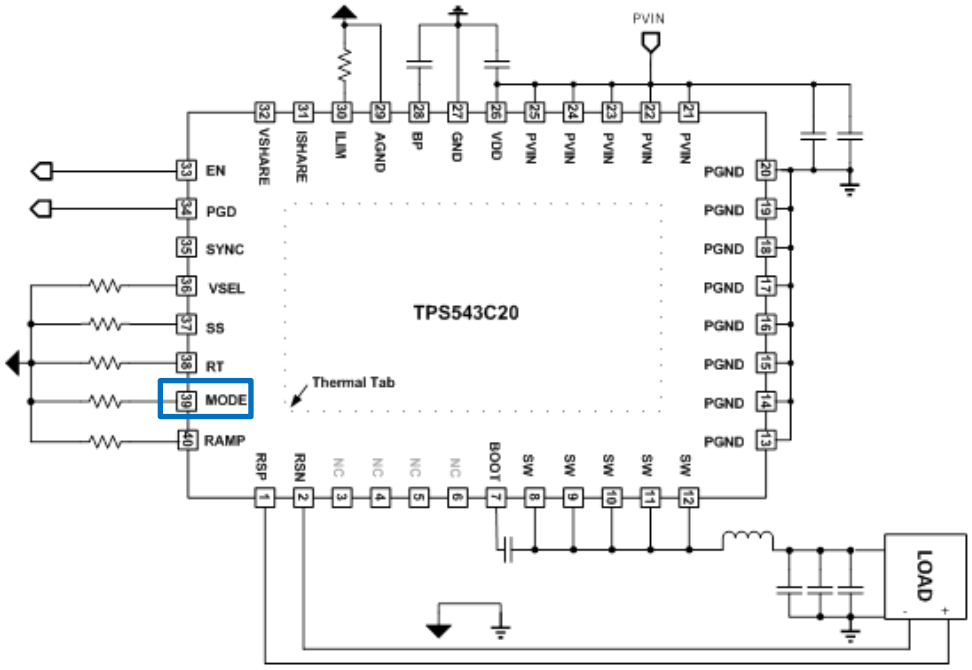
Or use values below for standard Fsw:

SWITCHING FREQUENCY					
F_{SW}	V_O switching frequency Max frequency for multi-phase is 1MHz	V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 66.5 kΩ	300	kHz
		V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 48.7 kΩ	400	
		V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 39.2 kΩ	500	
		V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 28.0 kΩ	700	
		V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 22.6 kΩ	850	
		V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 19.1 kΩ	1000	
		V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 15.4 kΩ	1200	
		V_{IN} = 12 V, V_{VO}= 1.0 V,	RT = 8.06 kΩ	2000	

Single Phase Configuration—6 Pins to Setup:
API/BB Selection Options

MODE pin (39): 6 options to choose

API/BB	Resistor Value—Pin 39
Both Off	Open
API=On; BB = Off	15.4K Ω
Both ON at 1x	121K, API = 15mV, BB=30mV
Both ON at 2x	187K, API = 25mV, BB=30mV
Both ON at 3x	8.66K, API = 35mV, BB=30mV
Both ON at 4x	78.7K, API = 45mV, BB=30mV



- When API enables, the RSP/RSN has high pass filter (2.5pF and 2.5MΩ). If the threshold is passing this frequency, API will be active.

- **1x stands for most sensitive and 4x stands for least sensitive**

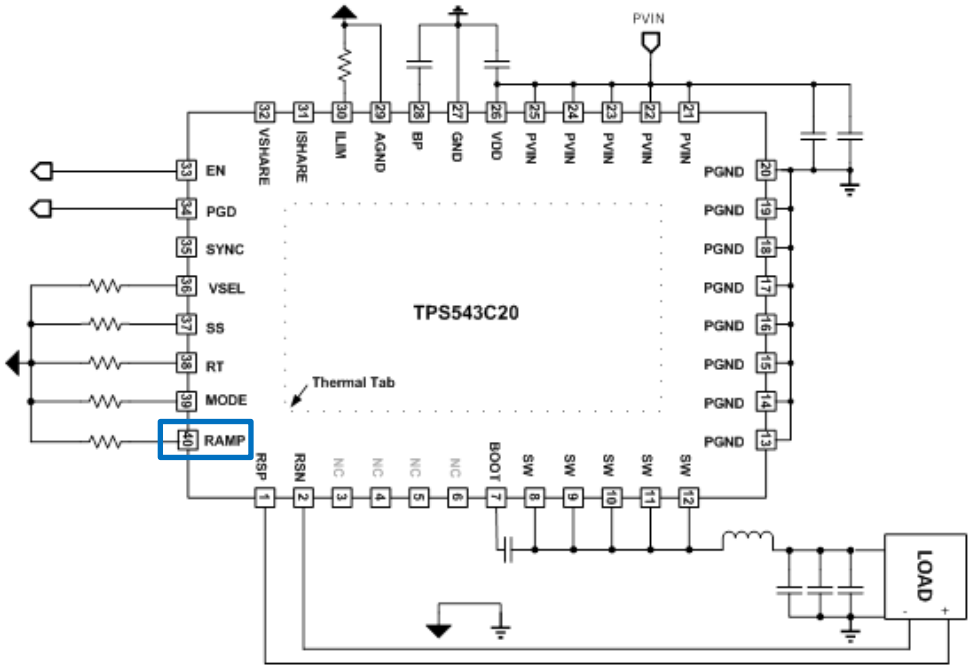
Single Phase Configuration—6 Pins to Setup: RAMP Selection Options

RAMP pin (40): 10 options to choose

Table 3. RAMP Pin-strapping Selection

C_{RAMP} (pF)	RESISTOR VALUE (kΩ)(1)
1	0
1.42	8.66
1.94	15.4
2.58	23.7
3.43	34.8
4.57	51.1
6.23	78.7
8.91	121
14.1	187
29.1	Open

(1) The E48 series resistors with tolerance of 1% or less are recommended.



TPS543C20 is defined to be ease-of-use, for most applications, we recommend ramp resistor to be 187 kΩ to achieve the optimized jitter and loop response. For detailed design procedure please see the WEBENCH® Power Designer.

Single Phase Configuration—6 Pins to Setup:
OCP setup

ILIM pin (30): OCP detects near peak inductor

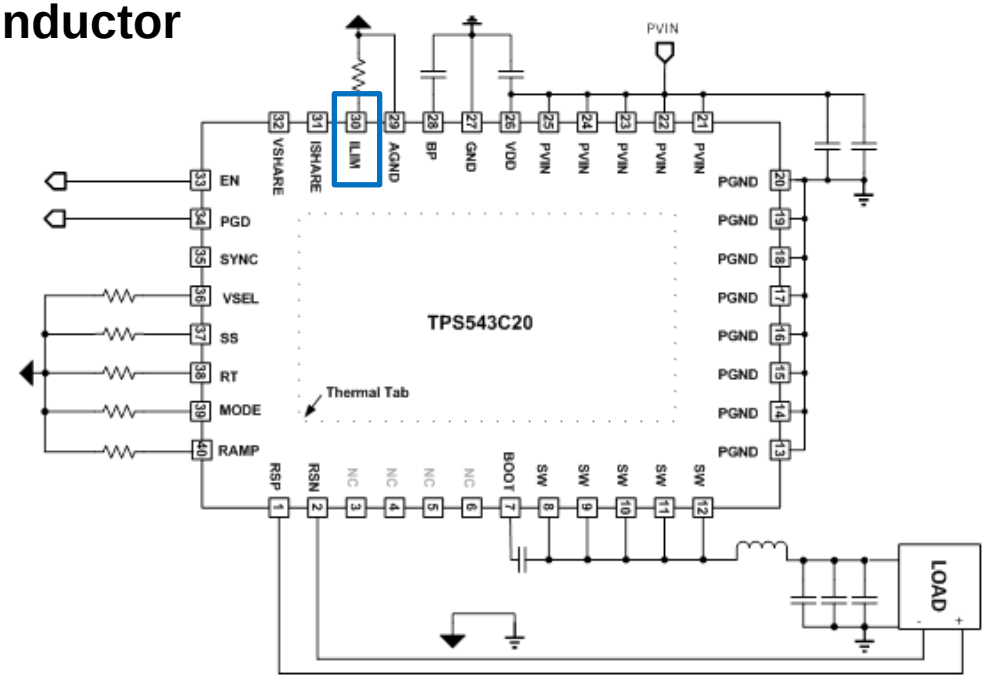
$$I_{OCP} = V_{ILIM}/(16 \times R_{DS(on)}) - I_{IND(ripple)}/2$$

$$= \frac{V_{ILIM}}{16 \times R_{DS(on)}} - \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- $R_{DS(on)}$ is the on-resistance of the low-side MOSFET.

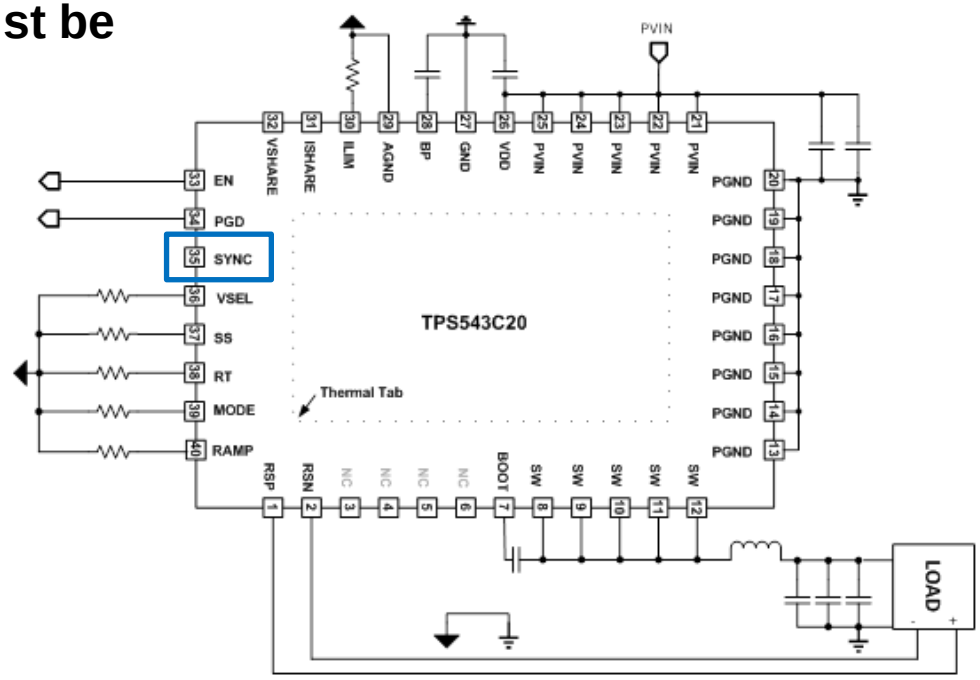
½ of Inductor Current Ripple



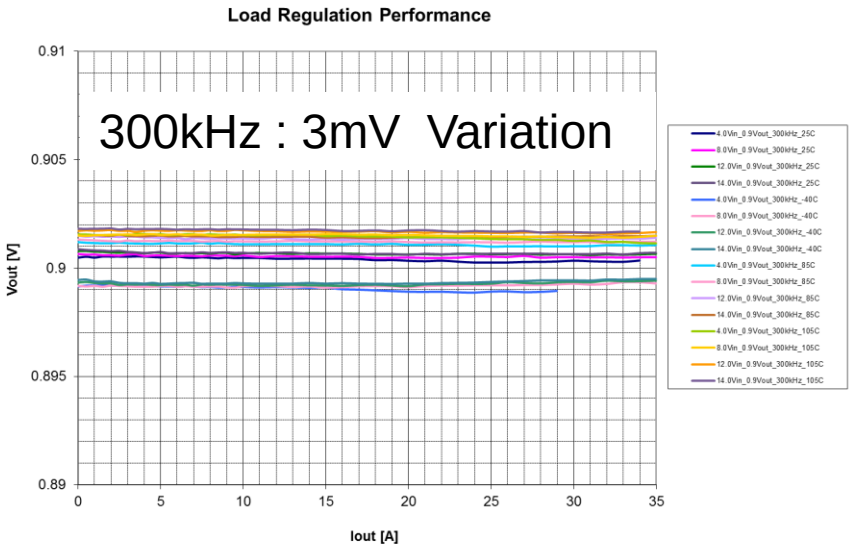
Use Rdson = 0.62mΩ for above equation due to die sense

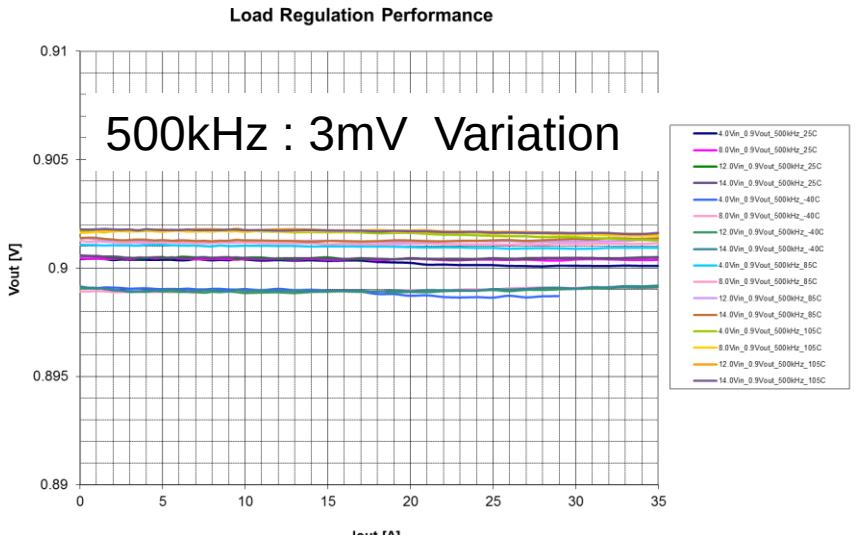
SYNC in Single Phase Configuration

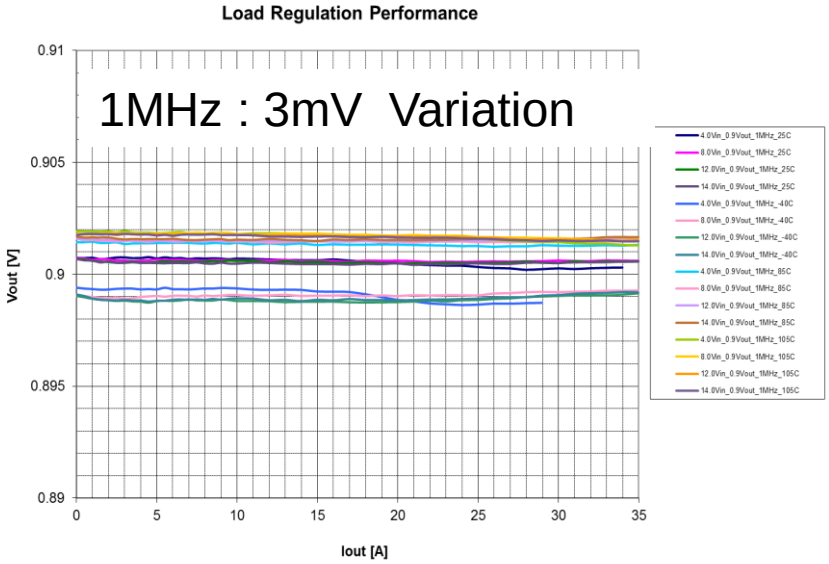
SYNC pin (35): External frequency must be higher or equal to RT setting



TPS543C20 VOUT Regulation: 4Vin-14Vin, -40C to 105C







Fault Protection

- Input Voltage UVLO
  - 3.8V UVLO for Vbias and VIN
- UV Protection
  - 83% of reference voltage
- OV Protection
  - 117% of reference voltage
- Over Current protection
  - Fixed HS OCP and programmable LS OCP
- Hiccup for OV, UV, OC

Summary

- Advanced Control Scheme
  - TPS43C20 is a true fixed-frequency, non-comp IFET converter
    - Fast transient response
    - Wide LC stability range with **“Constant Phase”** Character
    - Ease of design
    - Supports very high frequency, low duty operation
- Advanced Integrated MOSFET
  - Very low (sub-mΩ) Rdson, high efficiency performance
    - TPS543C20:~3.0/0.9mΩ
    - TPS543B20:~4.1/1.9mΩ
- Full of Feature sets
  - True remote sense.
  - Sync capability, sync IN/OUT
  - Very tight OC accuracy (+/-10%)
  - API/Body brake function to help transient
  - **2-phase Stackable. Good design flexibility**
- Other:
  - 40A/25A versions in same package
  - Low bias voltage support (down to 4V)

Thank you !

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