

# Internally Compensated Advanced Current Mode (ACM) with the TPS543C20

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# Agenda

- Introduction to Advanced Current Mode (ACM)
- ACM Overview
- ACM Small Signal Analysis
- TPS543C20 Overview
- ACM Comparison to other Control Modes
  - D-CAP3™
  - Voltage Mode with Voltage Feedforward
- Summary

# Introduction to Advanced Current Mode (ACM)

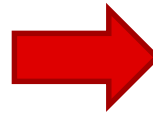
# Motivation for Internally Compensated ACM

## COT (D-CAPx™)

- ✓ No external compensation required
- ✓ Fast Transient Response
- ✓ Simple, easy to design with less BOM
- No true fixed frequency
- Higher jitter (during transients)
- Inability to stack – no CLK sync
- Challenge to employ traditional methods of gain-phase measurements

## CMC/ VMC

- ✓ Proven methods to calculate/ measure bode plots to implement stable Designs
- ✓ True fixed frequency operation; ability to sync to external clock to eliminate beat noise and facilitate stacking
- ✓ Good, low-jitter performance
- Requires external Type2/3 compensation
- Larger BOM and more complex Designs
- Tempered transient response



New!

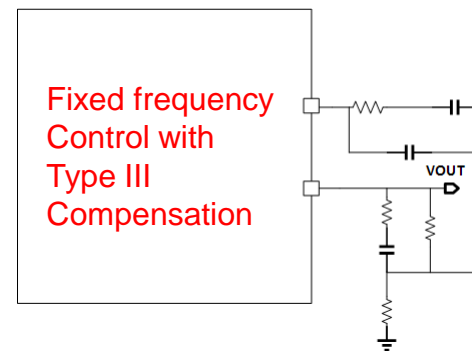
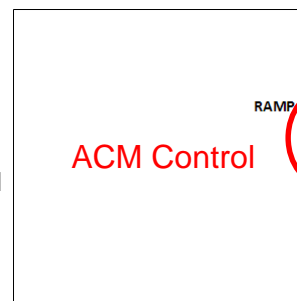
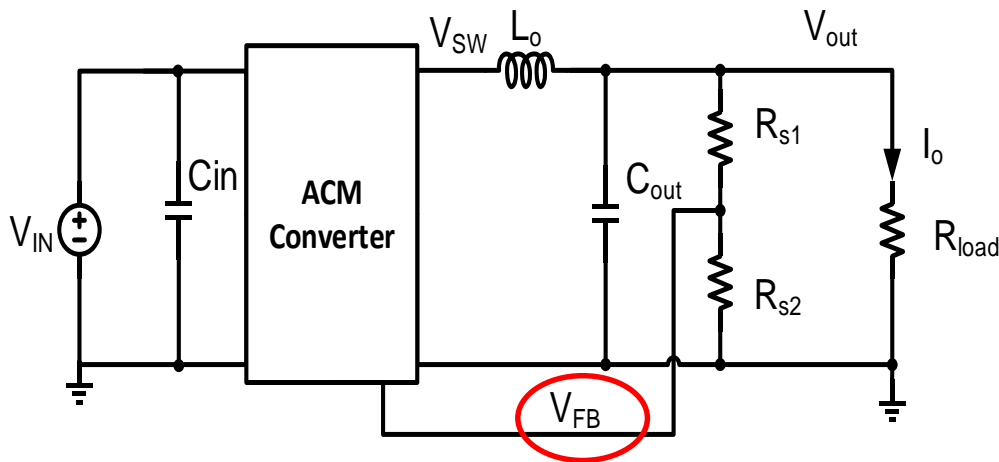
## Internally Compensated ACM

- ✓ No external compensation required
- ✓ Fast Transient Response
- ✓ Simple, easy to design with less BOM
- ✓ Proven methods to calculate/ measure bode plots to implement stable Designs
- ✓ True fixed frequency operation; ability to sync to external clock to eliminate beat noise and facilitate stacking
- ✓ Good, low-jitter performance

# ACM Control Introduction



- DC-DC Converter using ACM
  - Without external compensation, ACM converter only needs  $V_{FB}$  single for control loop.
  - The external passive components can be minimized to save total system cost and size.
  - Ease of use, no need to design the PID or PI compensation



# ACM Control Advantages Overview cont'd



## True Fixed Frequency Modulation

- Preset clock oscillator to determine switching frequency
- Synchronization to external clock, enable easier stackability
- Better jitter performance compare with various frequency

## Benefit

- Predictable EMI noise filtering
- Power scaling to simplify design and layout
- Low EMI noise

## Internal Compensation with Fast Transient

- Ease of use, without complicated compensation design
- No external compensation components, reduce BOM and PCB area
- Flexible loop optimization to cover wide L, C range

## Benefit

- Greatly reduce design to release cycle
- Increase system power density
- Design flexibility and tolerance for variations

## Other Features

- Large single to noise ratio by emulated ramp
- Multi-mega Hz Switching
- Asynchronous Pulse Insertion (**API**) and Body Braking
- DC current feedback for resonant frequency damping

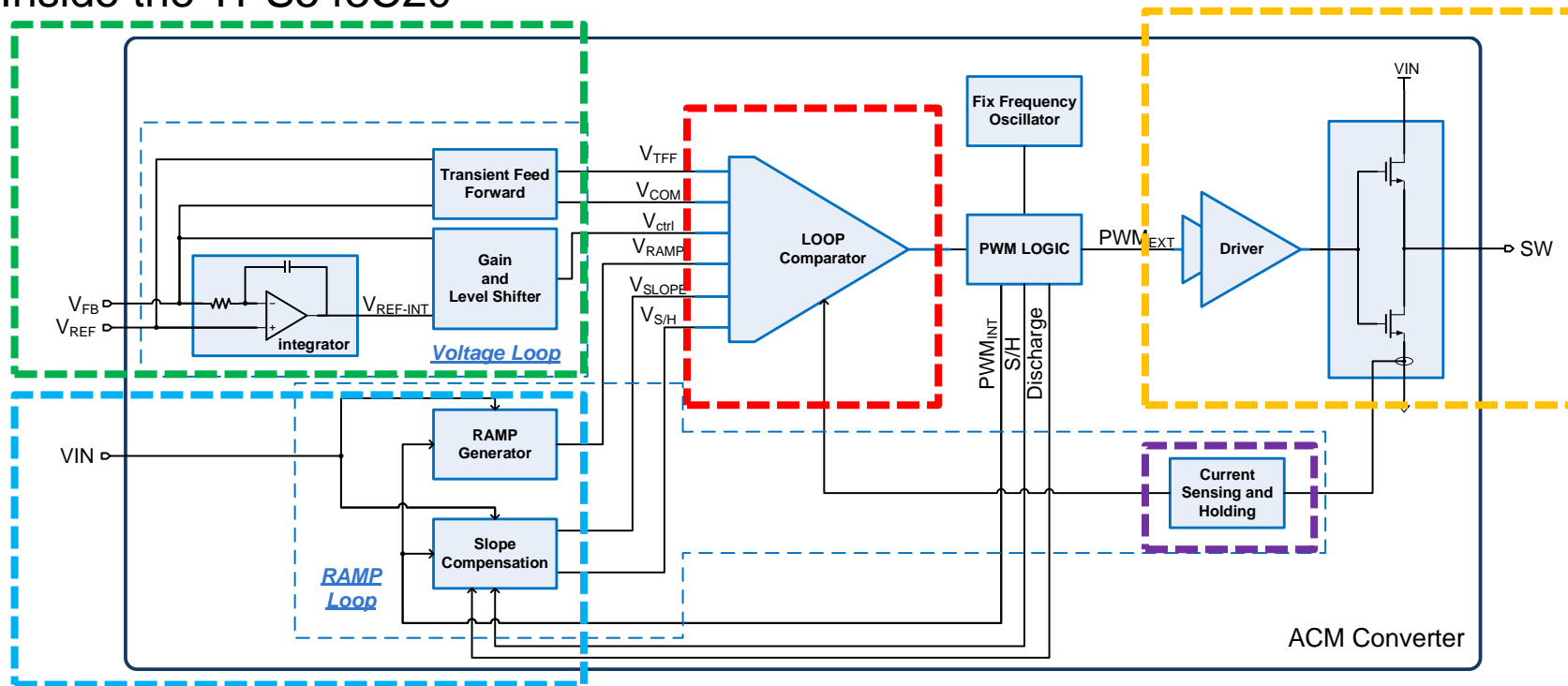
## Benefit

- Better switching jitter performance
- Size reduction and fits automotive applications
- Further improve transient performance
- Supports huge output capacitance

# ACM Control Overview

# ACM Control Overview - Block Diagram

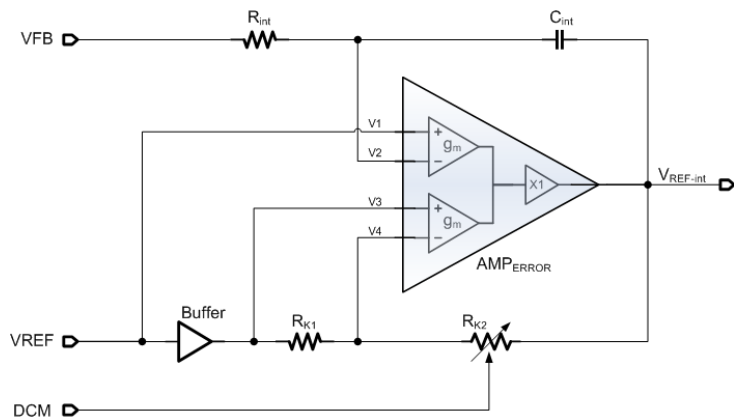
- Inside the TPS543C20





# ACM Control Overview: Voltage loop – Integrator

- We used a four inputs error amplifier to do the integration. One pair of the input is doing the integration, while the other pair is controlling the gain of this integrator.
- The system diagram of this new internal integrator is shown below. V1 and V2 are used to do the feedback for integration and V3 and V4 are used to control the gain.



**VFB:** This voltage is the feedback voltage of the DC-DC Converter

**VREF:** This is the reference voltage of the system.

**DCM:** DCM mode enable digital signal.

**V<sub>REF-INT</sub>:** The output of the integrator

**AMP<sub>ERROR</sub>:** Four input amplifier for the integrator

**Buffer:** The voltage buffer to separate the VREF from the loading of R<sub>K1</sub> and R<sub>K2</sub>.

**R<sub>int</sub> and C<sub>int</sub>:** The resistor and capacitor providing the integration function.

**R<sub>K1</sub> and R<sub>K2</sub>:** the resistor pair to set the gain of the integrator. The resistance of R<sub>K2</sub> is controlled by DCM

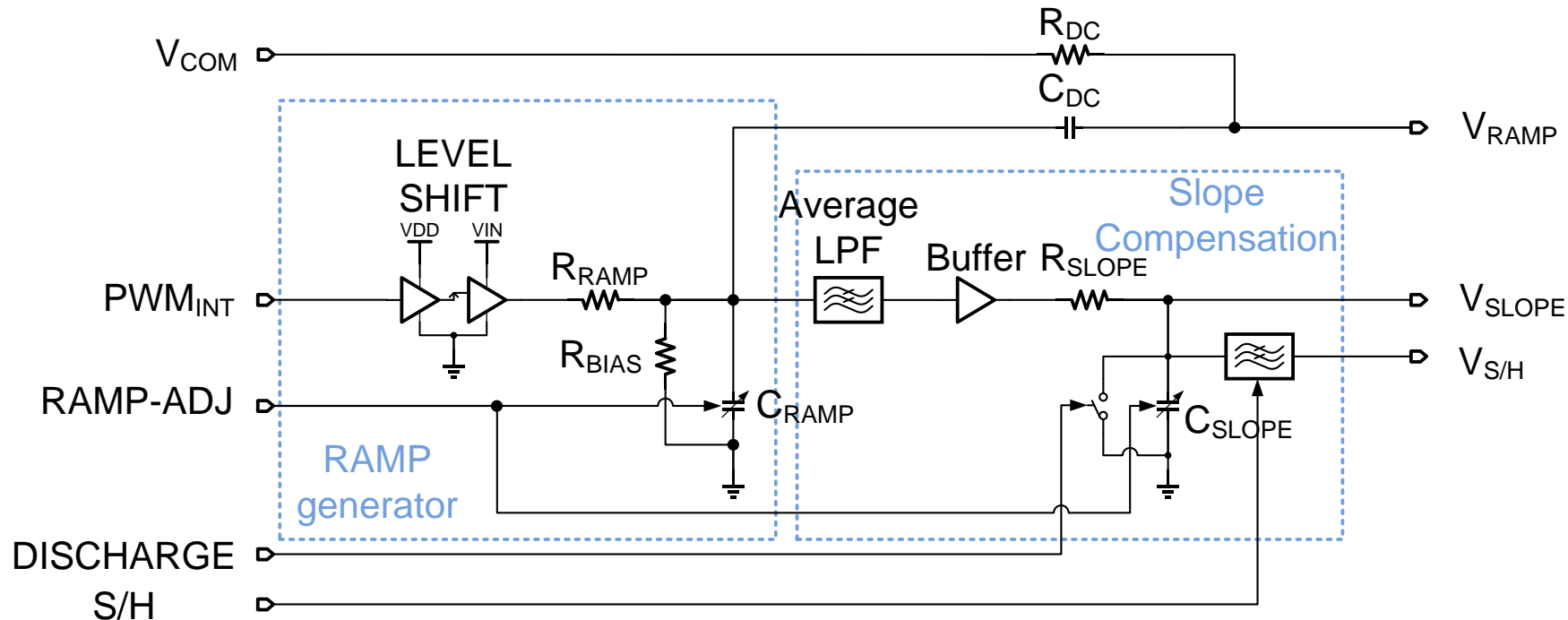
**AC response of integrator:**

$$V_{REF-int} = V_{REF} \cdot \frac{s + \frac{k \cdot (V_{REF} - V_{FB}) + V_{REF}}{(k+1) \cdot V_{REF} \cdot C_{int} R_{int}}}{s + \frac{1}{(k+1) \cdot C_{int} R_{int}}} \quad \text{Where, } k = \frac{R_{K2} + R_{K1}}{R_{K1}}$$

# ACM Control Overview:

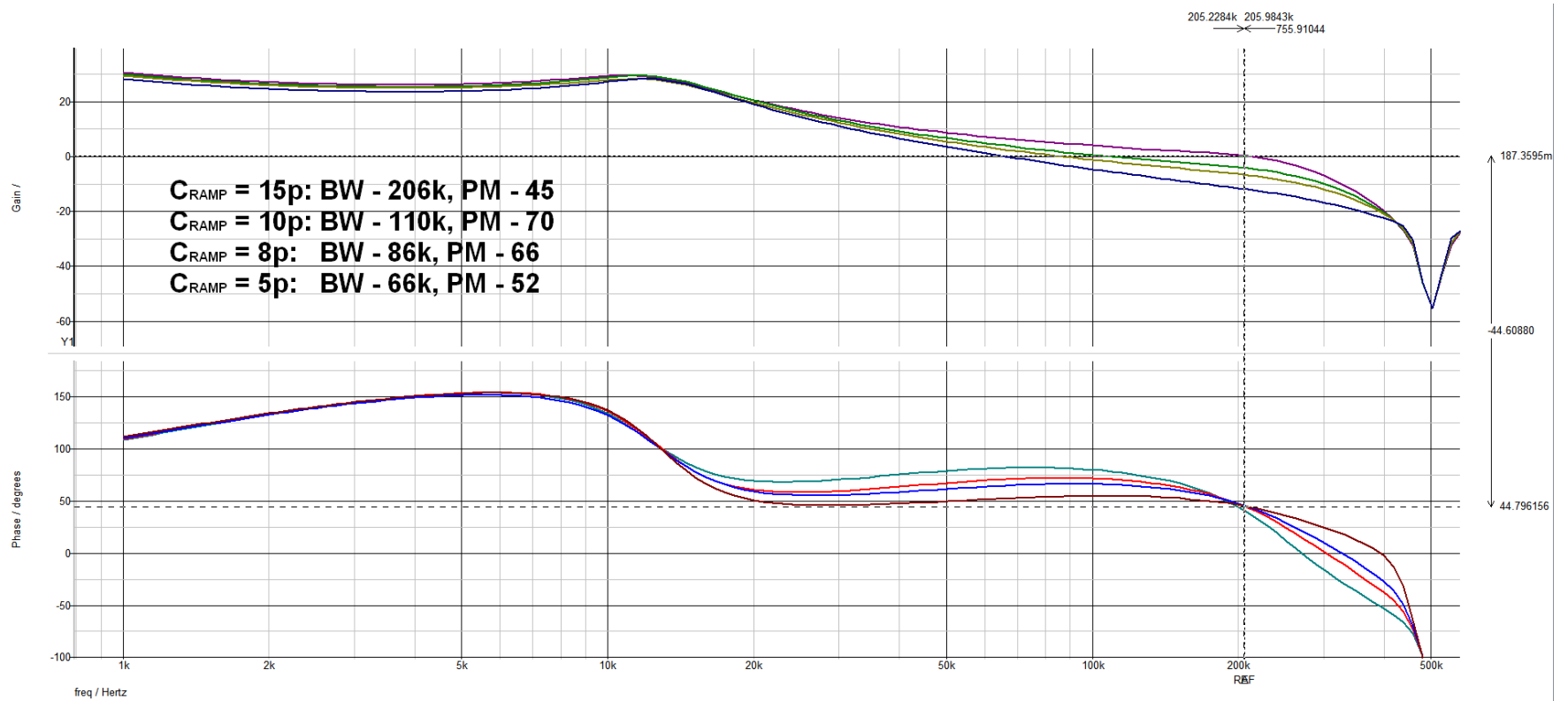
## Ramp loop – RAMP Generator and slope compensation

- The RAMP generator and slope compensation is shown below



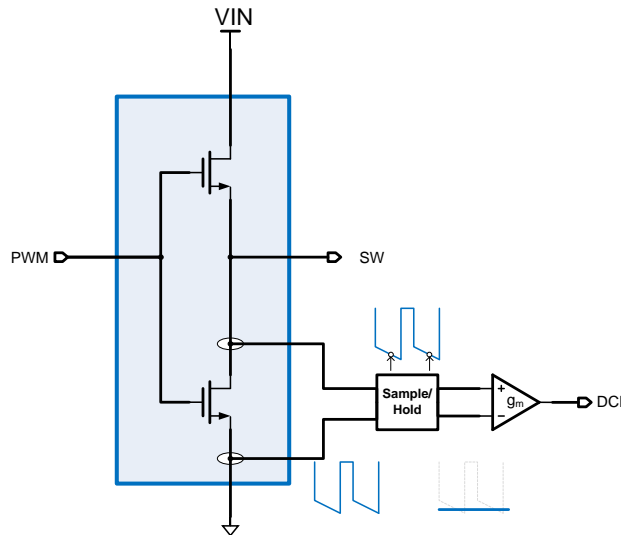
# ACM Control Overview:

## AC plot with different RAMP setting



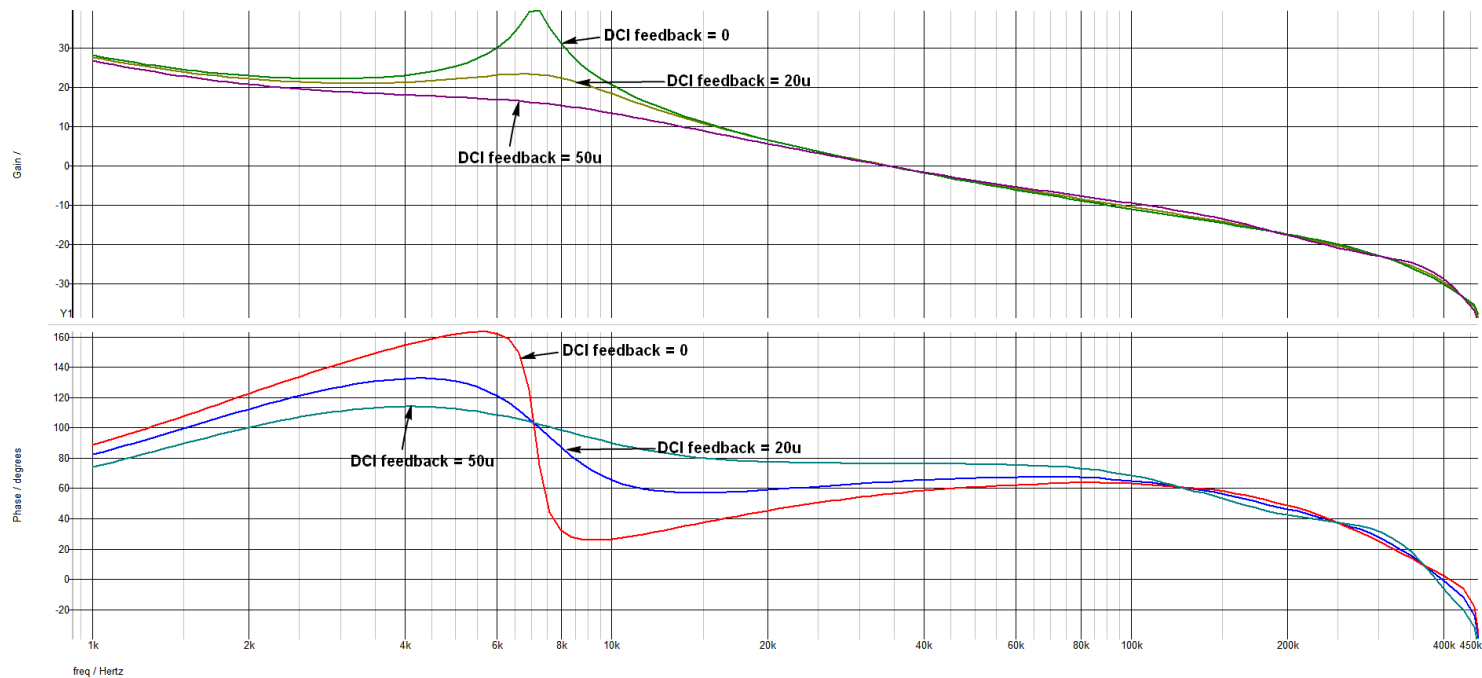
# ACM Control Overview: DC Current Feedback Loop

- To decrease the Q value at the double pole frequency, a small DC current feedback is added to the loop.
- The current information is sensed from the power stage, for example from the low side FET. And it is sampled and hold at one point during off time, normally at the end of off time.
- A gm amplifier changes this S/H current information to current and feedback to the loop comparator.



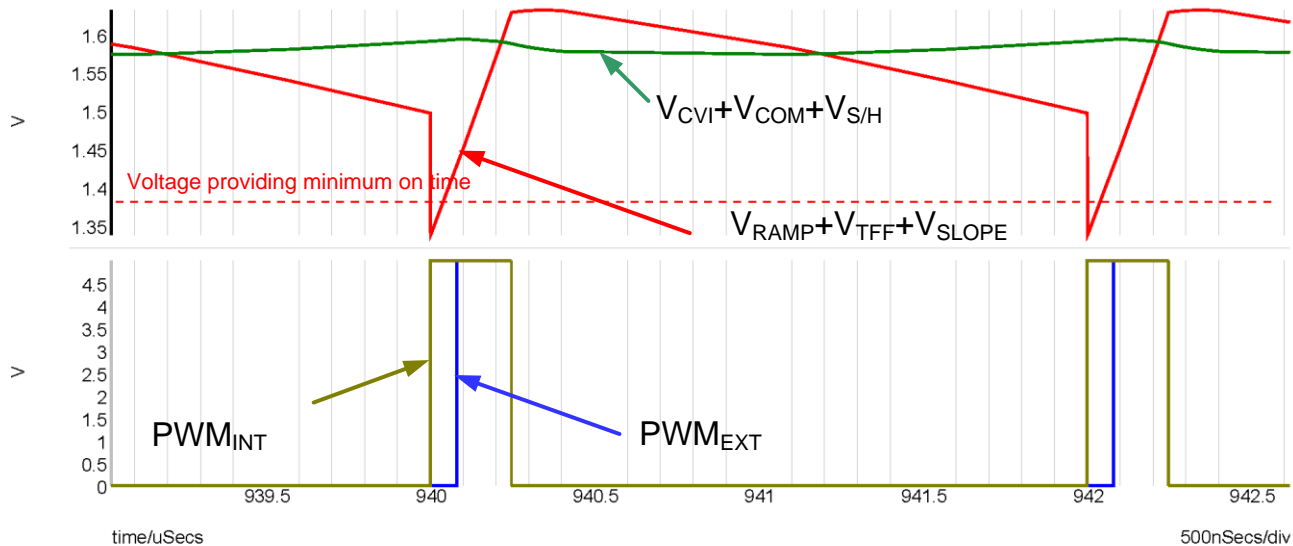
# ACM Control Overview: DC Current Feedback Loop—cont.

- The bode plots with different DCI feedback value are compared below:



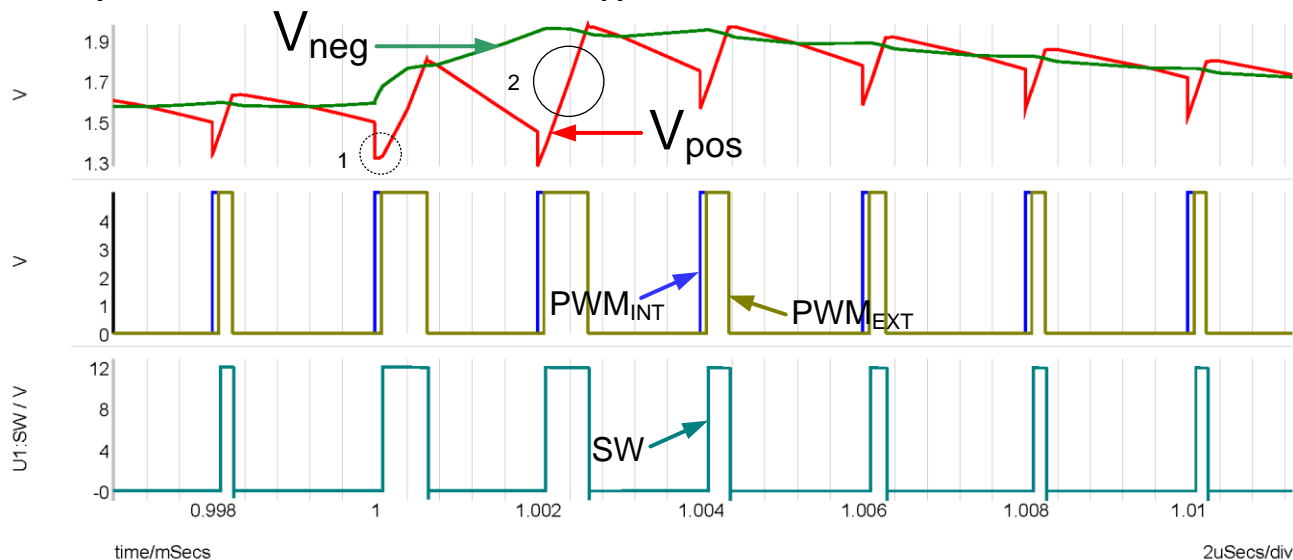
# ACM Control Overview: Control Signal Waveform—cont.

- We can add all of the positive inputs of the loop comparator together and compare it with all of the negative inputs. The waveform is shown below:



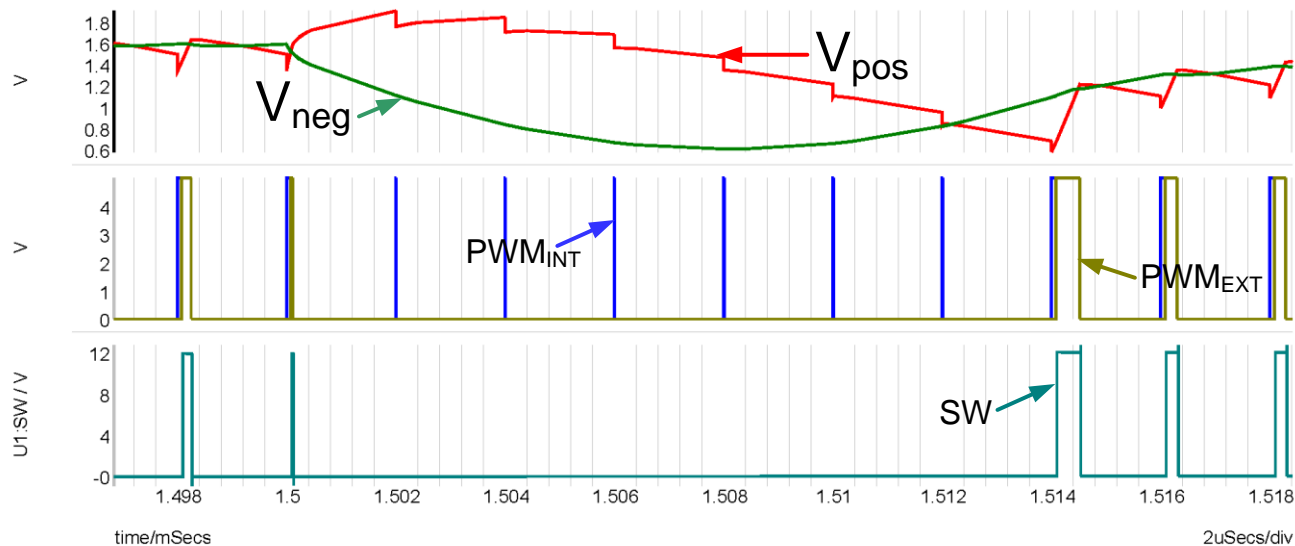
# ACM Control Overview: Control Signal Waveform—cont.

- During load step up transient,  $V_{out}$  dips when the load increases. The  $V_{neg}$  (sum of negative inputs of the loop comparator) will increase and slope of the  $V_{pos}$  (sum of positive inputs of the loop comparator) will decrease. The duty cycle will be bigger to pull the  $V_{out}$  back to target. The waveform is shown below:



# ACM Control Overview: Control Signal Waveform—cont.

- During load step down transient,  $V_{out}$  rise when the load decrease. The  $V_{neg}$  will decrease and slope of the  $V_{pos}$  will increase. The duty cycle will be smaller to pull the  $V_{out}$  back to target. The waveform is shown below:

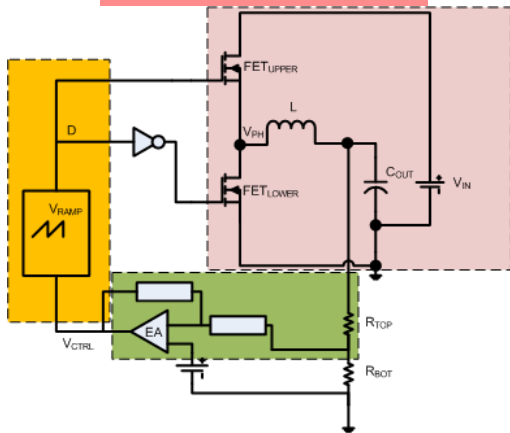




# ACM Small Signal Analysis

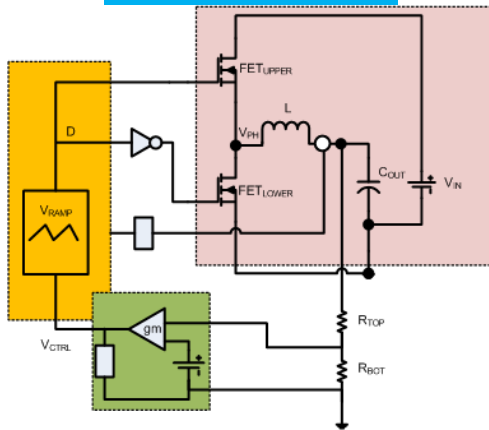
# DC-DC Topology: Control vs Ramp

## Voltage Mode



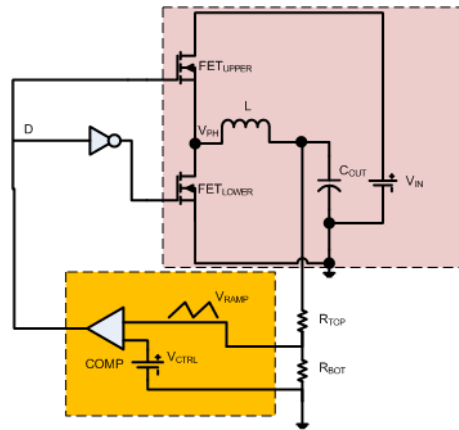
$V_{RAMP}$  is saw tooth waveform  
 $V_{CTRL}$  is EA output

## Current Mode



$V_{RAMP}$  is proportional to the inductor current  
 $V_{CTRL}$  is gm output

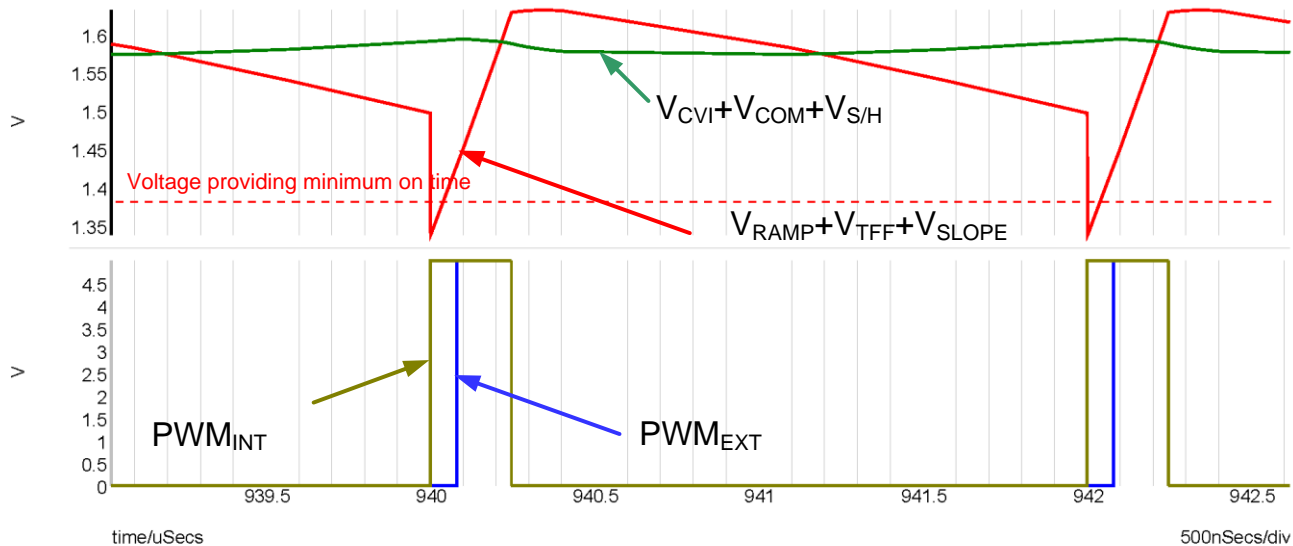
## COT Mode



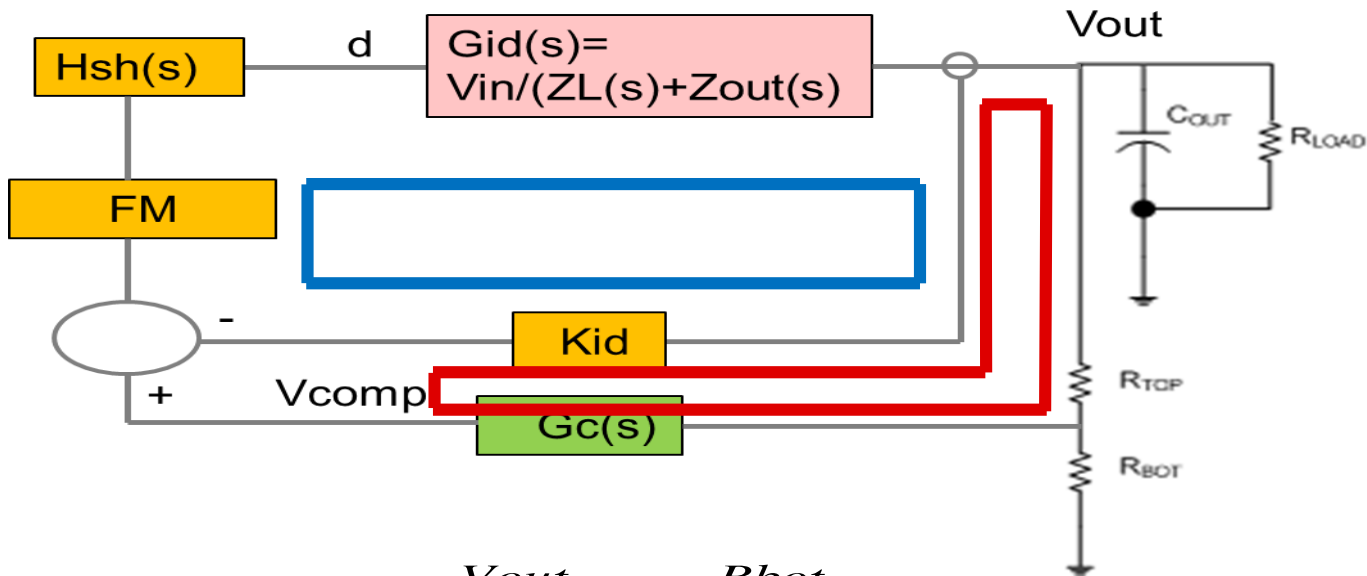
$V_{RAMP}$  is proportional to the inductor current  
 $V_{CTRL}$  is the reference voltage

# ACM Control vs Ramp

- We can add all of the positive inputs of the loop comparator together and compare it with all of the negative inputs. The waveform is shown below:



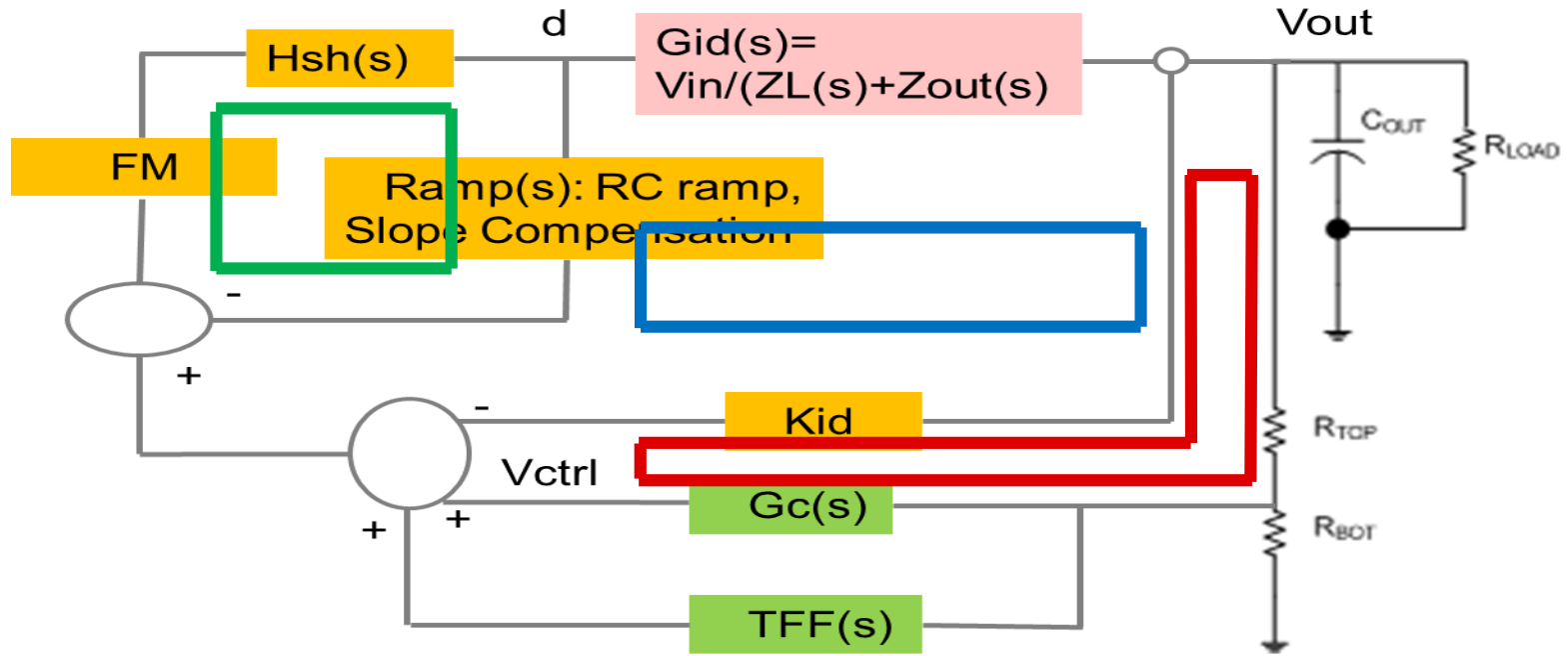
# Convert Block Diagram to TF: Current Mode



$$LoopGain = \frac{V_{out}}{V_{comp}} \cdot \frac{R_{bot}}{R_{bot} + R_{top}} \cdot G_c$$

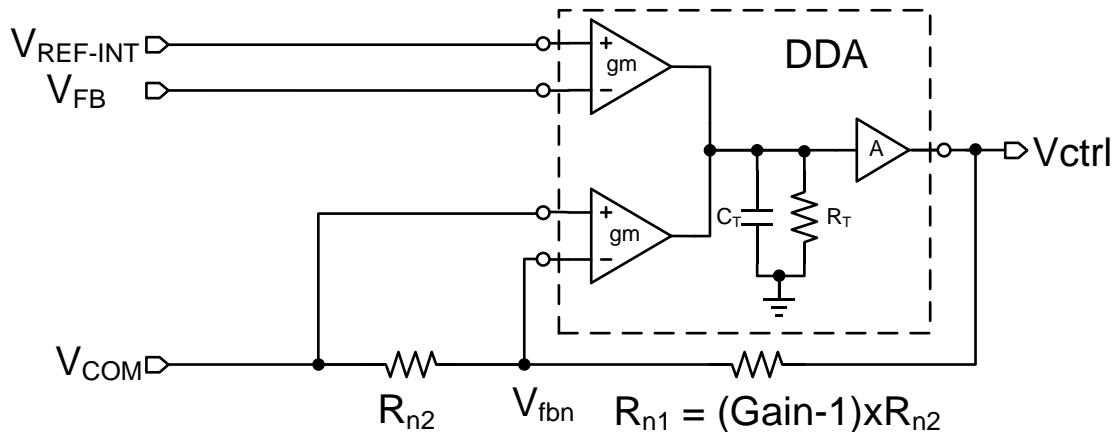
$$\frac{V_{out}}{V_{comp}} = \frac{a}{1 + a \cdot b}$$

# Block Diagram to TF: ACM



Next slides show the transfer function of each block and loop gain transfer function

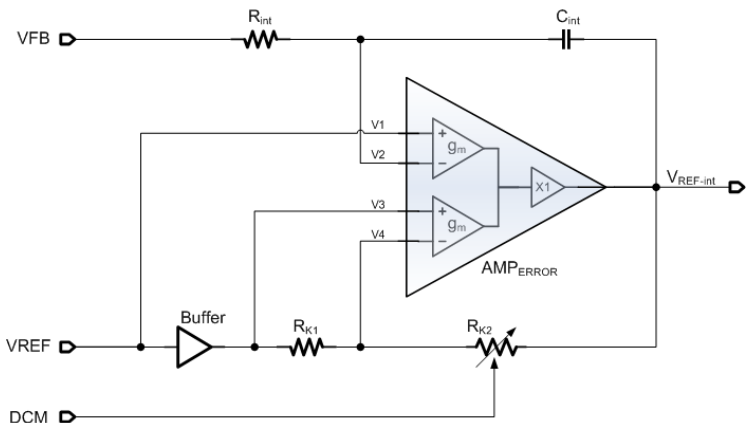
# Control Voltage TF



- AC model: Set  $V_{COM}$  as zero

$$V_{ctrl} = \frac{R_{n2} + R_{n1}}{R_{n2}} (V_{REF-INT} - V_{FB})$$

# Control Voltage TF: Con't



- AC model: Set  $V_{VREF}$  as zero  
 $V4 = -V2$

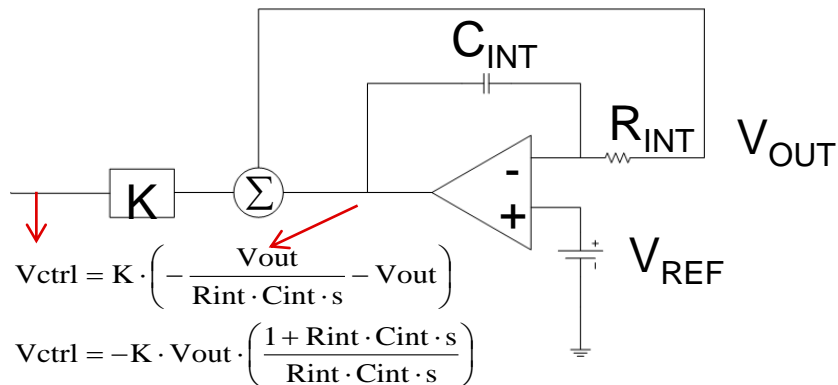
$$\frac{Rk1}{Rk2 + Rk1} \cdot Vref\_int = -1 \cdot \frac{VFB + s \cdot Cint \cdot Rint \cdot Vref\_int}{s \cdot Cint \cdot Rint + 1}$$

$$Vref\_int(s) := -\frac{H \cdot (Rk1 + Rk2)}{Rk1 + s \cdot Cint \cdot Rint \cdot (2 \cdot Rk1 + Rk2)}$$

How does  $V_{ctrl}$  effect the stability of the system?

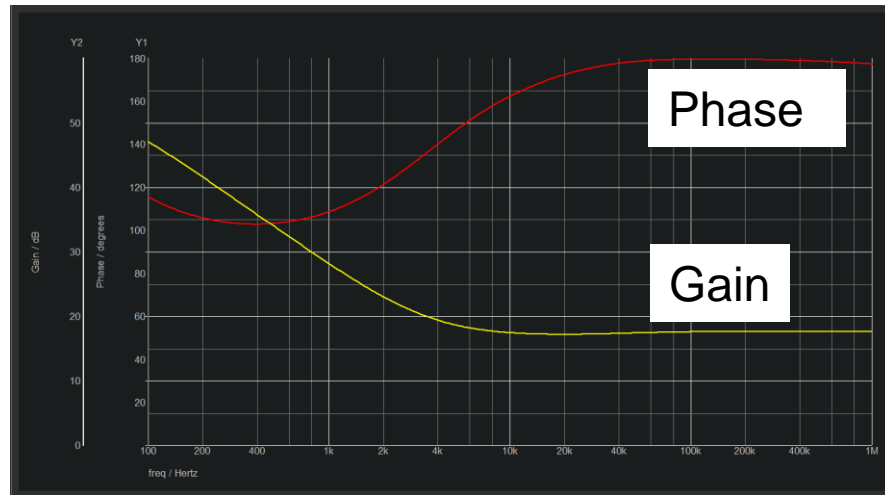
What are the meaning behind of this signal?

# Control Voltage TF: Con't



$V_{ctrl}$  signal reveals:

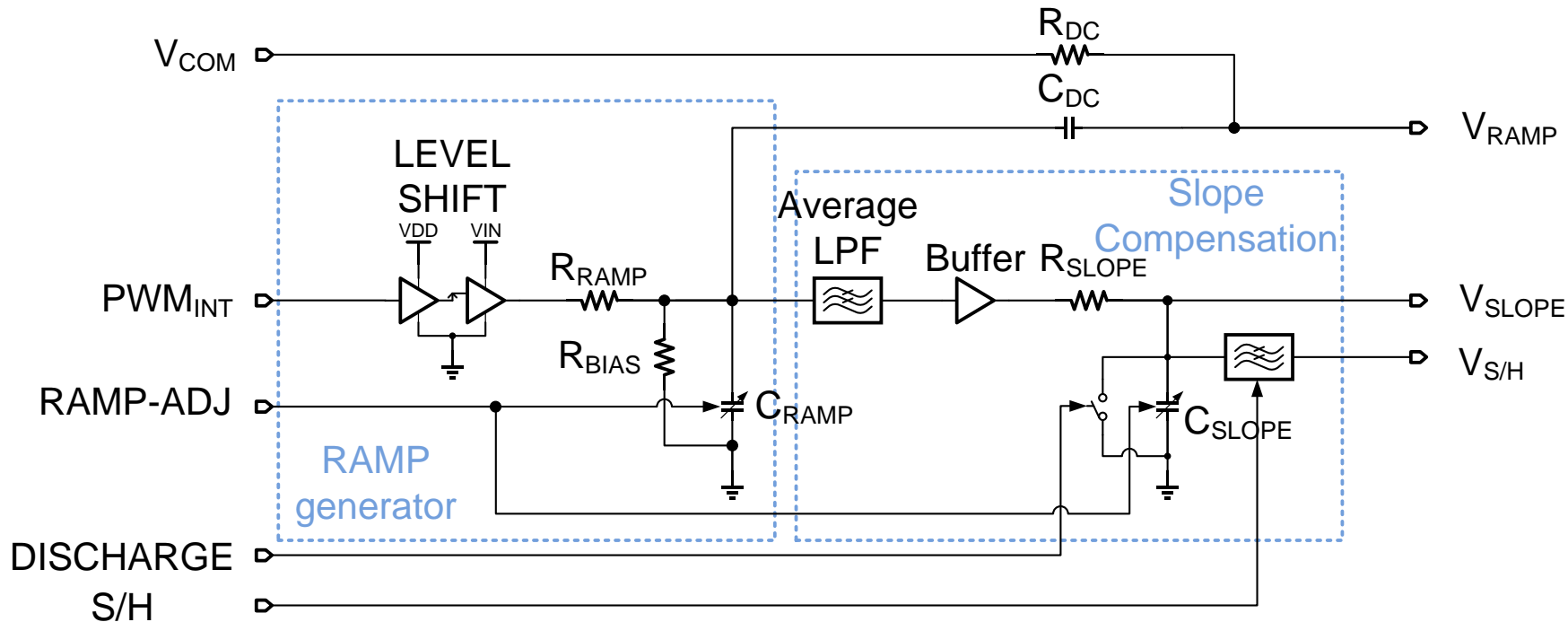
1. A zero with constant gain, K at frequency  $> f_z$
2. Adjusting the gain, K, can affect the bandwidth
3. Set the settling time
4. Set the lowest LC corner frequency limit to design





# RAMP Generator and Slope Compensation TF

- The RAMP generator and slope compensation is shown below



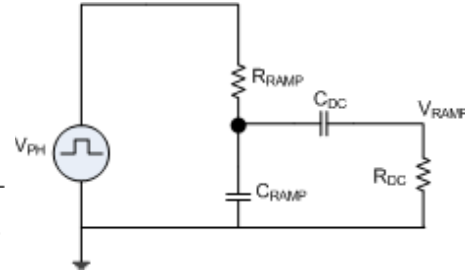
# RAMP and Slope Transfer Function:

## Ramp TF:

$$Z_p(s) := \frac{\frac{1}{s \cdot C_{ramp}} \cdot \left( \frac{1}{s \cdot C_{dc}} + R_{dc} \right)}{\frac{1}{s \cdot C_{ramp}} + \left( \frac{1}{s \cdot C_{dc}} + R_{dc} \right)} \rightarrow V_{zp}(s) := \frac{Z_p(s) \cdot V_{pwm}}{Z_p(s) + R_{ramp}} \rightarrow V_{ramp}(s) := \frac{R_{dc} \cdot V_{zp}(s)}{R_{dc} + \frac{1}{s \cdot C_{dc}}}$$

$$V_{ramp} = \frac{s \cdot C_{dc} \cdot R_{dc} \cdot V_{pwm}}{C_{dc} \cdot R_{dc} \cdot C_{ramp} \cdot R_{ramp} \cdot s^2 + (C_{dc} \cdot R_{dc} + C_{dc} \cdot R_{ramp} + C_{ramp} \cdot R_{ramp}) \cdot s + 1}$$

$$V_{ramp} = \frac{V_{pwm}}{C_{ramp} \cdot R_{ramp} \cdot s + 1}$$



## Slope TF:

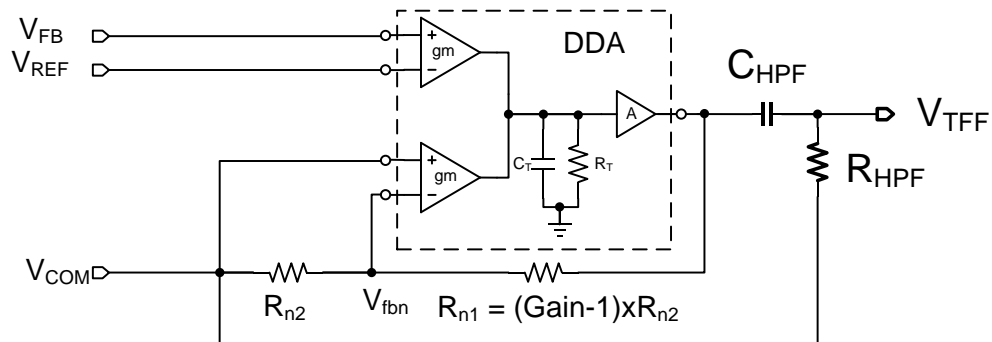
With:  $C_{dc} \cdot R_{dc} > C_{ramp} \cdot R_{ramp}$  and  $f \gg 1$

$$V_{slope} = \frac{1}{s \cdot C_{sl} \cdot R_{sl} + 1} \cdot \frac{V_{pwm} \cdot T_{on}}{2 \cdot T_{sw}}$$

When D is small,  $V_{RAMP} \gg V_{SLOPE}$ ;  $V_{RAMP}$  dominates in the loop transfer function  
Reveal the highest LC frequency at  $C_{ramp} \cdot R_{ramp}$

# Transient Feed Forward TF

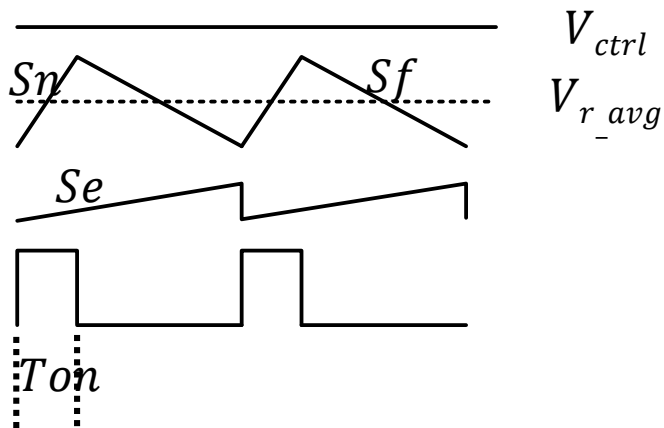
Implementation as  $V_{ctrl}$  and  $V_{COM}$



$$V_{tff}(s) := \frac{R_{n2} + R_{n1}}{R_{n2}} \cdot K_{ddap} \cdot (-V_{ctrl}(s)) \cdot \frac{s \cdot R_{hpf} \cdot C_{hpf}}{s \cdot R_{hpf} \cdot C_{hpf} + 1}$$

$K_{ddap}(1/5)$  is an internal gain of DDA

# FM Gain Derivation



$$V_{ctrl} = V_{r\_avg} + \frac{1}{2} S_n \cdot ton + S_e \cdot ton$$

$$S_n = \frac{dV_{ramp}}{dt} = \frac{V_{in} - V_o}{R_{ramp} \cdot C_{ramp}} \quad S_e = K_{sl} \cdot S_f = K_{sl} \cdot \frac{dV}{dt} = K_{sl} \cdot \frac{V_o}{R_{ramp} \cdot C_{ramp}}$$

Perturbation and Linearization:

$$V_{in} = V_{IN} + \hat{v}_{in}$$

$$d = D + \hat{d}$$

$$FM = \frac{1}{\frac{1 \cdot T_{sw}}{R_{ramp} \cdot C_{ramp}} \cdot ((0.5 - D) + 2 \cdot D \cdot K_{sl})}$$

# Sampling TF

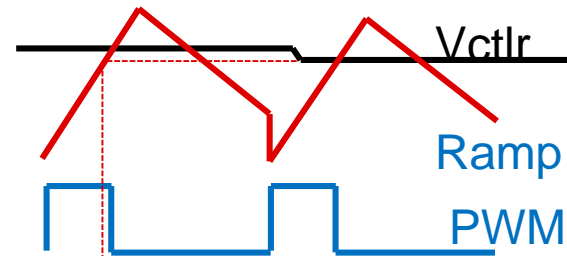
- Sampling refers to only one D per switching cycle.
- Need to transform back to continuous-time representation by zero-order-hold:

$$H_{zoh}(s) = \frac{1 - e^{-s \cdot T_{sw}}}{s \cdot T_{sw}} \quad \leftarrow \text{Like PWM signal}$$

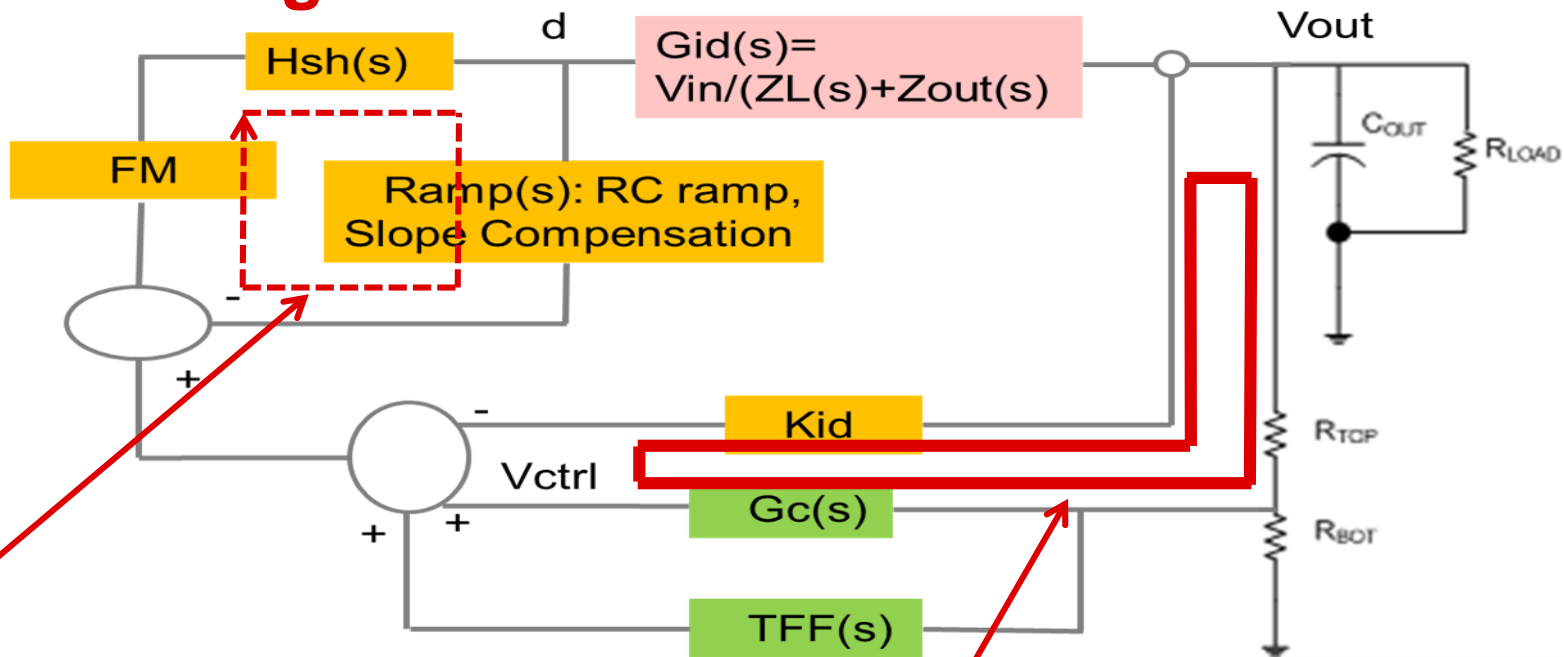
$$\frac{FM \cdot H_{sh}}{1 + FM \cdot V_{ramp\_total} \cdot H_{sh}} \cdot V_{ctrl} = \frac{1 - e^{-s \cdot T_{sw}}}{s \cdot T_{sw}}$$

$$H_{sh}(s) = \frac{1 - e^{-s \cdot T_{sw}}}{(s \cdot T_{sw} + e^{-s \cdot T_{sw}} - 1)} \frac{(0.5 - D + 2 \cdot D \cdot K_{sl}) \cdot T_{sw} \cdot s}{V_{pwm} + 1.29 \cdot V_{ramp\_avg}}$$

- Refer to Jiwei Fan's paper: [Design and Characterization of DE-DRC for Step-Down Converter](#)
- Refer to F. Dong Tan and R.D. Middlebrook paper: [A Unified Model of Current Programmed Converters](#)



# ACM Block Diagram to TF



$$TF_{loop1}(s, V_{in}) := \frac{(FM(V_{in}) \cdot H_{sh}(s, V_{in}))}{1 + FM(V_{in}) \cdot H_{sh}(s, V_{in}) \cdot (V_{ramp}(s) + V_{slope}(s, V_{in}))}$$

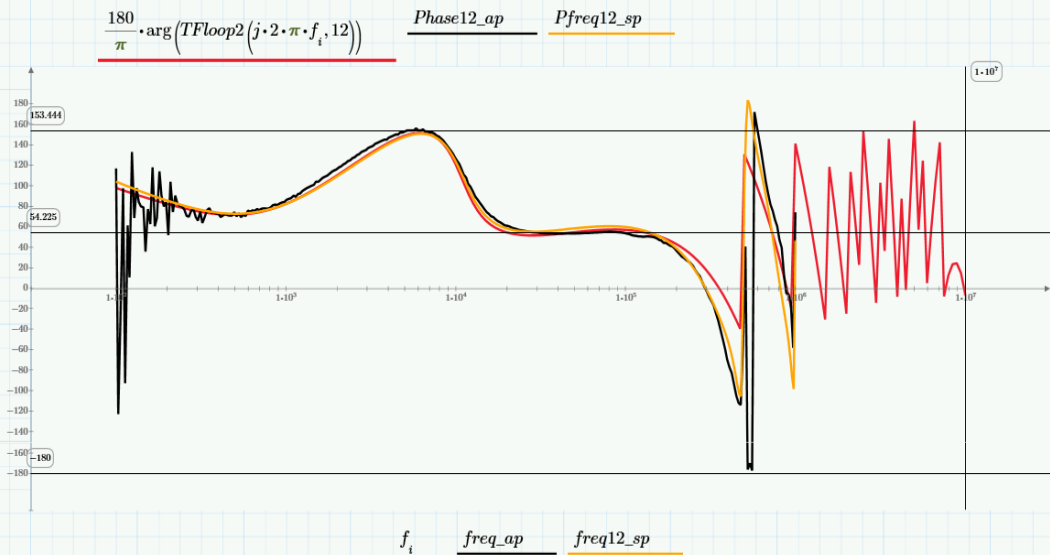
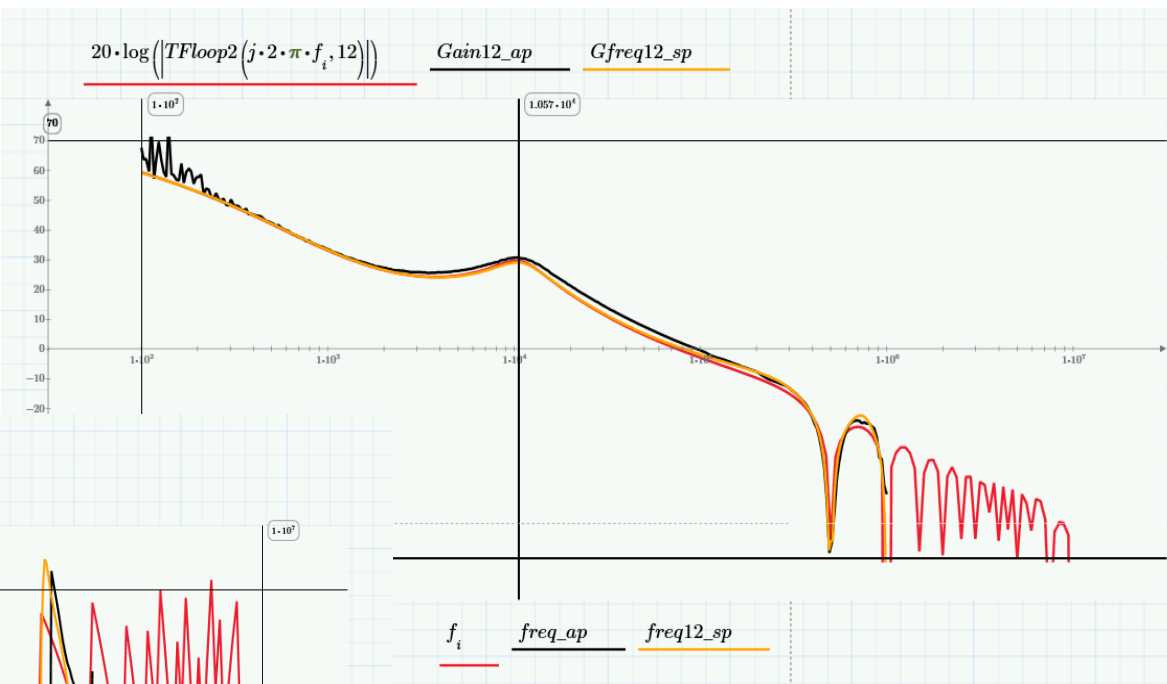
$$TF_{loop2}(s, V_{in}) := \frac{TF_{loop1}(s, V_{in}) \cdot G_{id}(s, V_{in}) \cdot Z_{out}(s)}{1 + TF_{loop1}(s, V_{in}) \cdot G_{id}(s, V_{in}) \cdot Kid} \cdot ((V_{ctrl}(s) - V_{tff}(s)))$$

# Comparison

Lab Data by AP

Simplis Data

Model



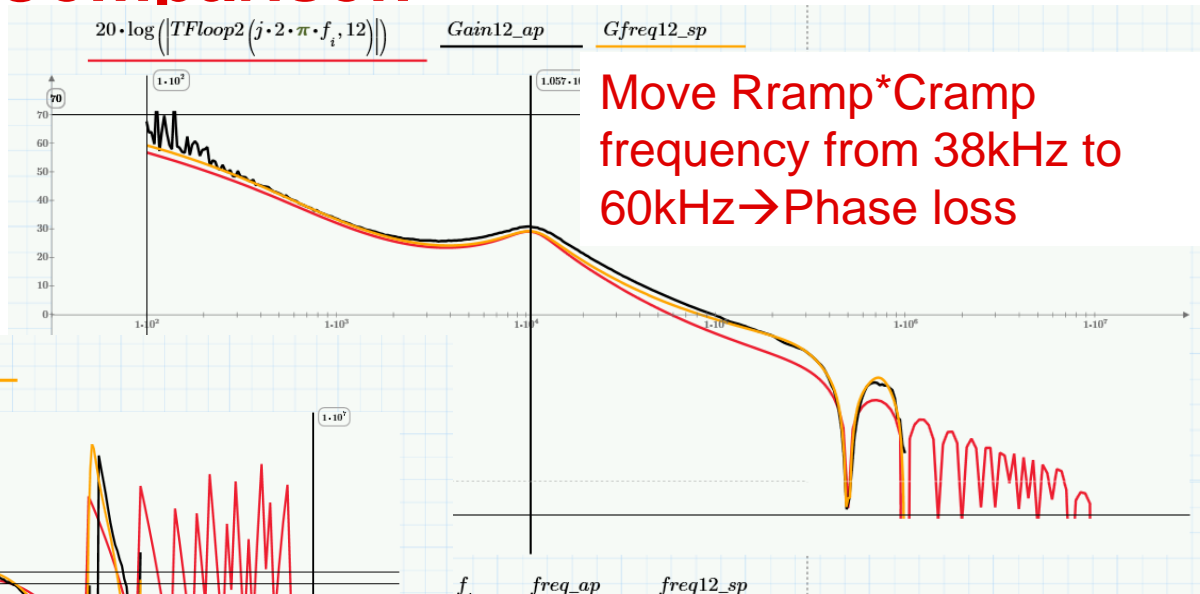
Vin = 12V, 0.9Vout, 500kHz,  
470nH/0.16mOhm, 1x330uF(1.5mOhm)+  
150uF (0.7mOhm)  
Cramp = 14.1pF

# Cramp Parameter Comparison

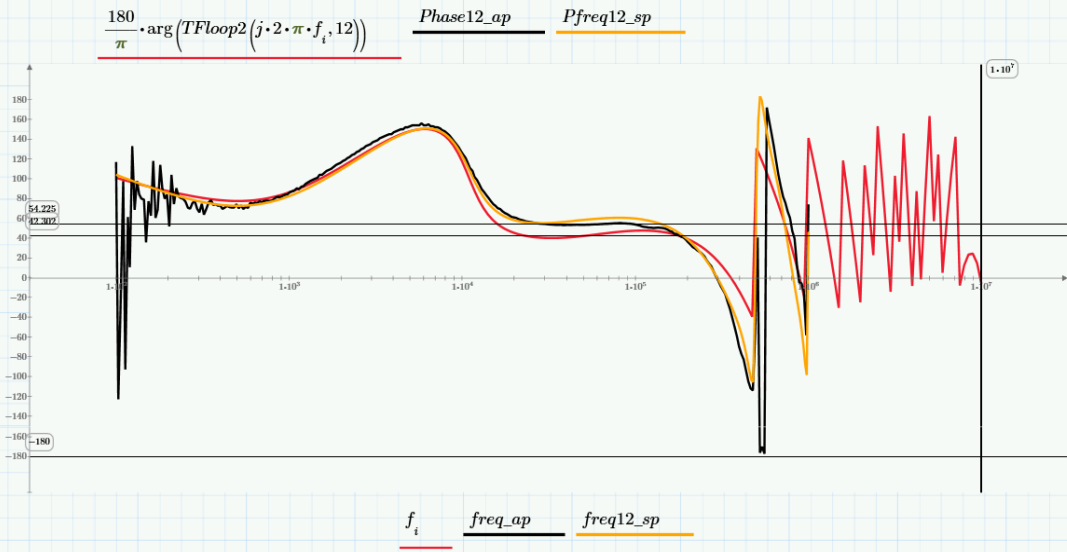
Lab Data by AP : Cramp = 14.1pF

Simplis Data: Cramp = 14.1pF

Model: Cramp = 8.91pF



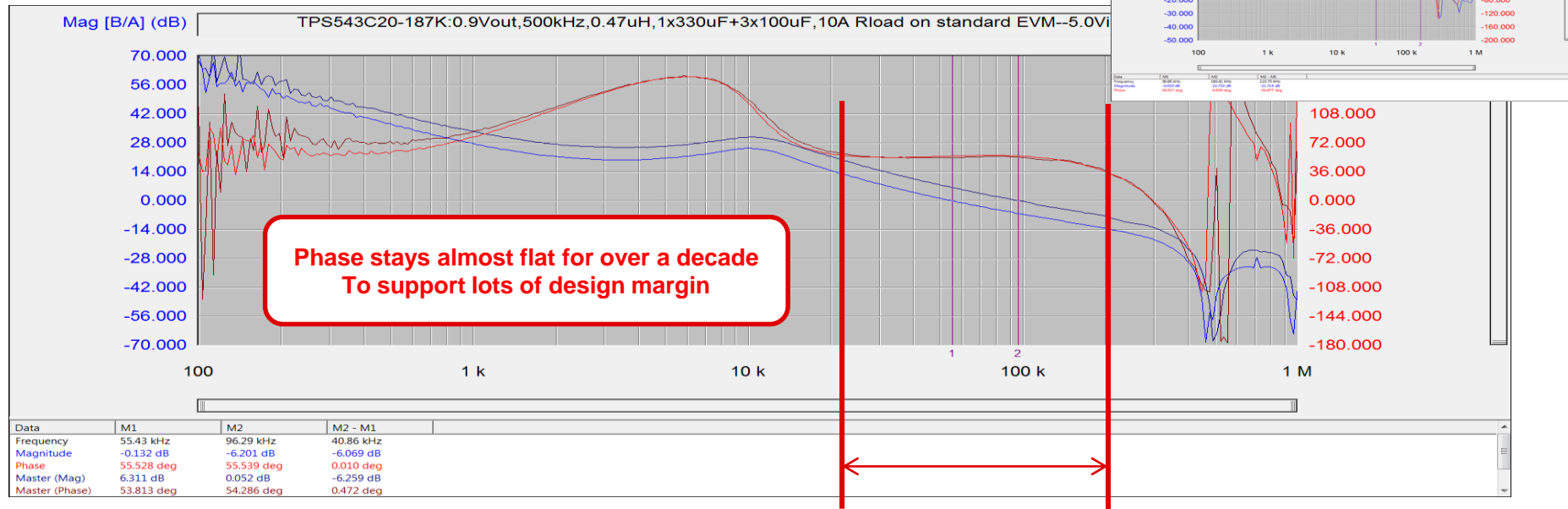
Vin = 12V, 0.9Vout, 500kHz,  
 470nH/0.16mOhm,  
 1x330uF(1.5mOhm)+ 150uF  
 (0.7mOhm)  
 Cramp = 14.1pF  
 Cramp = 8.91pF (Model)



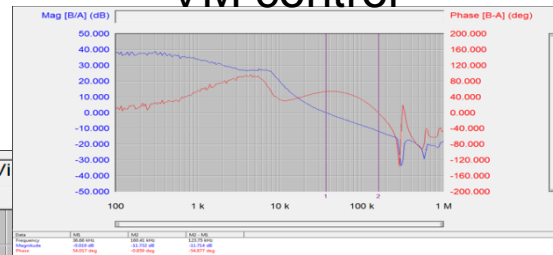


# ACM's Constant Phase Character

0.9V, 500kHz, 10A Load and  $V_{in} = 5V$  vs. 12V

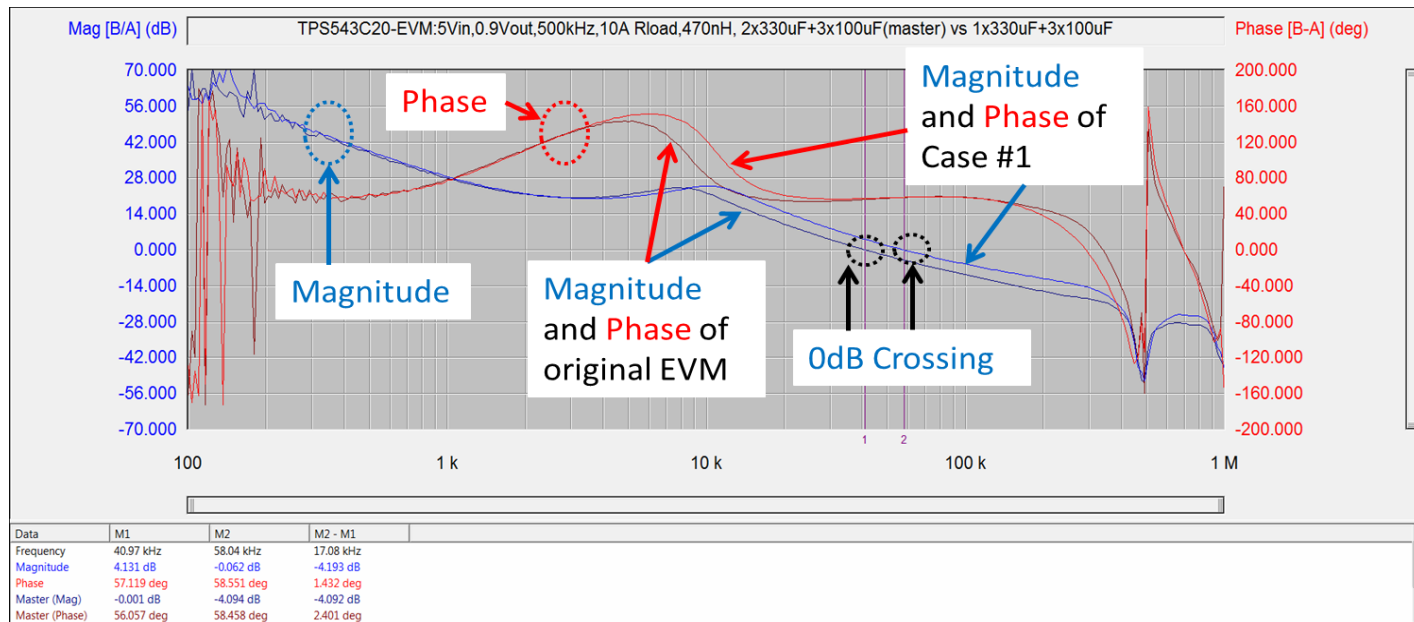


VM control



# ACM's Constant Phase Character

5Vin, 0.9Vout, 500kHz, 10A Load: 1/3 Output Capacitor Reduction

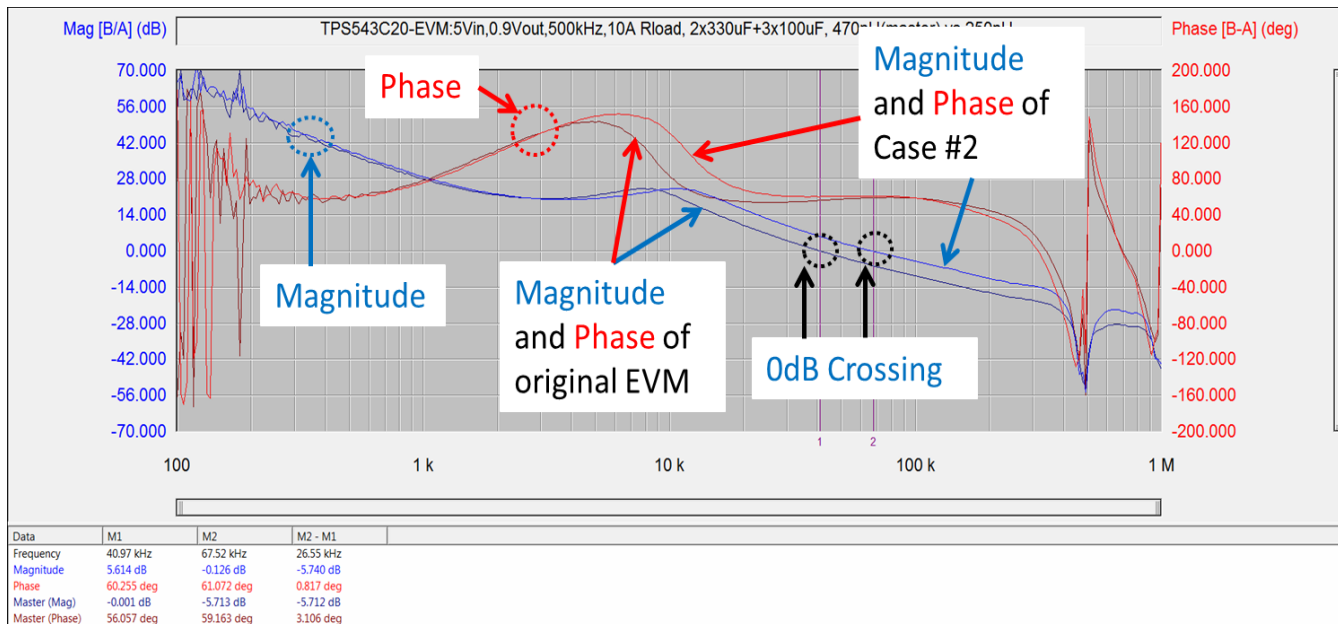


Original Configuration:  $L=470\text{nH}$ ,  $C_{out}=2 \times 330\mu\text{F} + 3 \times 100\mu\text{F}$

**Case 1** Configuration:  $L=470\text{nH}$ ,  $C_{out}=1 \times 330\mu\text{F} + 3 \times 100\mu\text{F}$

# ACM's Constant Phase Character

5Vin, 0.9Vout, 500kHz, 10A Load: 1/2 Output Inductor Reduction

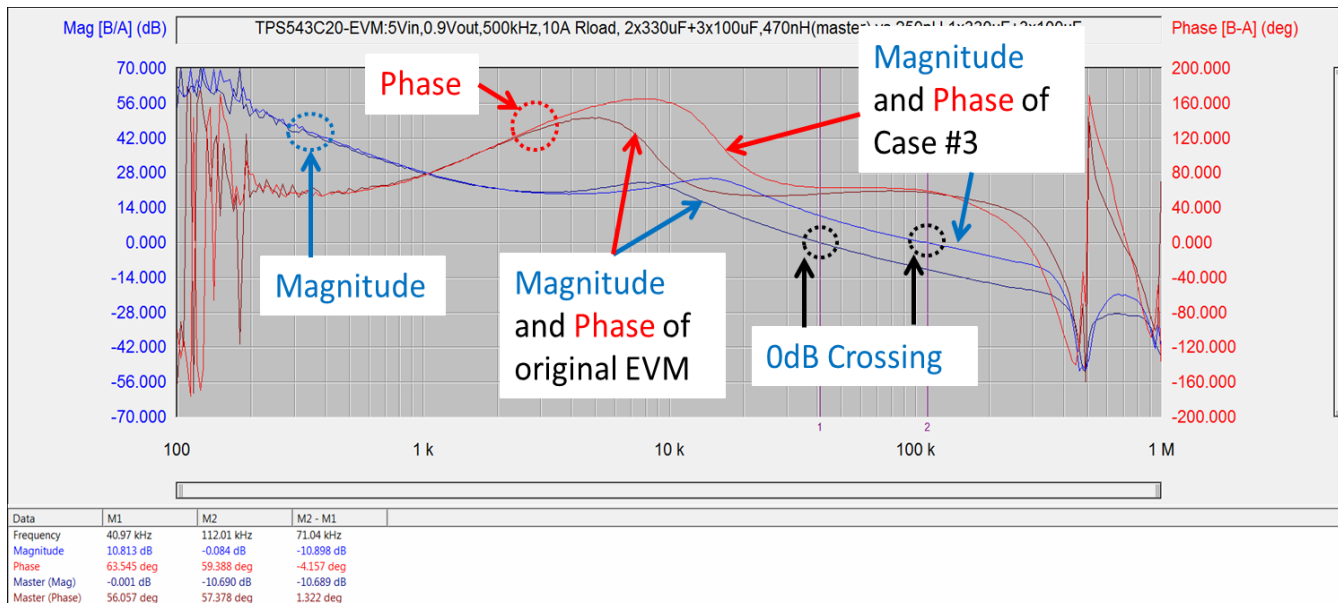


Original Configuration:  $L=470\text{nH}$ ,  $C_{out}=2\times 330\mu\text{F} + 3\times 100\mu\text{F}$

Case 2 Configuration:  $L=250\text{nH}$ ,  $C_{out}=2\times 330\mu\text{F} + 3\times 100\mu\text{F}$

# ACM's Constant Phase Character

5Vin, 0.9Vout, 500kHz, 10A Load: 1/2 Output Inductor and 1/3 Cout Reduction



Original Configuration:  $L=470\text{nH}$ ,  $C_{out}=2 \times 330\mu\text{F} + 3 \times 100\mu\text{F}$

Case 3 Configuration:  $L=250\text{nH}$ ,  $C_{out}=1 \times 330\mu\text{F} + 3 \times 100\mu\text{F}$

# TPS543C20 Overview and Comparison

# TPS543C20

## 4.0Vin to 16Vin, 40A Stackable, Fixed-Fsw Synchronous Step-Down SWIFT™ Converter



### Features

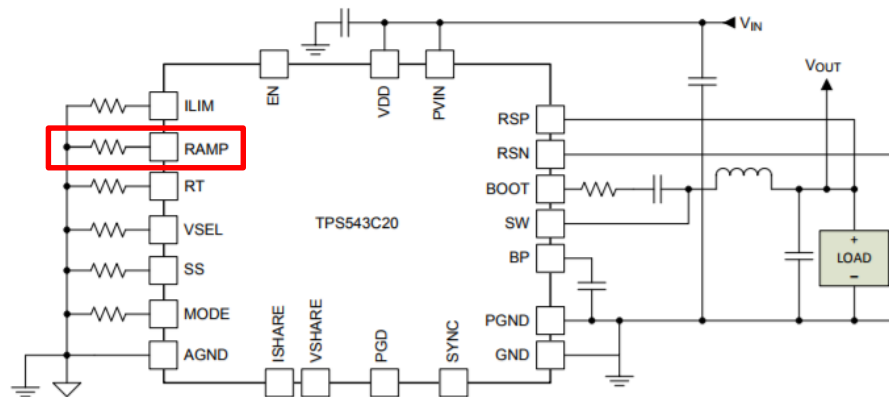
- Output Voltage Range 0.6V to 5.5V
- **Advanced Current Mode (ACM) True Fixed Frequency with CLK Synchronization**
- Low R<sub>dson</sub>: ~3.0/0.9mΩ;
- **2-phase stackable** with Ishare, Vshare, Fsync
- **Fully Differential Remote Voltage Sense**
- 10 V<sub>ref</sub> choices: 0.6V; 0.7 to 1.1V in 50mV steps
- 10 SS choices: 0.5, 1, 2, 4, 5, 8, 12, 16, 24, 32ms
- Adj. Fsw: 300Khz to 2MHz (1Ph) /1MHz (2+ Ph)
- **High accuracy Over Current Limit (Hiccup I-lim)**
- **Asynchronous Pulse Injection (API) / Body Braking**
- 5x7x1.5mm, 0.5mm pitch 40 pin Stacked Clip QFN

### Applications

- Communications RRU, Switches, Routers
- Enterprise Computing, Servers, Datacom
- ASIC, SoC, FPGA, DSP core and I/O Voltage Rails
- High-Power Programmable Logic Controllers

### Benefits

- Fixed Frequency with No External Compensation for a wide range of switching frequencies
- 90+% efficiency over a wide load range
- Up to 80A POL needs with flexible sync positions
- +/-0.5% setpoint accuracy over temperature
- High accuracy for multiple V<sub>out</sub>
- Optimize for efficiency or BOM size by adjusting frequency
- +/-10% I-lim Accuracy over temp & process
- Option to better manage undershoot/ overshoot



# TPS543B20

## 4.0Vin to 18Vin, 25A Stackable, Fixed-Fsw Synchronous Step-Down SWIFT™ Converter



### Features

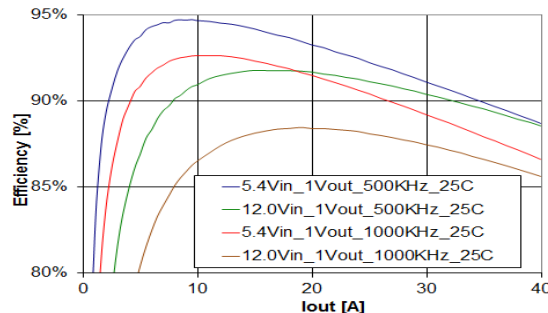
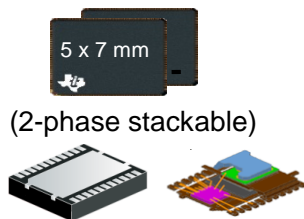
- Output Voltage Range 0.6V to 5.5V
- **Advanced Current Mode (ACM) True Fixed Frequency with CLK Synchronization**
- Low R<sub>dson</sub>: ~4.1/1.9mΩ;
- **2-phase stackable** with Ishare, Vshare, Fsync
- **Fully Differential Remote Voltage Sense**
- 10 V<sub>ref</sub> choices: 0.6V; 0.7 to 1.1V in 50mV steps
- 10 SS choices: 0.5, 1, 2, 4, 5, 8, 12, 16, 24, 32ms
- Adj. Fsw: 300Khz to 2MHz (1Ph) /1MHz (2+ Ph)
- **High accuracy Over Current Limit (Hiccup I-lim)**
- **Asynchronous Pulse Injection (API) / Body Braking**
- 5x7x1.5mm, 0.5mm pitch 40 pin Stacked Clip QFN

### Applications

- Communications RRU, Switches, Routers
- Enterprise Computing, Servers, Datacom
- ASIC, SoC, FPGA, DSP core and I/O Voltage Rails
- High-Power Programmable Logic Controllers

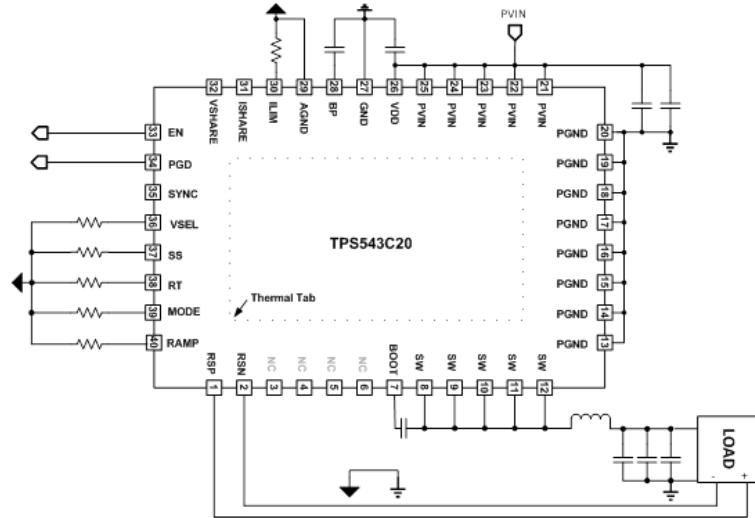
### Benefits

- Fixed Frequency with No External Compensation for a wide range of switching frequencies
- 90+% efficiency over a wide load range
- Up to 80A POL needs with flexible sync positions
- +/-0.5% setpoint accuracy over temperature
- High accuracy for multiple V<sub>out</sub>
- Optimize for efficiency or BOM size by adjusting frequency
- +/-10% I-lim Accuracy over temp & process
- Option to better manage undershoot/ overshoot



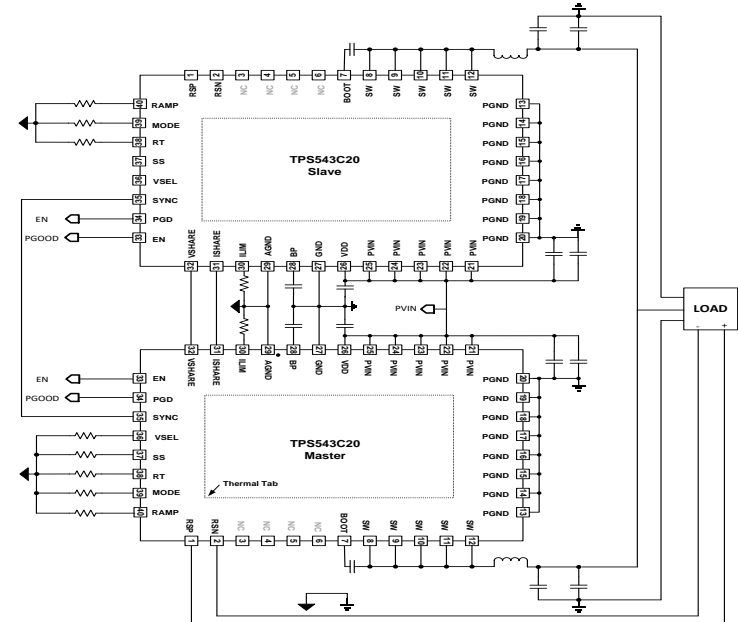
# Simplified Application Schematic

## Stand-alone Configuration



- No external compensation, Ramp pin sets internal compensation
- Adjustable Vref, SS, OC, Fsw by pin-strapping

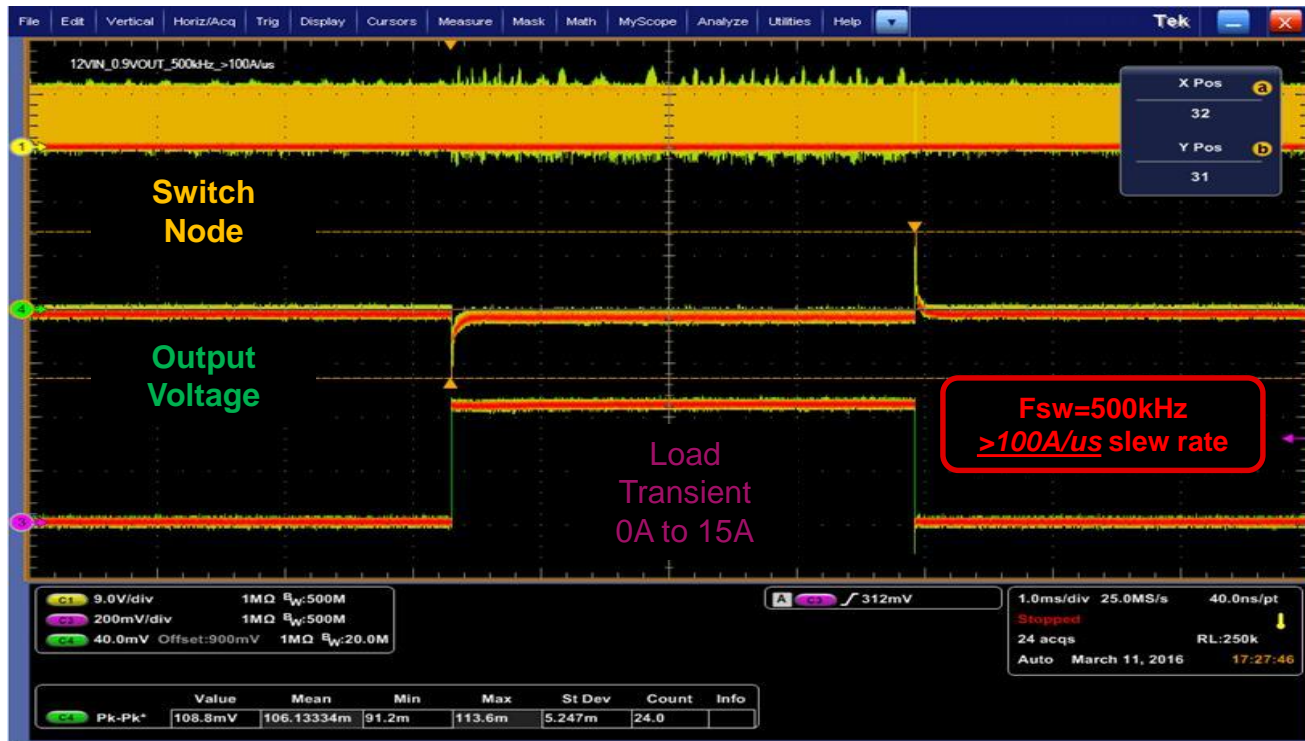
## Stackable Configuration



- Two phase interleaving, reduce input/output filters
- Layout friendly for two devices
- Pin-strap only programmed on Master



# Fast Load Transient Response



# High Switching Frequency Operation

12Vin, 0.9Vout, 20A load, 2MHz switching frequency



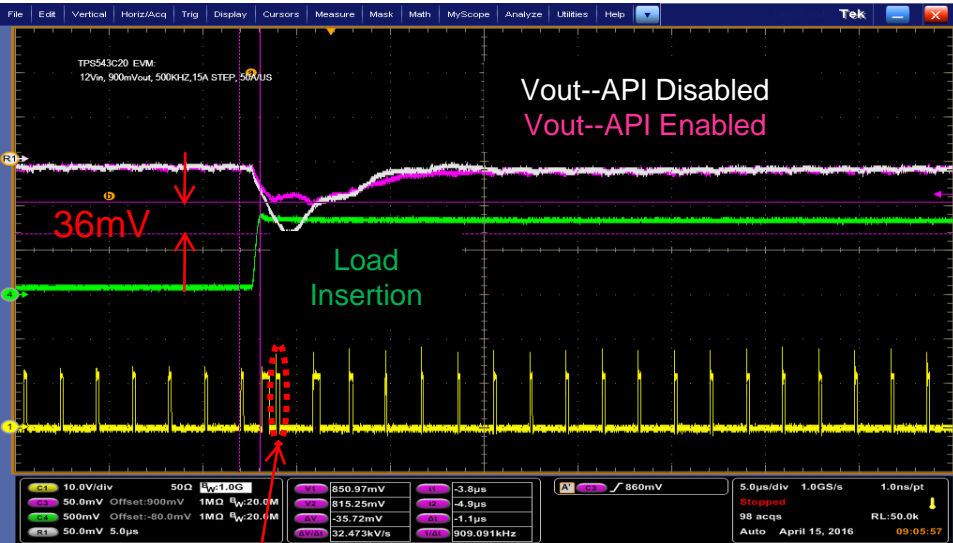
37.5ns Ton



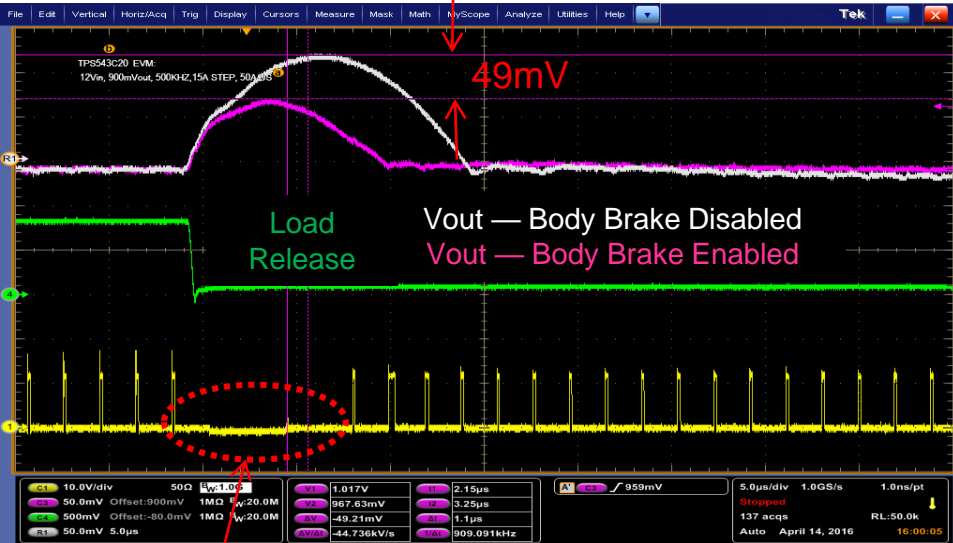
Very Small Switching Jitter

# Asynchronous Pulse Injection and Body Brake

## Further Improving Transient Performance



API—Undershoot Reduction



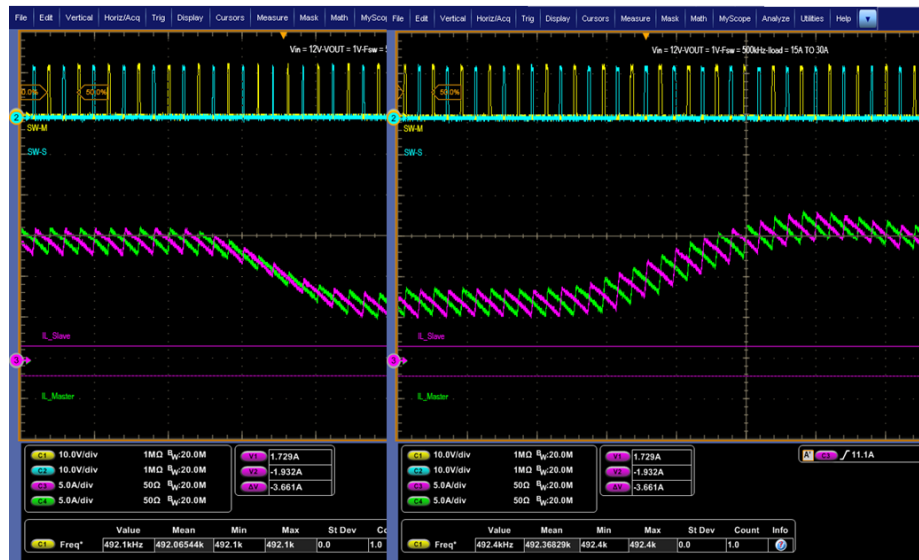
Body Brake—Overshoot Reduction

# Current Balancing in a Stackable Application

12Vin, 0.9Vout, 40A load, 500kHz switching frequency

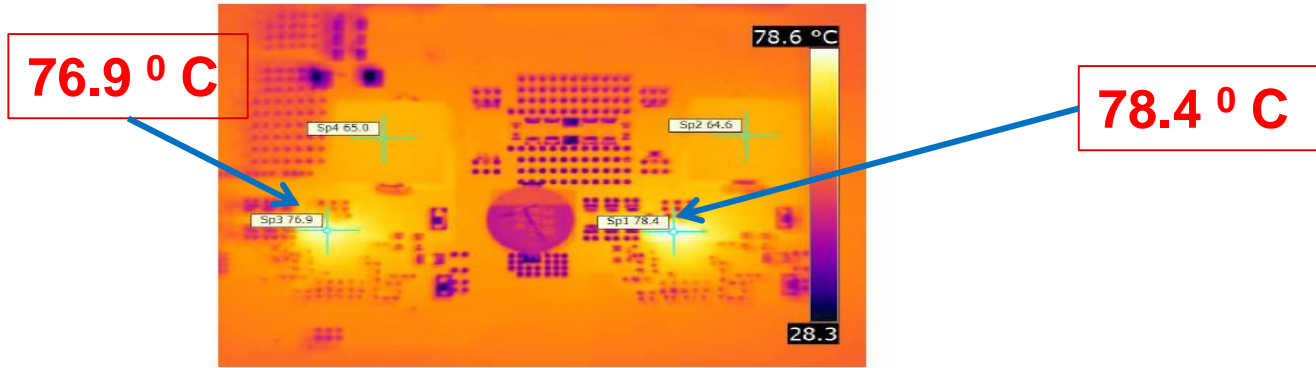


Current balance during steady state



Current balance during transient

# 2-Phase Stackable Thermal: 275Watts Output



### Image and Object Parameters

Camera Model	FLIR T300
Image Date	11/9/2016 11:35:06 PM
Image Name	IR_0208.jpg
Emissivity	0.95
Reflected apparent temperature	20.0 °C
Object Distance	1.0 ft

### Text Comments

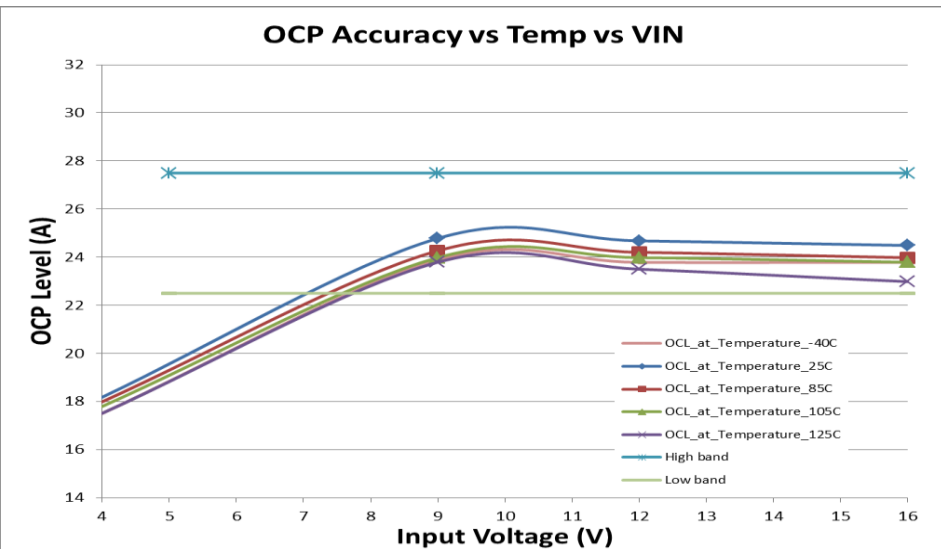
Sp1=IC1	78.4C
Sp2=Inductor1	64.6C
Sp3=IC2	76.9C
Sp4=Inductor2	65C

### Description

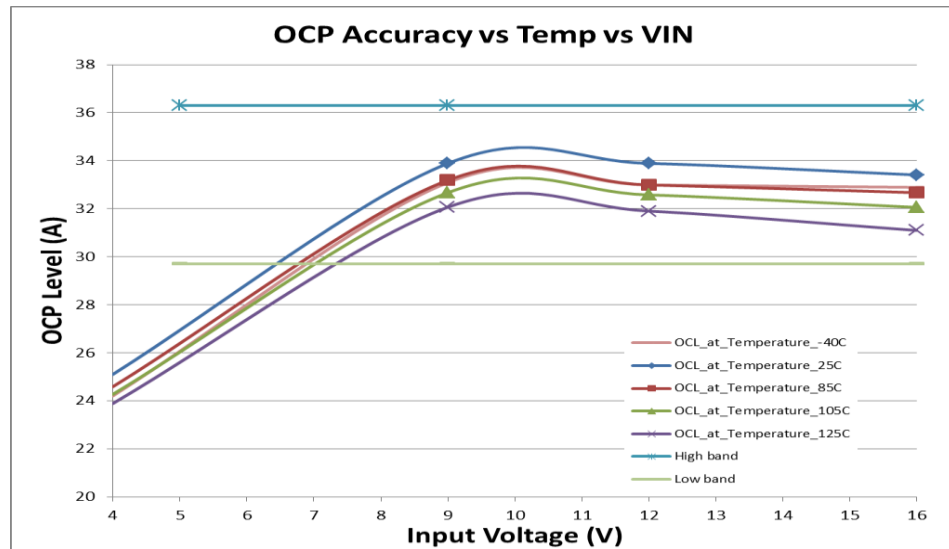
Vin=12V, Vout=5V, Iout=55A, Fsw=500kHz, Ta=room

# TPS543C20 Over Current Protection Accuracy

Tight current limit accuracy over temperature



24A Load Accuracy



33A Load Accuracy

# Control Mode Comparison

## TPS548D22

### Overview

- $V_{IN}$  4.5 – 16V
- $I_{OUT}$  40A
- $R_{dson}$ : 2.9-m $\Omega$ /1.2-m $\Omega$
- FSW: 425/50/875/1050kHz
- Control Mode: D-CAP3™

### Advantages

- No external compensation required
- Fast transient response

### Disadvantages

- Frequency jitter
- Limited  $V_{OUT}$  range: 0.6 – 5.5V

### Applications

- **Enterprise and Server**  
where there are fewer noise-sensitive analog components
- Low voltage processors that need **high accuracy** and **fast load transients**.

## TPS543C20

### Overview

- $V_{IN}$  4 – 14V
- $I_{OUT}$  40A
- $R_{dson}$ : 3.0-m $\Omega$ /0.9-m $\Omega$
- FSW: 300kHz – 2MHz
- Control Mode: ACM with Sync

### Advantages

- Fast transient response
- Low jitter fixed frequency operation
- No external compensation required

### Disadvantages

- Limited  $V_{OUT}$  range: 0.6 – 5.5V

### Applications

- **Communications and Industrial**  
applications where many signal chain devices are used.
- **Enterprise and Server**  
high power density and fast transient

## Competitive Voltage Mode

### Overview

- $V_{IN}$ : 5 – 21V
- $I_{OUT}$ : 35A
- $R_{dson}$ : 3.1-m $\Omega$ /1.27-m $\Omega$
- FSW: 300kHz to 1.5MHz
- Control Mode: VM w/  $V_{IN}$  Feedforward

### Advantages

- Low jitter fixed frequency operation
- Control loop is tunable adding flexibility for filter components
- Supports higher duty cycles

### Disadvantages

- Lack of remote sense
- Requires external compensation

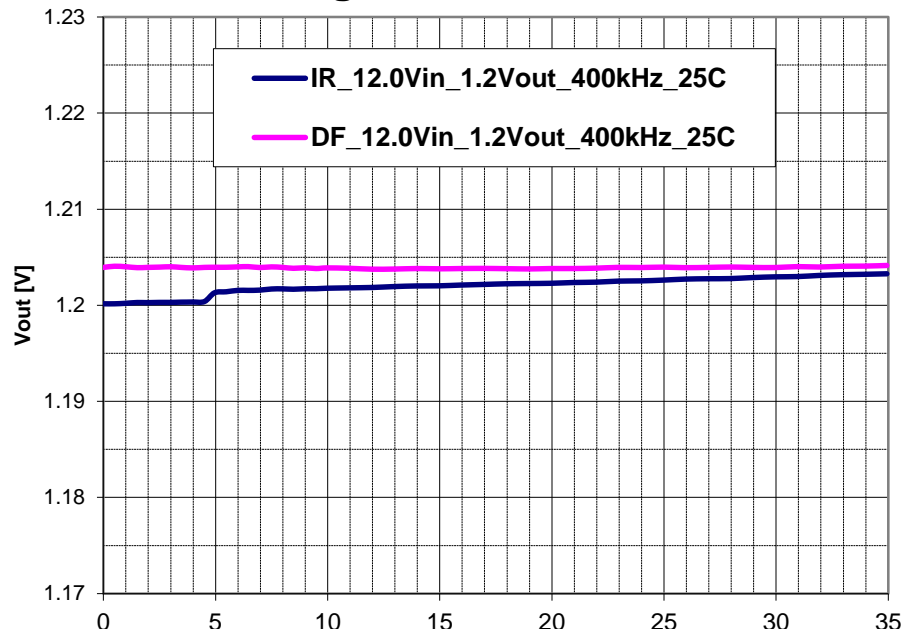
### Applications

- **Communications and Industrial**  
applications where many signal chain devices are used.

# TPS543C20 vs Competitive VM Comparison

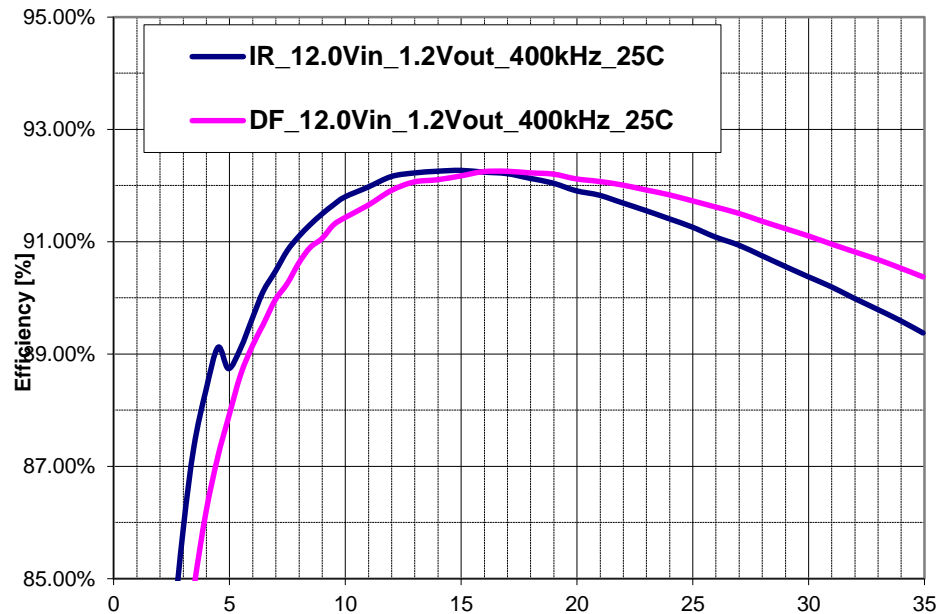
DC Performance: L=470nH, Cout=6x100uF

## Load Regulation Performance



IR3846 doesn't have remote sense

## Efficiency Performance



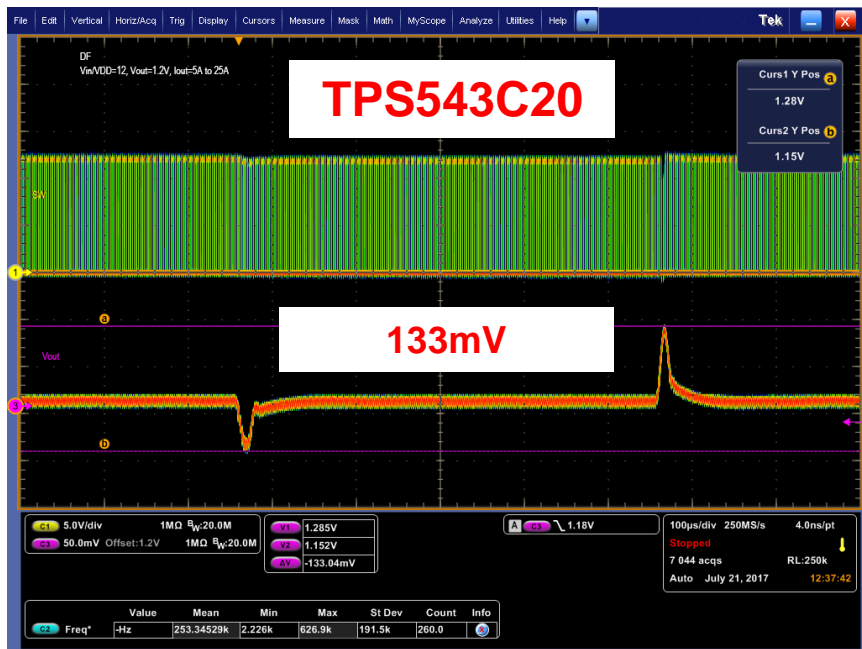
TPS543C20 has >1% higher efficiency at 35A  
~0.4W



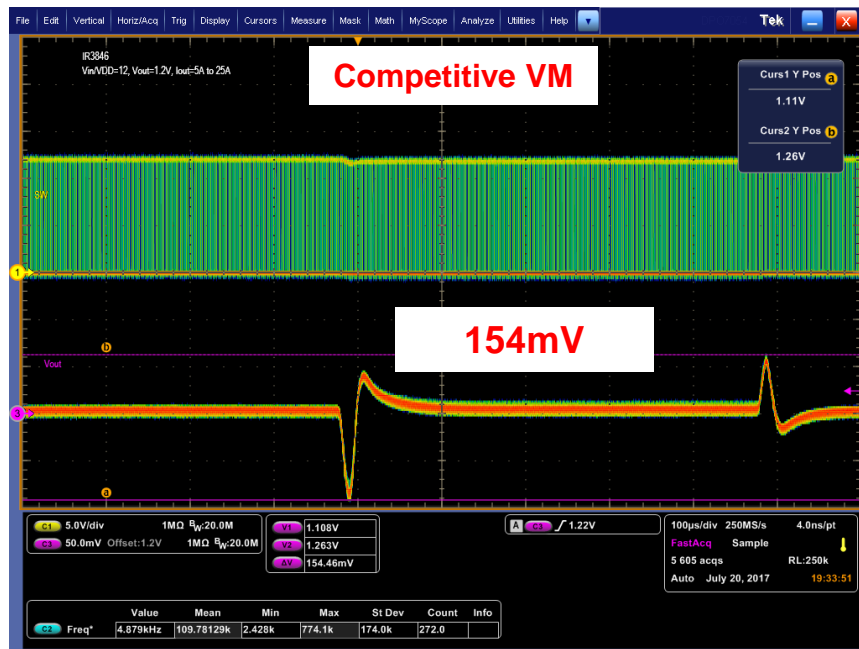
# TPS543C20 vs IR3846 Comparison

## Transient Performance

Vin=12V, Vout=1.2V, Fsw=400kHz, L=470nH, Cout=6x100uF, Iout=5A to 25A@2.5A/us

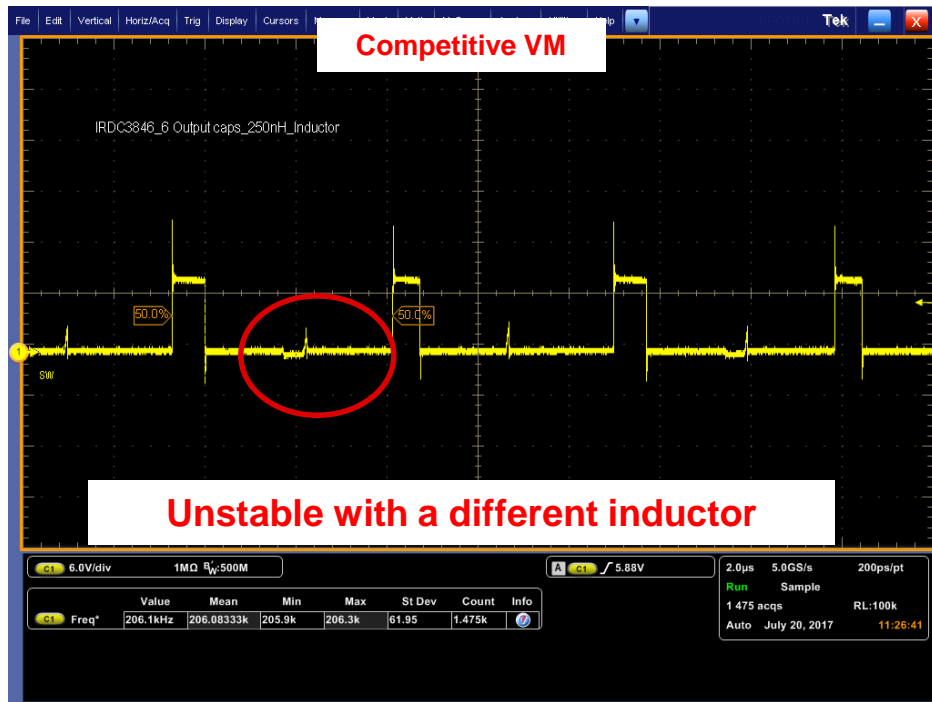


TPS543C20 only needs 1 resistor for internal compensation



Needs complicated TYPE III network

# Low Tolerance on Components Variation



- The voltage mode controlled device showed instability when modifying the inductor from 470nH to 250nH. The compensation needs to be re-designed
- ACM tolerates design variations better without the need to change compensation

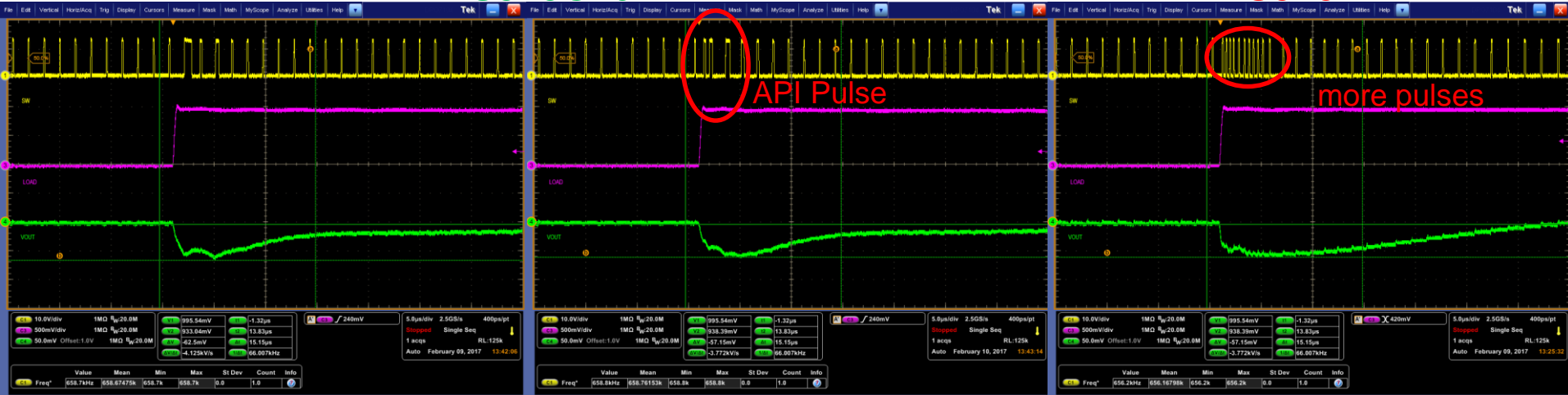
# TPS543C20 vs TPS548D22 Comparison

## Transient Performance—Undershoot

Vin=12V, Vout=1.2V, Fsw=650kHz, L=470nH, Cout=2x330uF+3x100uF, Iout=5A to 25A@50A/us

TPS543C20

TPS548D22



Without API: Undershoot = 62.5mV

With API: Undershoot = 57.2mV

With API: Undershoot = 57.2mV

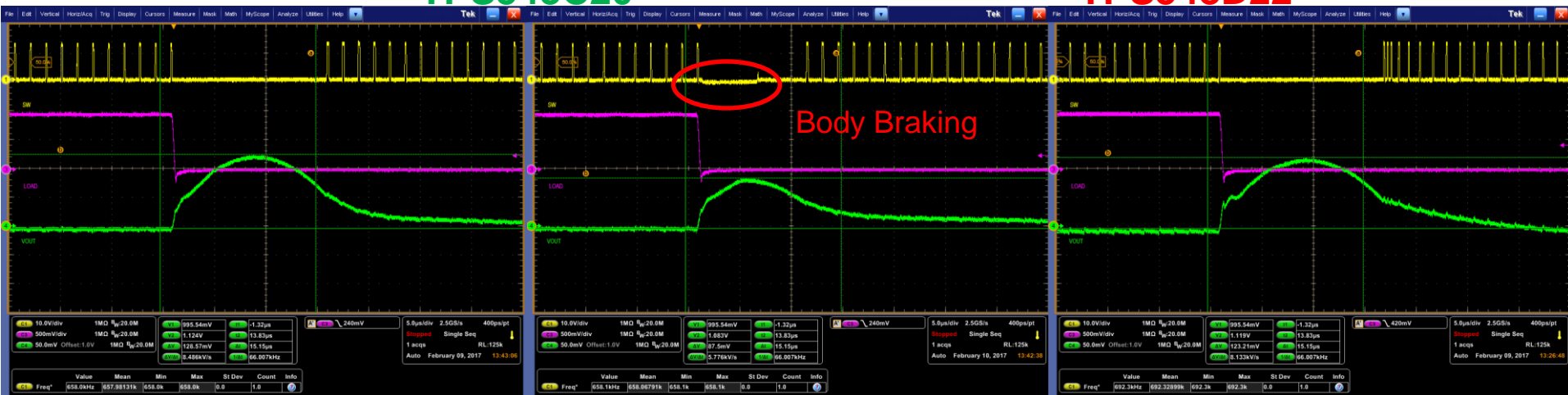
# TPS543C20 vs TPS548D22 Comparison

## Transient Performance—Overshoot

$V_{in}=12V$ ,  $V_{out}=1.2V$ ,  $F_{sw}=650kHz$ ,  $L=470nH$ ,  $C_{out}=2 \times 330\mu F + 3 \times 100\mu F$ ,  $I_{out}=5A$  to  $25A @ 50A/\mu s$

TPS543C20

TPS548D22



Without API: Undershoot = 128.6mV

With API: Undershoot = 87.5mV

With API: Undershoot = 123mV

# Summary

- ACM provides the fixed frequency advantage of Voltage Mode or Current Mode Control
- ACM does not need loop compensation, like constant on time or D-CAP converters
- ACM simulations compare well with actual lab measurements
- ACM will be used in future products from Texas Instruments to simplify a high performance point-of-load solution