TECH DAYS
Texas Instruments

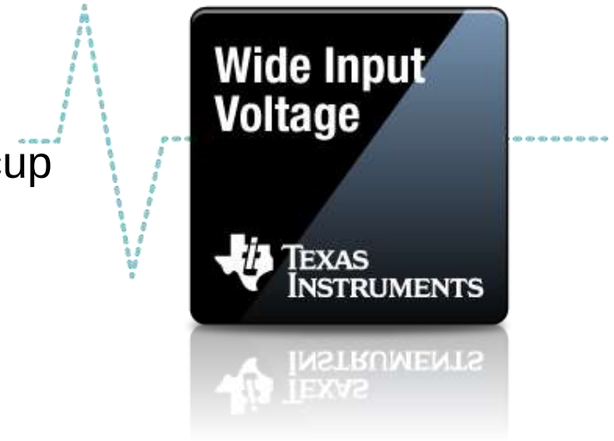
Bucks: What are all these features?

Buck Switching Regulators

Katelyn Wiggenhorn

Summary

- Monitor Operating Voltages
  - EN/UVLO
  - RESET/PGOOD
  - Soft Start
- 2) Operation Considerations
  - Operation over I_{OUT}: PFM, Auto Freq. Foldback, Current Limit & Hiccup
  - Operation over V_{IN}: Dropout, Freq Foldback
  - Light-load efficiency and calculations: Iq
- 3) EMI
  - Package and Pinout
  - Spread Spectrum Feature



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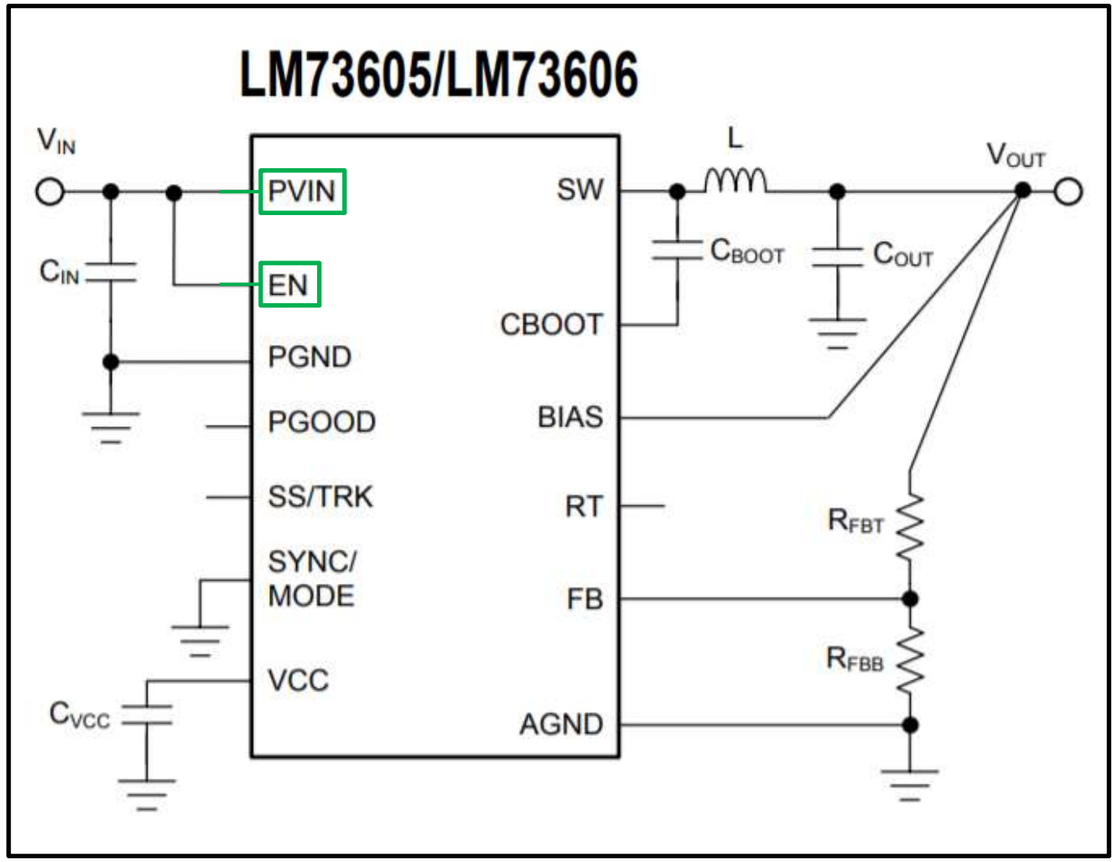
Basic Features:
EN/UVLO, Soft Start, Reset/PGOOD

UVLO

- **UVLO** – Disables IC at Under-Voltage Conditions

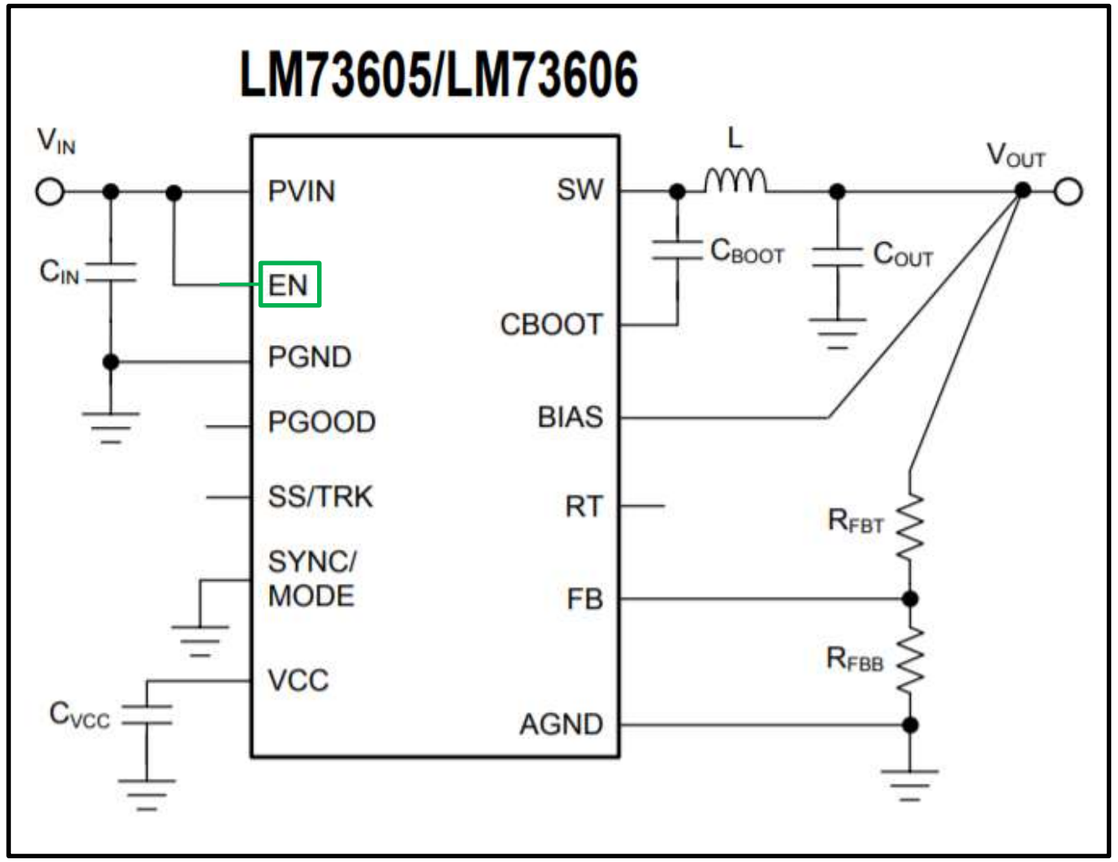
- Many types of UVLO may be featured in your converter/controller:
  - Internal LDO UVLO
    - Correlates with VIN Min spec
  - VIN UVLO – Use EN and resistors
    - Discussed in next slide



ENABLE

- **EN** - Used to enable and disable IC

- Options:
  - Connect EN to VIN to turn on the converter/controller when power is applied
  - Connect EN to VIN through a resistor divider to utilize UVLO
  - Connect EN to a controlled signal to externally sequence power-on of the IC.



ENABLE/UVLO Example

- EN Threshold for VOUT = 1.25V$_{Max}$
- VIN = 36V
- UVLO$_{Desired}$ = 12V

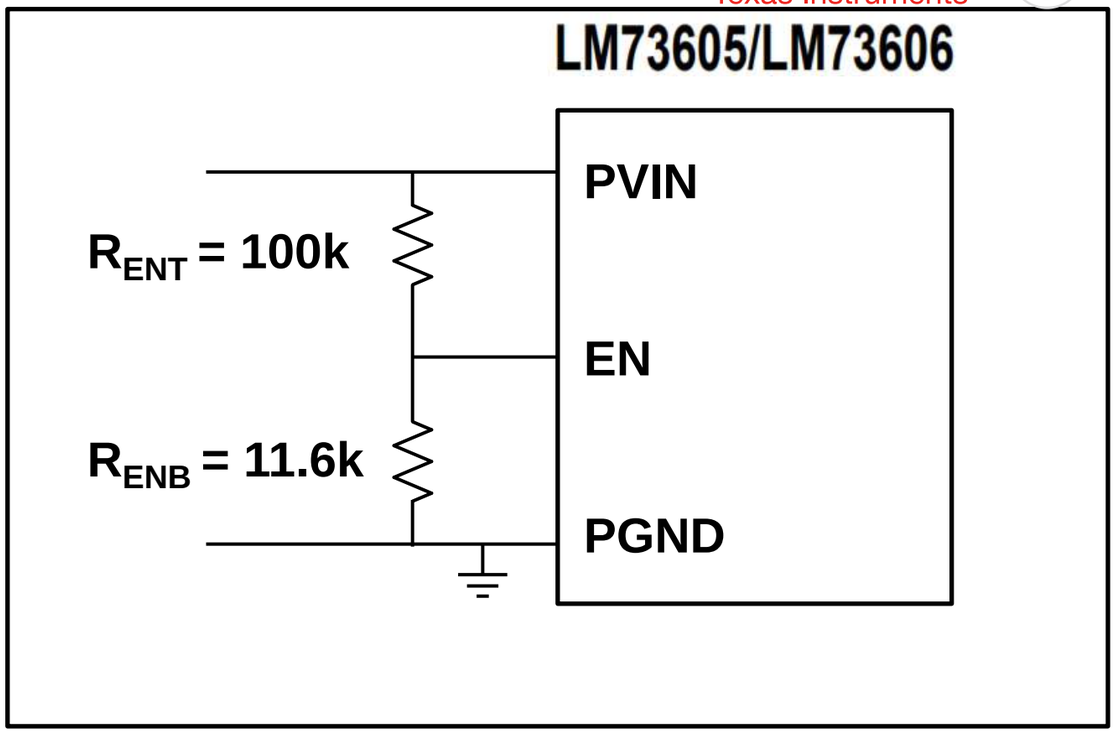
- Choose R_{ENT}=100k
- Calculate R_{ENB} from datasheet
  - $V_{EN\_VOUT\_H}$ = 1.25V
  - $V_{IN\_ON\_H}$ = 12V

- Larger resistance decreases power loss in resistors
- Smaller resistance decreases noise susceptibility

$$R_{ENB} = \frac{V_{EN\_VOUT\_H}}{V_{IN\_ON\_H} - V_{EN\_VOUT\_H}} R_{ENT}$$

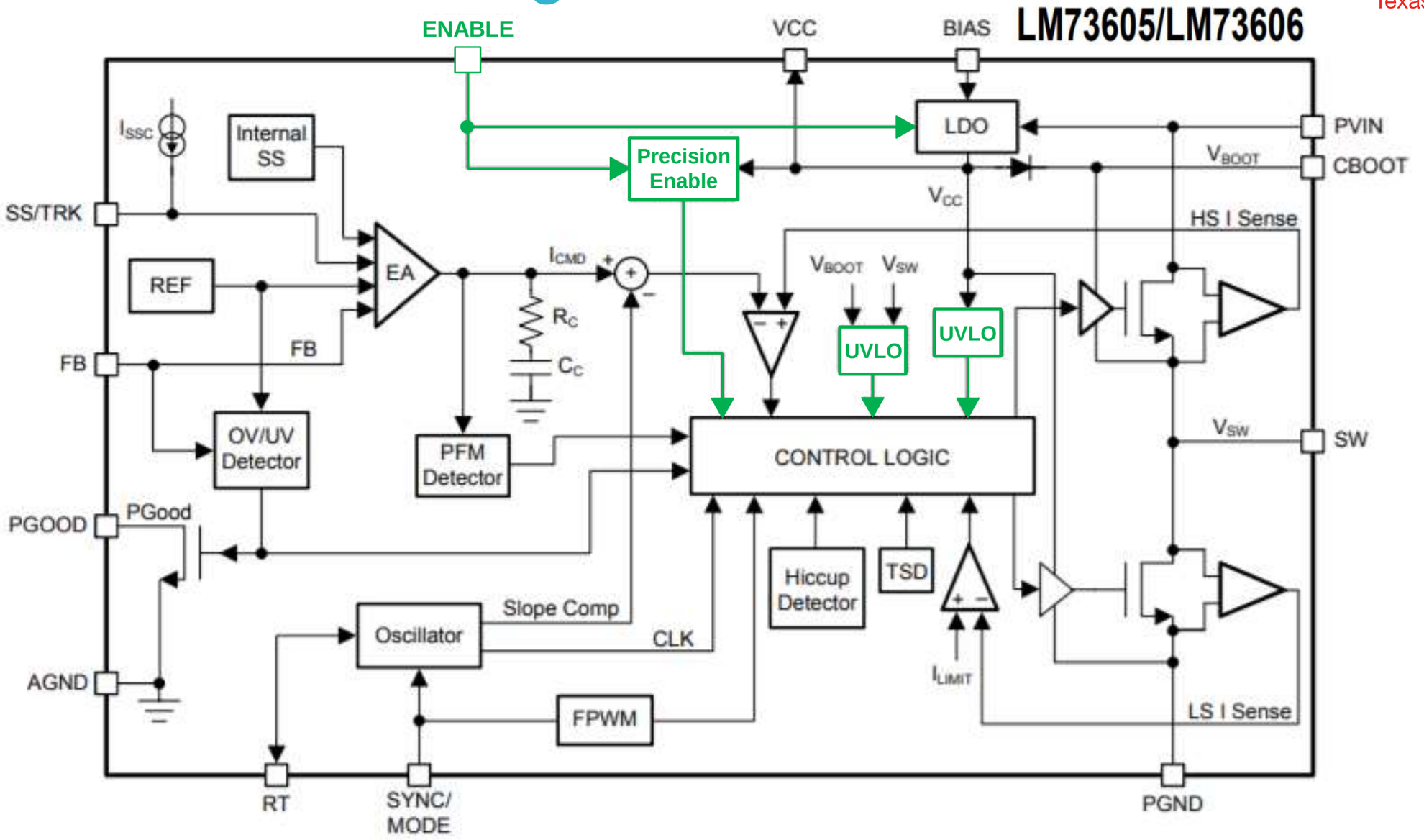
- $R_{ENB} = \frac{1.25}{12 - 1.25} * 100k$

- R_{ENB}=11.6k



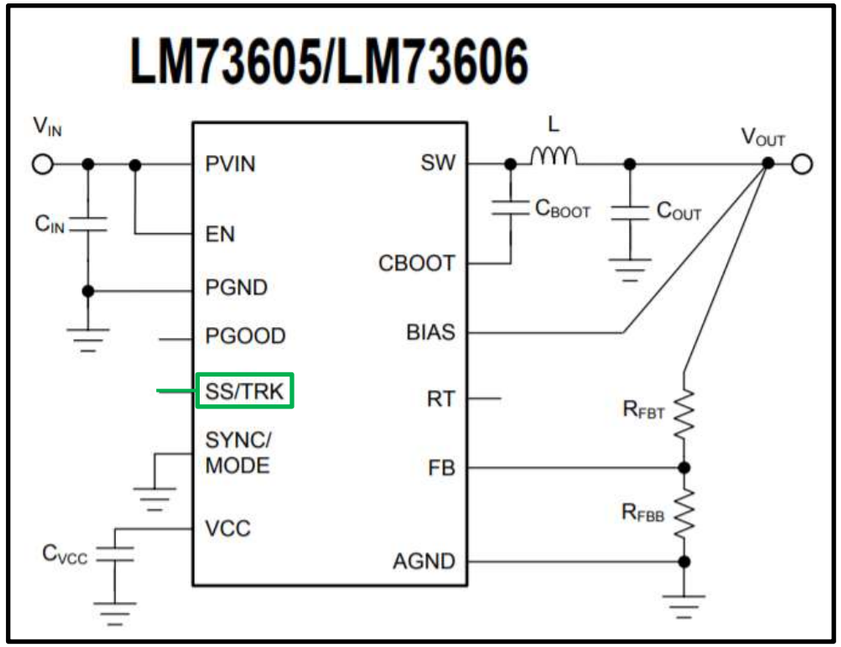
ENABLE (EN PIN)						
$V_{EN\_VCC\_H}$	Enable input high level for V_{CC} output	V_{EN} rising			1.15	V
$V_{EN\_VCC\_L}$	Enable input low level for V_{CC} output	V_{EN} falling	0.3			V
$V_{EN\_VOUT\_H}$	Enable input high level for V_{OUT}	V_{EN} rising	1.14	1.196	1.25	V
$V_{EN\_VOUT\_HYS}$	Enable input hysteresis for V_{OUT}	V_{EN} falling hysteresis		–100		mV
I_{LKG_EN}	Enable input leakage current	V_{EN} = 2 V		1.4	200	nA

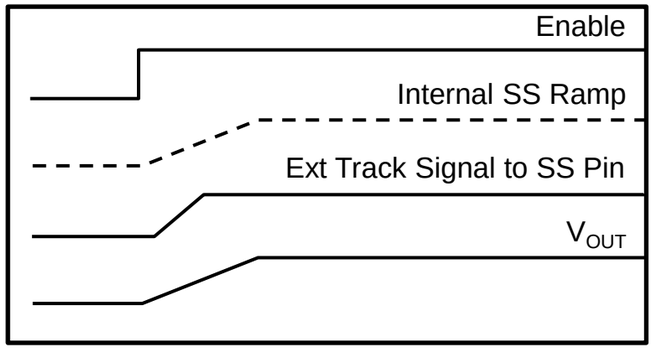
EN/UVLO in Block Diagram



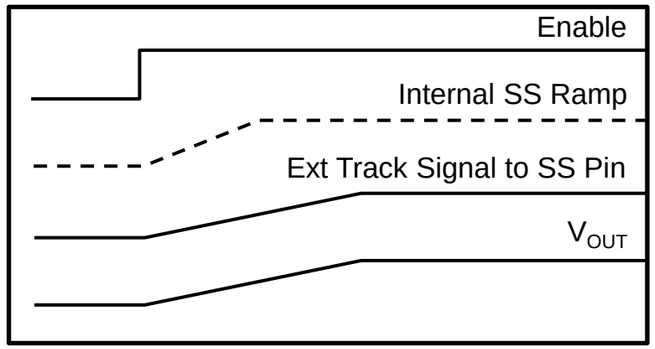
Soft Start

- Soft start limits peak inrush current at startup
- Internal Soft Start
  - Leave SS pin floating
- External Soft Start
  - Connect capacitor
  - Larger capacitor → Slower rise-time





Fast Ramp – Internal SS



Slow Ramp – External SS

Soft Start Example

- VIN = 12V
- Desired rise time = 50ms (>internal soft start)

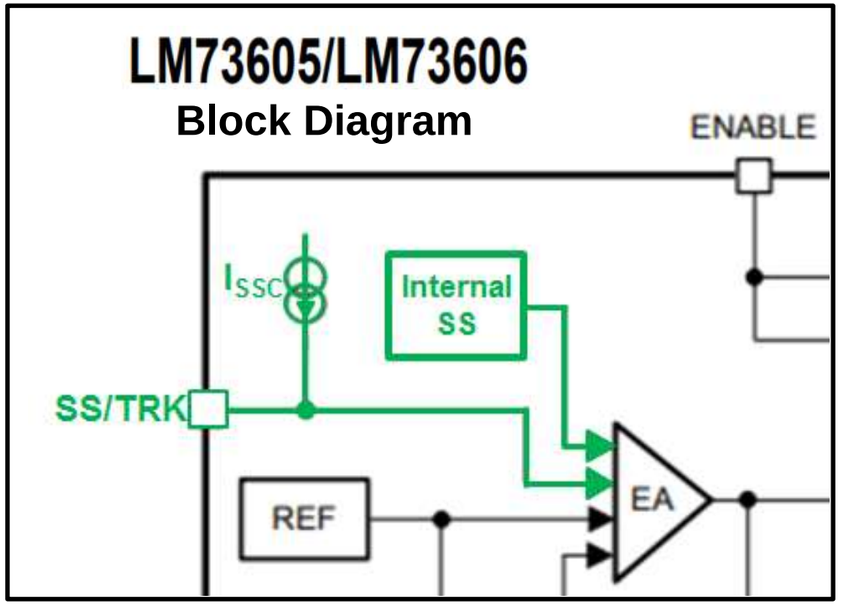
- Check datasheet – find equation: $C_{SS} = I_{SSC} * t_{SS}$
- I_{SSC}=2uA
- t_{SS}=50ms desired

- C_{SS}=100nF

$$C_{SS} = I_{SSC} \times t_{SS} \quad (12)$$

where

- C_{SS} = soft-start capacitor value (F)
- I_{SSC} = soft-start charging current (A)
- t_{SS} = desired soft-start time (s)

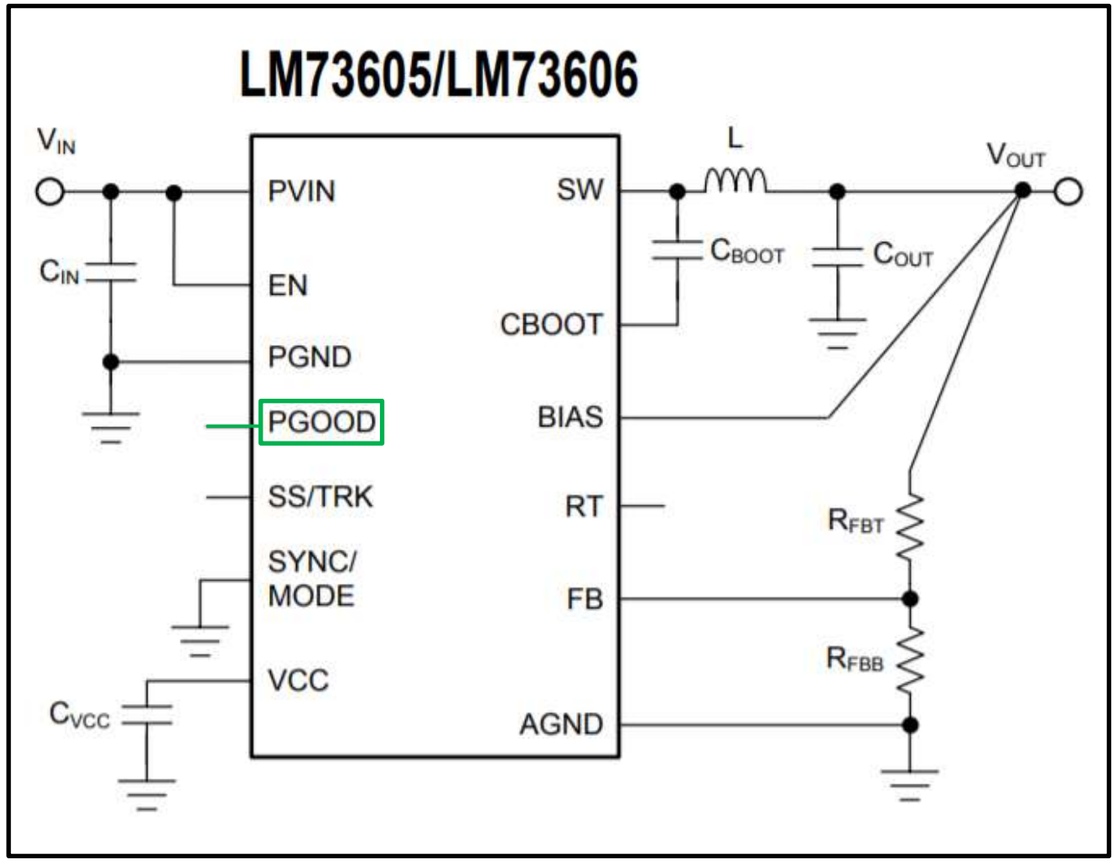


Or derive the equation with datasheet specs

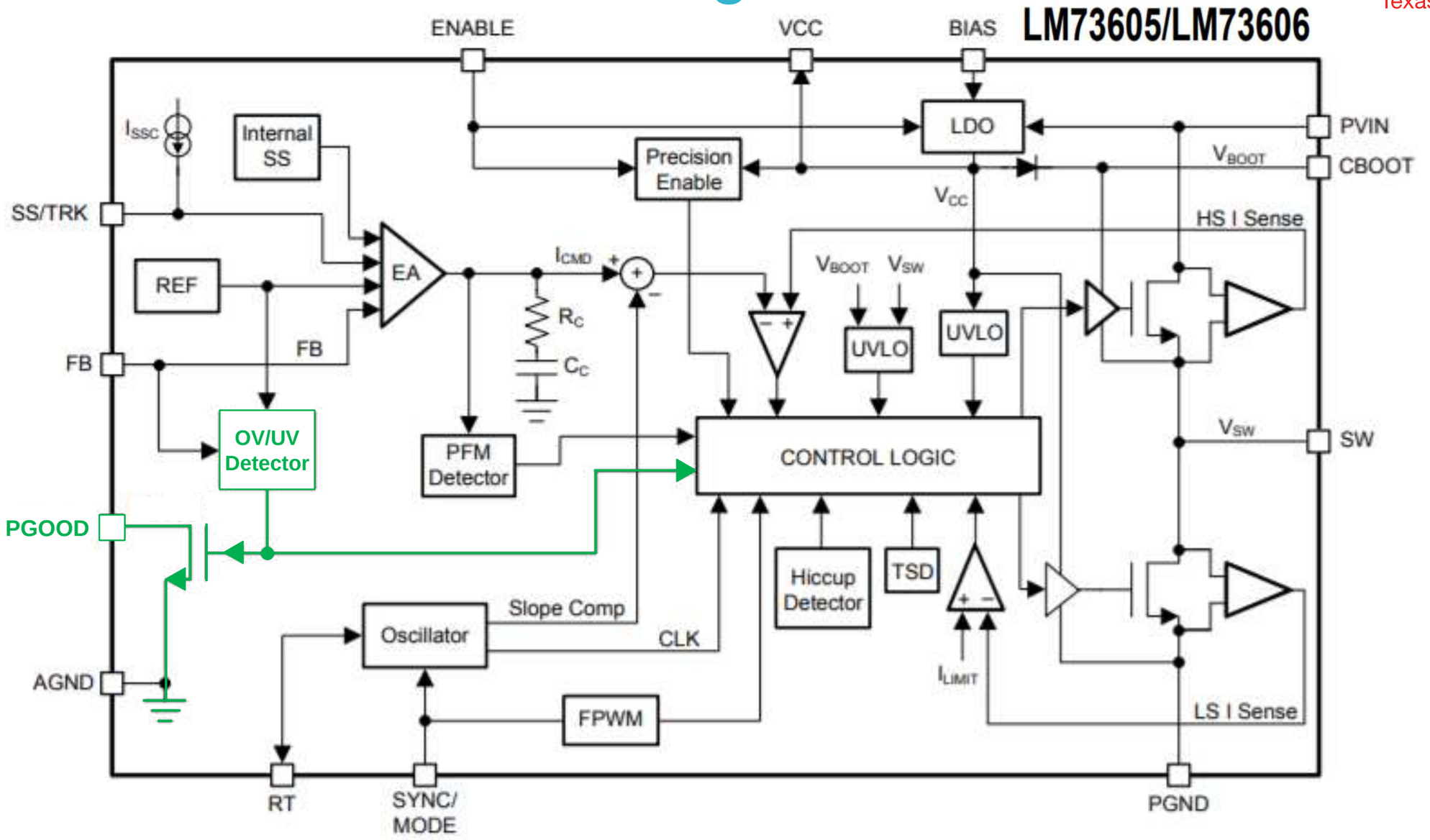
SOFT START (SS/TRK PIN)						
t_{SS}	Internal soft-start time	C_{SS} = OPEN, from EN rising edge to PGOOD rising edge	3.5	6.3		ms
I_{SSC}	Soft-start charge current		1.8	2	2.2	µA
R_{SSD}	Soft-start discharge resistance	UVLO, TSD, OCP, or EN = 0		1		kΩ
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	PWM mode	0.987	1.006	1.017	V

RESET/PGOOD

- **RESET/PGOOD** - Used to signal when the output of the converter/controller is at the desired level
- Prevents false RESET flags with:
  - Hysteresis
  - Glitch Protection
- Connect to external circuitry to signify when it is okay to rely on this regulated voltage



RESET/PGOOD in Block Diagram



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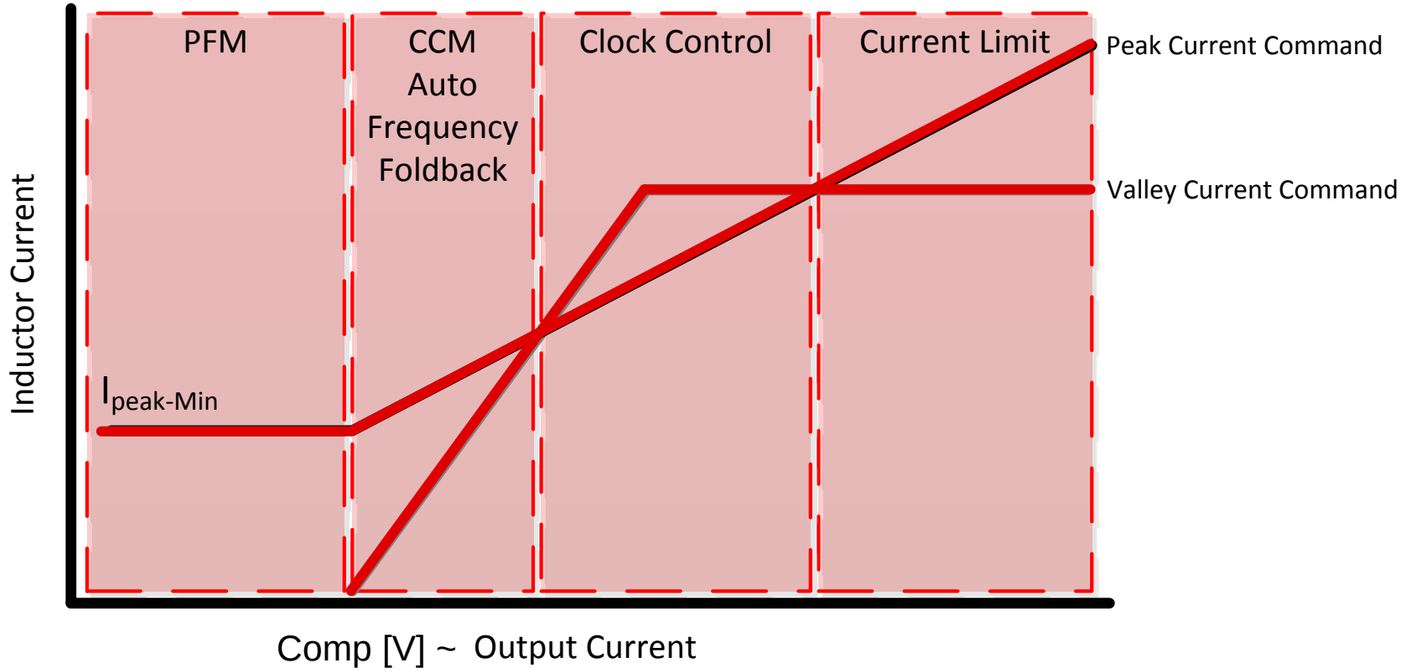
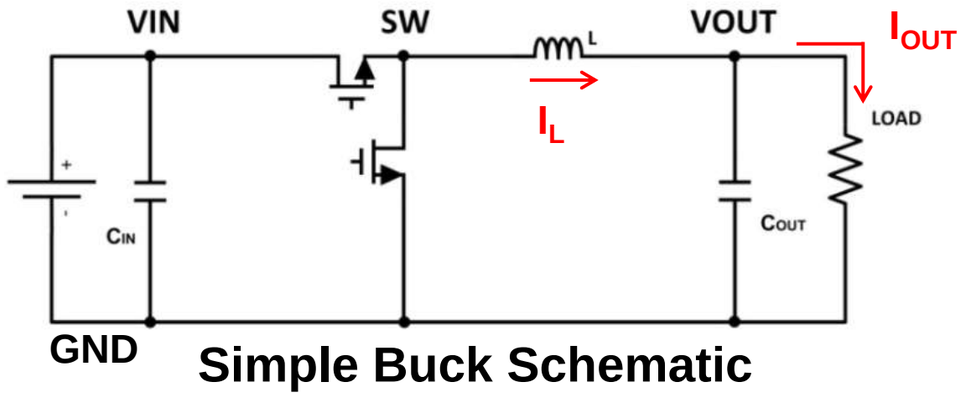
Advanced Features:

PFM, Automatic Frequency Foldback, Clock Control, Current Limit, Hiccup

Comp Curve

- Rules of Operation
  - 1. Inductor current (I_L) will not go above Peak Current Command in normal operation
  - 2. IL will always drop to at least Valley Current Command

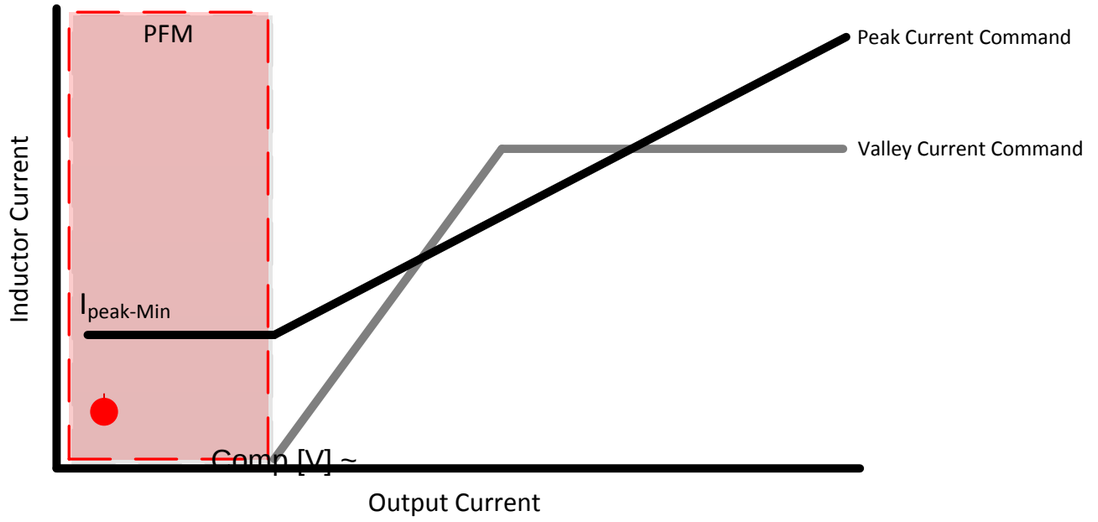


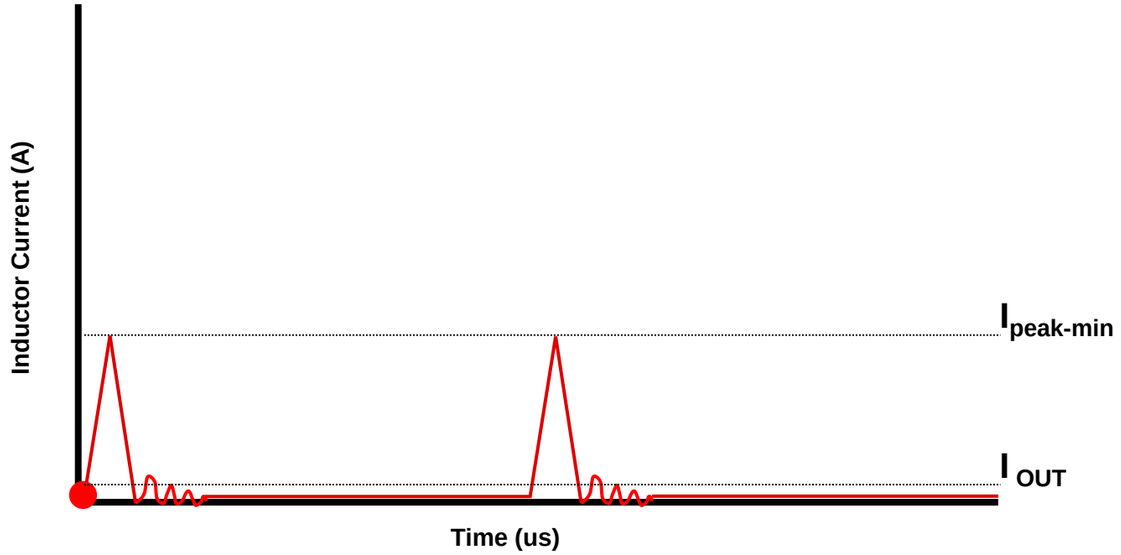


Simple Buck Schematic

PFM

- Light load
- SW is HIGH (HS FET ON, LS FET OFF)
  - Current goes up to $I_{peak-min}$
- SW is LOW (HS FET OFF, LS FET ON)
  - Current goes down to 0A
- SW is OFF (HS and LS FETs OFF)
  - DCM Ringing
- Start next switch when FB (V_{OUT}) hits low threshold
- DCM Pulse frequency increases as I_{OUT} increases
- Good light load efficiency

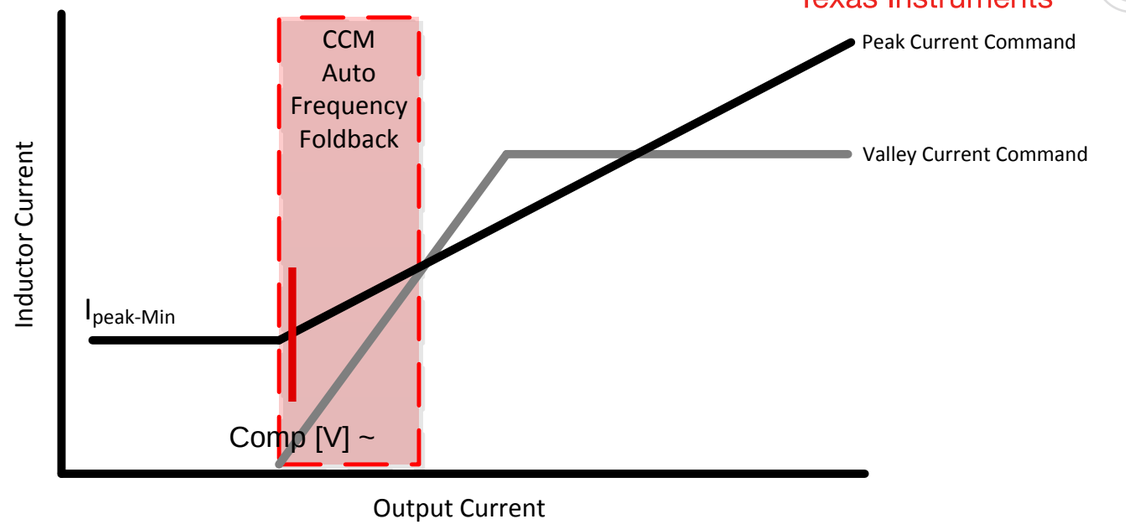


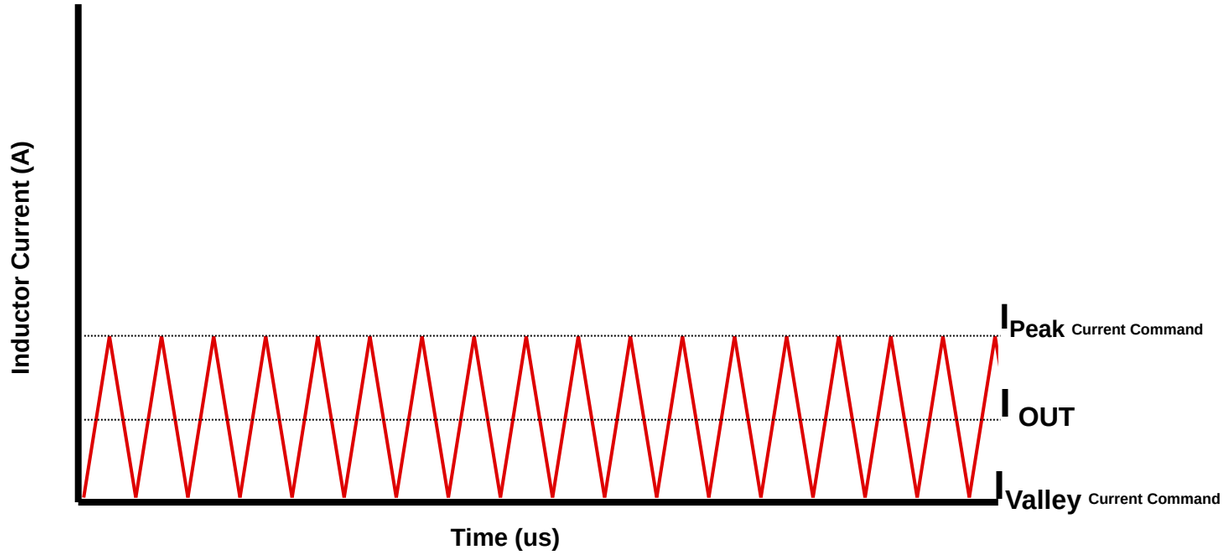


CCM Auto Frequency Foldback

- SW is HIGH until Inductor Current hits Peak Current Command
- SW is LOW until I_L:
  - Reaches Valley Current Command
  - Or goes below Valley Current Command

- Auto foldback improves efficiency with lower switching frequency

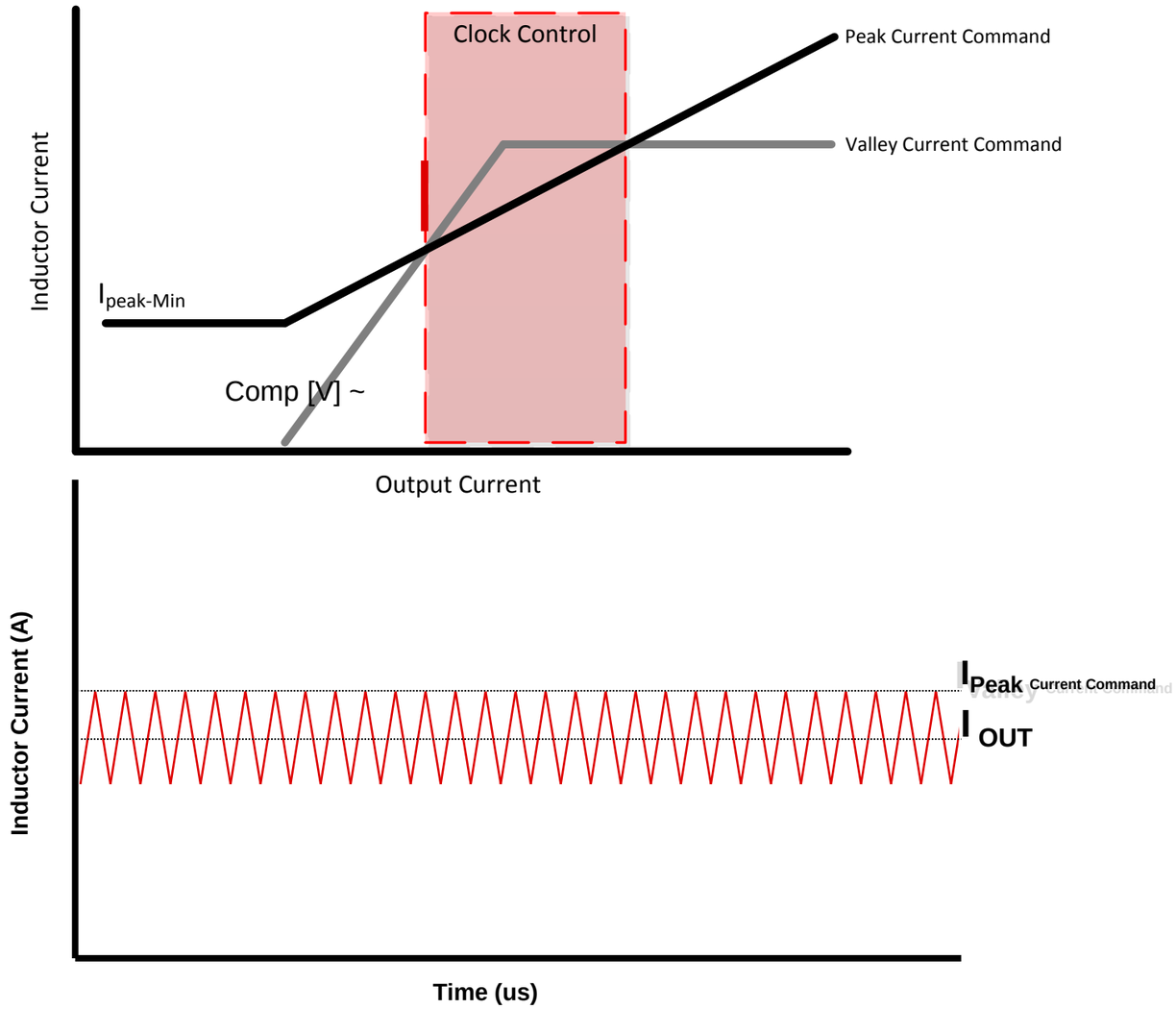




Clock Control

- SW is HIGH until Inductor Current hits Peak Current Command
- SW is LOW for time set by Clock

- Constant Frequency

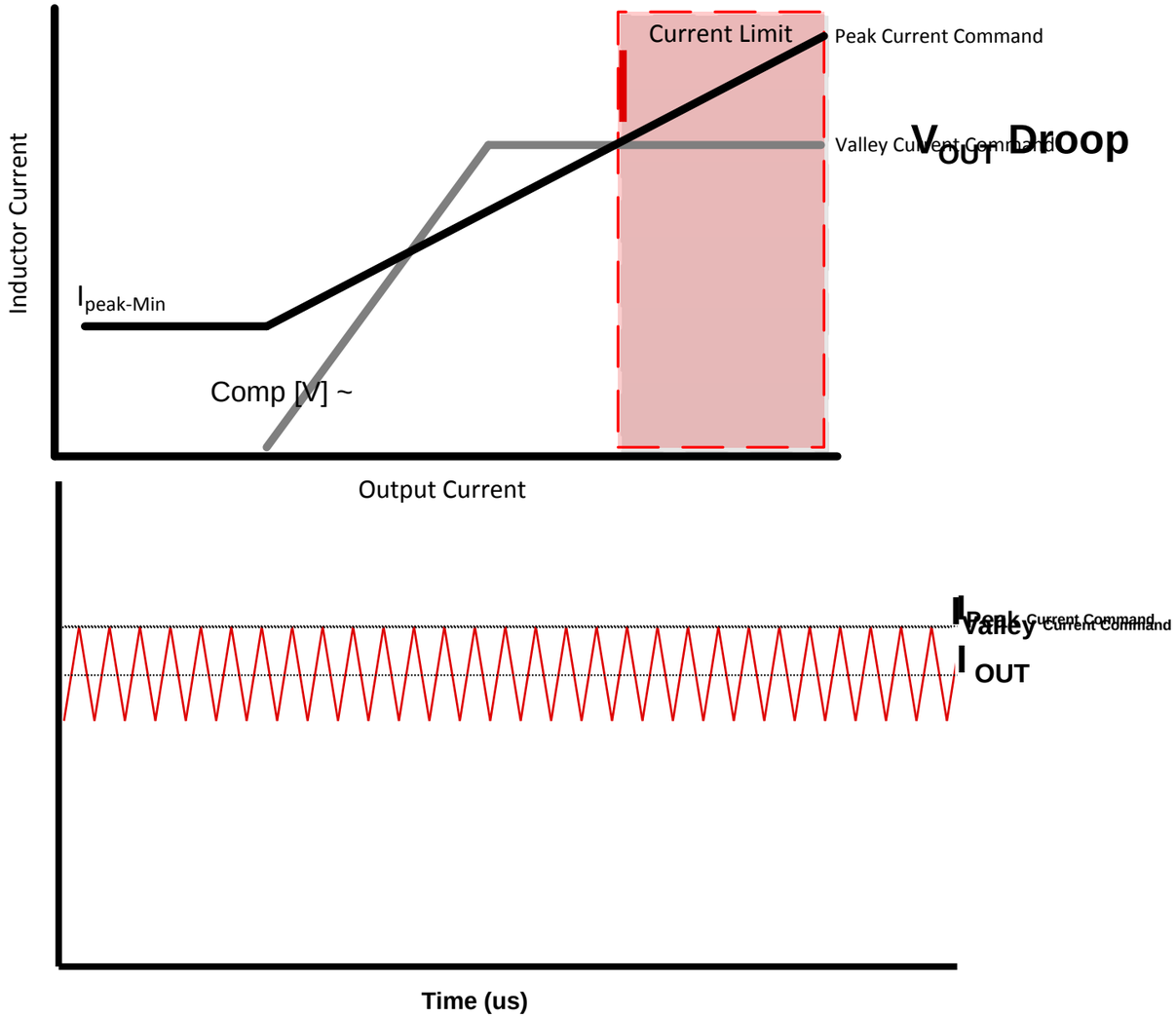


Current Limit Operation

- SW is HIGH until Inductor Current hits Peak Current Command
- SW is LOW for time set by Clock

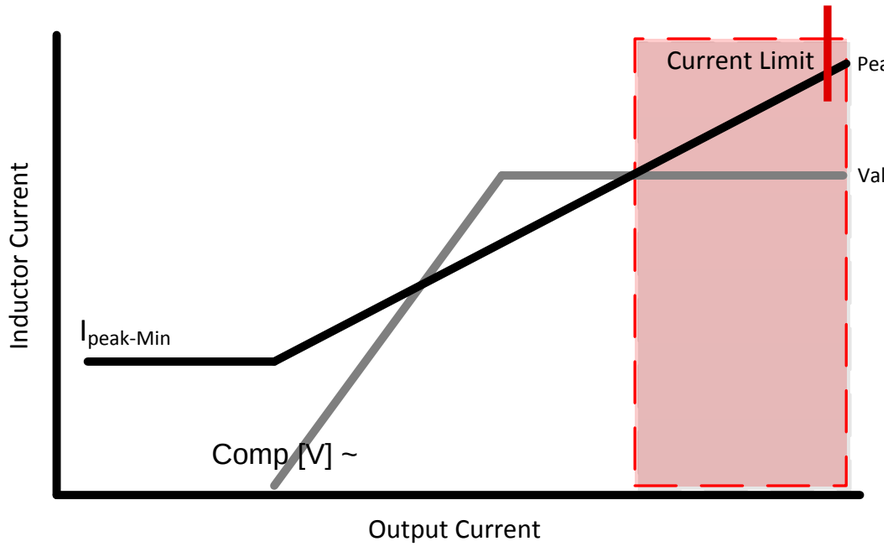
- If IL has not reached Valley Current Command, SW will stay LOW until it does.

- Frequency folds back
  - Limits current
  - V_{OUT} Droops – used to trigger hiccup

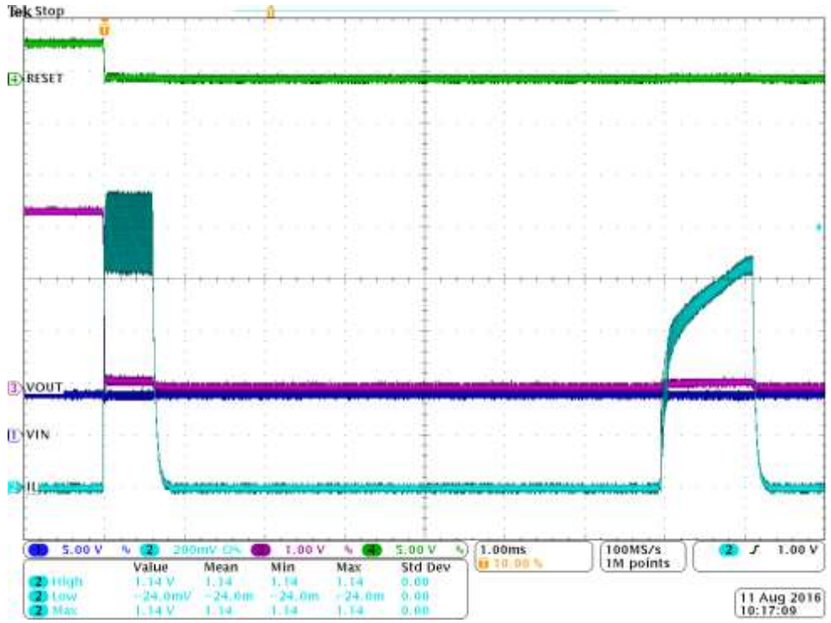


Hiccup Operation

- Hiccup
- Disables converter when V_{OUT} droop detected
  - Usually ~40% V_{OUT_NOM}
  - See datasheet
- Tries again after set time
  - Usually 10’s of ms
  - See datasheet

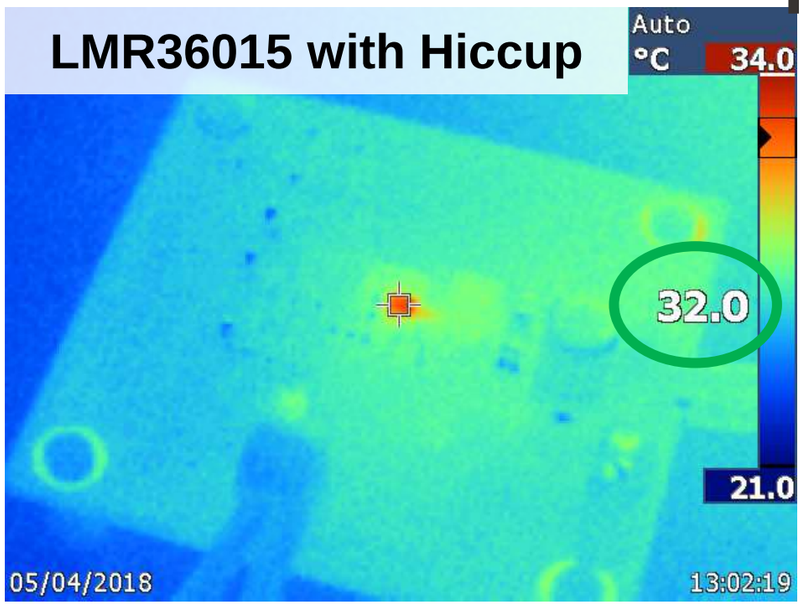


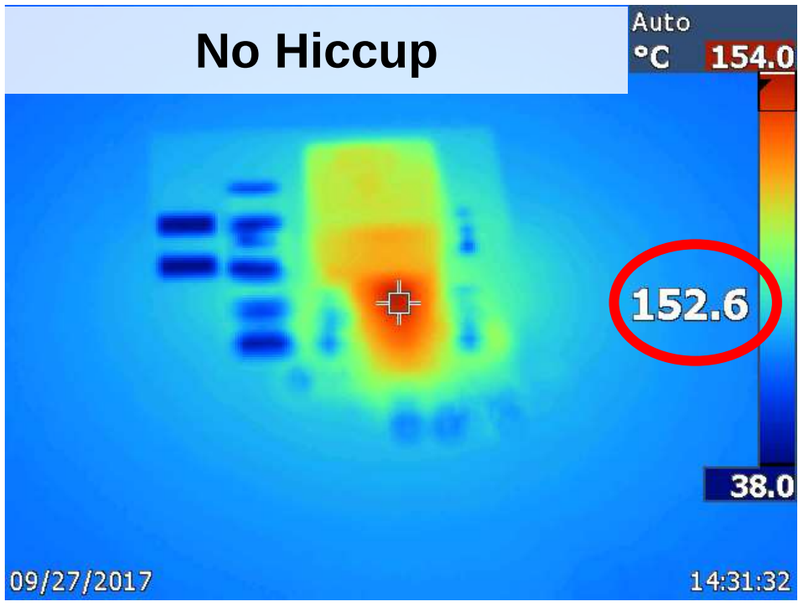
V_{OUT} Droop



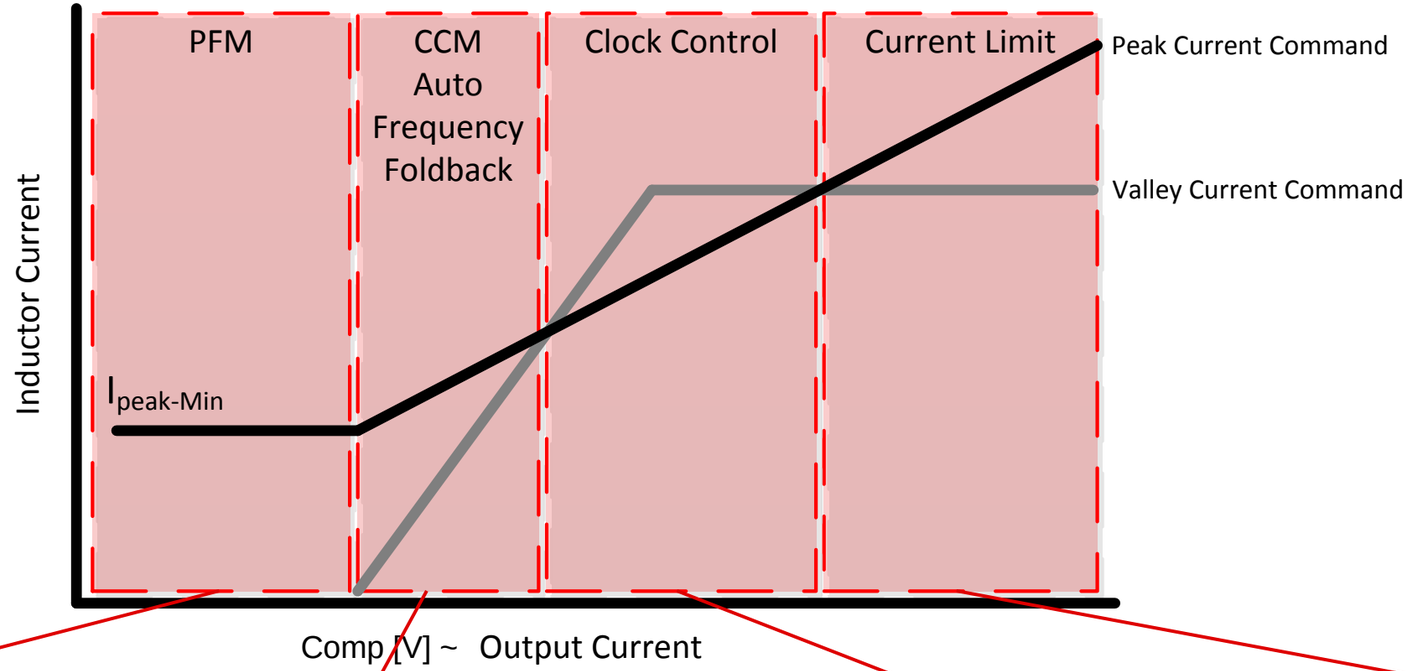
Hiccup vs No Hiccup

- Advantage of Hiccup
  - Reduces power consumption during short circuit
  - Reduces heat during short circuit





Benefits and Drawbacks of each Region



- \+ Good light load efficiency
- \- Higher ripple on VOUT

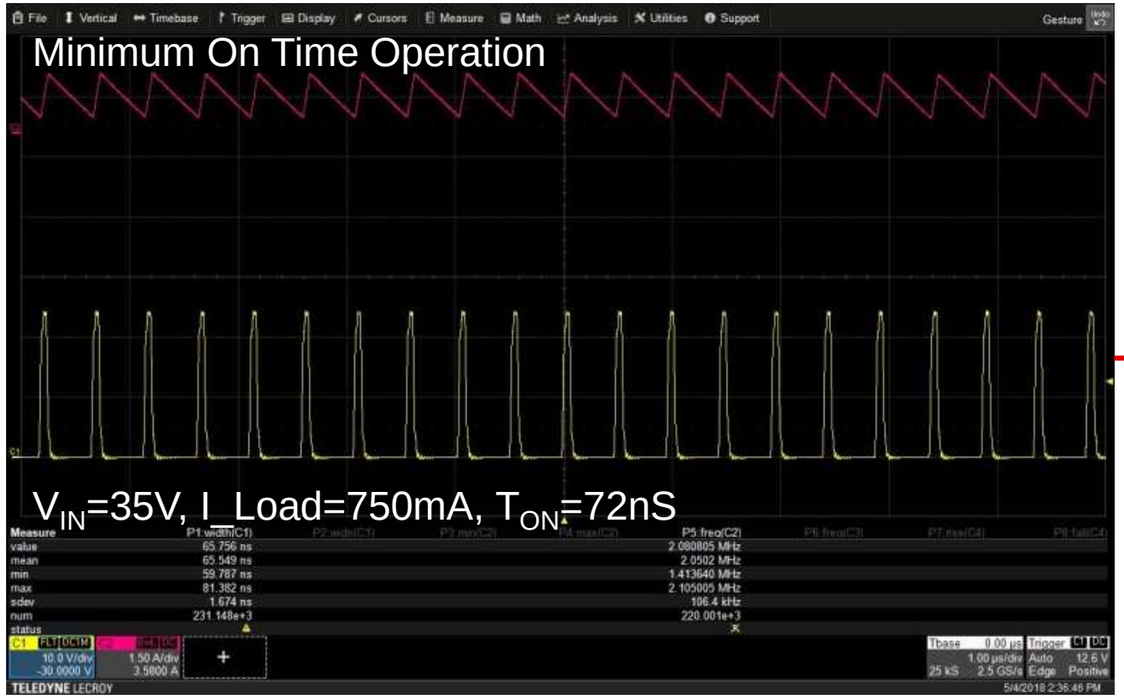
- \+ Higher efficiency when folding back
- \+ Can have constant frequency at higher I_L based on design

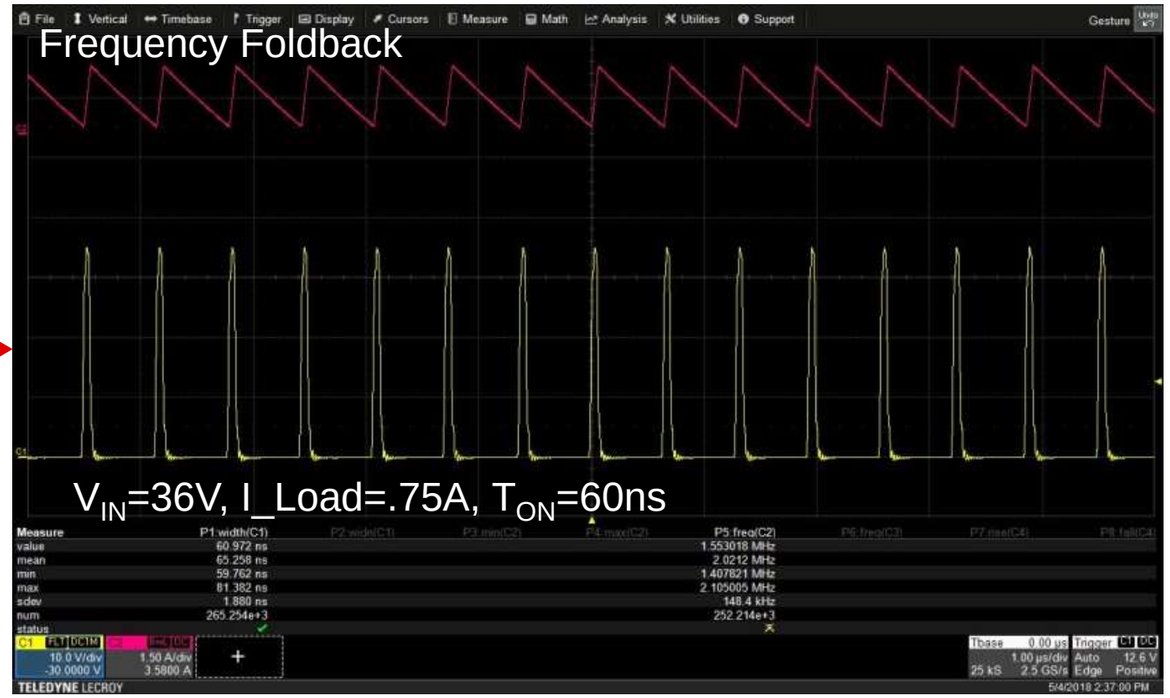
- “Normal Operation”
- \+ Constant Frequency

- \+ Protects device
- Will enter hiccup if VOUT droops to datasheet value

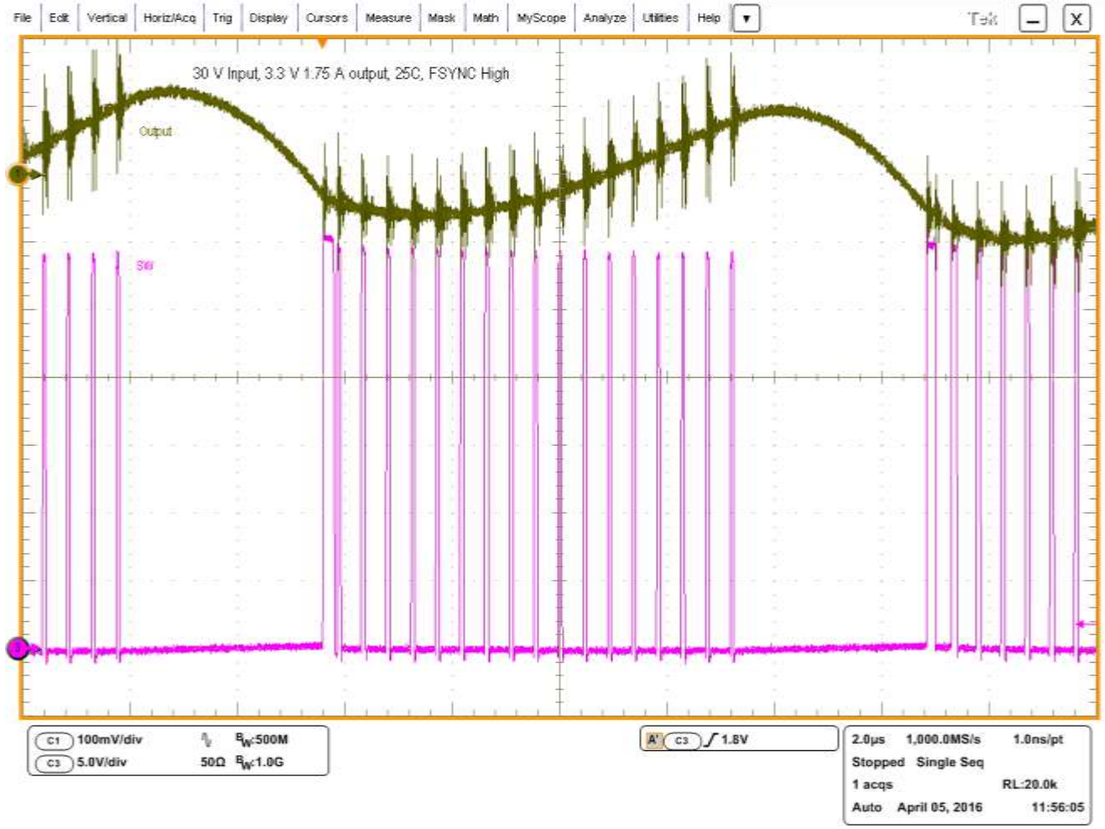
Frequency Foldback Example

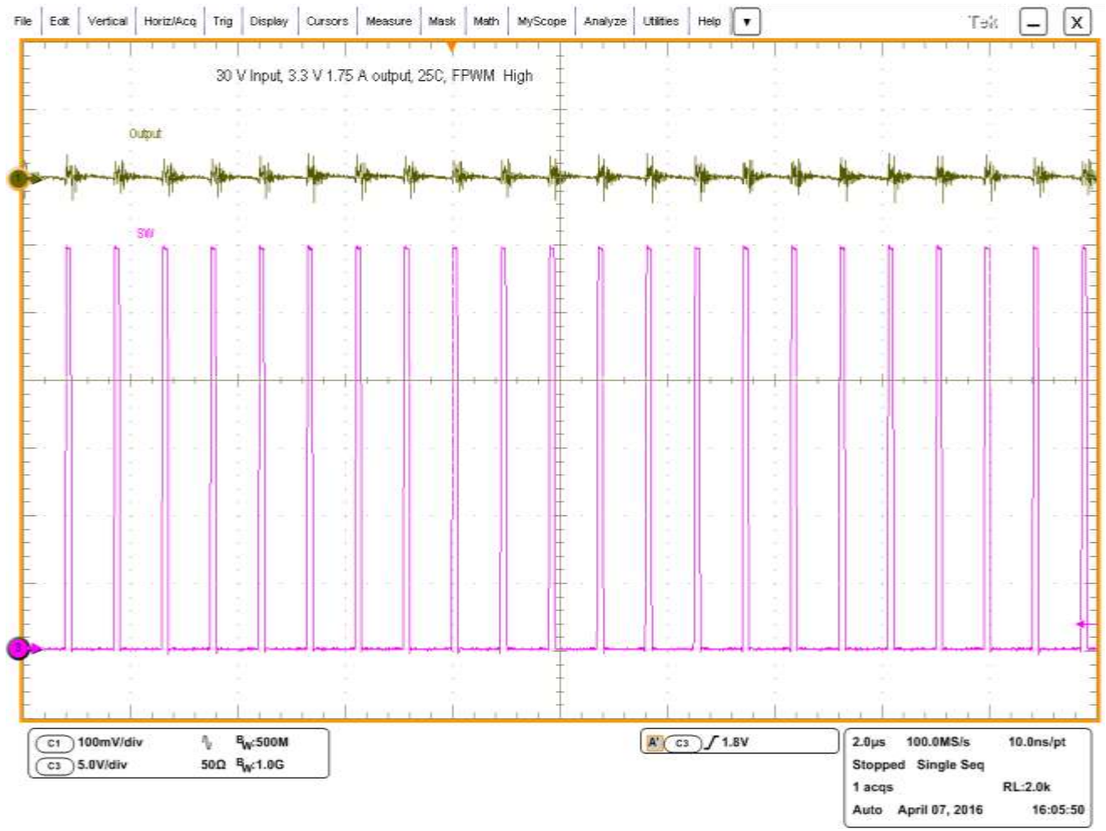
- $V_{IN} = (T_S \times V_{OUT})/t_{ON}$
- LMR33630:
  - T_S=500ns; V_{OUT}= 5V; $T_{ON\_MIN(typ)}$=72ns
  - V_{IN}= (T_S x V_{OUT})/t_{ON} =(500ns x 5V)/72ns = 35V





Not All switchers are equal: High-VIN output ripple





Competitor has +/-100mV output ripple for high-VIN operation

LM53635 Has smooth frequency foldback at high input voltage.

T_{ON_MIN} Datasheet Specs

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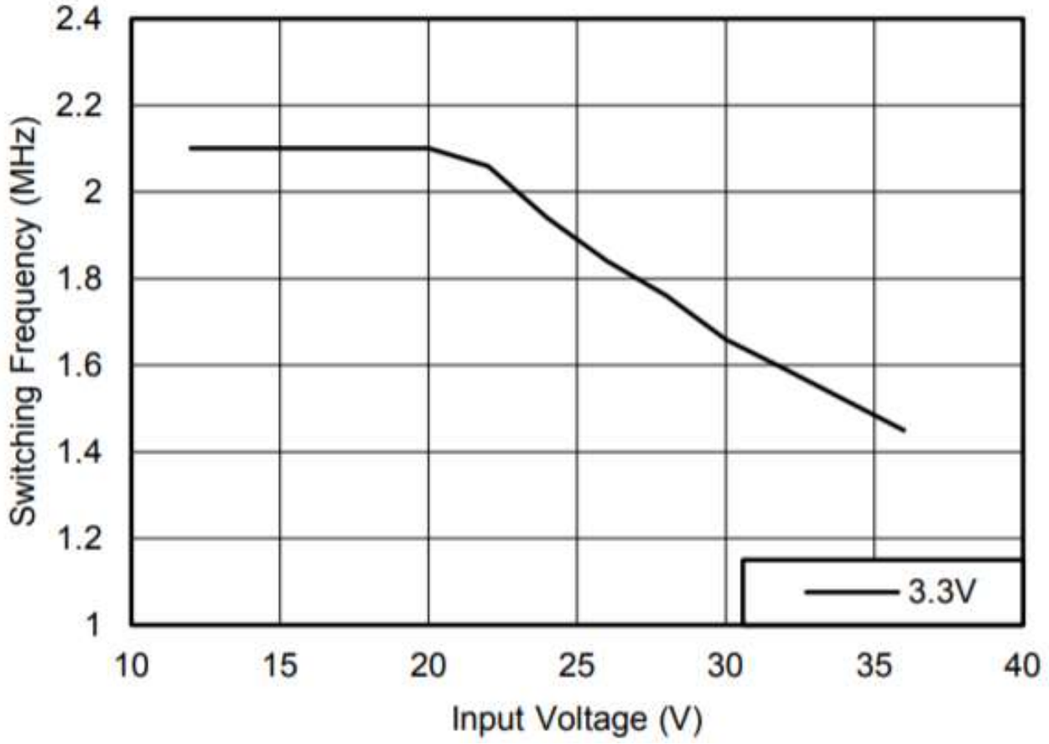
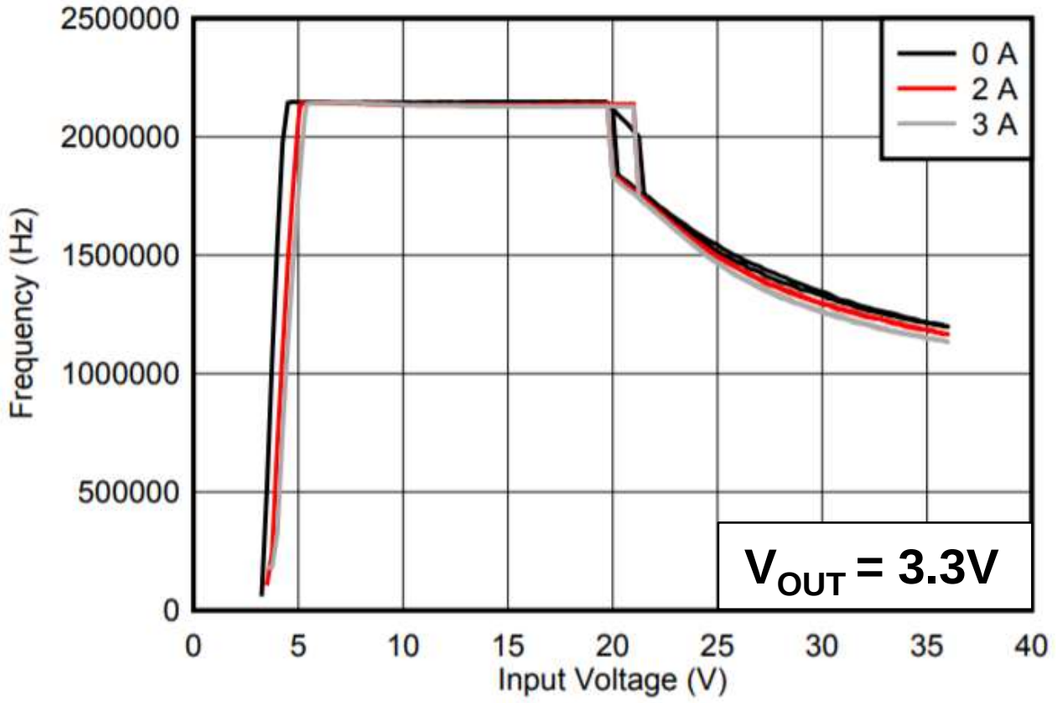
LMR33630



Foldback by sensing T_{ON}, hits T_{ON_MIN}

LM53602

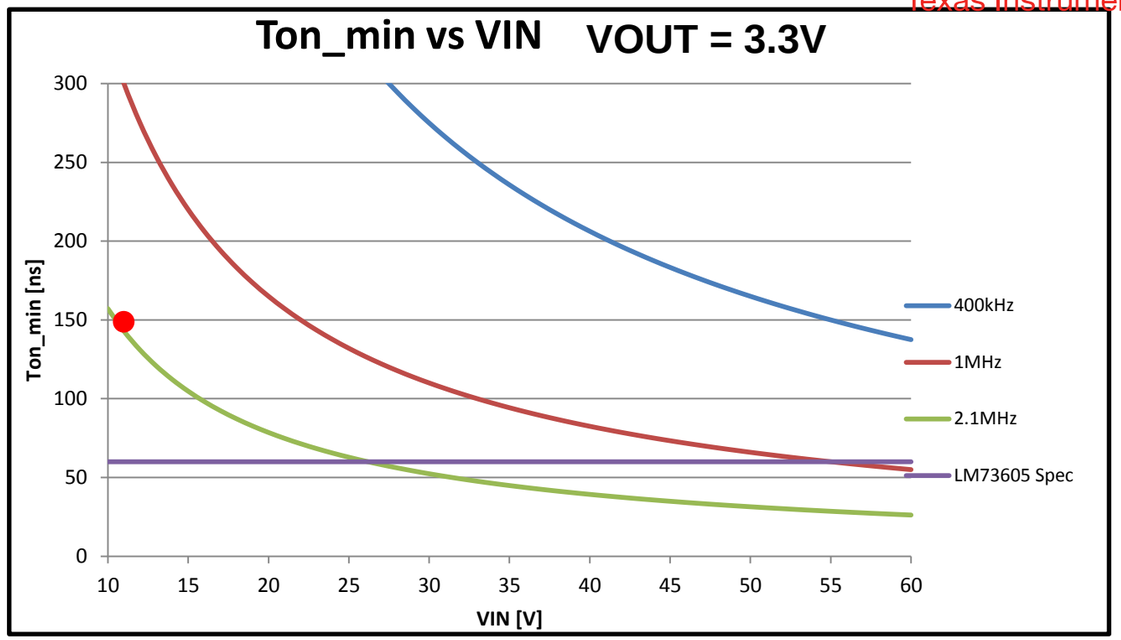


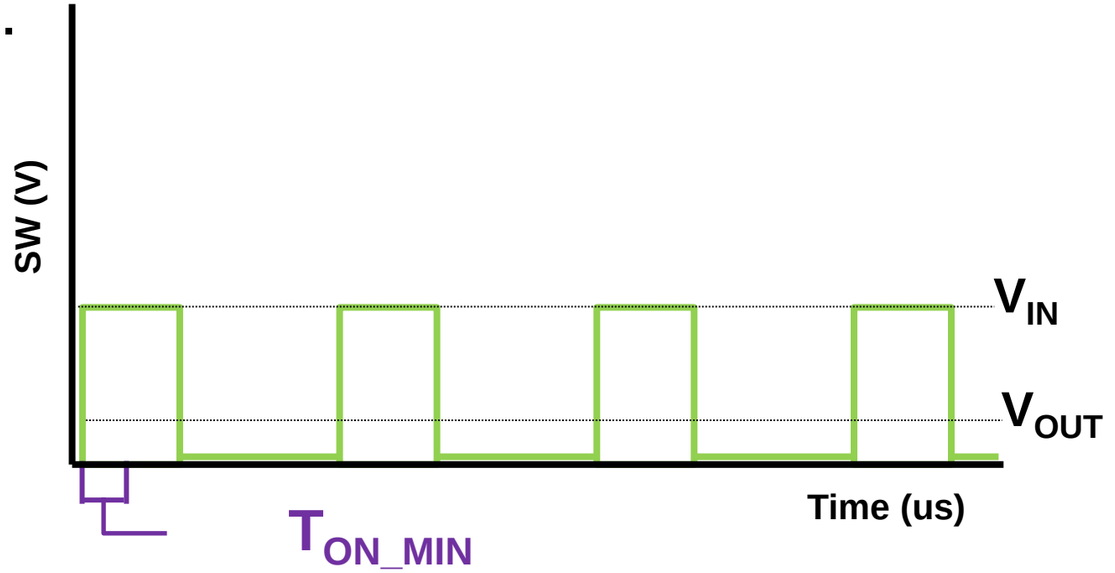
Foldback by sensing VIN, avoids T_{ON_MIN}

T_{ON_MIN} Frequency Foldback

- As V_{IN} Increases:
  - Duty Cycle Decreases
  - T_{ON} reduces
- T_{ON} will eventually need to go below T_{ON_MIN} (spec'd in datasheet)
- The IC cannot switch HIGH for shorter than T_{ON_MIN} so the frequency folds back.
  - Duty cycle reduces
  - V_{OUT} remains the same
  - T_{ON_MIN} is not violated

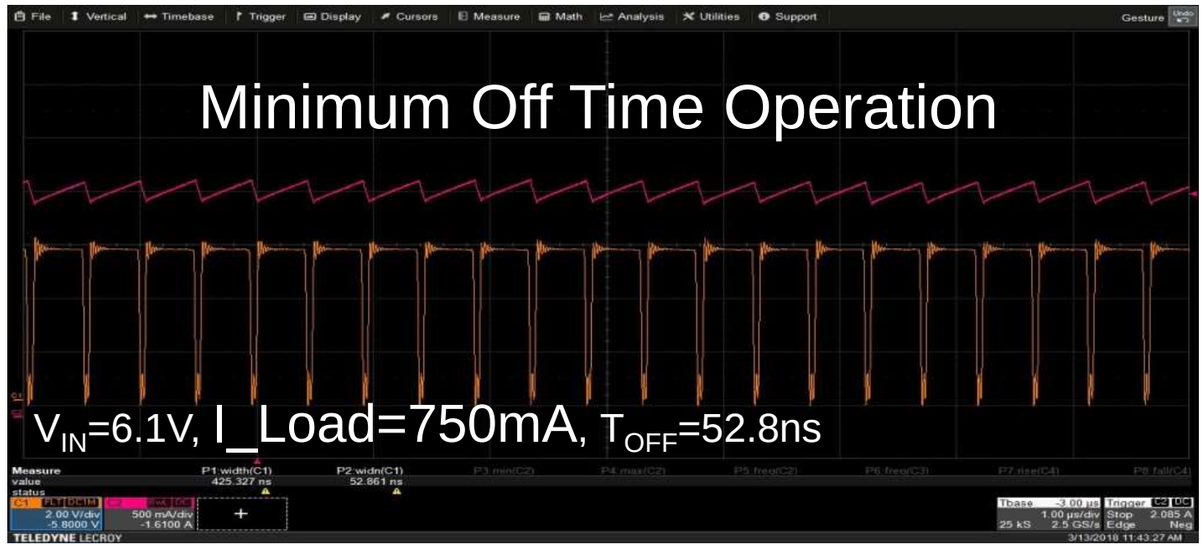
Note* Heavy Load Helps!

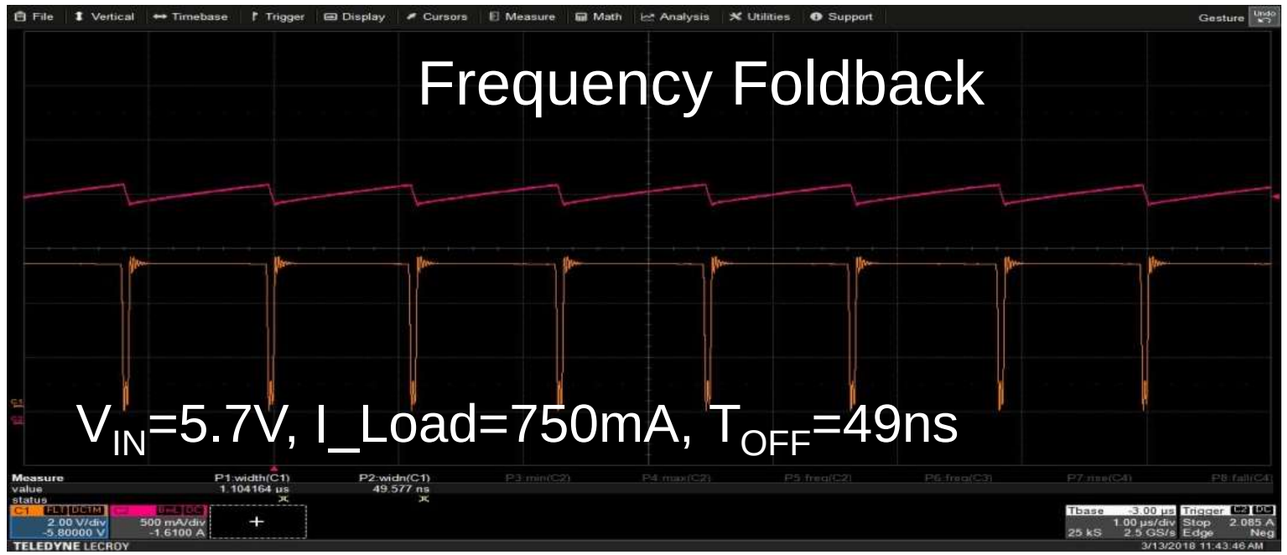




Key Features for Automotive: Dropout

- $V_{IN\text{-}Min} = (V_{IN} \times D_{MAX}) - (R_{DS\_ON} \times I_{IN}) - (R_{DCR} \times I_{L\_RMS})$
- $V_{OUT} = (V_{IN} \times D_{MAX})$
- $5V/0.98 = V_{IN\_MIN\_FSW} = 5.10V$
  - There is significant variation between the calculated value of frequency fold-back and the actual value of frequency fold-back. We recommend providing sufficient margin as necessary.





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Understanding Quiescent Current Specifications

Key Features for Automotive: Low-Iq

- Always-on automotive applications require power even when car is off
  - Body electronics (keyless entry)
  - Cluster, Infotainment (keep-alive MCU)

- These applications requires very low no-load operating current (Iq)

- OEMs set standards for Iq at module level
  - Sometimes < 100uA

- Suppliers will want per DC/DC Iq's in 10uA to 40uA range

Key Features for Automotive: Low-Iq

Product Folder | Order Now | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

LMR33630

SNVSAN3A – AUGUST 2017 – REVISED FEBRUARY 2018

LMR33630 SIMPLE SWITCHER® 3.8-V to 36-V, 3-A Synchronous Step-Down Voltage Converter

1 Features

- Configured for Rugged Industrial Applications
  - Input Voltage Range: 3.8 V to 36 V
  - Output Voltage Range: 1 V to 24 V
  - Output Current: 3 A
  - Peak-Current-Mode Control
  - Short Minimum On-Time of 70 ns
  - Frequency: 400 kHz, 1.4 MHz, 2.1 MHz
  - Junction Temperature Range –40°C to +125°C
- Integration Simplifies Design and Reduces Size
  - Integrated Synchronous Rectification
  - Integrated Compensation Network
- Best-in-Class Power Dissipation
  - >91% Efficiency at Full Load
  - Low Shutdown Quiescent Current of 5 µA
  - Low Operating Quiescent Current of 24 µA
- Flexible System Interface
  - Power-Good Flag and Precision Enable
- Create a Custom Design Using the LMR33630 with the WEBENCH® Power Designer

2 Applications

- Motor Drive Systems: Drones, AC Inverters, VF Drives, Servos
- Factory and Building Automation Systems: PLC CPU, HVAC Control, Elevator Control
- General Purpose Wide V_{IN} Power Supplies

3 Description

The LMR33630 SIMPLE SWITCHER® regulator is an easy-to-use, synchronous, step-down DC/DC converter that delivers best-in-class efficiency for rugged industrial applications. The LMR33630 is capable of driving up to 3 A of load current from an input of up to 36 V. The LMR33630 provides high light load efficiency and output accuracy in a very small solution size. Features such as a power-good flag and precision enable provide both flexible and easy-to-use solutions for a wide range of applications. The LMR33630 automatically folds back frequency at light load to improve efficiency. Integration eliminates most external components and provides a pinout designed for simple PCB layout. Protection features include thermal shutdown, input undervoltage lockout, cycle-by-cycle current limit, and hiccup short-circuit protection. The LMR33630 is available in an 8-pin HSOIC package.

Device Information(1)

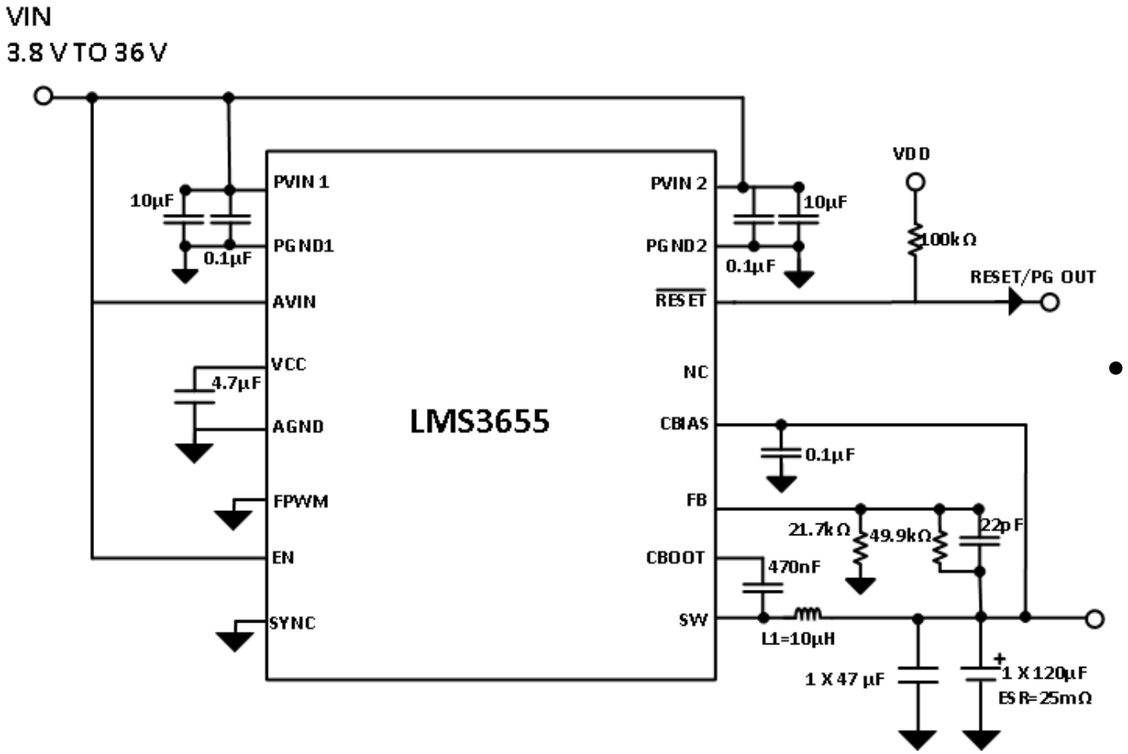
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMR33630	HSOIC (8)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Three Measurements for Quiescent Current:

- Shut Down Current
  - Part disabled; Enable tied to GND.
- Non-Switching Iq
  - Part enabled, feedback tied high. This value can be found in the EC table, and is traditionally measured open loop on the ATE.
- Switching Iq
  - Also known as operating quiescent current or no load input current.

Calculating Operating I_Q Based on EC Table



- $I_{Q\_SW}=I_Q + I_{EN} + (I_B + I_{DIV}) \times (V_{OUT}/ (n_{eff} \times V_{IN})$
  - $I_{Q\_SW}= I_{VIN}$ = No Load Current
  - $I_Q = I_{Q\_NON-SW}$ = Current Drawn at Input Pin
  - I_{EN} = Current Drawn at Enable Pin
  - I_B = Current Drawn at Bias Pin
  - I_{DIV} = Current Drawn at Feedback Divider
  - n_{eff} = Light Load Efficiency
- Example (LMS3655):
  - $I_{Q\_SW}= I_{VIN}$ = 23.2µA
  - $I_Q = I_{Q\_NON-SW}$ = 7.5µA
  - I_B = 32µA
  - I_{DIV} = 0µA (Fixed Output Variant)
  - n_{eff} = .85

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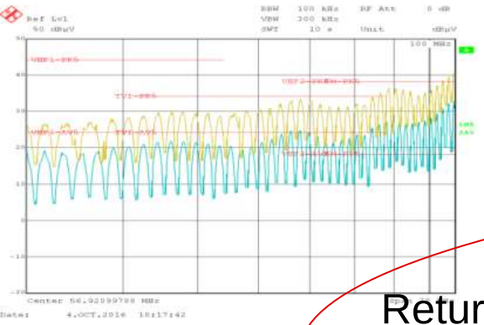
Wide Input Converters: EMI Optimized

What makes a low EMI Buck



SW node capacitive coupling to the environment

C = 7fF

SW dV/dt

Near E-Field coupling

Return path of coupling is over Input wires

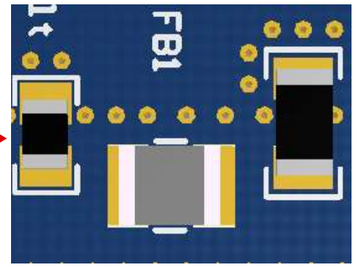
-> Now it's source of the Common Mode Noise

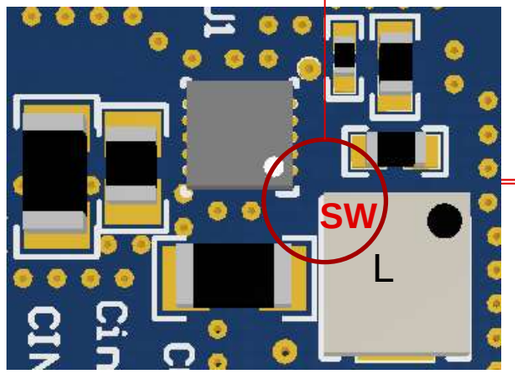
Buck

EMI Filter

DC Source

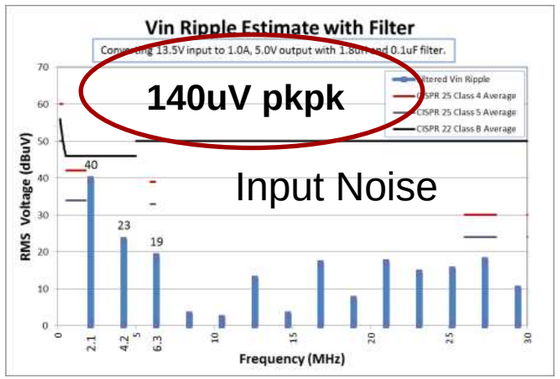
Input cable





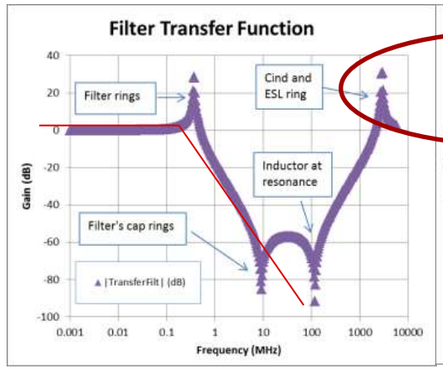
Output cable

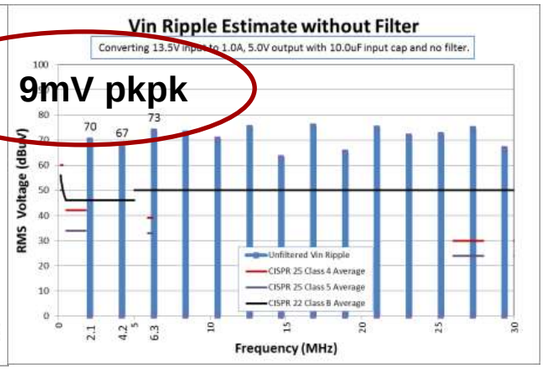
Load



Input Noise

Low pass





Output Noise

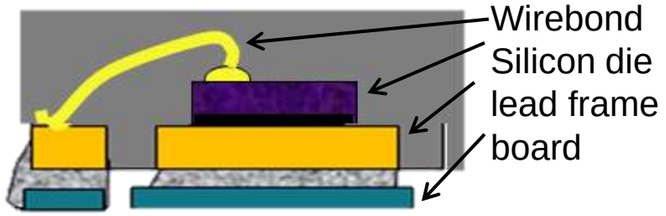
-12dB/Oct -40dB/Dec

Examples:
1mV pkpk on PCB trace

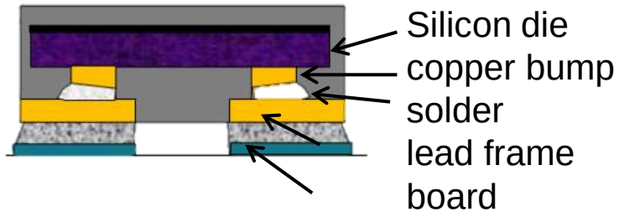
140uV pkpk with unshielded Cable similar to CISPR

EMI Optimization: Hot Rod Package

Standard wirebond QFN package



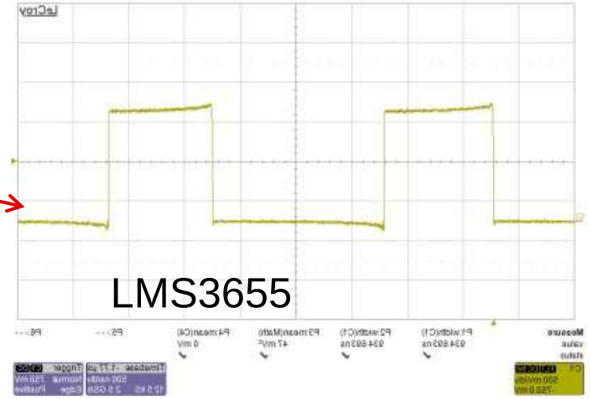
Flip chip on lead frame QFN

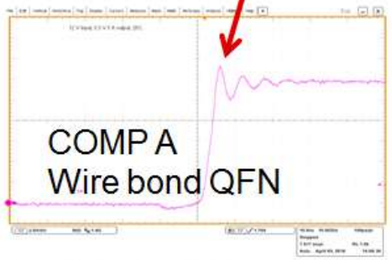


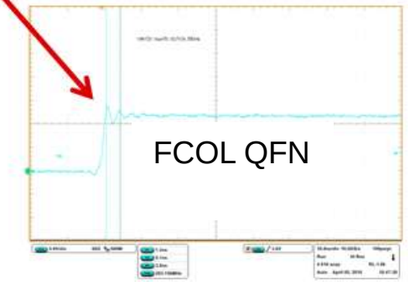
Die is flipped and placed directly onto the lead frame

Minimize EMI through:

1. **No-wirebond VSON packaging**
2. Symmetric pinout
3. Spread spectrum feature



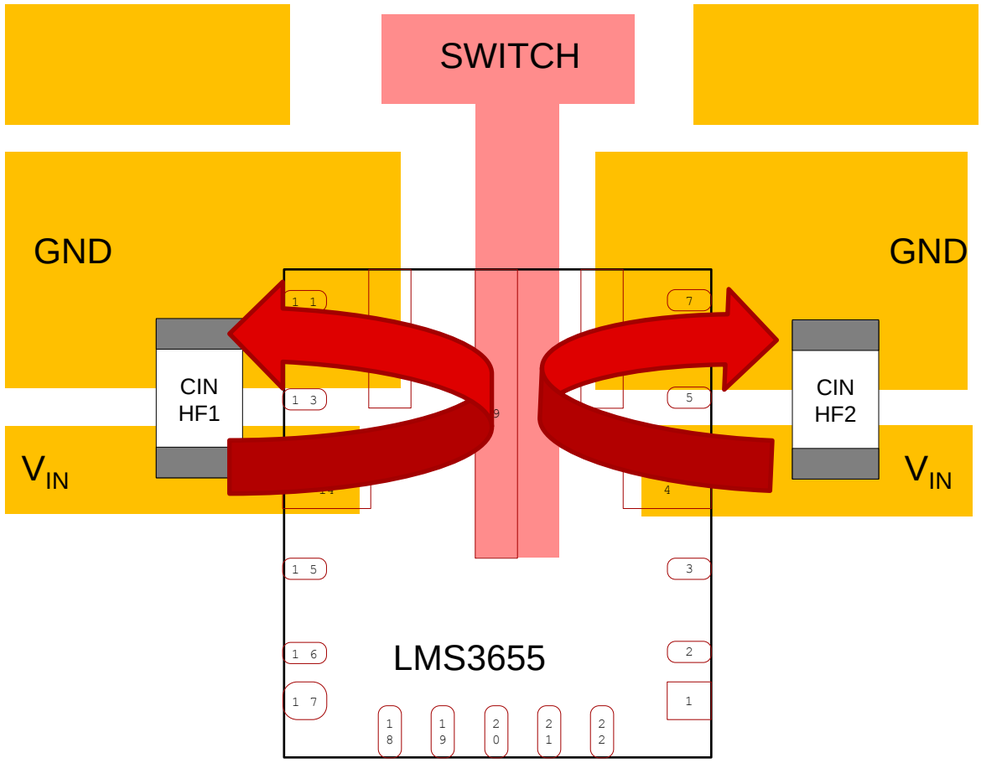


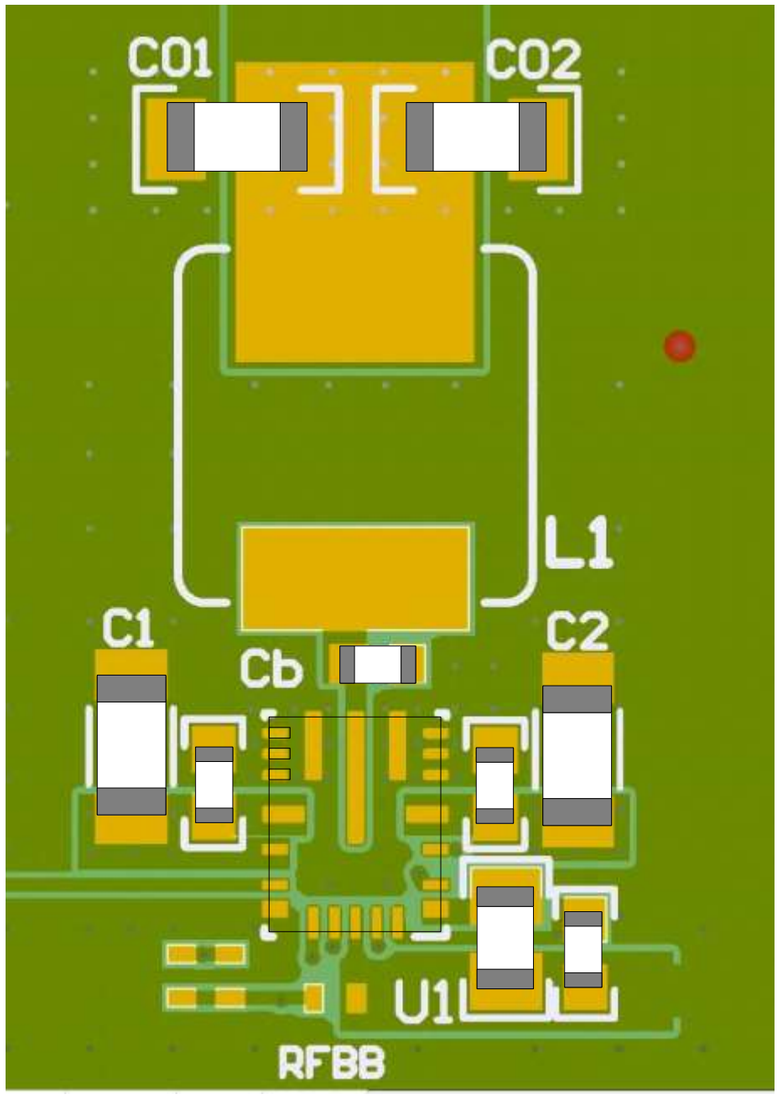


EMI Optimization: Symmetric Pinout

Minimize EMI through:

1. No-wirebond VSON packaging
2. **Symmetric pinout**
3. Spread spectrum feature



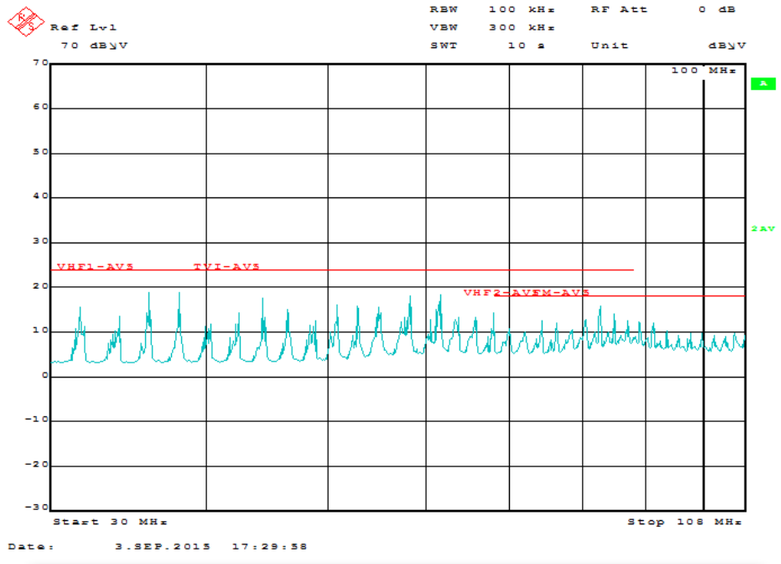


EMI Optimization: Spread Spectrum Feature

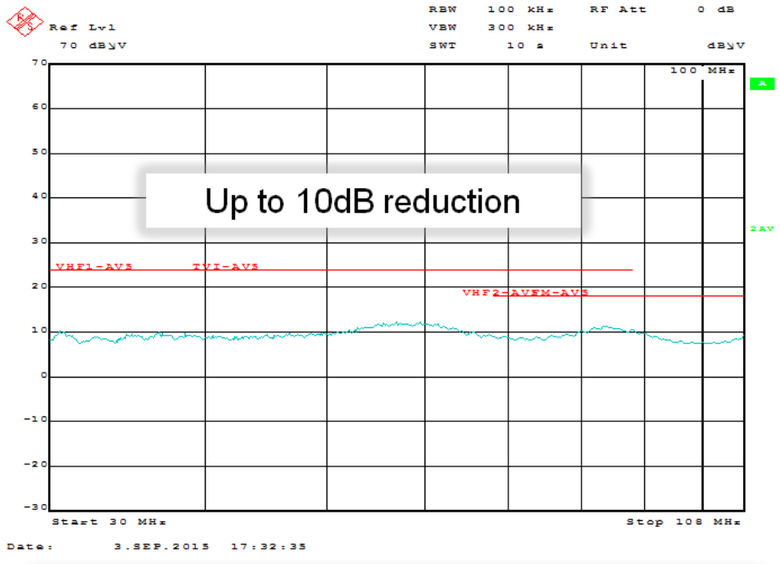
TECH DAYS
Texas Instruments

Minimize EMI through:

1. No-wirebond VSON packaging
2. Symmetric pinout
3. **Spread spectrum feature**



LMS3655 without spread spectrum



LMS3655 with spread spectrum

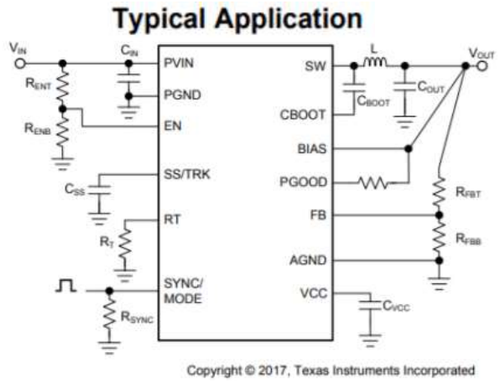
Spread spectrum makes it easier to design and meet OEM standards for conducted and radiated EMI

TECH DAYS
Texas Instruments

Design Tools

Design Tools

- WEBENCH
  - Every part in our portfolio is on WEBENCH
- Tina/PSpice
  - Every part in our portfolio has simulation files
- Design Guidelines
  - Every datasheet has an example circuit and design details
  - Every IC has an EVM
- Debugging
  - E2E



TI E2E™ Community

TECH DAYS
Texas Instruments

Understanding, measuring, and reducing output noise in DC/DC switching regulators

Practical tips for output noise reduction

Katelyn Wiggenhorn, Applications Engineer, Buck Switching Regulators

Robert Blattner, Applications Engineer, Buck Switching Regulators

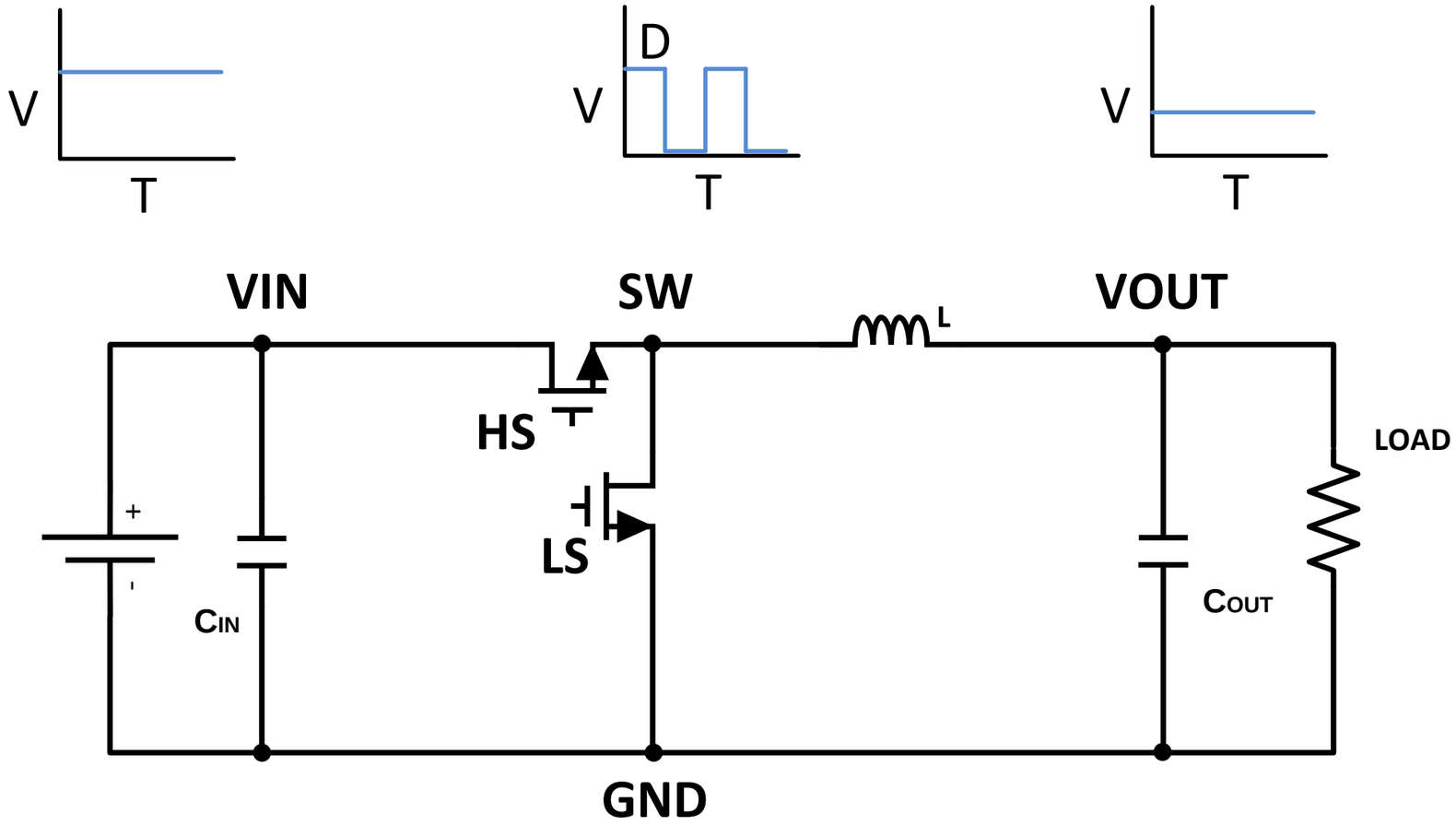
Detailed agenda

TECH DAYS
Texas Instruments

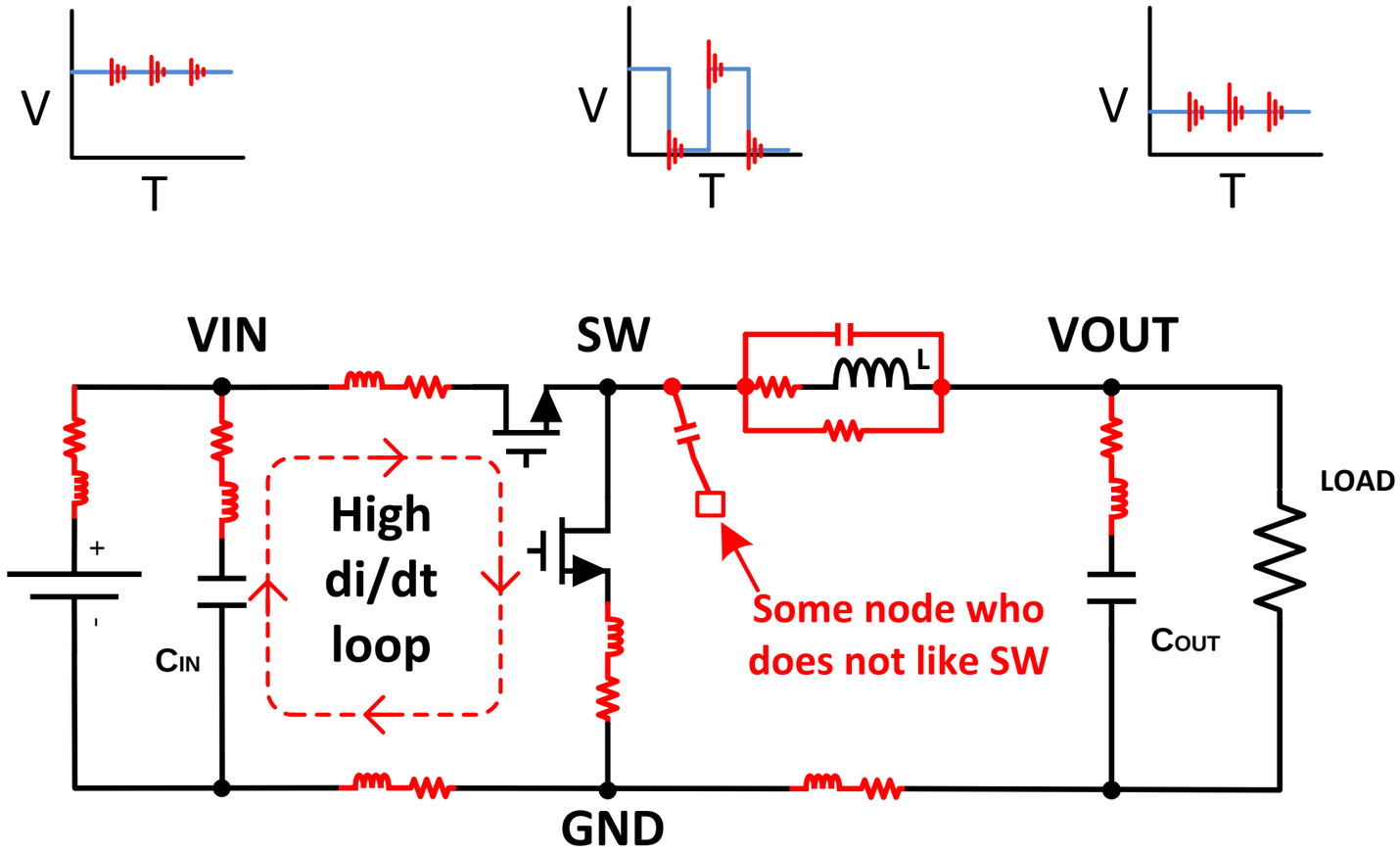
- Understanding the Noise Sources
  - DC/DC converter operation overview
  - Noise components (high frequency vs low frequency)
  - Relevant parasitic elements in the circuit
- Measuring Noise
  - What is “real” vs “fake” noise
  - Examples of measurement techniques (good vs. bad)
- Reducing Noise (high frequency and low frequency)
  - Layout techniques and comparison (good vs. bad)
  - Passive component selection and placement
  - Filtering techniques and examples

Understanding the sources of noise

The buck regulator

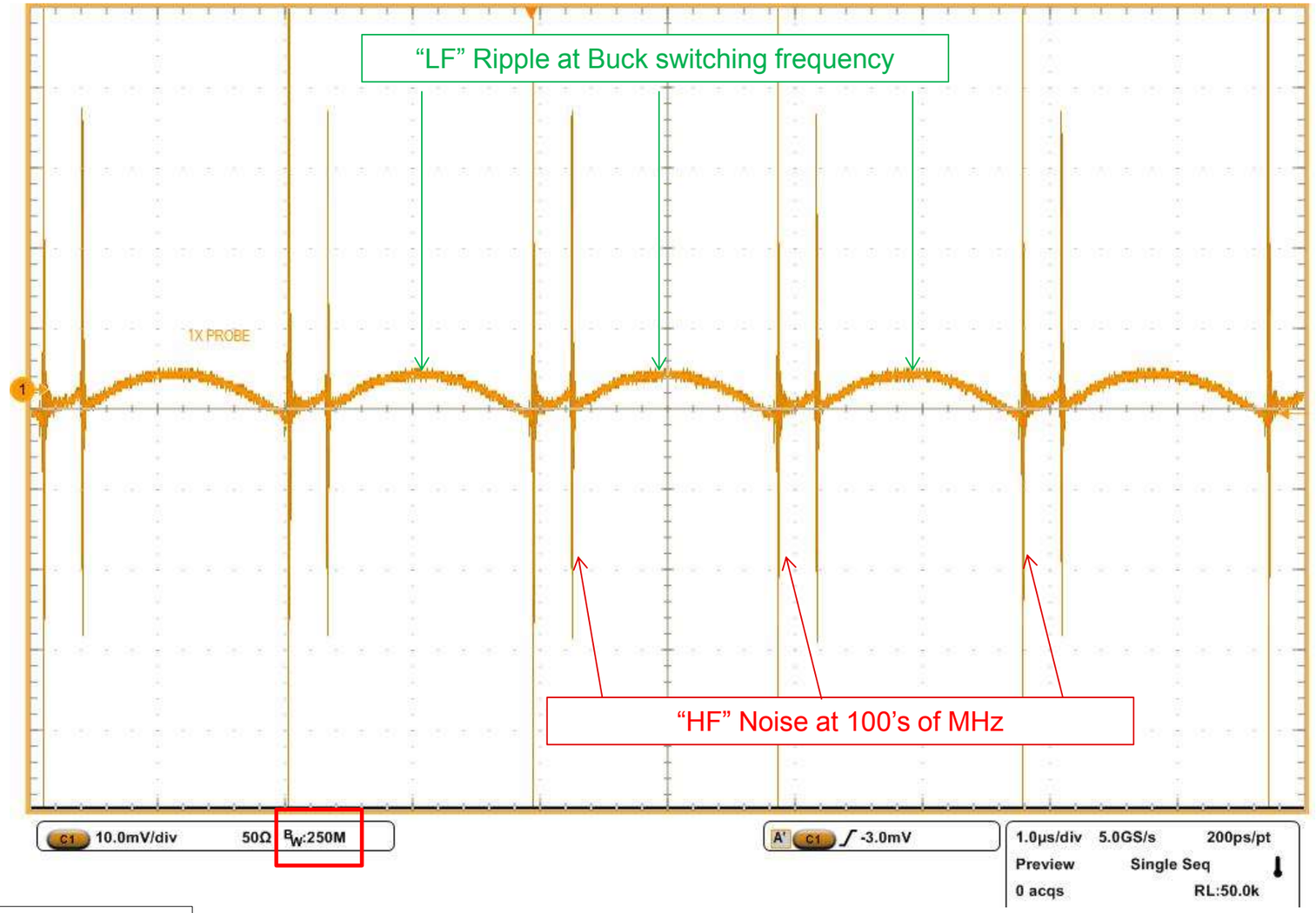


Less ideal buck regulator



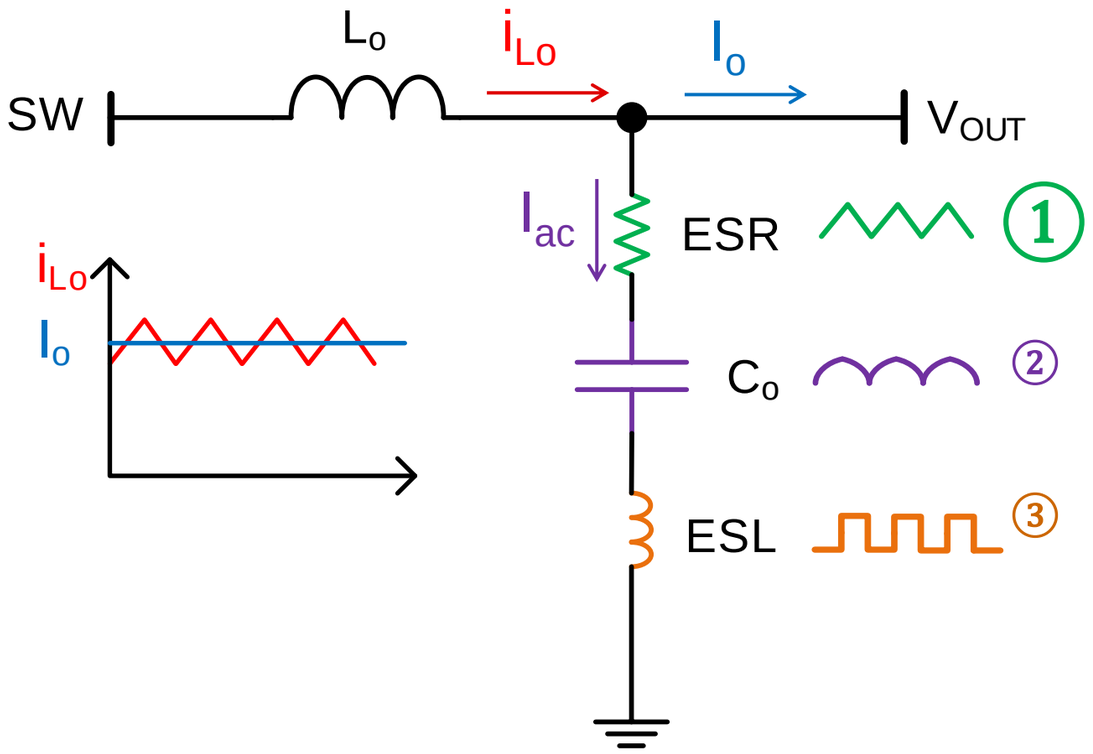
“Free” components in red

Output ripple and noise (example)



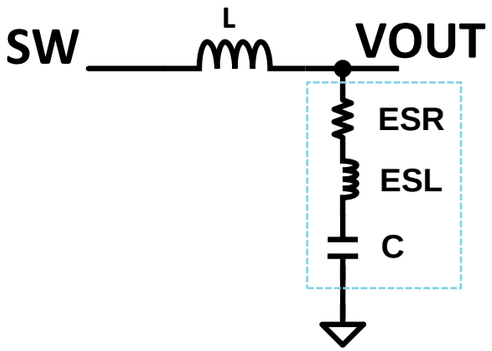
LF ripple origin

- Result of the inductor ripple current and output capacitor impedance



Total LF Ripple = ① + ② + ③

LF ripple with different capacitor types



"47µF" Capacitor

Inductor ripple current

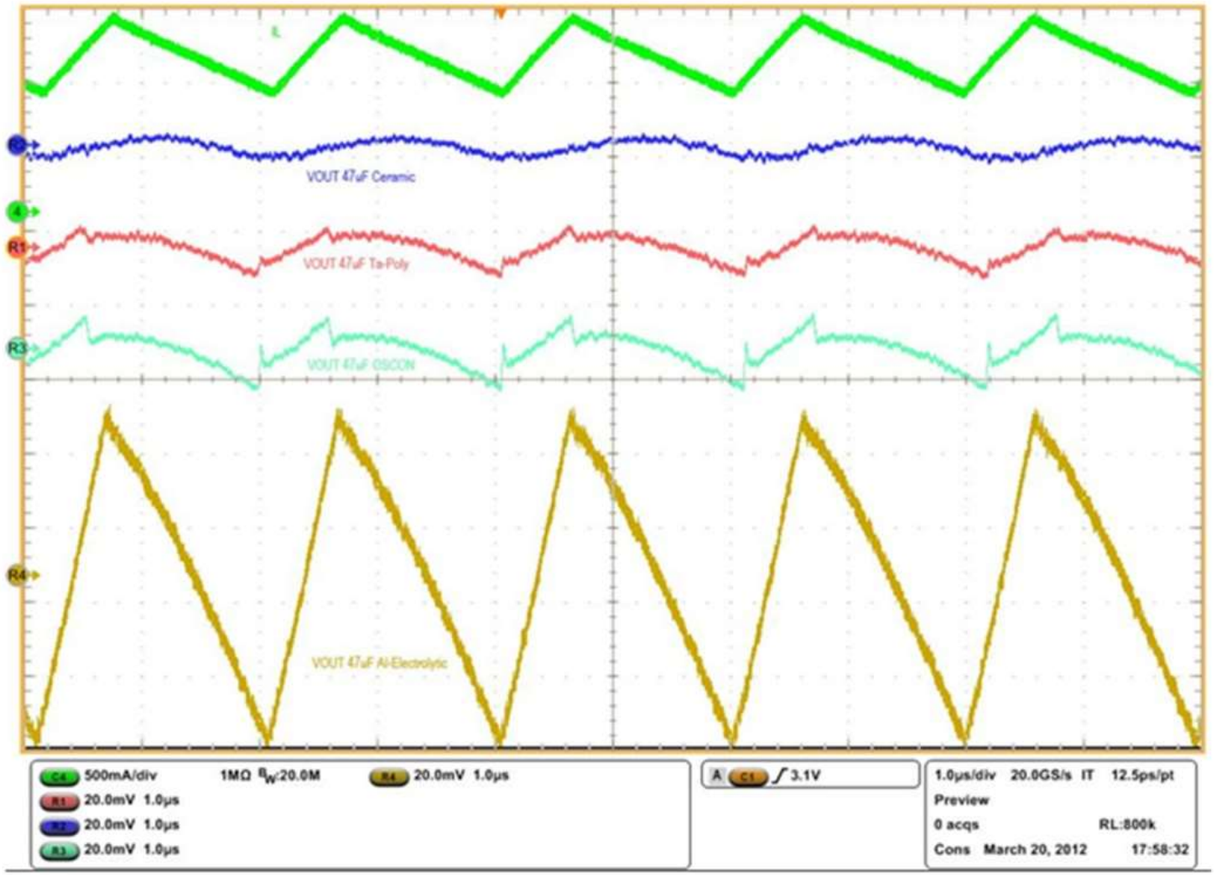
VOUT RIPPLE — Ceramic cap (C dominated, low ESR low ESL)

VOUT RIPPLE — Tantalum cap (medium ESR, some ESL)

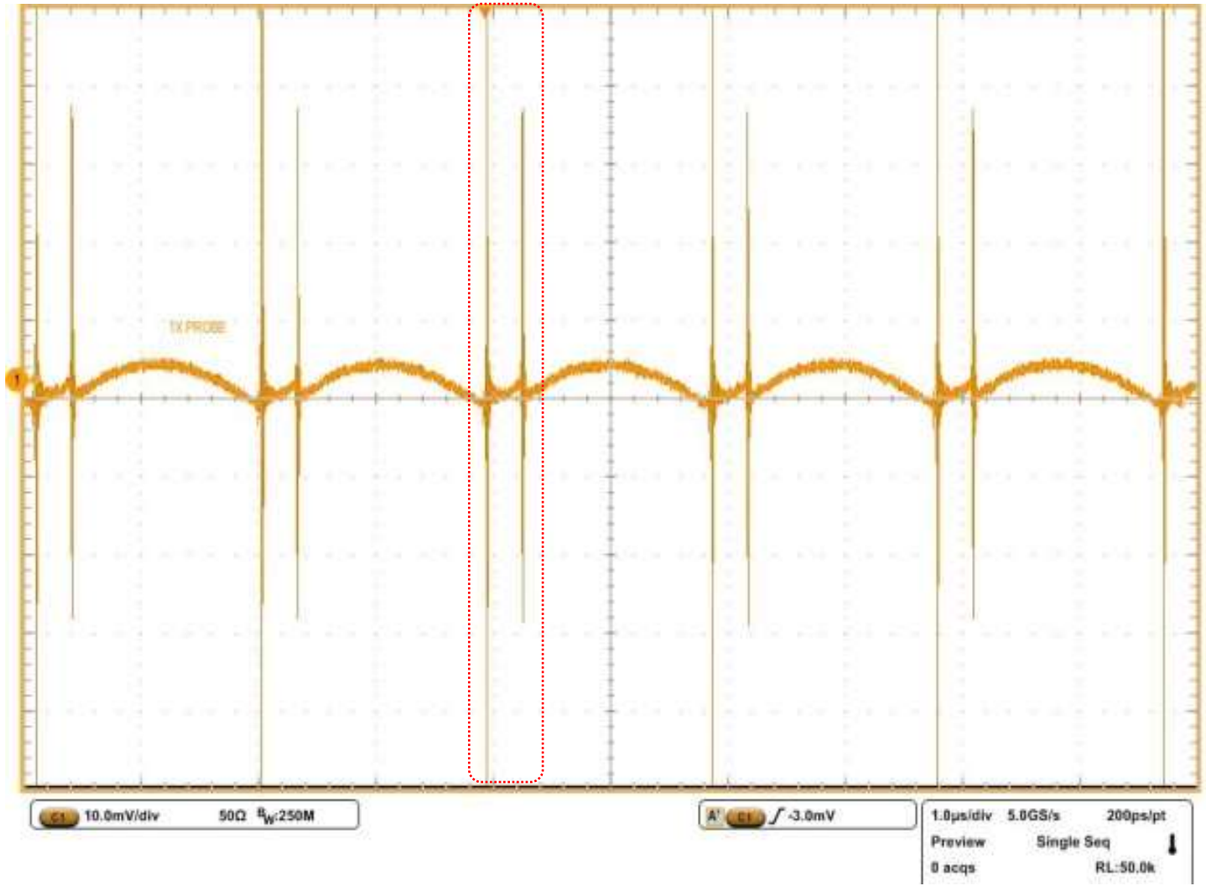
VOUT RIPPLE — OSCON cap (medium ESR, some more ESL)

VOUT RIPPLE — Aluminum Electrolytic cap (ESR dominated)

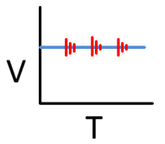
Each capacitor above is 47µF.
The difference is the chemistry

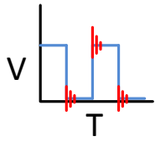


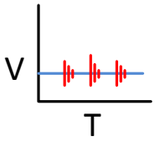
HF noise origin

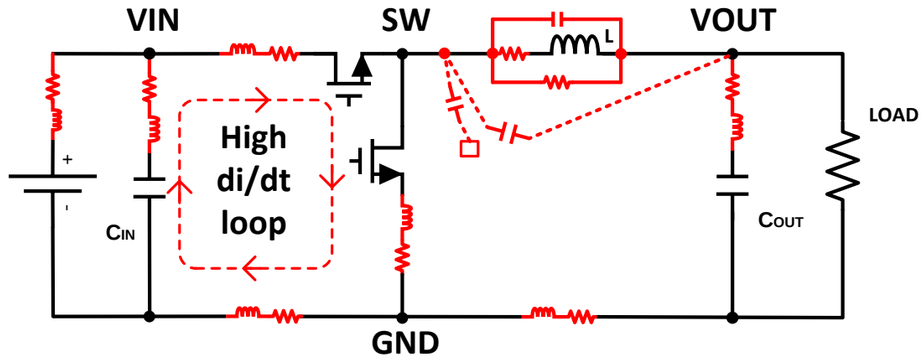


- Who is generating the noise?
  - High di/dt current loop and any inductance in its path
  - Noise appears on the SW node as ringing at each edge





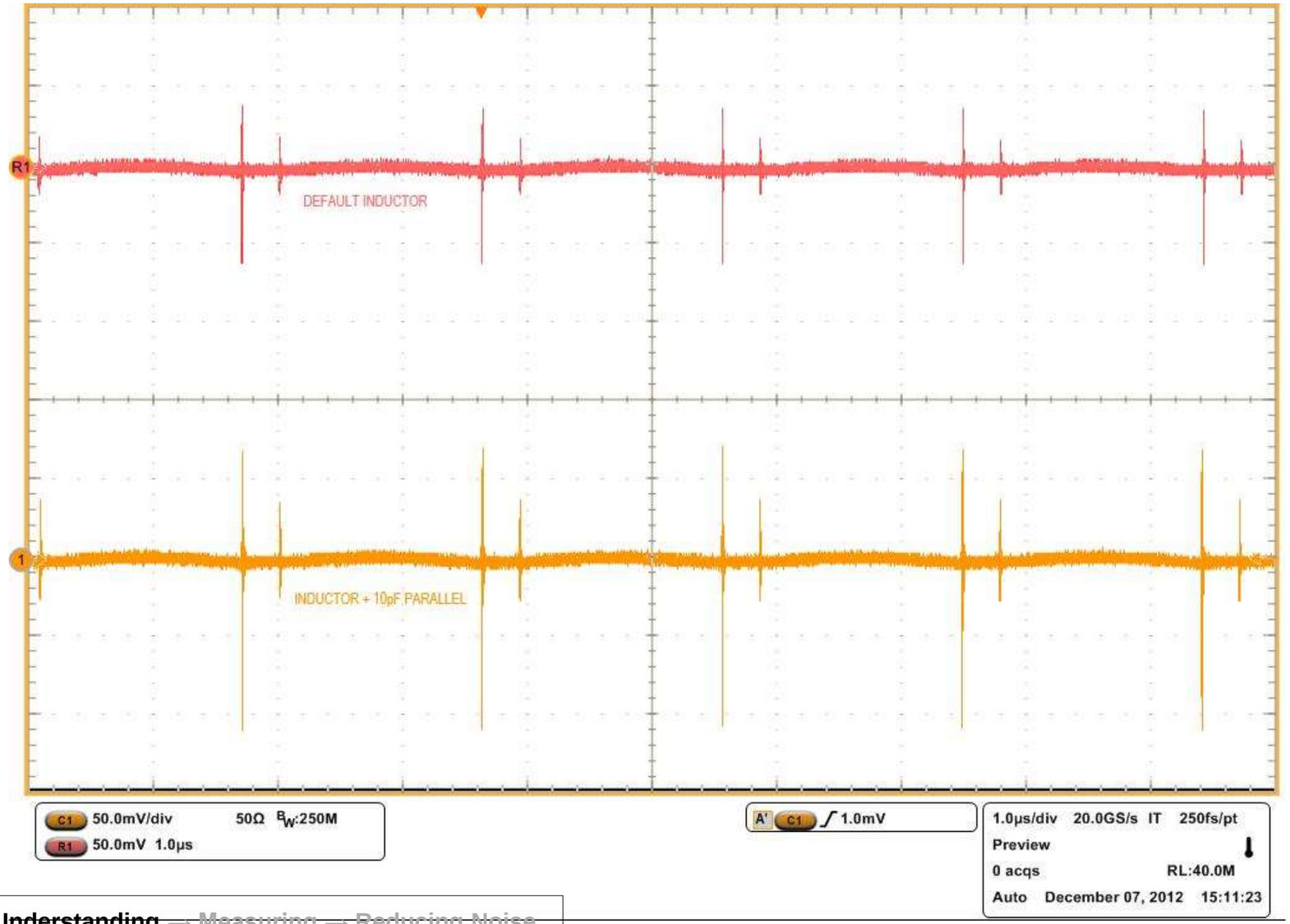




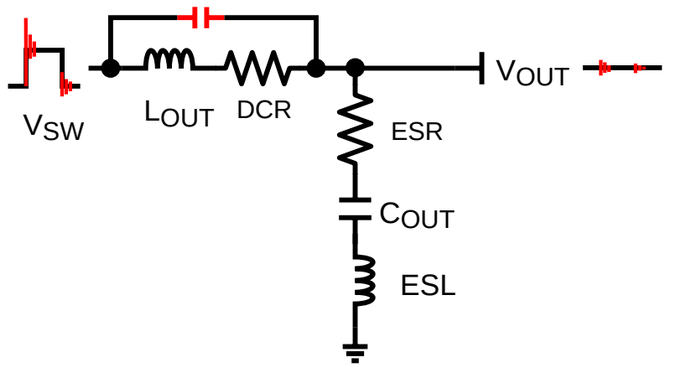
"Free" components in red

- How is the ringing coupled to the output?
  - Parasitic capacitance
    - Across the inductor (could be a few 10's of pF)
    - Between overlapping copper areas on the PCB

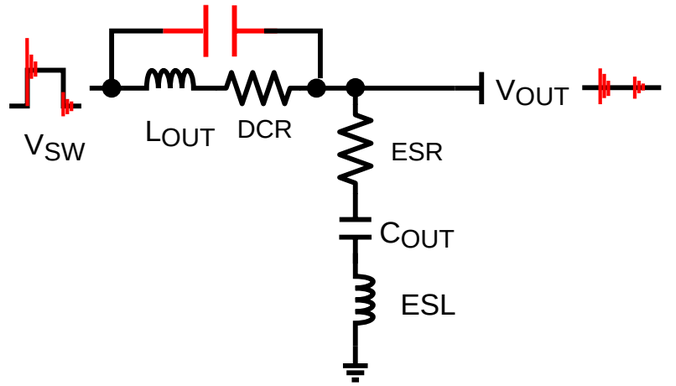
HF noise vs inductor parasitic capacitance



Inductor A



Inductor B

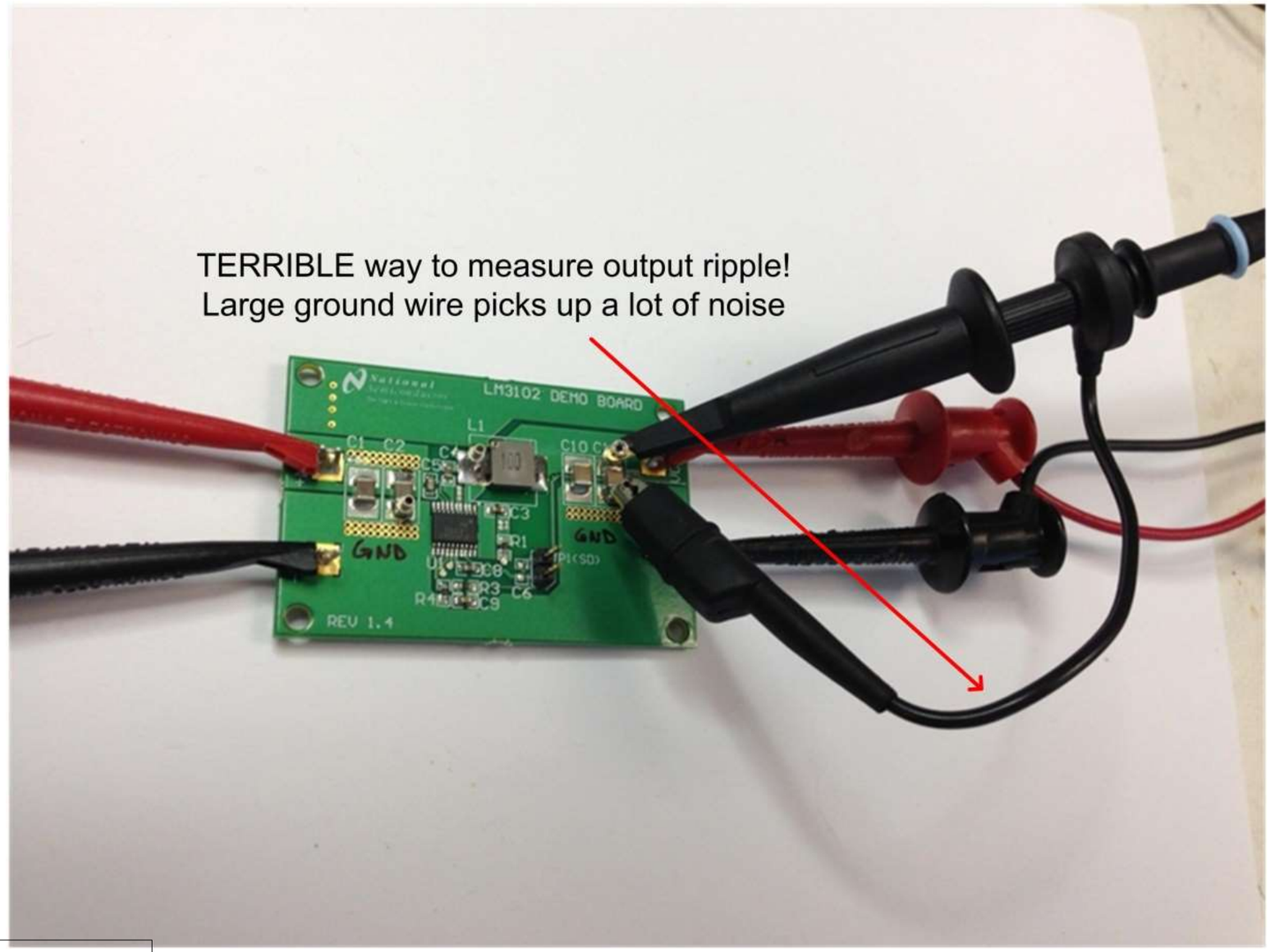


Measuring noise

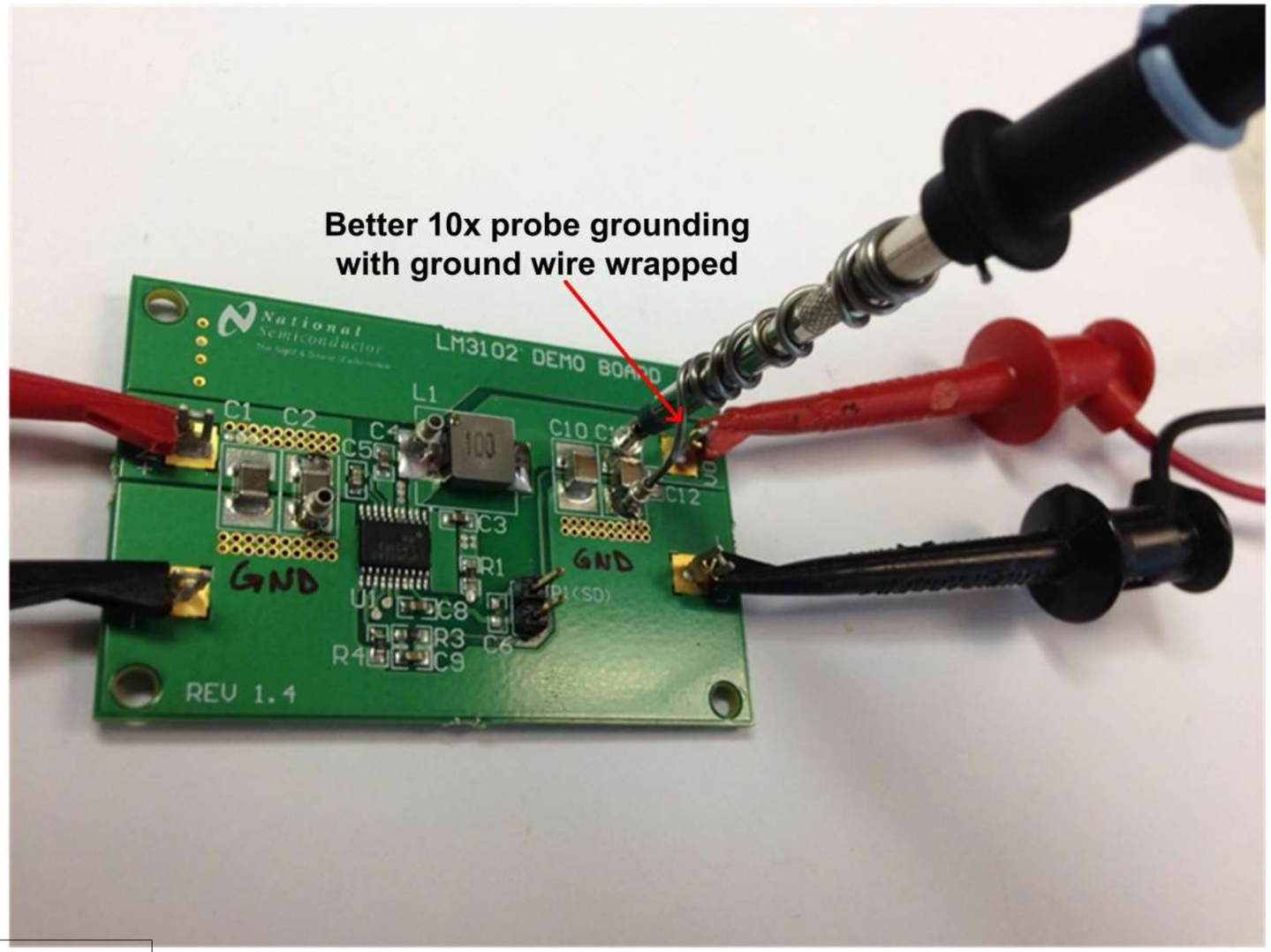
Measuring noise

- Before we explore ways/tools for reducing the output noise, let’s make sure we are measuring it properly.
- Improper measurement techniques can results in exaggerated output noise.
- Exaggerated output noise measurements can result in overly conservative “methods” for fixing it.
- It is important to know the “real” amount of noise before we start reducing it.

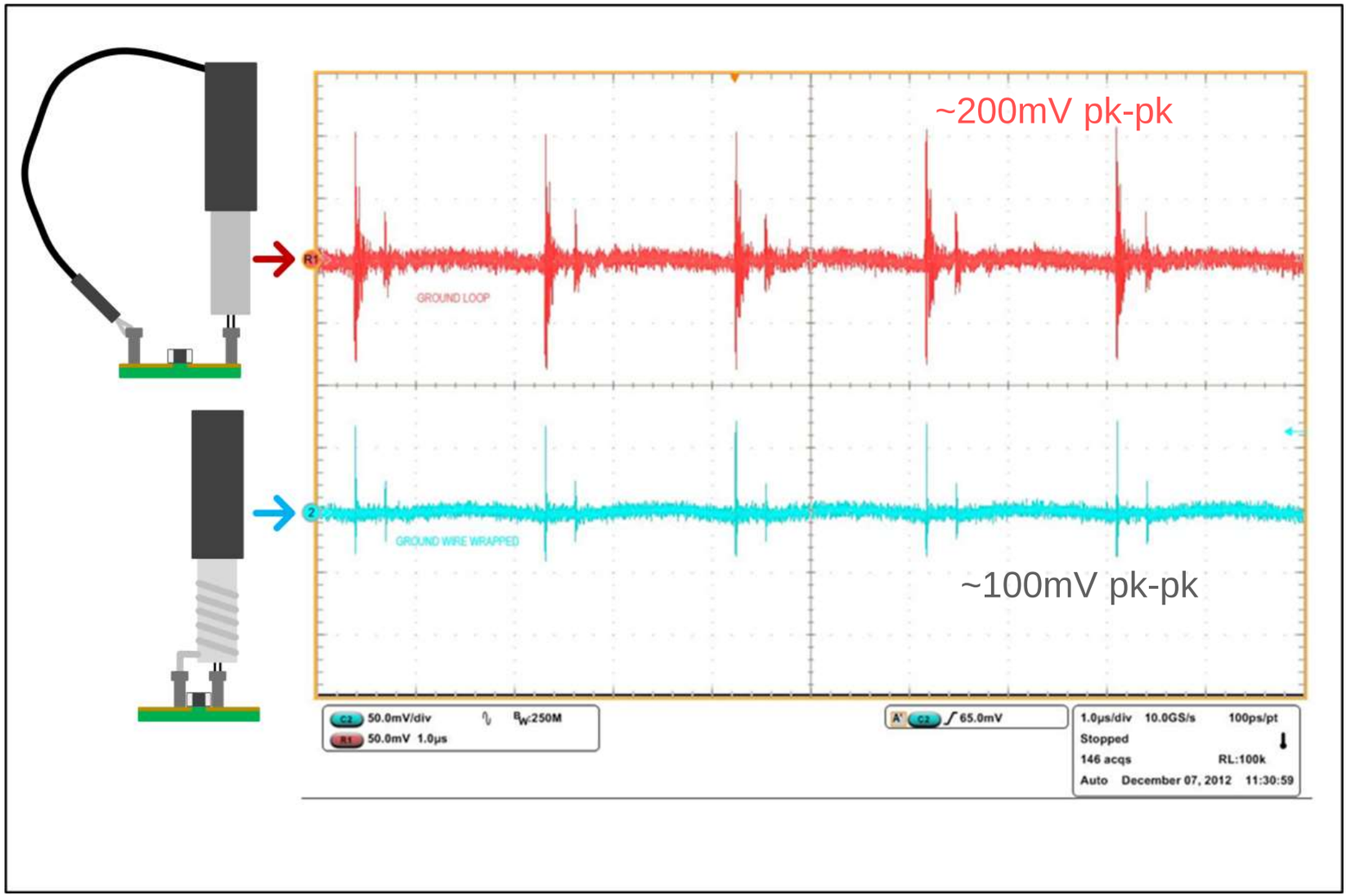
BAD Measurement (example)



Improved measurement (example)



Comparison

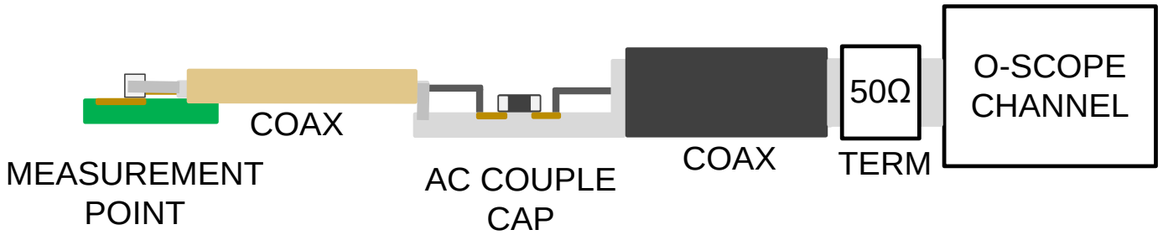


~2x difference in measured noise!

The circuit is exactly the same.
The difference is the measurement technique.

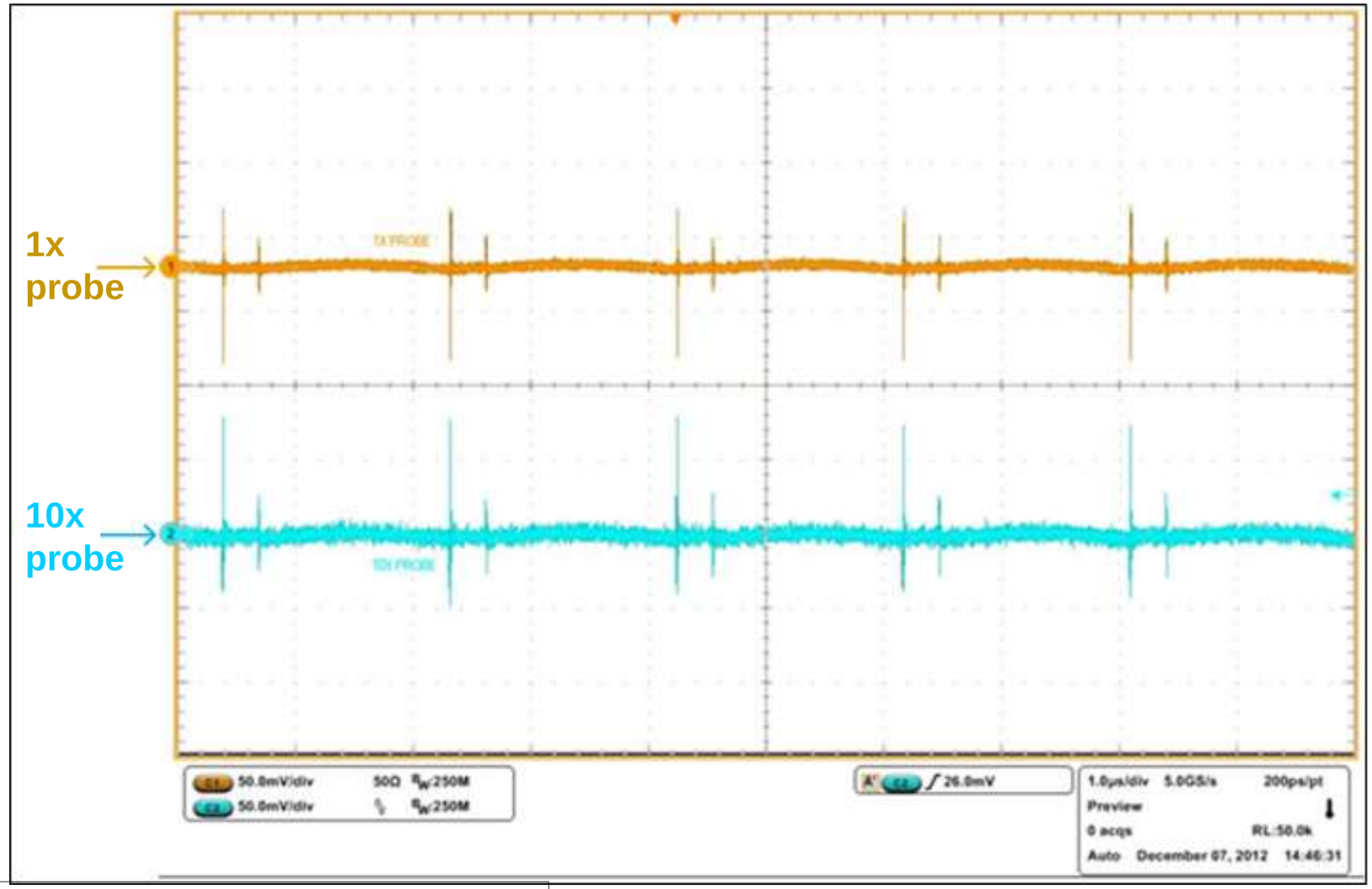
Making a 1x probe (example)

- Short coax cable soldered to the output
- 0.1µF coupling capacitor
- 50Ω termination



- Probe frequency response
- High pass filter with cutoff frequency at 31.8kHz. OK for most modern switchers with loaded output.
- Probe OK for 250MHz scope BW

Advantage of 1x probe



Cleaner reading
Can zoom to 1mV/div for sub 1mV measurements

Fuzzy due to the scope vertical sensitivity limitations of a 10x probe.
Cannot zoom below 10mV/div

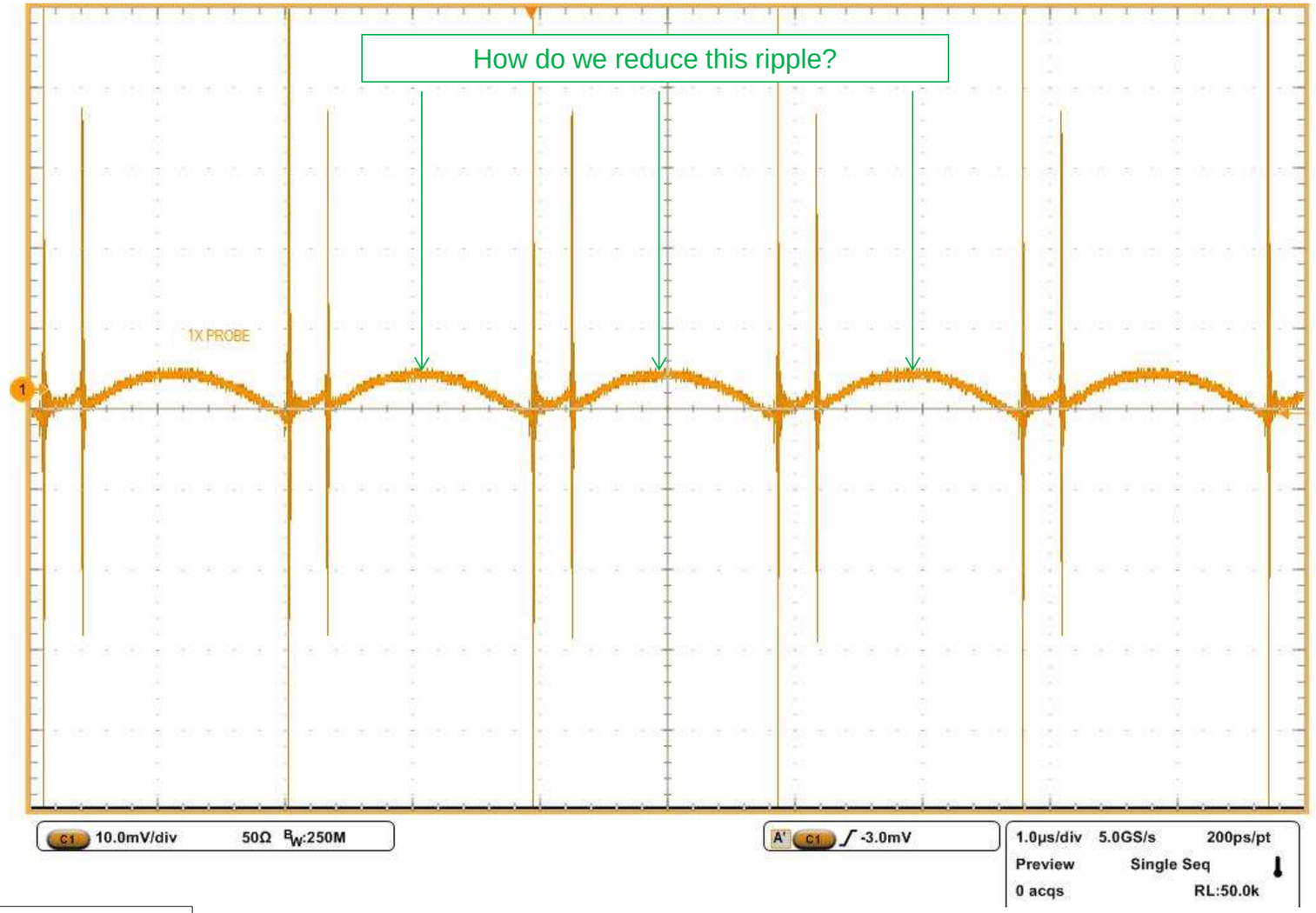
Reducing noise

Reducing noise - toolbox

- LF Ripple
  - Inductor vs Switching Frequency
  - Output capacitor
  - Post filtering
- HF Noise
  - Component placement
  - Component selection (with attention to packaging parasitics)
  - PCB routing and stack-up
  - Filtering
    - Input filters (conducted EMI)
    - Output filters (small HF capacitors)

LF ripple reduction

LF ripple reduction

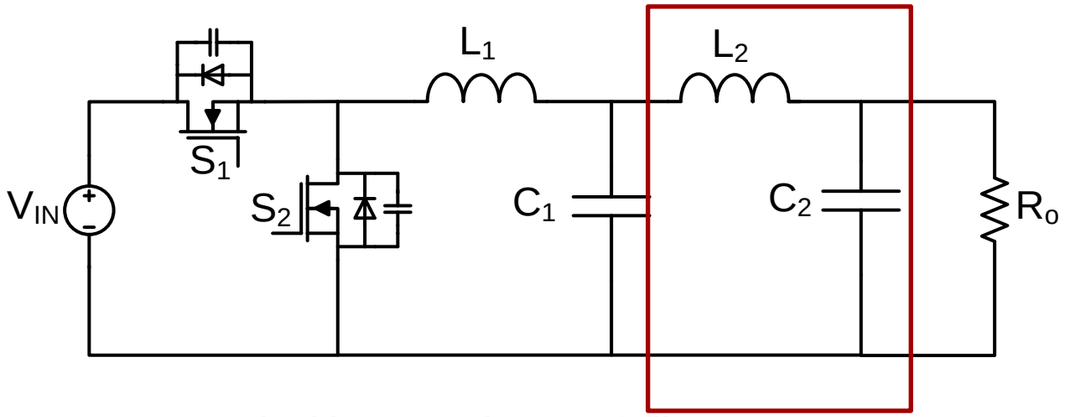


LF ripple – switching frequency and inductance

- We understand that the LF ripple is a function of the inductor ripple current and the output capacitor(s) impedance.
- We can:
  - **Lower the ripple current**
    - For the same inductor, increase the switching frequency
      - Tradeoff: increased switching losses
    - For the same switching frequency, increase the inductance
      - Tradeoff: increased solution size
  - **Lower the capacitor impedance**
    - Use low ESR and low ESL capacitors
      - Tradeoff: perhaps cost
    - Use multiple capacitors in parallel
      - Tradeoff: cost, board space

LF ripple – second stage filter

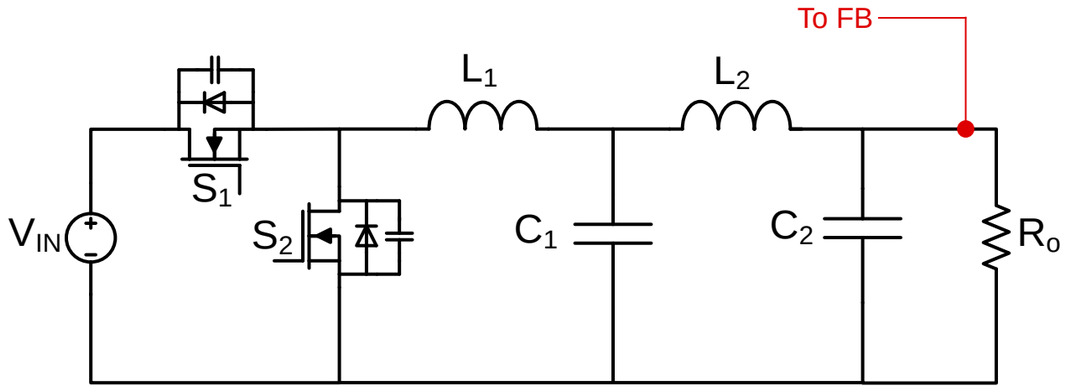
- Certain applications, such as test and measurement, are sensitive to the voltage ripple and routinely require very low output voltage ripple, such as 0.1%.
- To attain this level of attenuation it is required to add another pair of L and C to the output of a buck regulator as shown in the image below.



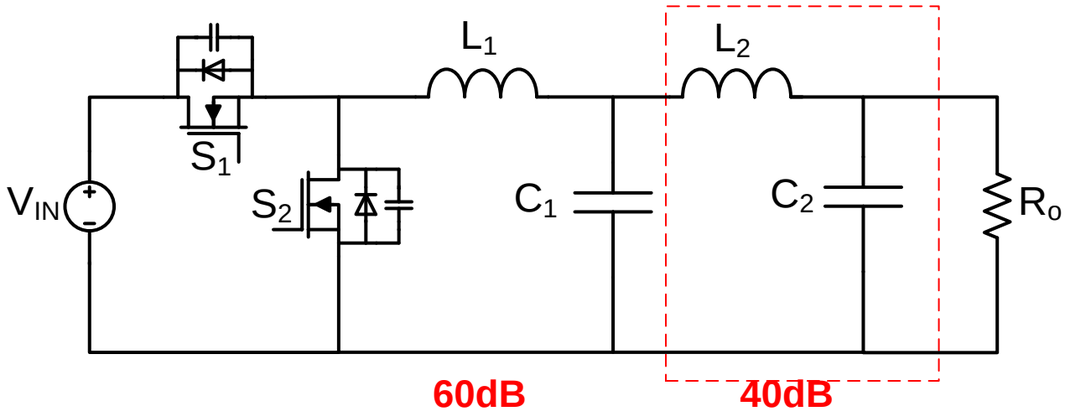
Buck with a second-stage LC filter

Second stage filter and output sense

- Common concern is how to position the 2nd stage filter – before or after the feedback (VOUT) sense point.
- **Assumption**: The second stage filter should be placed after the VOUT sensing point to avoid instabilities.
- **Reality:** Regardless of the connection the filter still interacts with the original output capacitance and there is resonance created.
- Connecting the filter before the VOUT sense:
  - allows us to account for it in the stability review
  - there is no load regulation penalty – resistive drop is compensated by the sense.



Second stage filter – component calculations

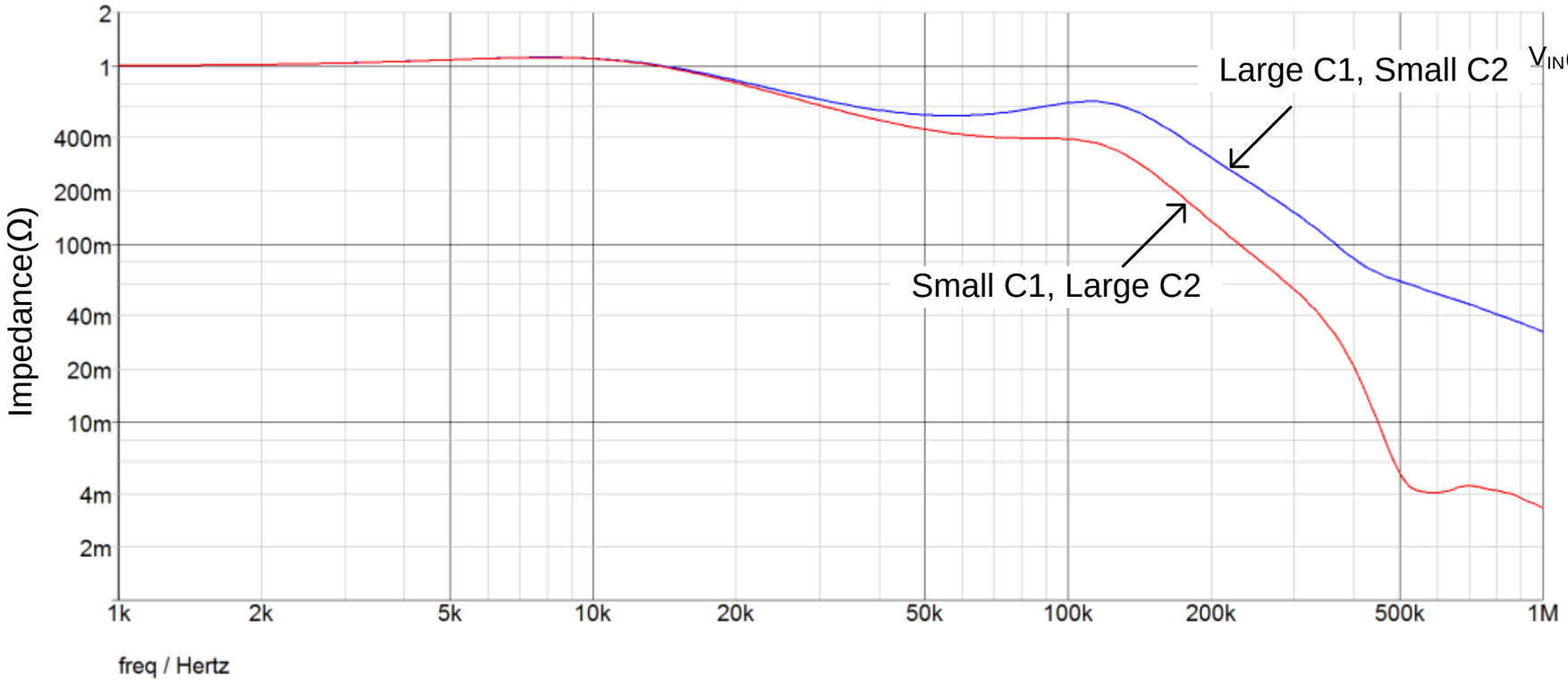


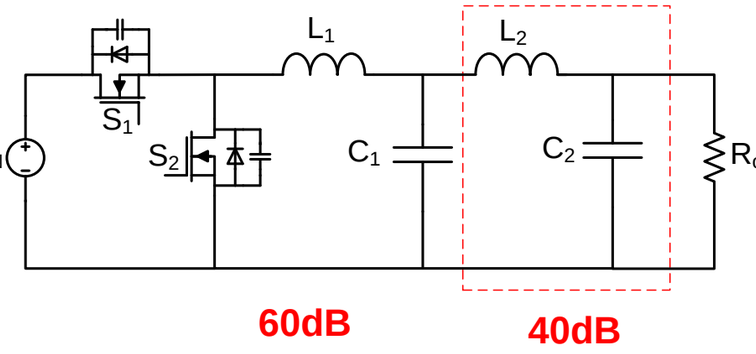
Buck with a second-stage LC filter

- Improper design of the second stage filter could make the converter unstable.
- Two objectives
  1. Attenuation
  2. Loop stability

Second stage filter – component calculations

- To ensure low impedance and to make sure the filter doesn't affect the loop substantially, the ratio of first stage (C1) to second stage capacitance (C2) is set to 1:10
- The value of the secondary inductor is then chosen for the remainder 40dB attenuation.





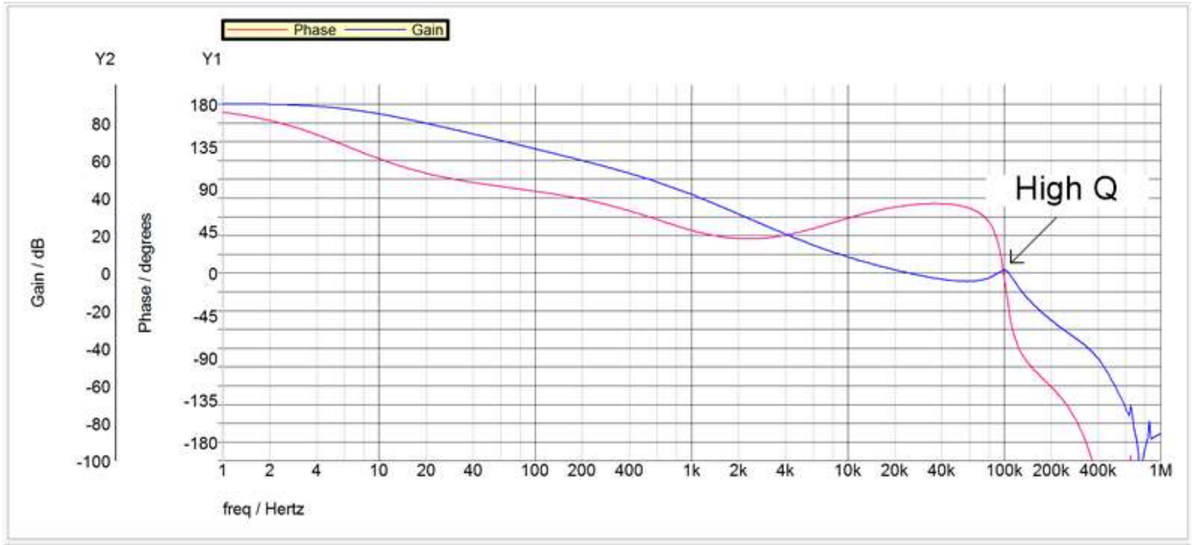
Steps:

1. Calculate L1 (usually based on ripple current)
2. Calculate C1 based on the 1st stage attenuation
3. Set C2 to be 10 x C1
4. Calculate L2 based on the 2nd stage attenuation

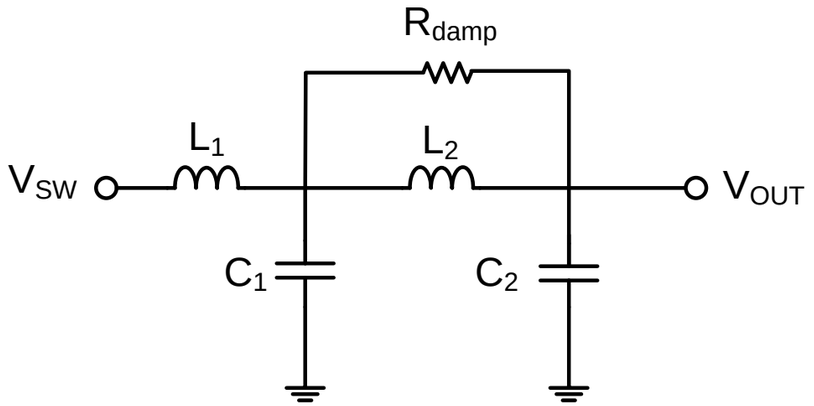
Closed output impedance with different filter designs

Second stage filter – Q and damping

- There may be a need to add a damping resistor in parallel with the inductor



High Q results in low phase margin



Placing the resistor parallel to the inductor damps the Q

Second stage filter – choosing Rdamp and L2

- LMZM23601 with second stage filter.

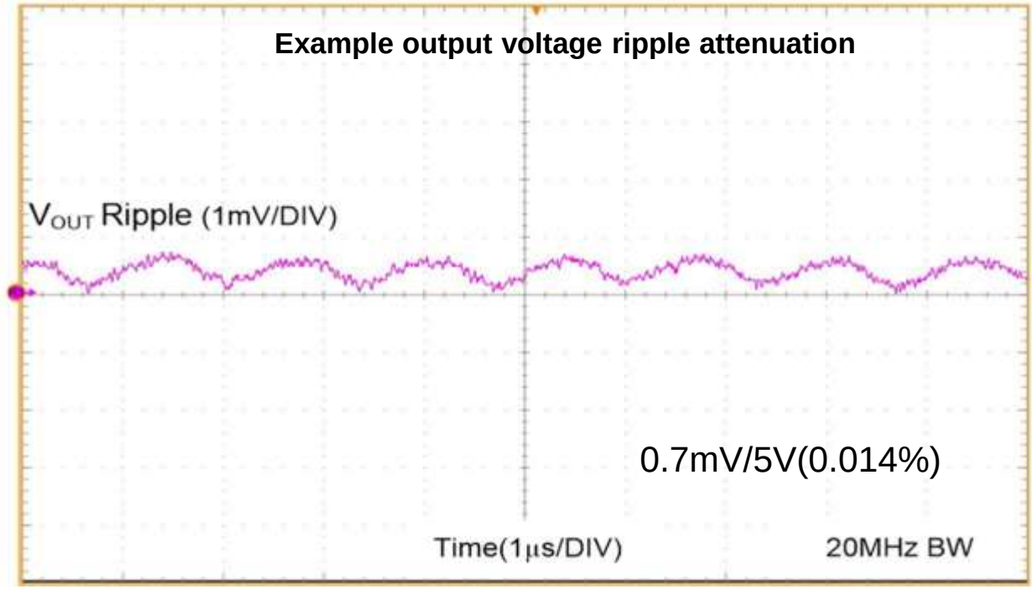
Filter Calculator with Equations

LMZM23601 with a second-stage filter

Second stage filter - results

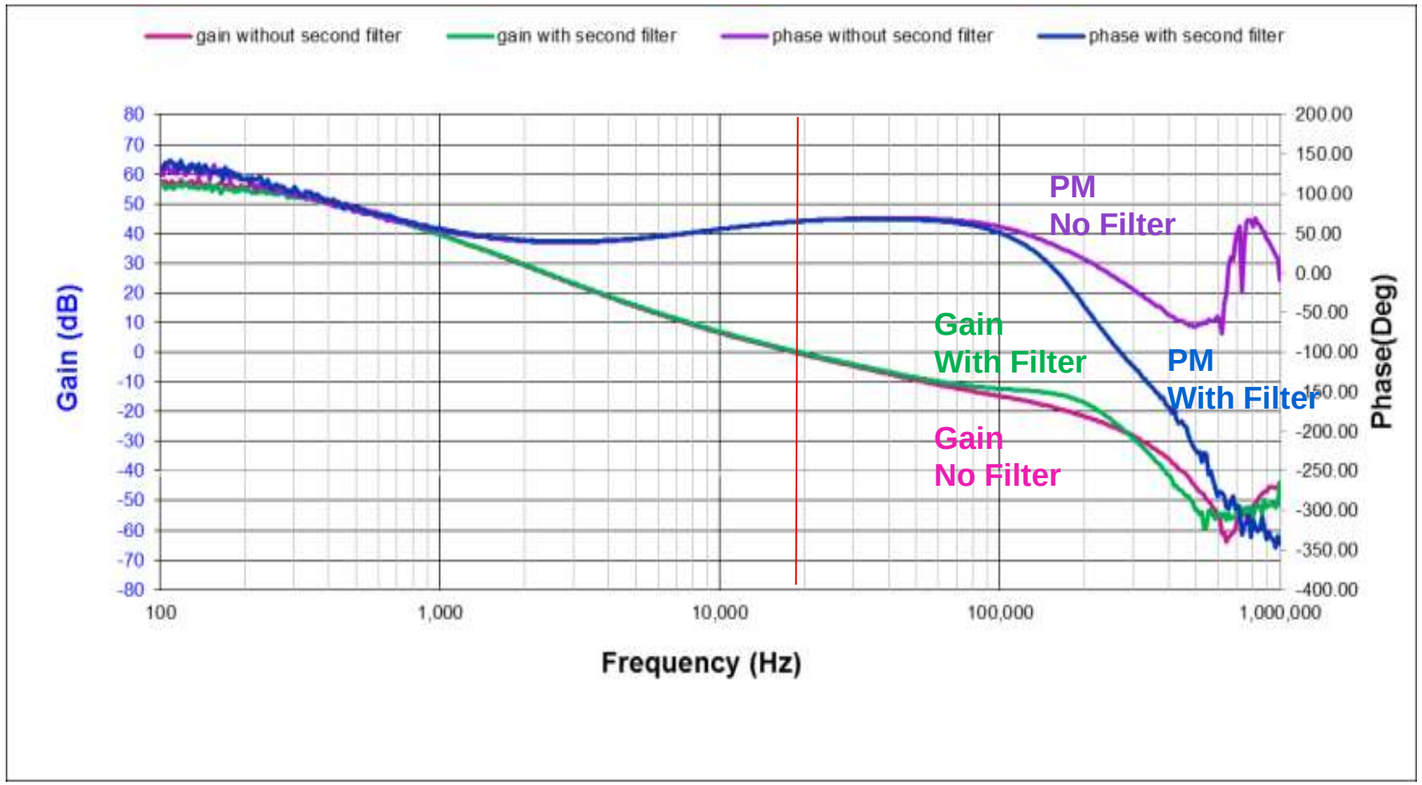
- LMZM23601 with second stage filter.

Attenuation



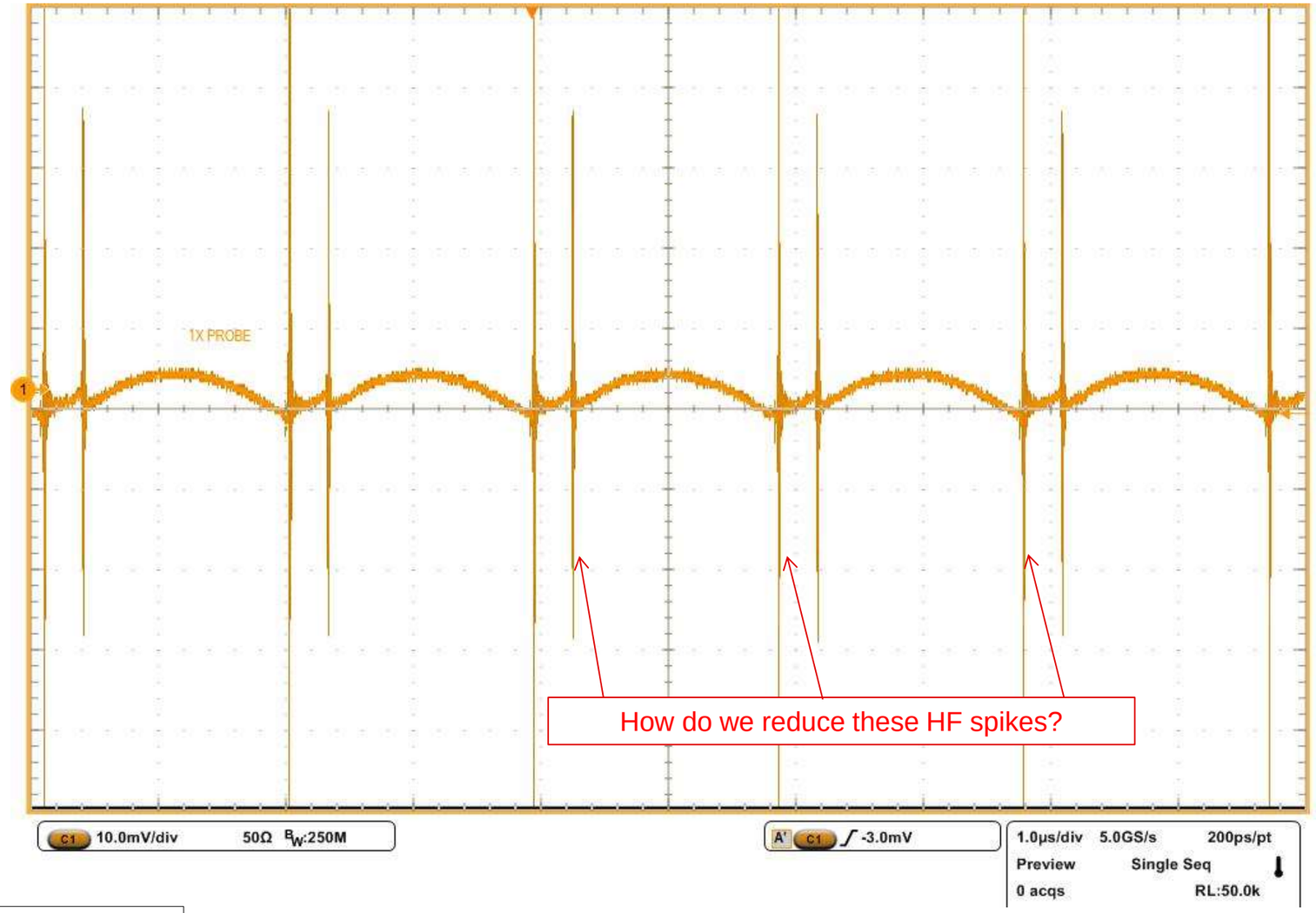
Stability

Bode plot with and without the second-stage filter



HF noise reduction

HF noise reduction



HF noise reduction – component placement

- First step is to optimize (minimize) the area of the **high di/dt loop**.
- For Buck, the high di/dt loop is formed by the input capacitor and the power MOSFETs (switches).
  - Input capacitor as close as possible to IC = Smaller loop area
  - Smaller loop area = Lower ringing on SW node
  - Lower ringing on SW node = Lower output noise
- So first step = optimize input capacitor placement for Buck

HF noise reduction – component placement

TECH DAYS
Texas Instruments

- For a Buck converter…
  - The **INPUT cap** position affects the **OUTPUT noise**!
  - The **INPUT cap** position affects the **OUTPUT noise**!
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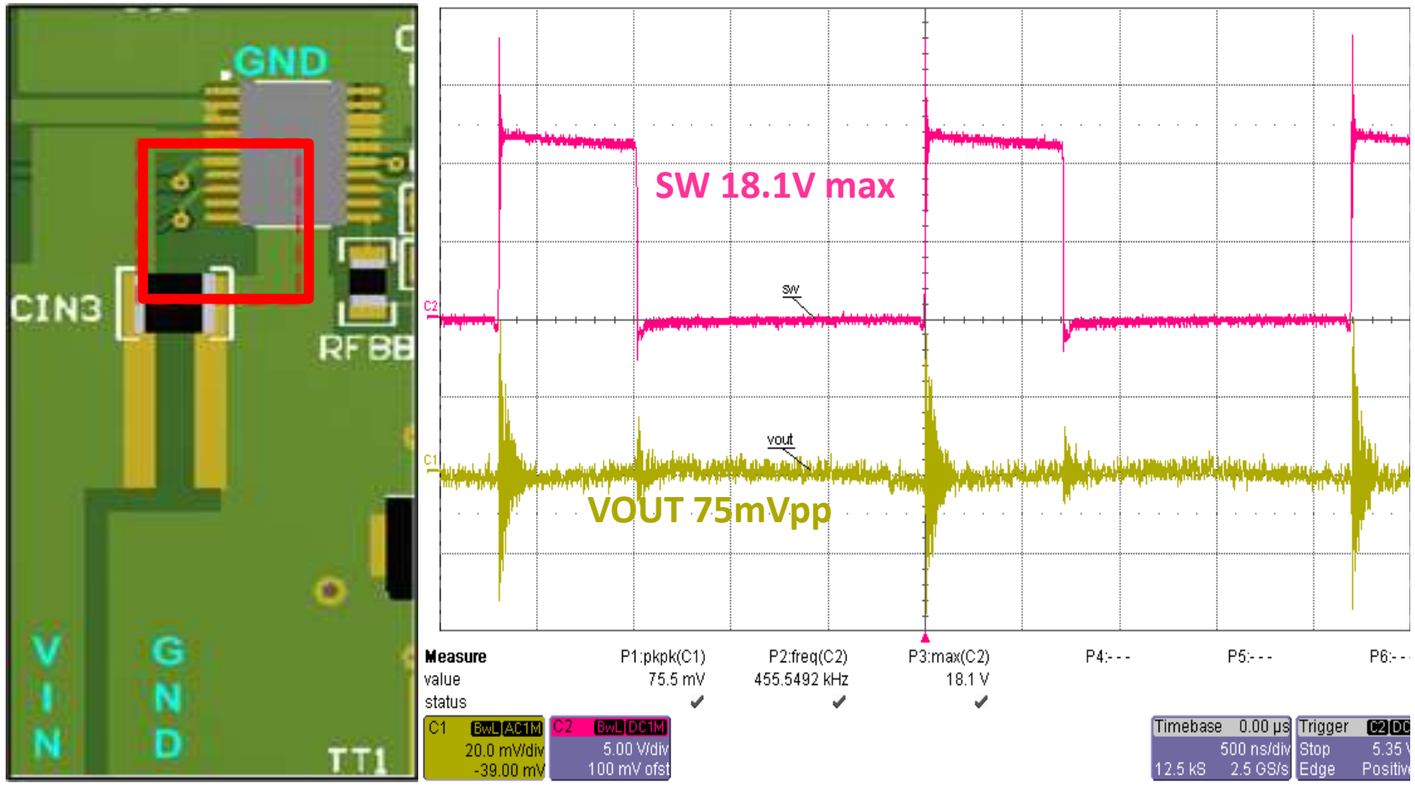
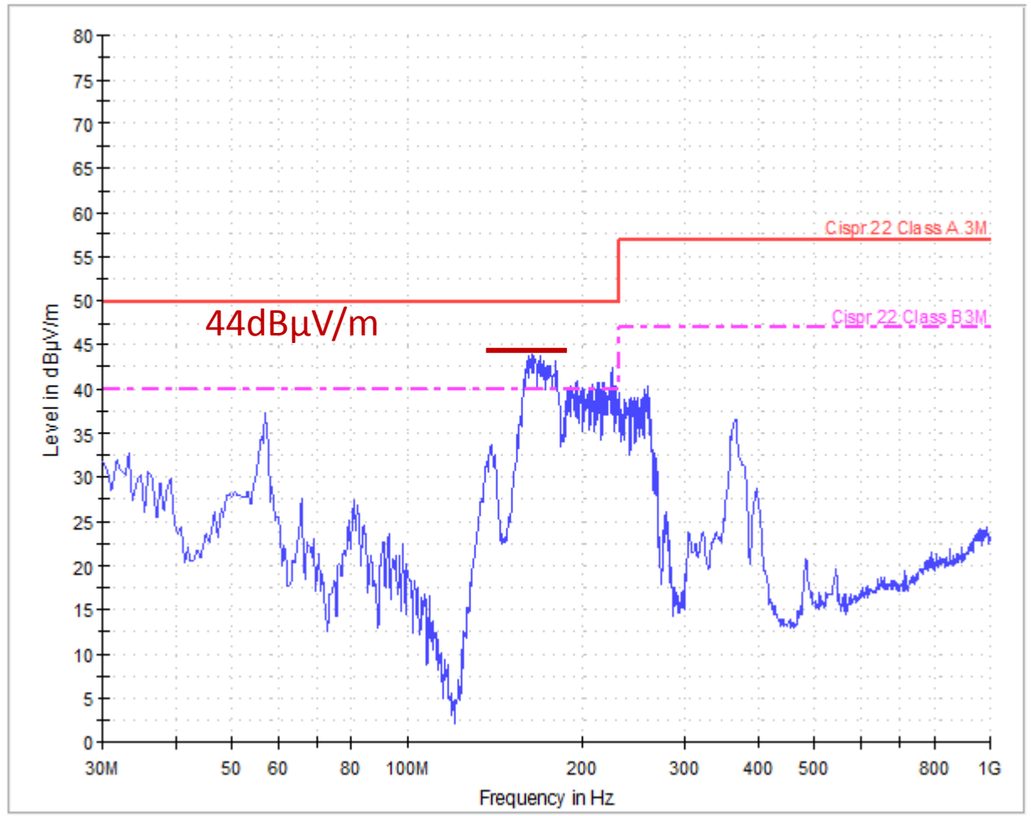
High di/dt capacitor placement - example

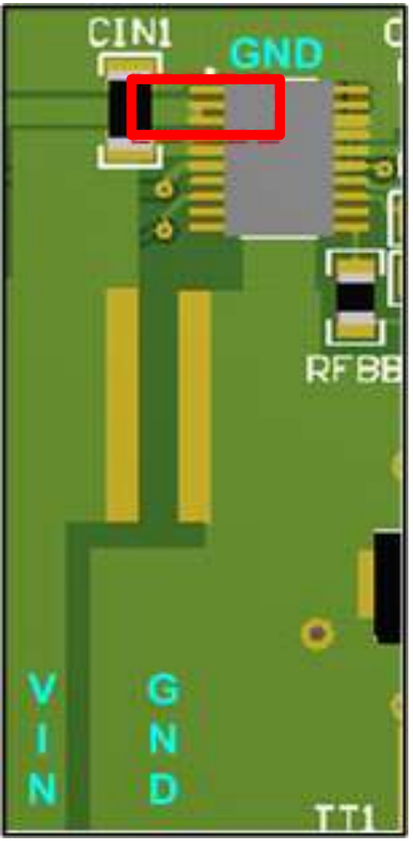
- Buck Regulator comparison with Cin location
- 12V input, 3.3V output, 2A Buck

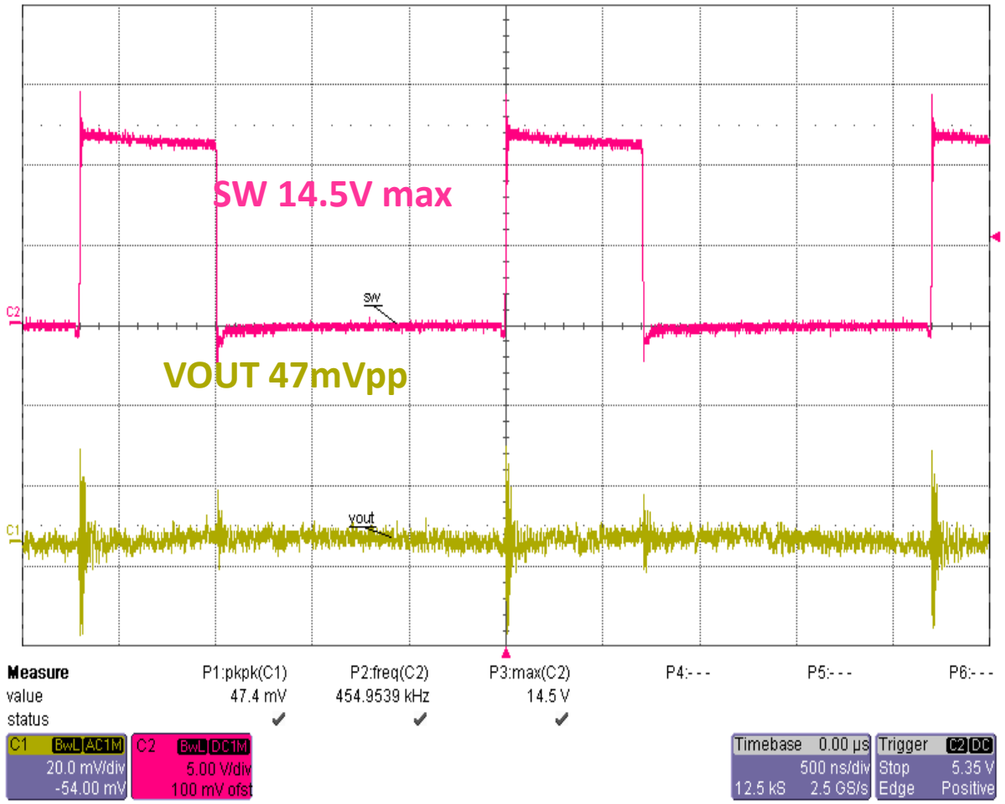


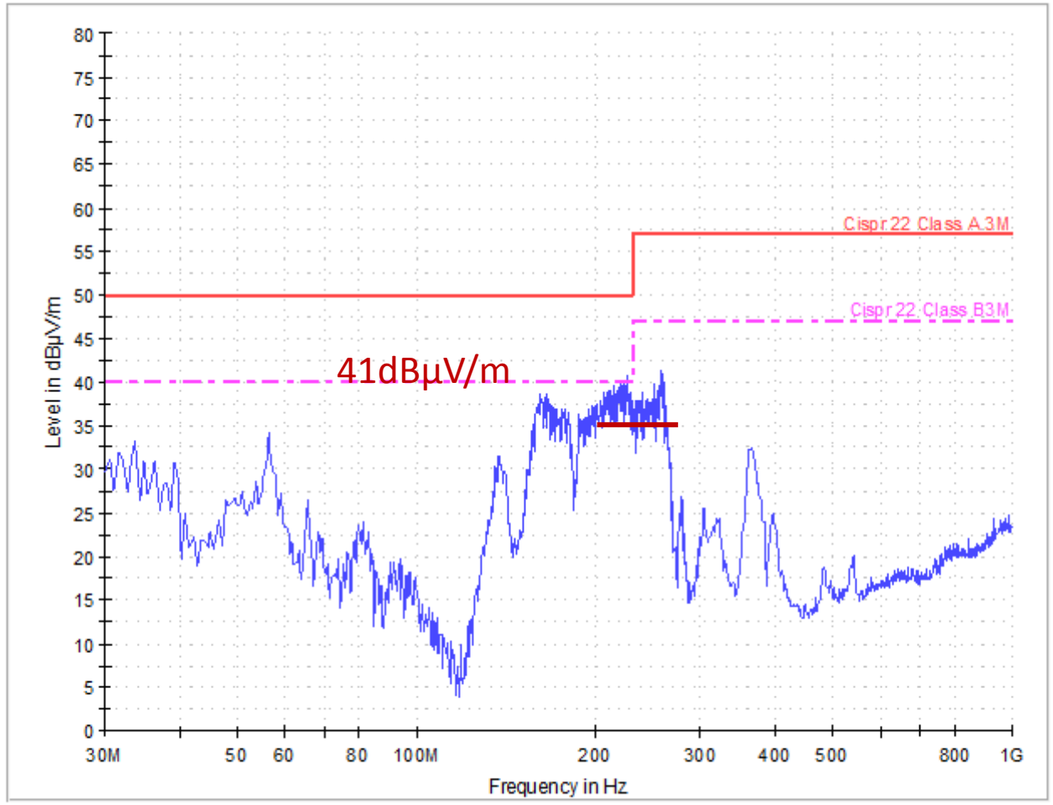


High di/dt capacitor placement - example

- Buck Regulator comparison with Cin location (2 times smaller loop area)
- 12V input, 3.3V output, 2A Buck

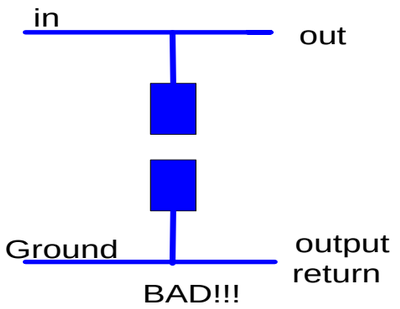


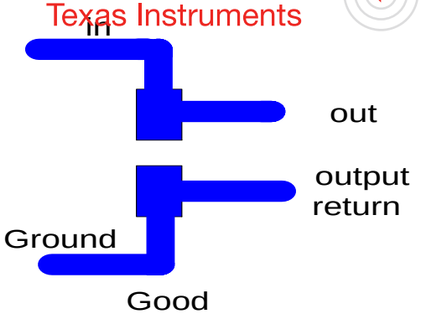


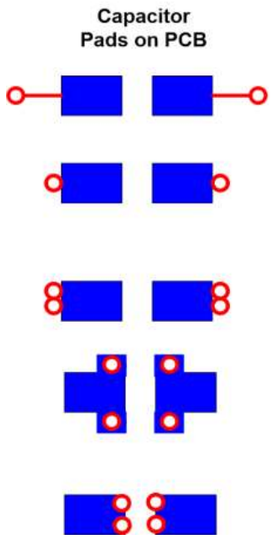


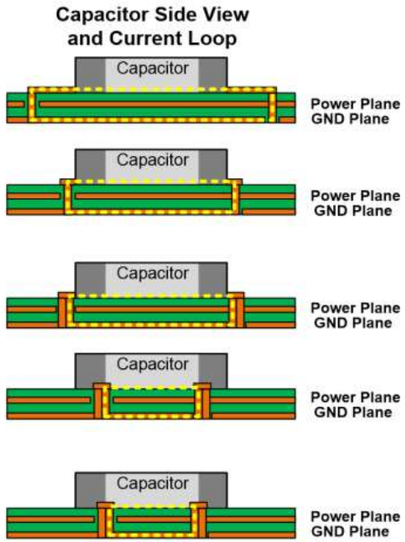
Bypass capacitor routing - example

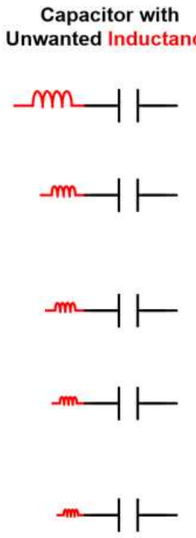
- **Place bypass capacitors on same side of board as component being decoupled**
- **Locate as close to pin as possible**
- **Keep trace width thick and short**

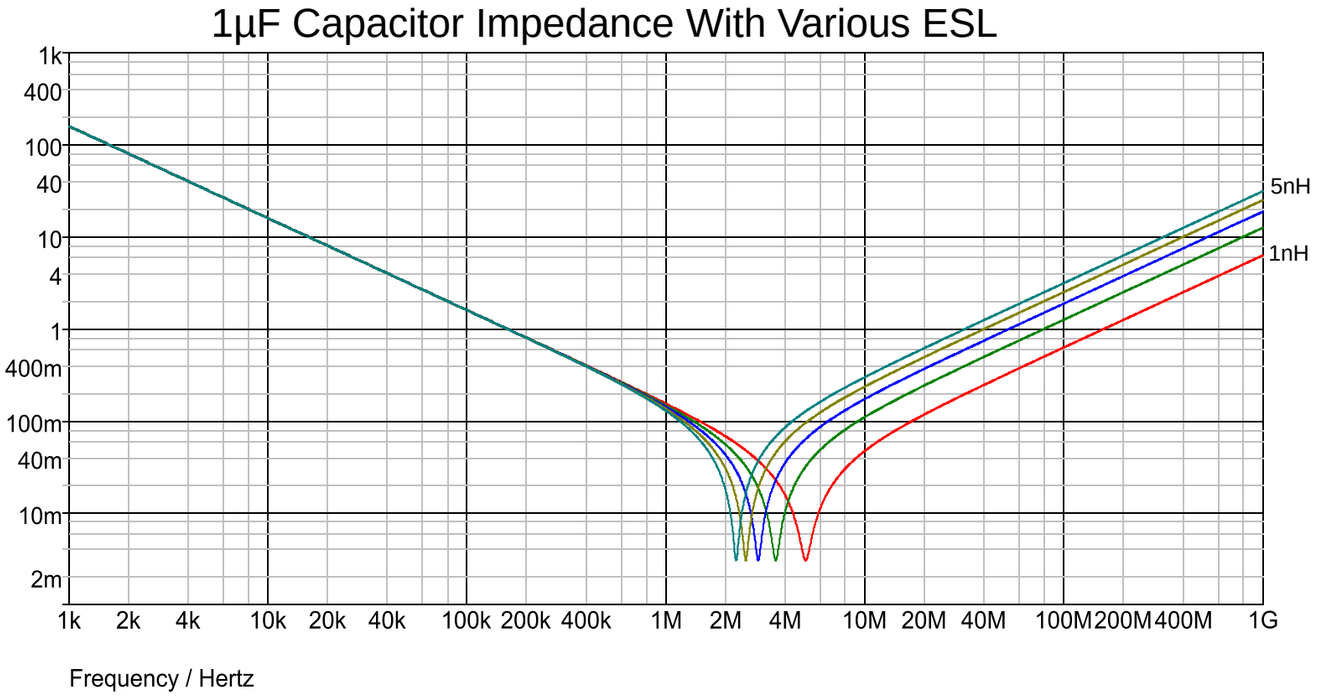






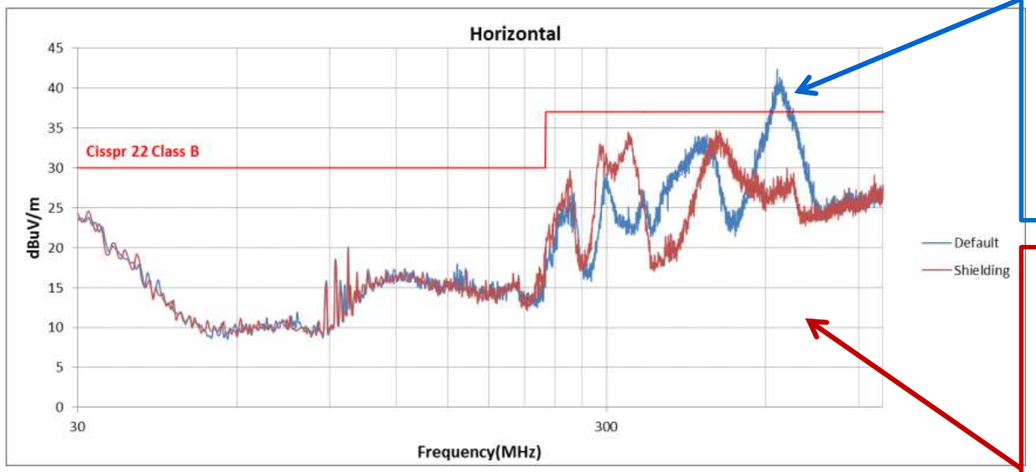


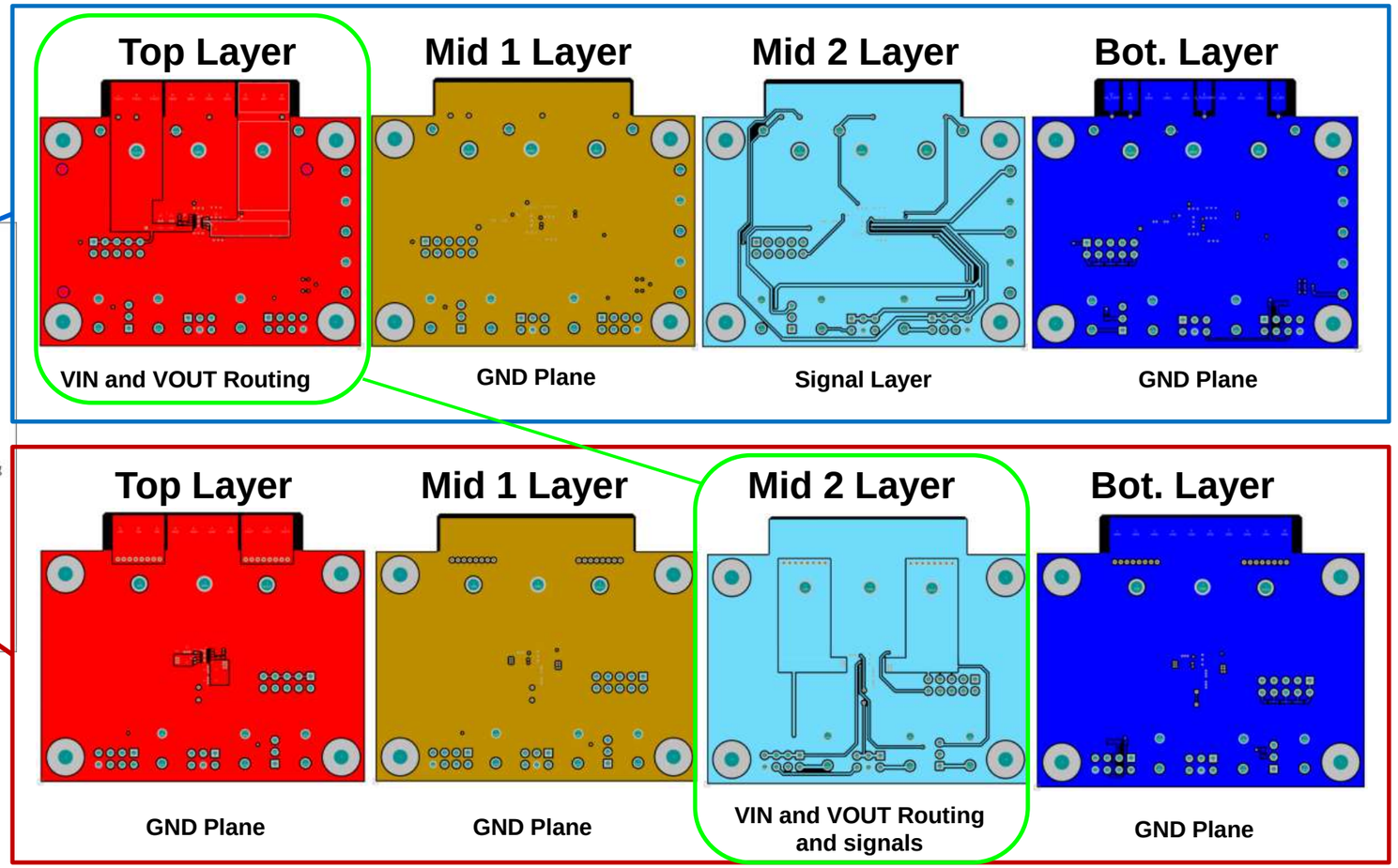




HF noise reduction – board layout tricks

Shielding

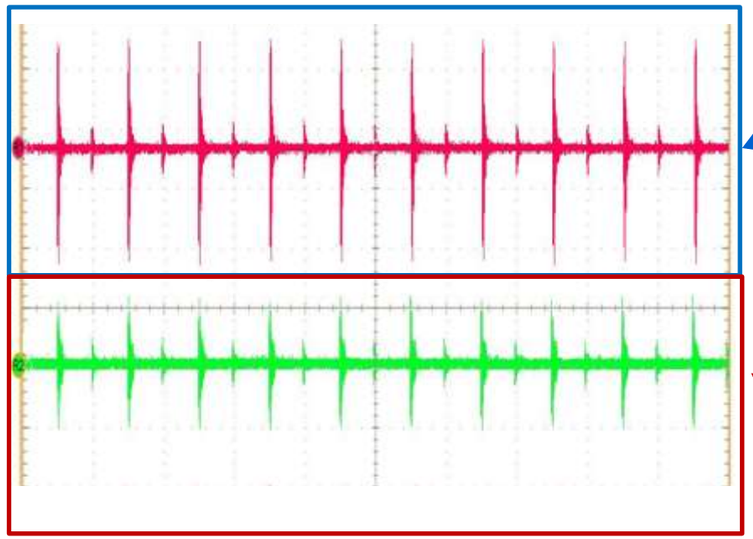


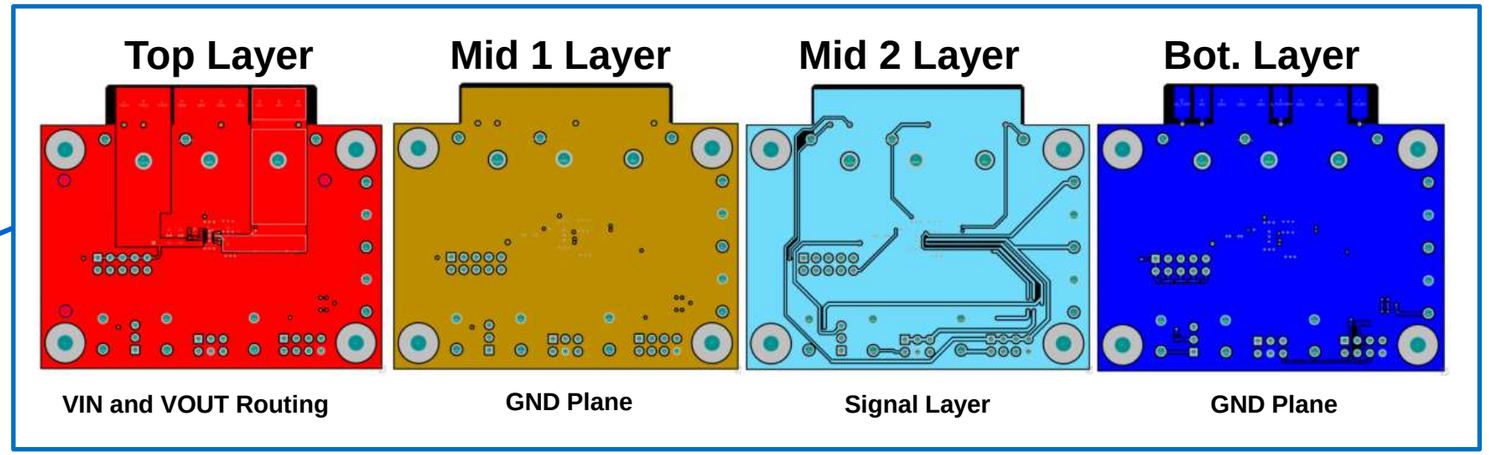


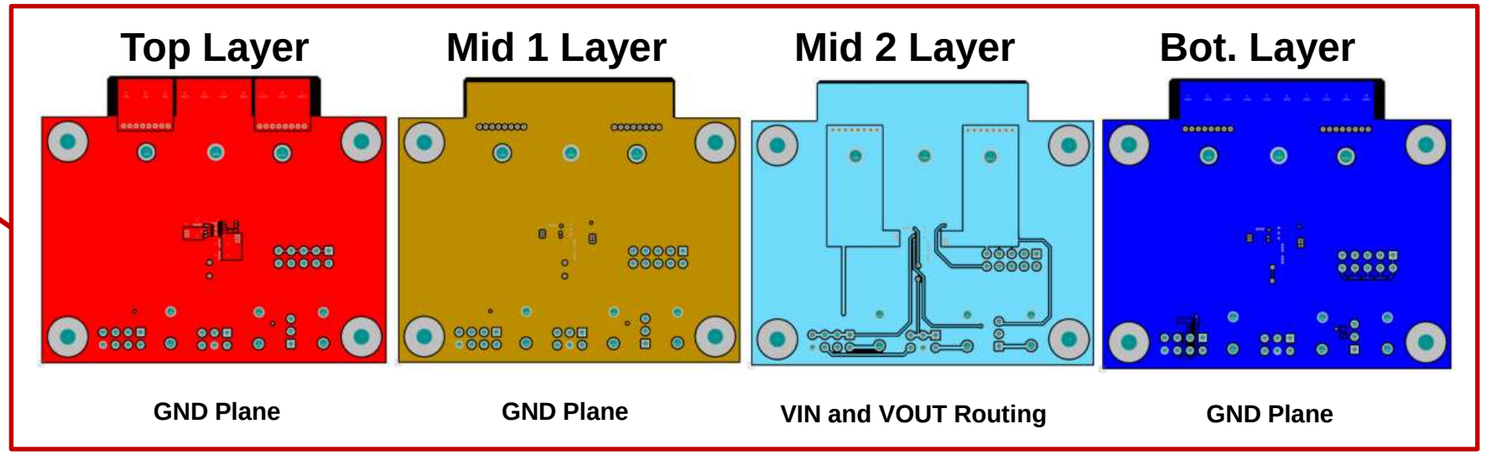
- Same BOM!
- Different stackup
  - Shielding the input (noisy) and output lines
  - Fail by ~5dB vs Pass by ~2dB

HF noise reduction – board layout tricks

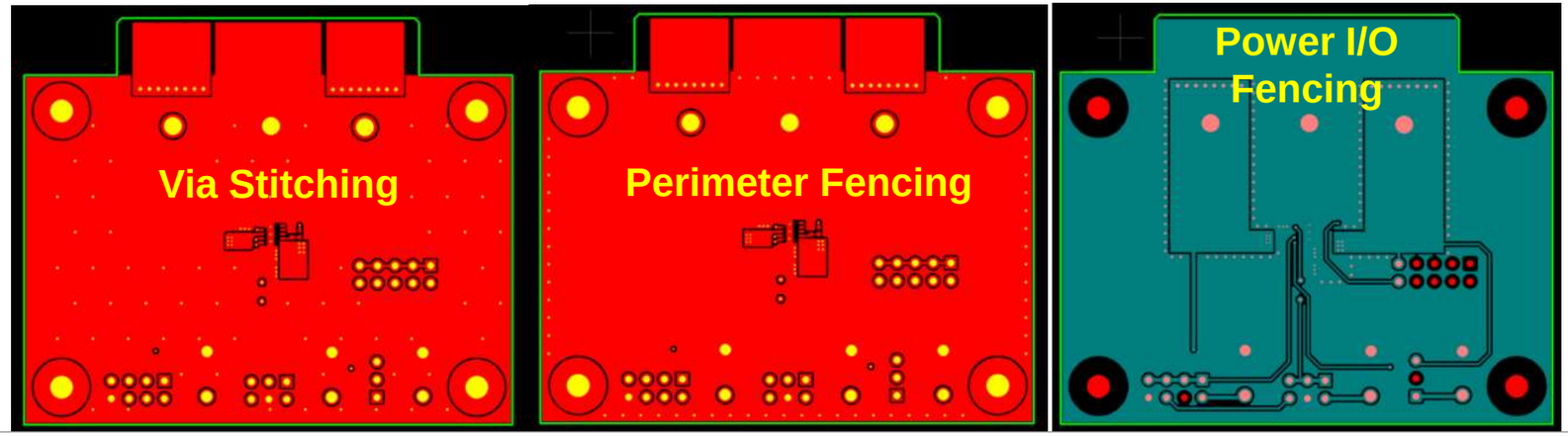
Shielding

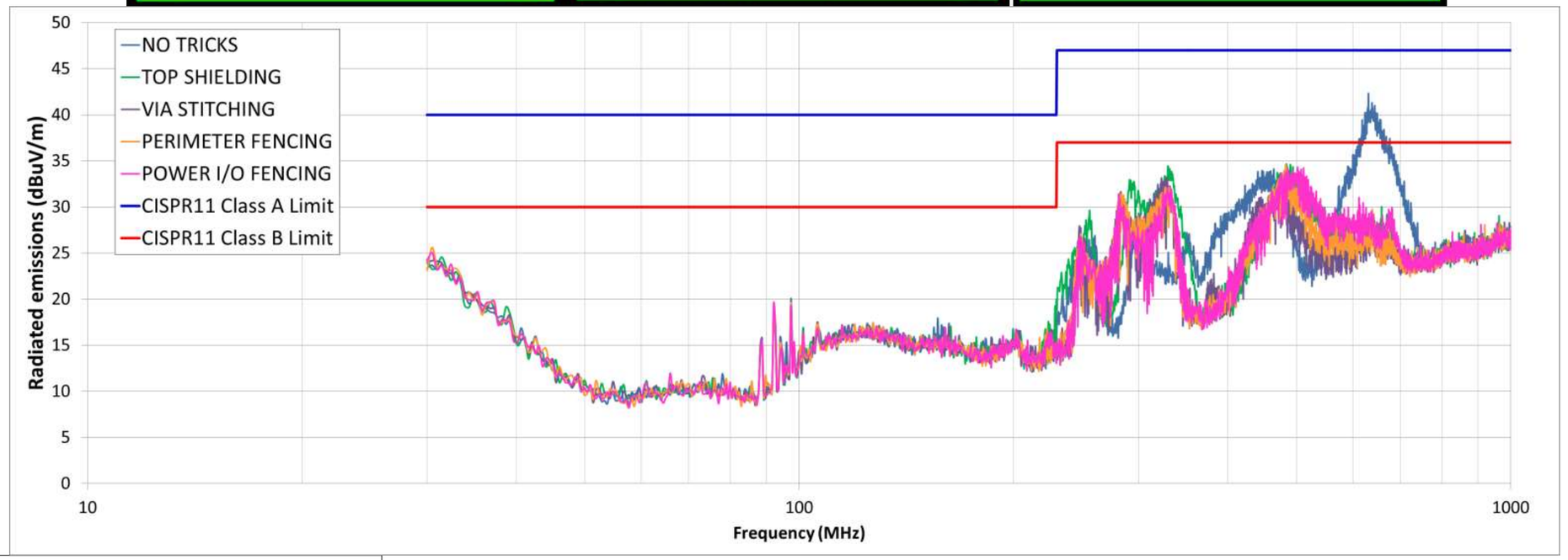




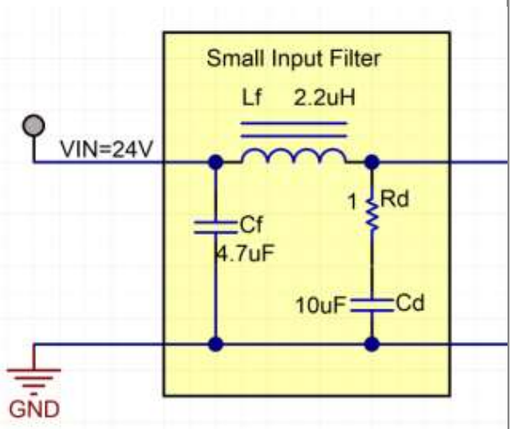


HF noise reduction – board layout tricks

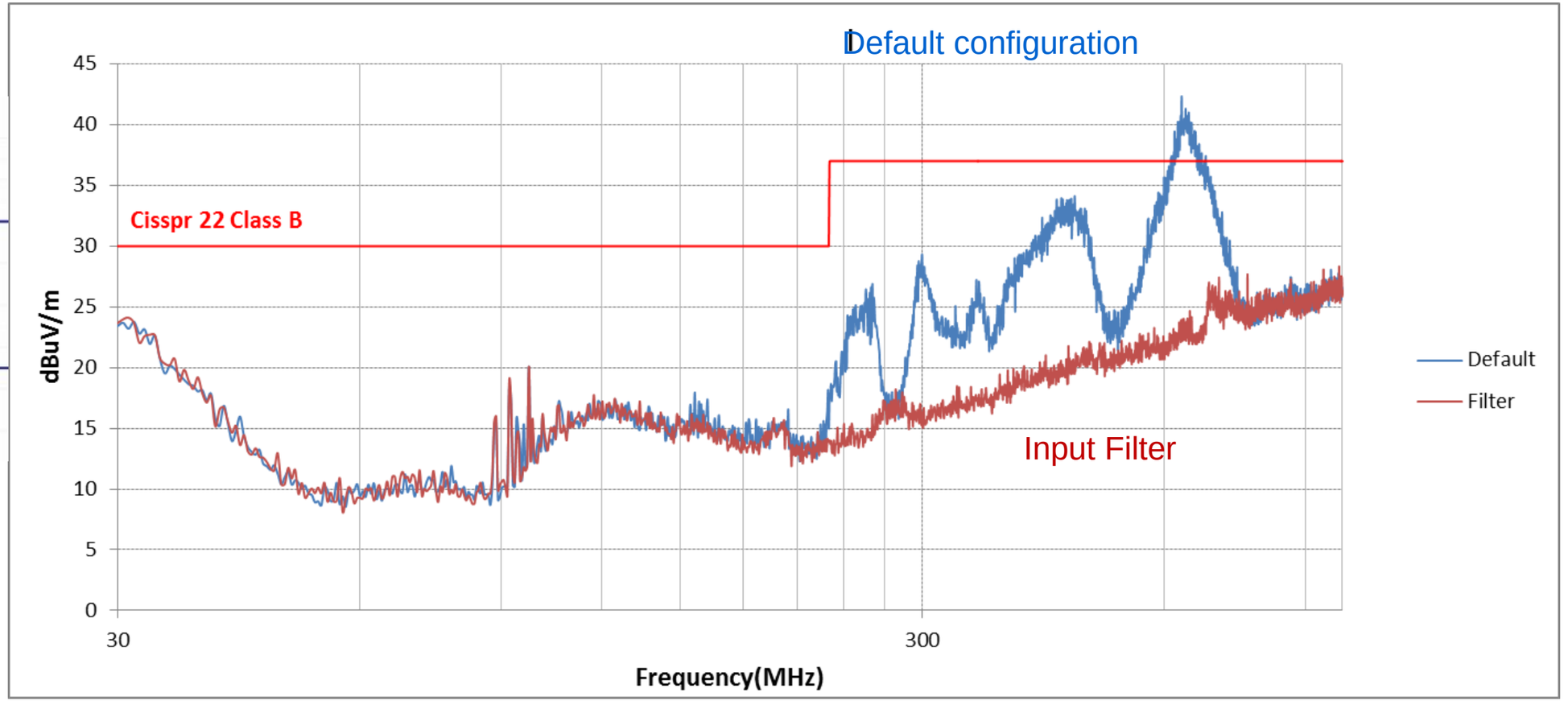




Conducted EMI filter and radiated EMI performance

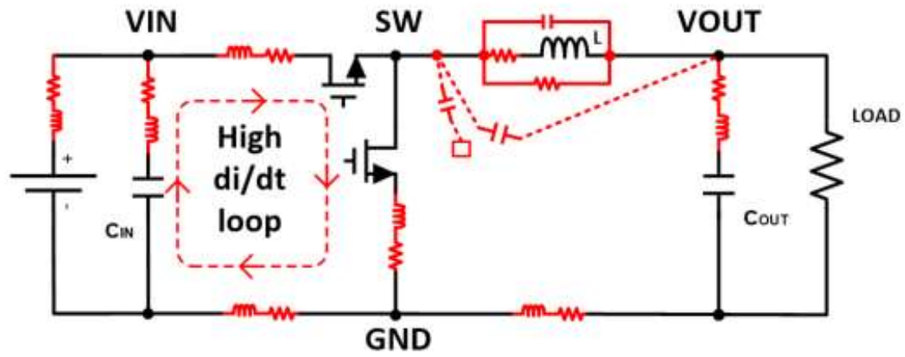


Calculator



HF noise reduction – package level parasitics

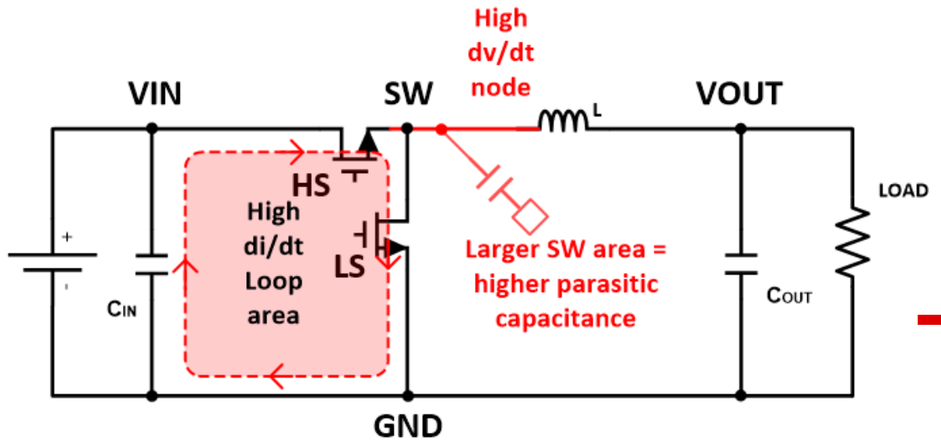
- Some packaging options are better for reducing inductance in the high di/dt loop.
- Power module packages can integrate a high frequency bypass capacitor.
- IC Pinout and Construction Matters

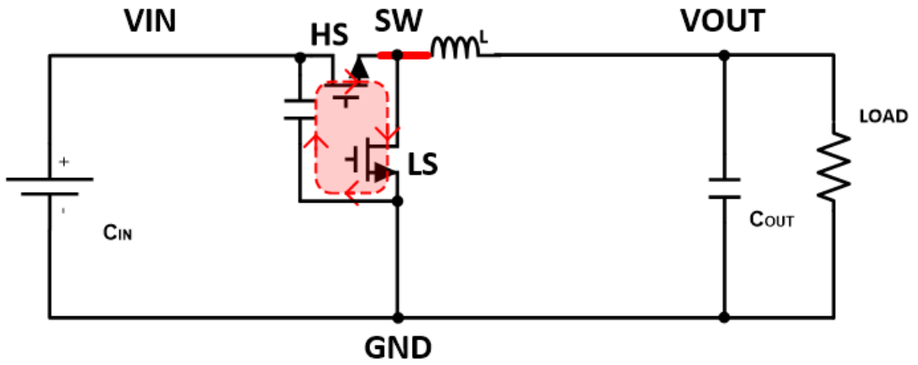


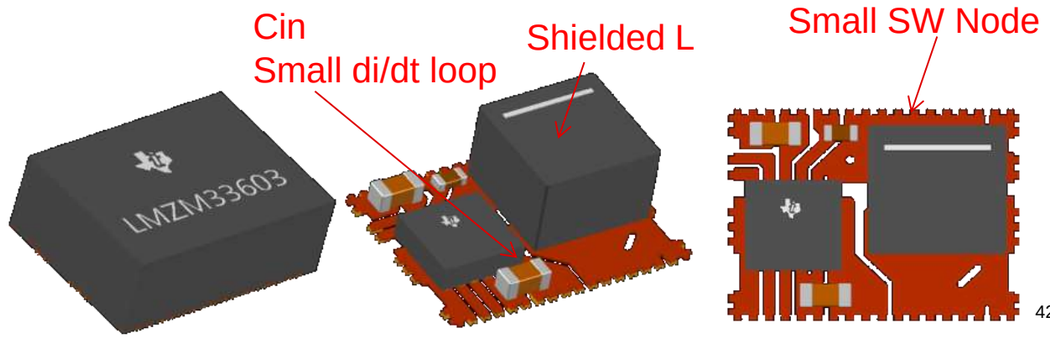
HF noise reduction – DC-DC power modules save you layout troubles

- Reducing the high di/dt loop area – integrated input capacitance.
- Reducing the high dv/dt node area – integrated L and smaller switch node.

Discrete solution without optimized layout → DC-DC Power Module

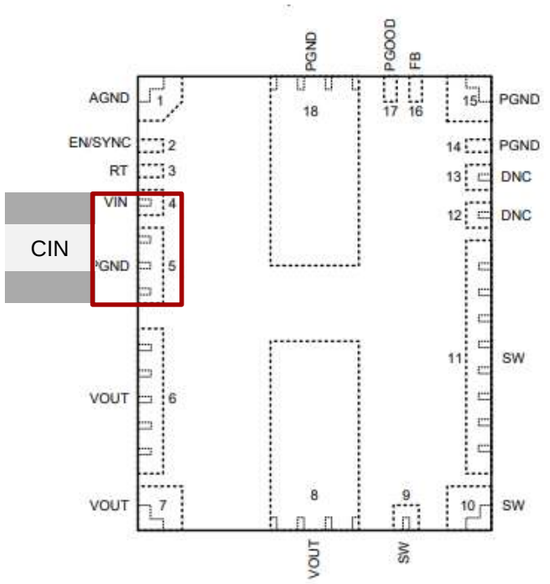




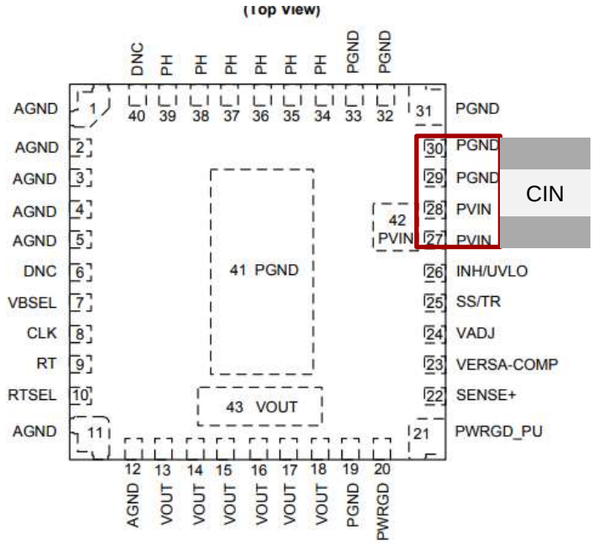


HF noise reduction – proper pinout

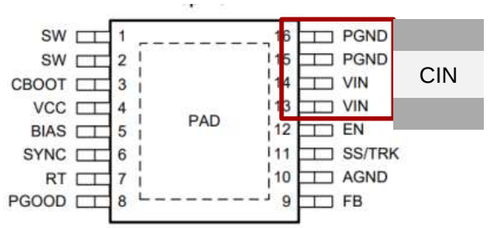
- To minimize the di/dt loop, it is best if the Buck regulator has VIN and PGND pins next to each other. This allow for placing the input capacitor as close as possible to the IC.



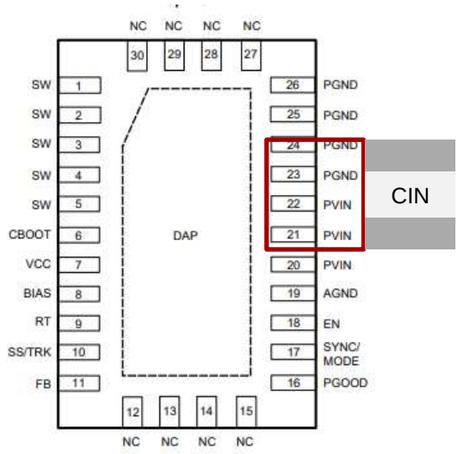
LMZM33603



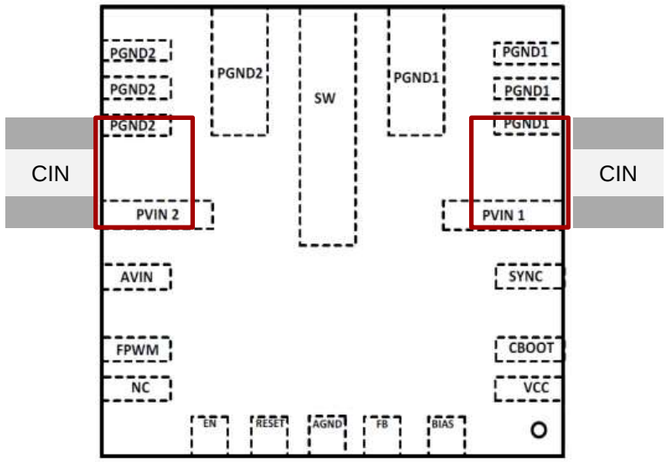
LMZ36002



LM46002

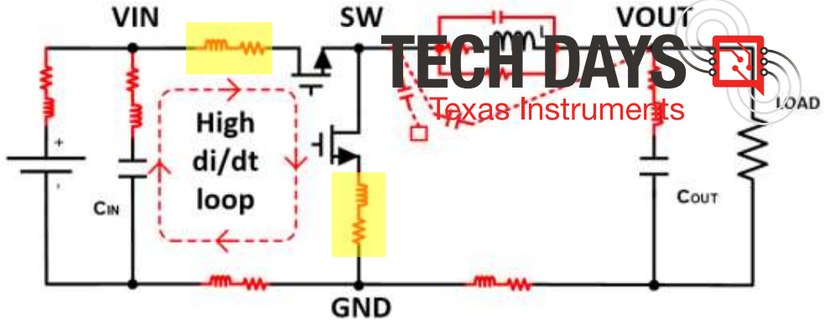


LM73606



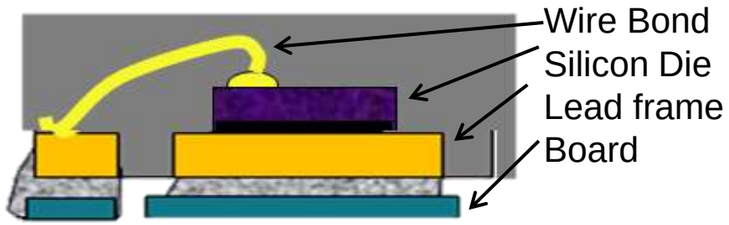
LMS3635

IC package construction can help

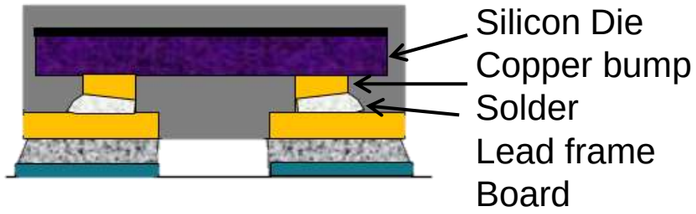


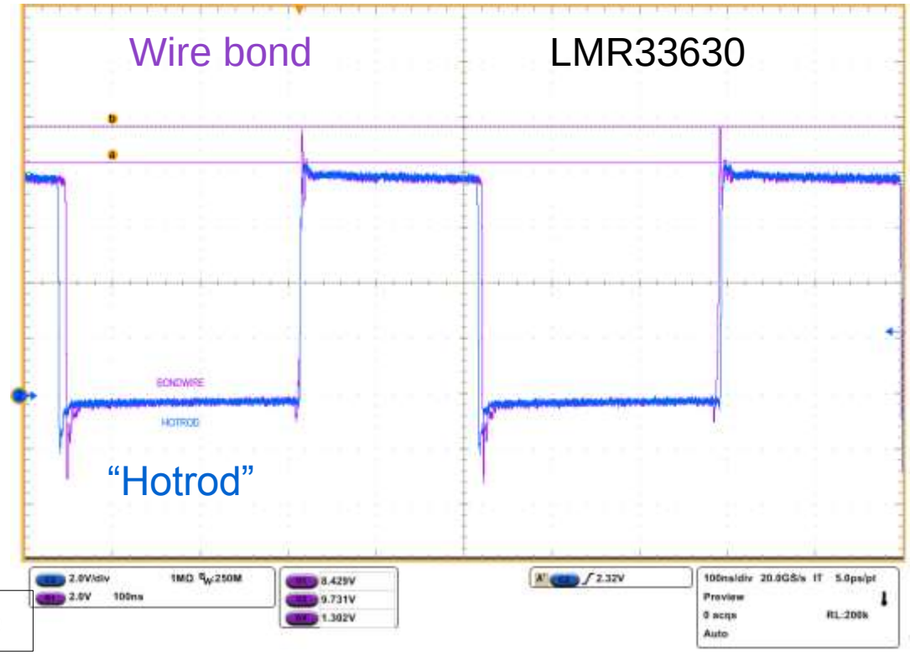
- Bond wire vs Copper pillar interconnects

Standard wire bond QFN package



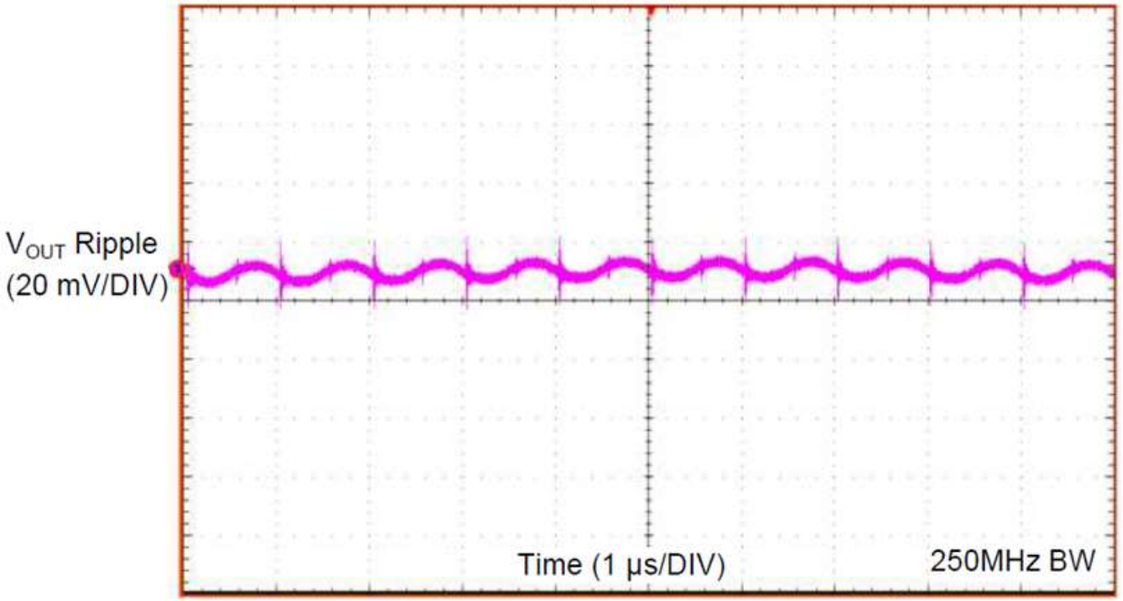
‘Hotrod’ flip chip on lead frame QFN



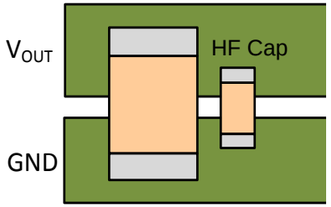


HF filtering

- After careful input capacitor placement and layout there will be some left over high frequency noise – we cannot completely eliminate parasitic L and C.

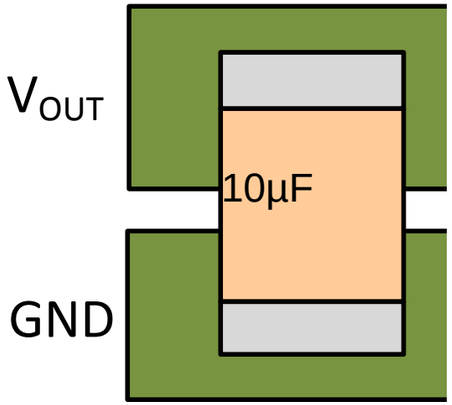


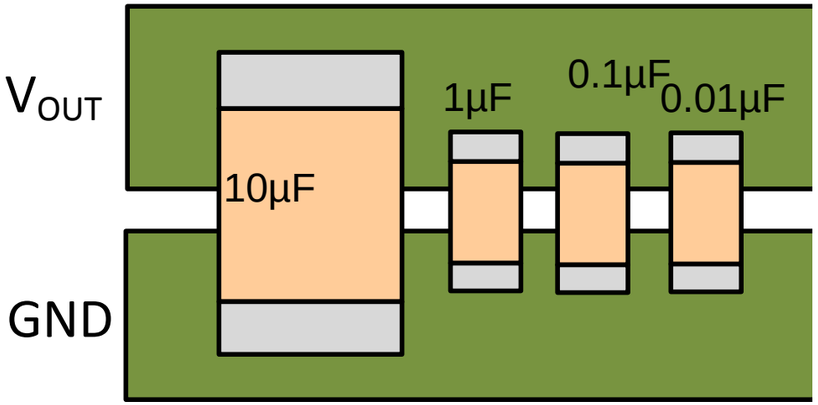
- How can we reduce it?

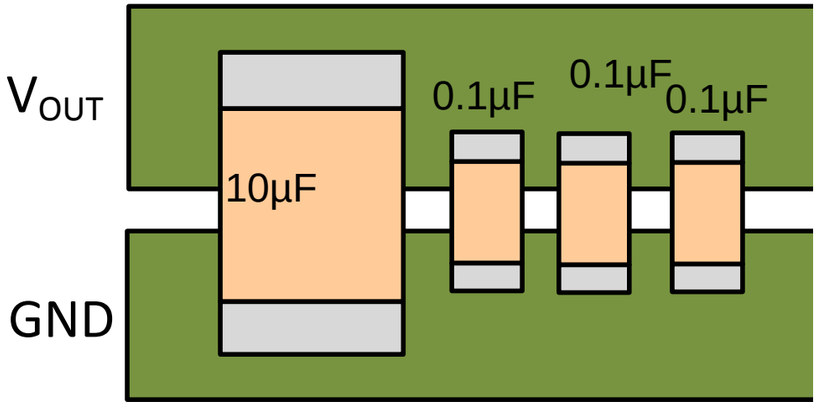


HF filtering

- Which one is better?



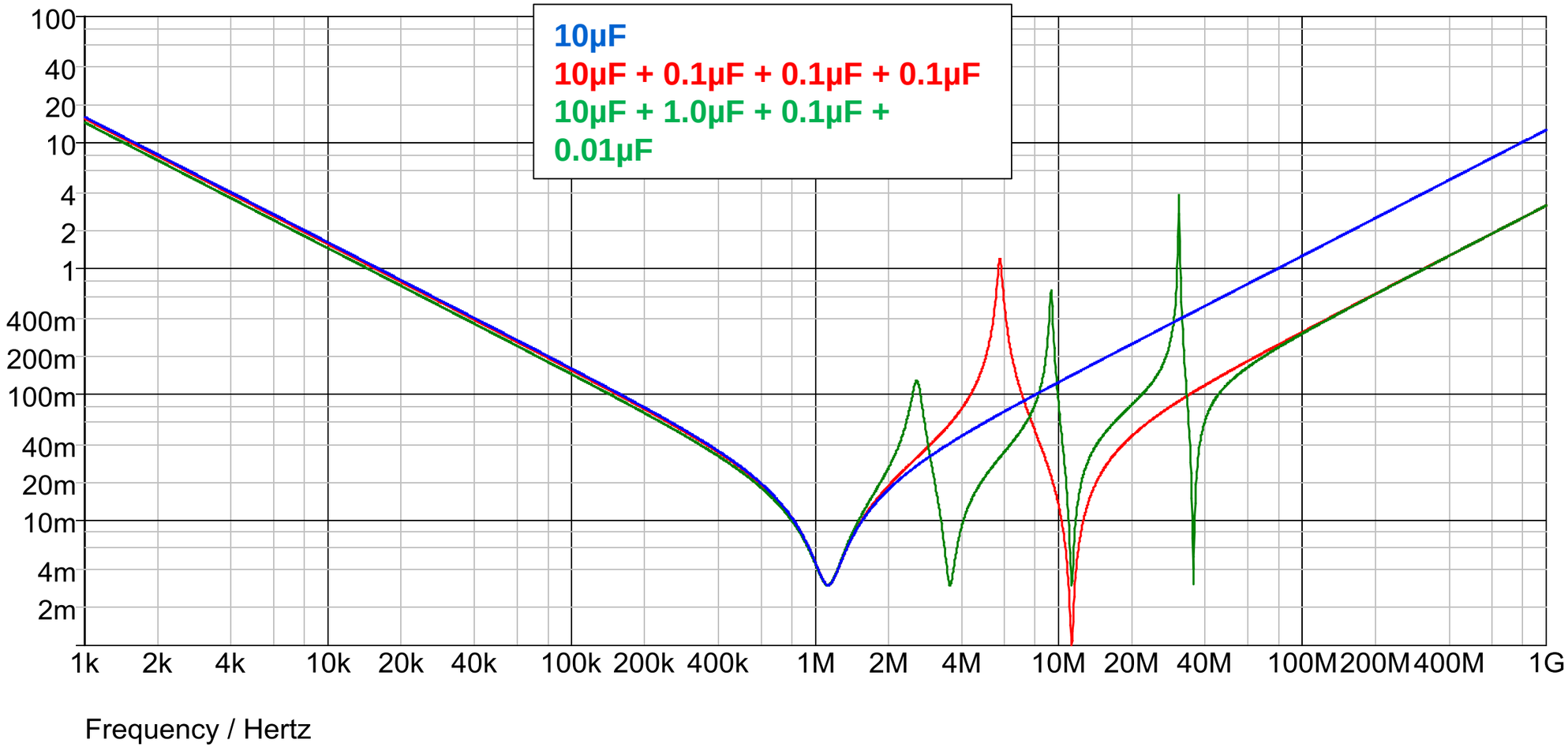




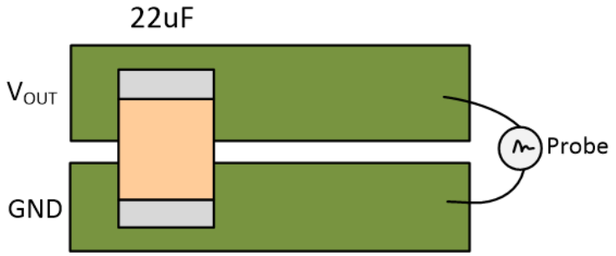
HF filtering

SIMetrix schematic example:

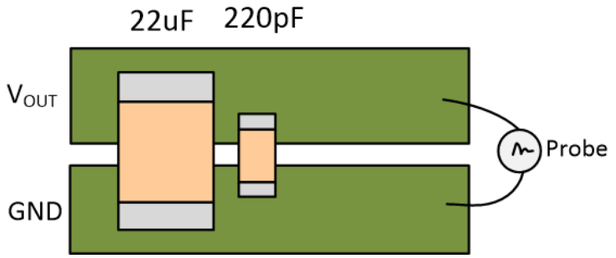
parallel_capacitor_impedance.sxsch



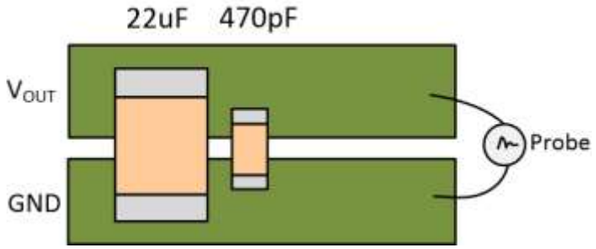
HF filtering with wrong capacitor (example)



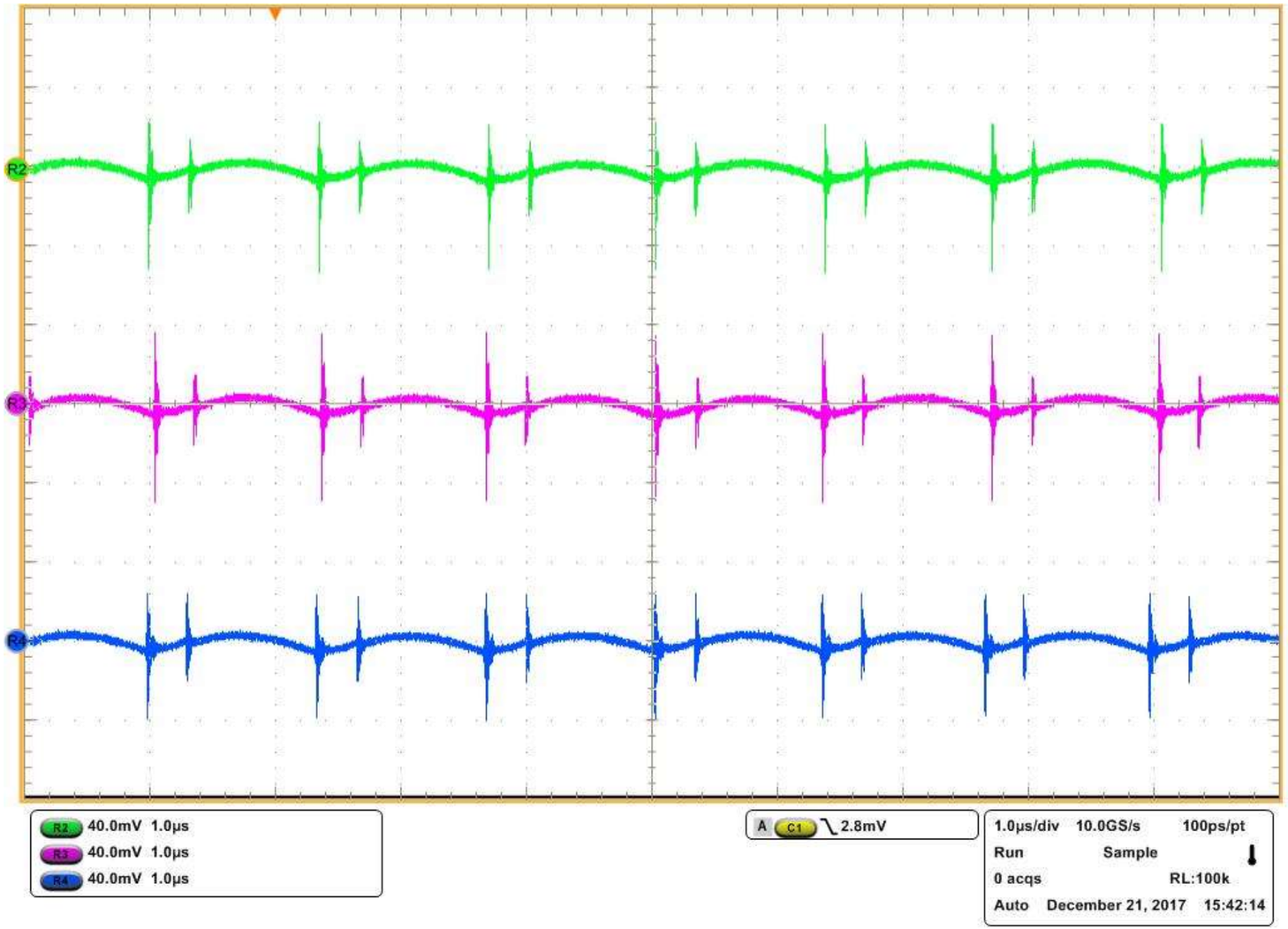
76.2mV



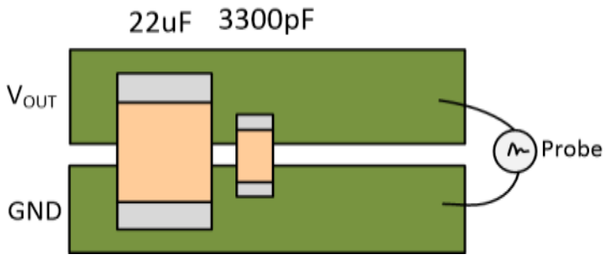
85.7mV



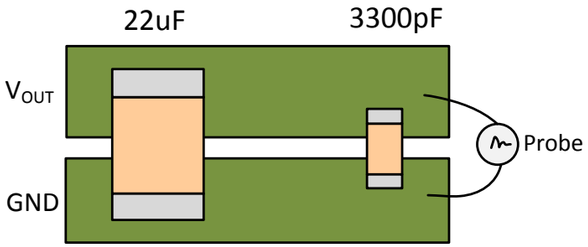
64.4mV



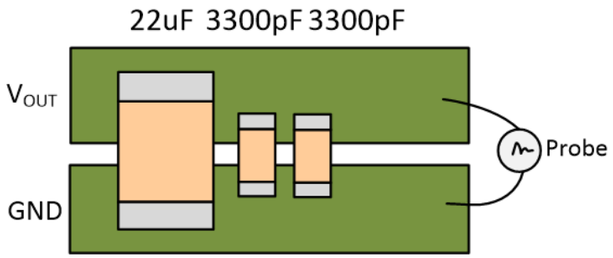
HF filtering - utilizing PCB parasitic inductance



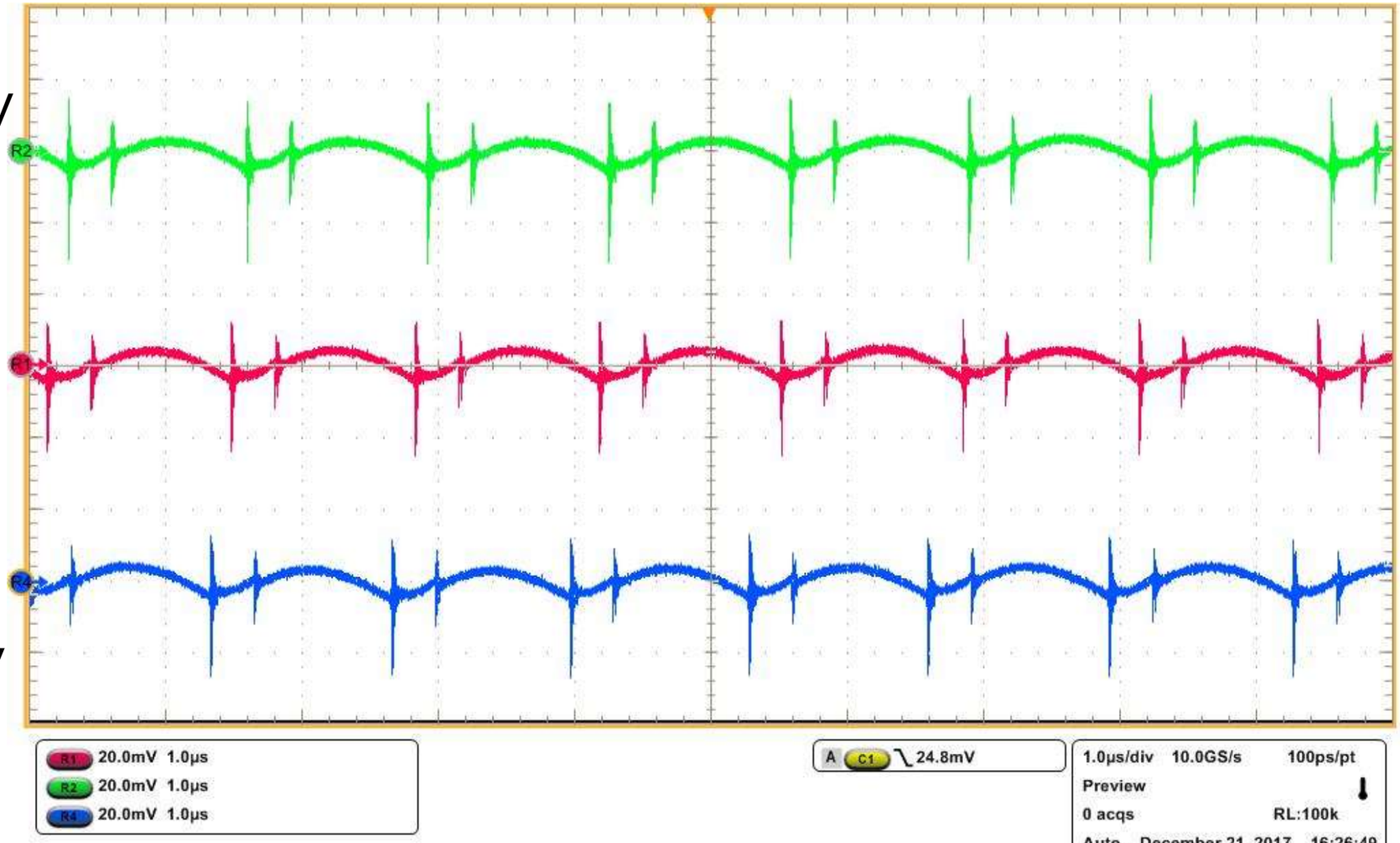
48.4mV



37.9mV



40.3mV

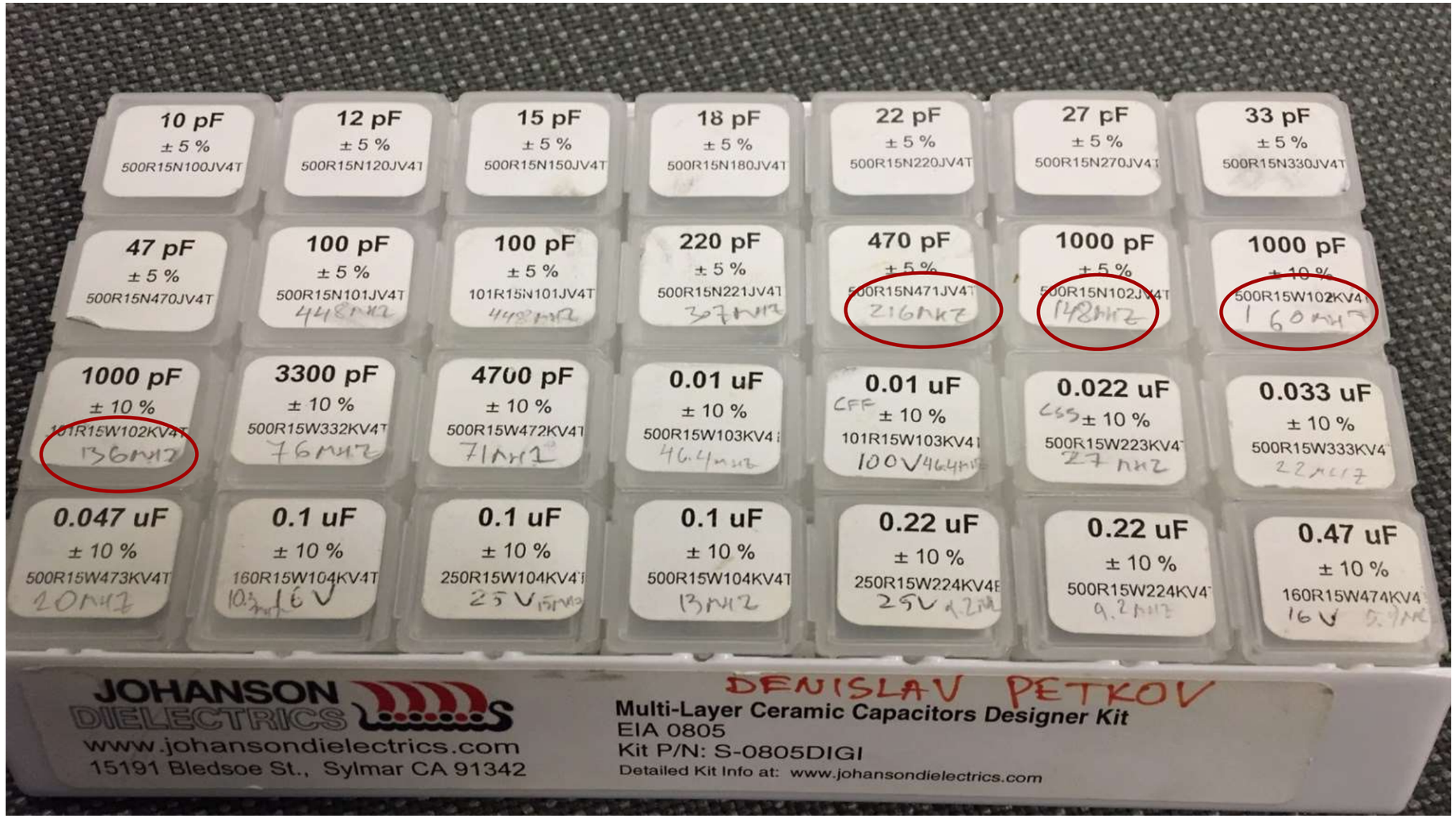


HF filtering – strategy

- Leave footprint in the layout for 2-3 HF filter capacitors.
- Measure the ringing frequency and pick a capacitor with an impedance notch close to, but lower than that frequency.
- Use multiple capacitors of the same value in parallel to avoid new peaks in the impedance curve.

HF filtering – pick the correct capacitor

- Measure your caps
- Mark up your capacitor kit!
- This data may also be available from the capacitor vendor.



Summary

- Understanding the Noise Sources
- Measuring Noise
- Reducing Noise (high frequency and low frequency)

Resources

- **Application Notes and Blogs on EMI and Noise Reduction**
  - Simple Success With Conducted EMI From DCDC Converters
  - Simplify low EMI design with power modules
  - Wiki on Understanding, measuring, and reducing output voltage ripple
  - Design a second-stage filter for noise sensitive applications
  - PCB layout techniques for low noise power designs (in progress)