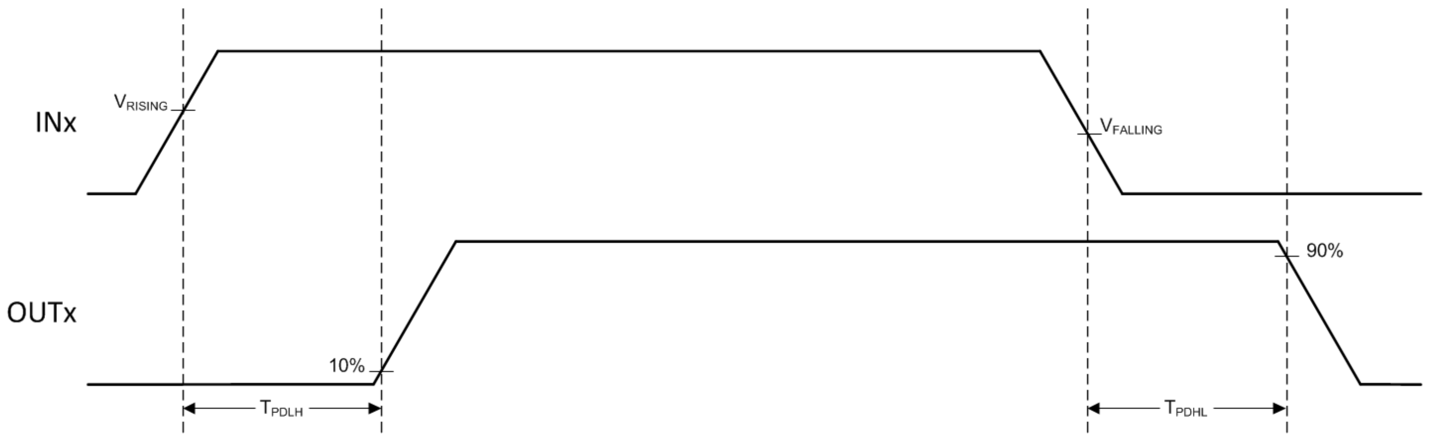
Critical isolated gate driver specifications

TIPL 503
TI Precision Labs – Isolated Gate Drivers

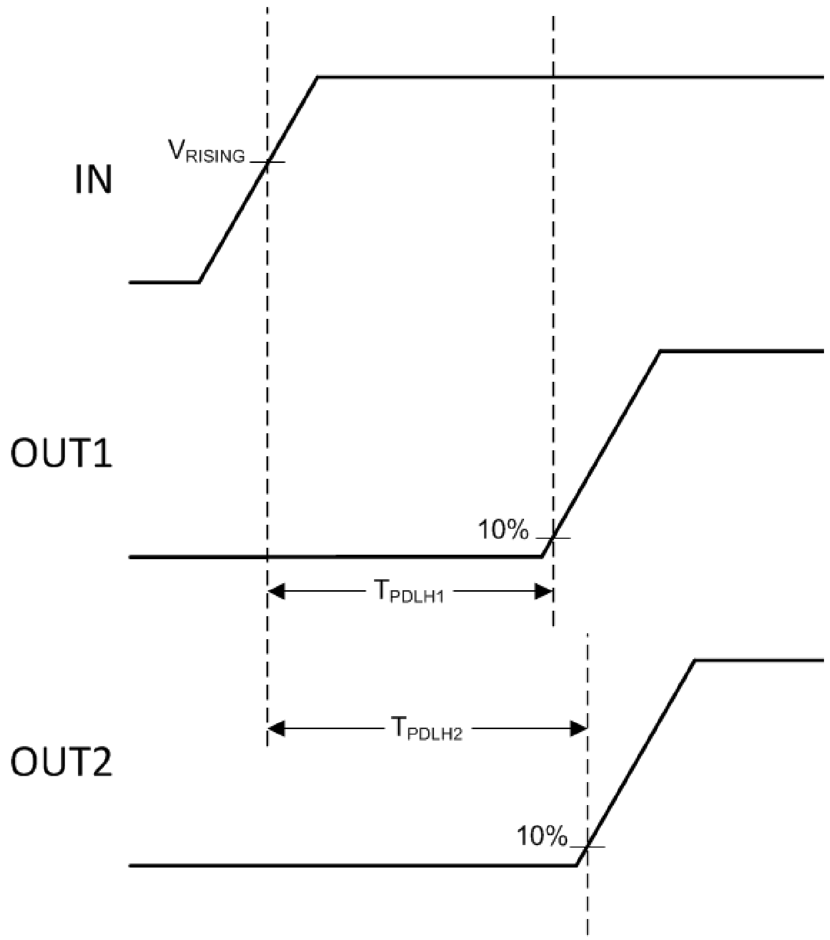
Presented and Prepared by Derek Payne

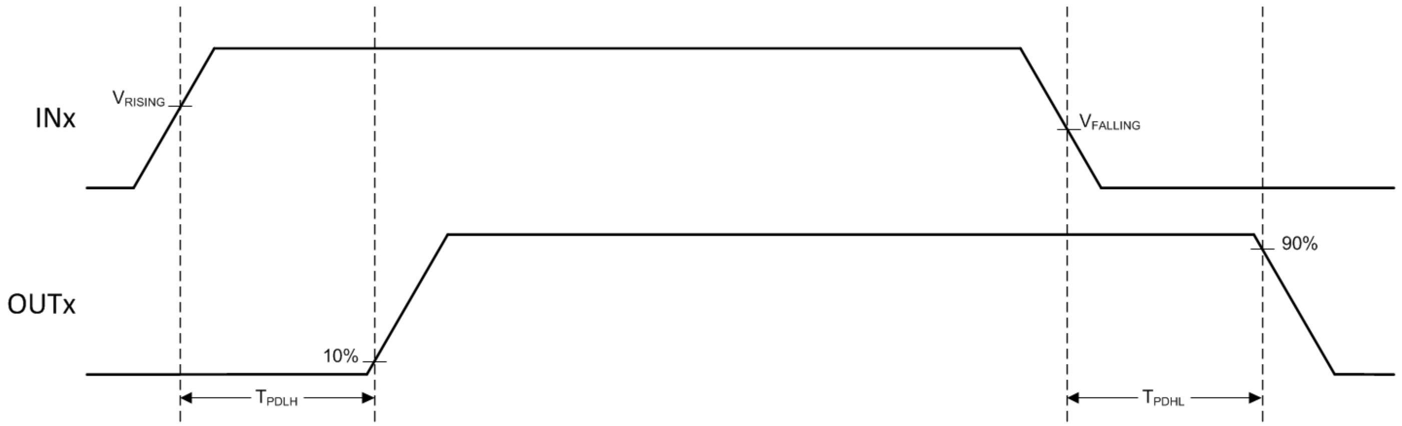
Parameters of Interest



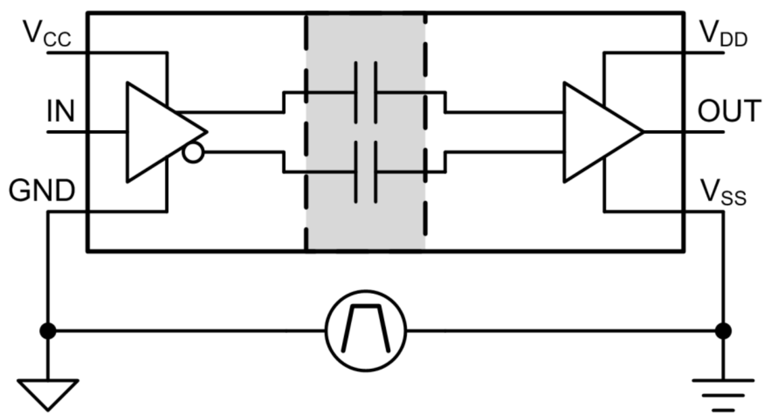
Propagation Delay

Timing Skew



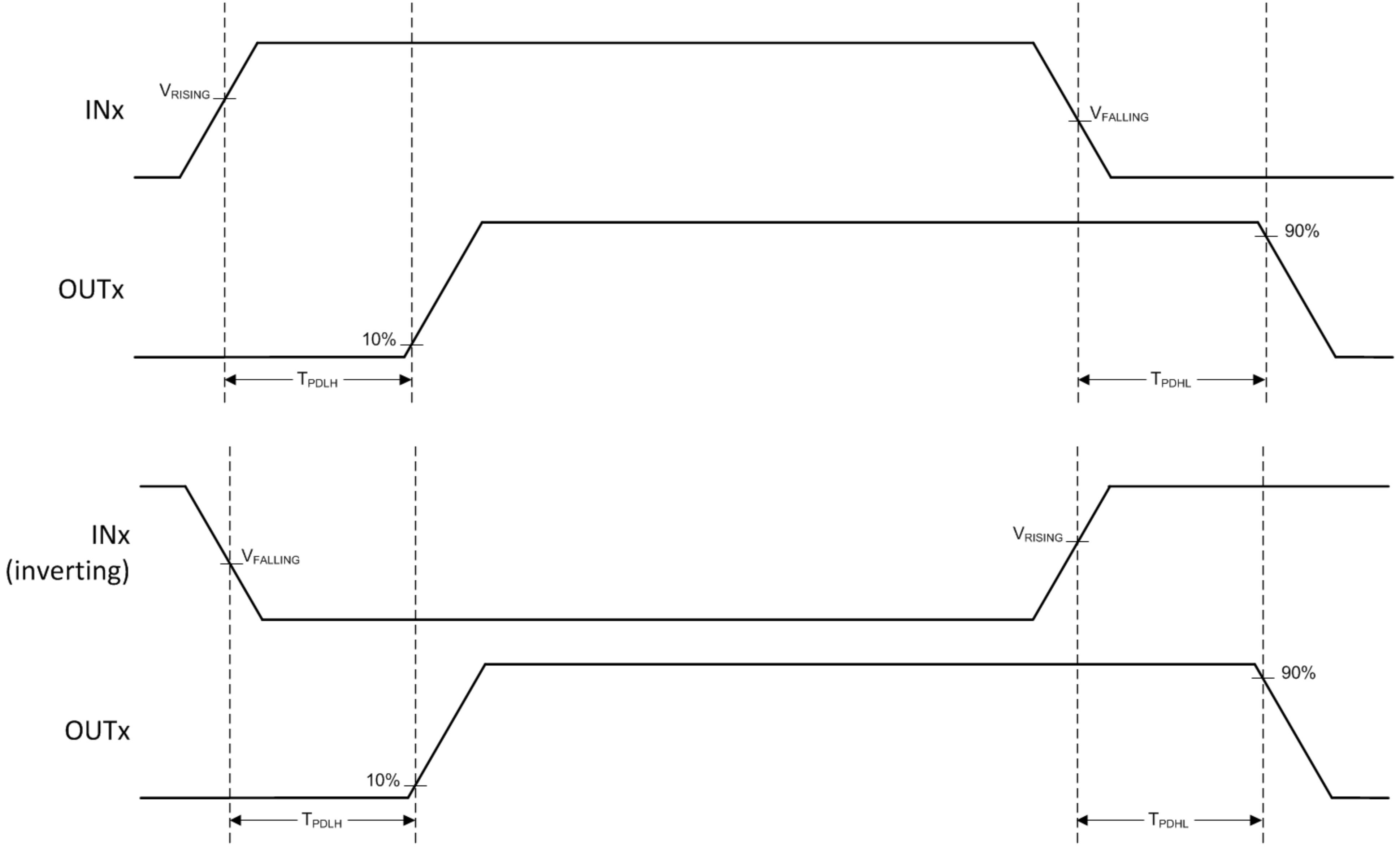


Pulse Duration Distortion

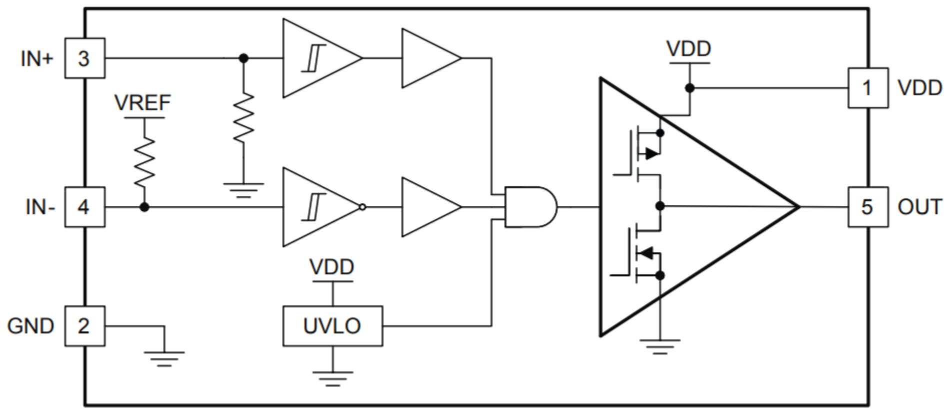


Common-Mode Transient Immunity (CMTI)

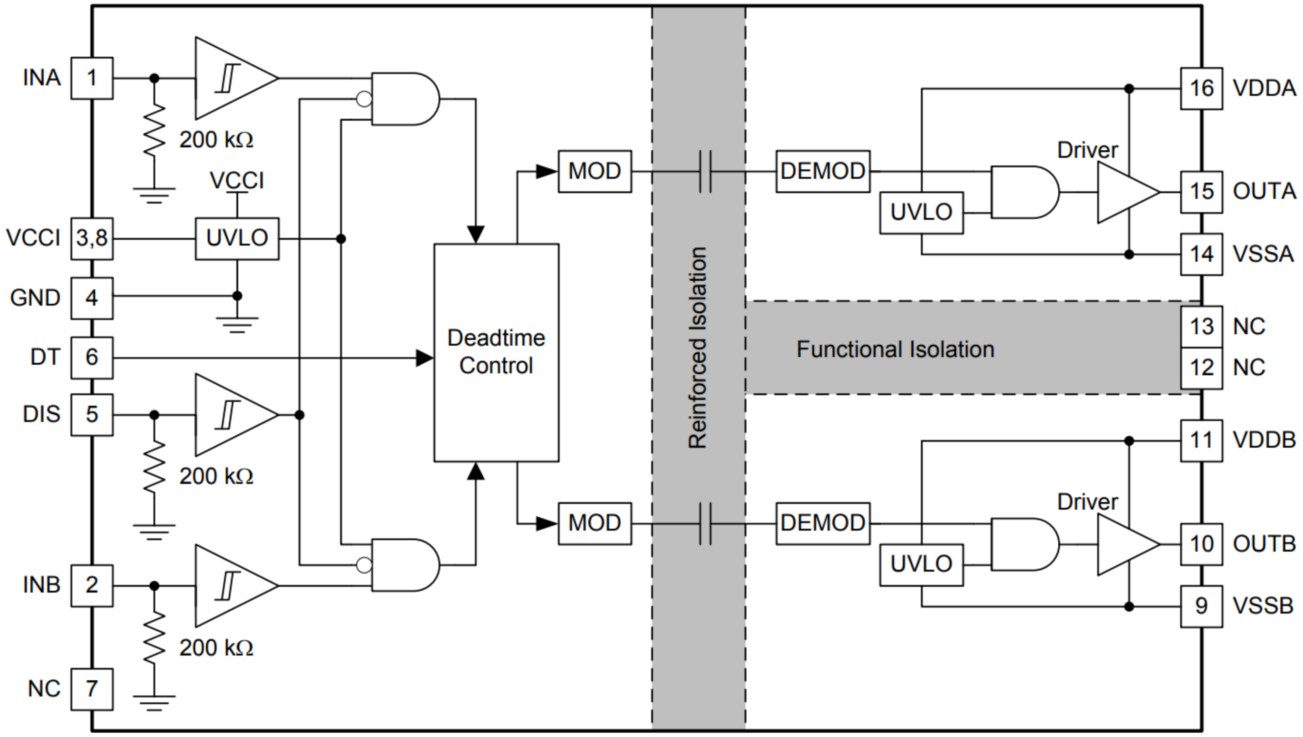
Propagation Delay

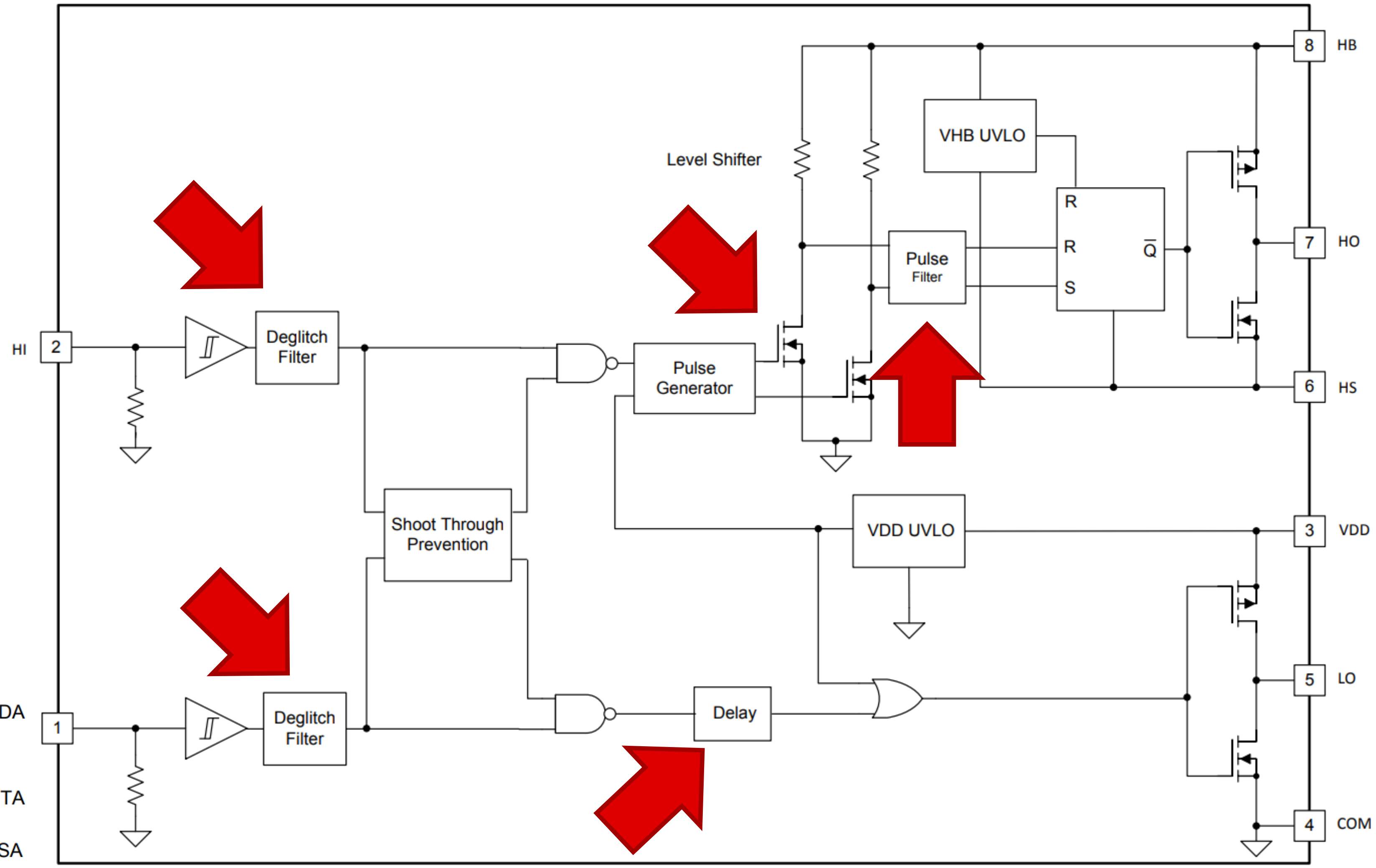


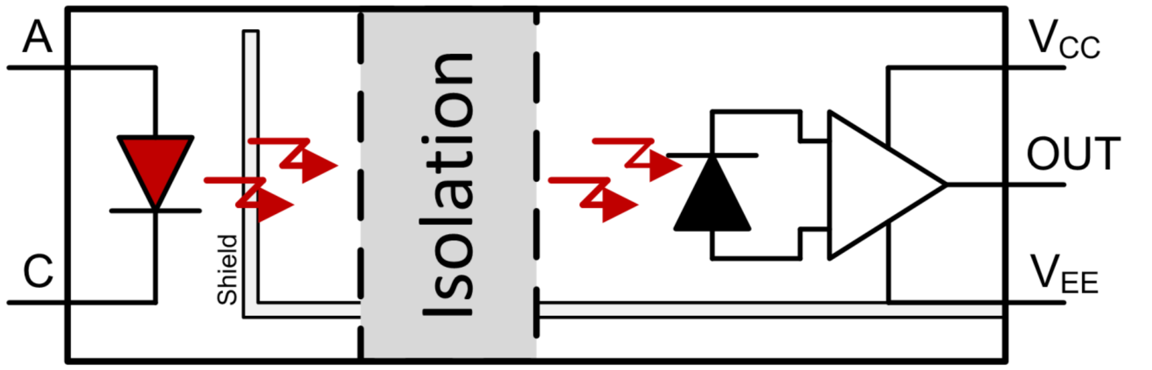
Propagation Delay



IN– Pull-Up Resistance to VREF = 500 kΩ, VREF = 5.8 V, IN+ Pull-Down Resistance to GND = 230 kΩ







Propagation Delay

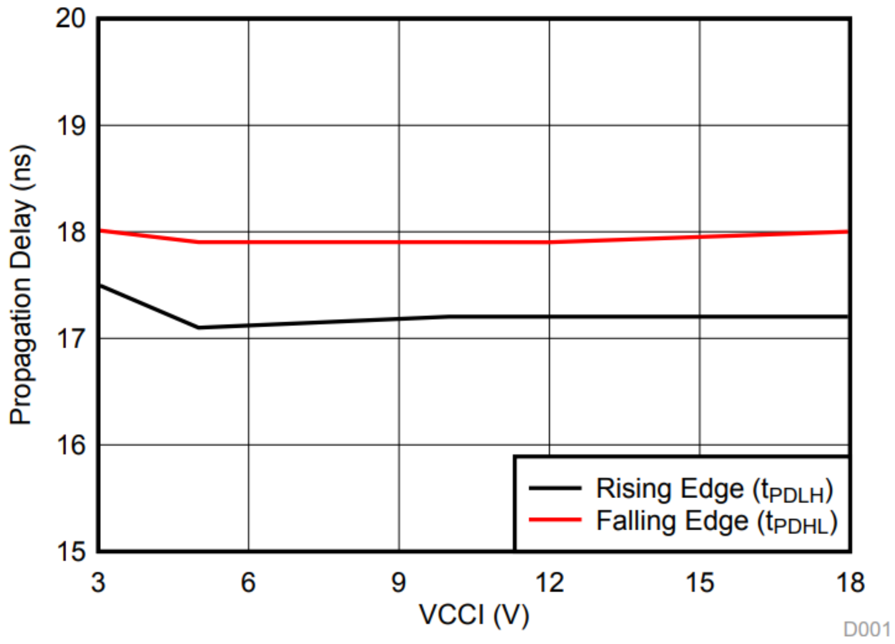


Figure 13. Propagation Delay vs. VCCI

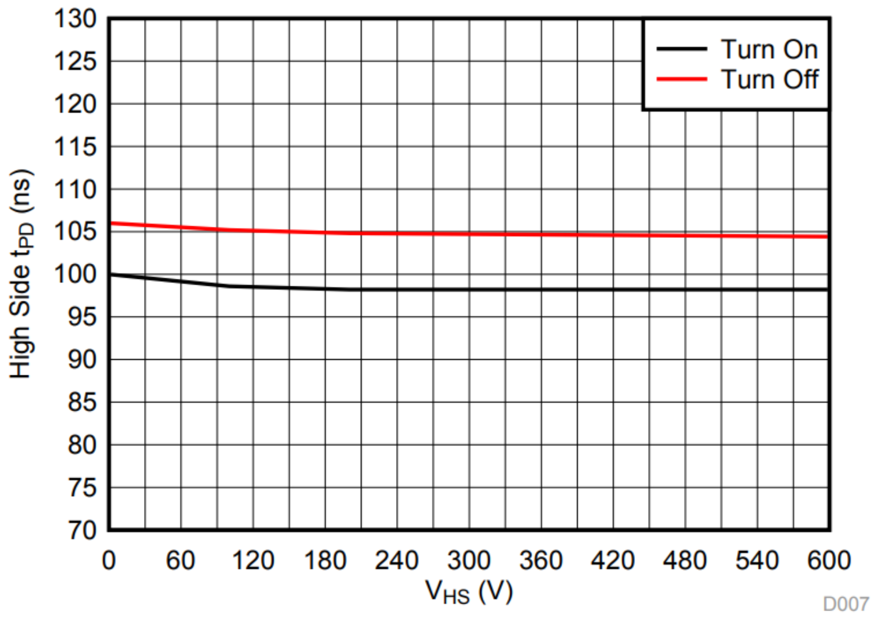
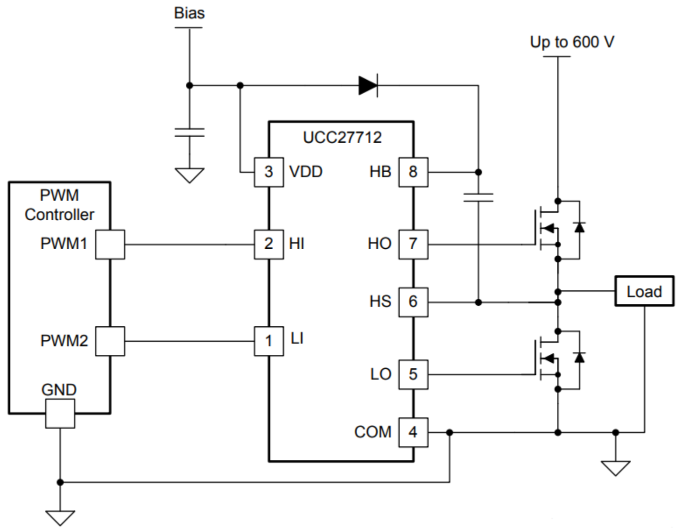


Figure 8. High-Side Propagation Delay vs HS



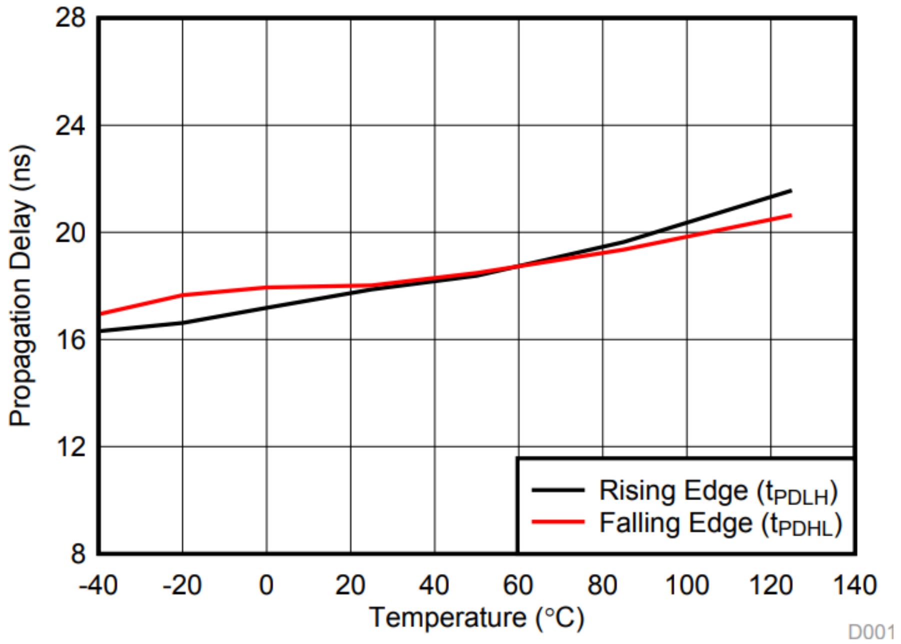
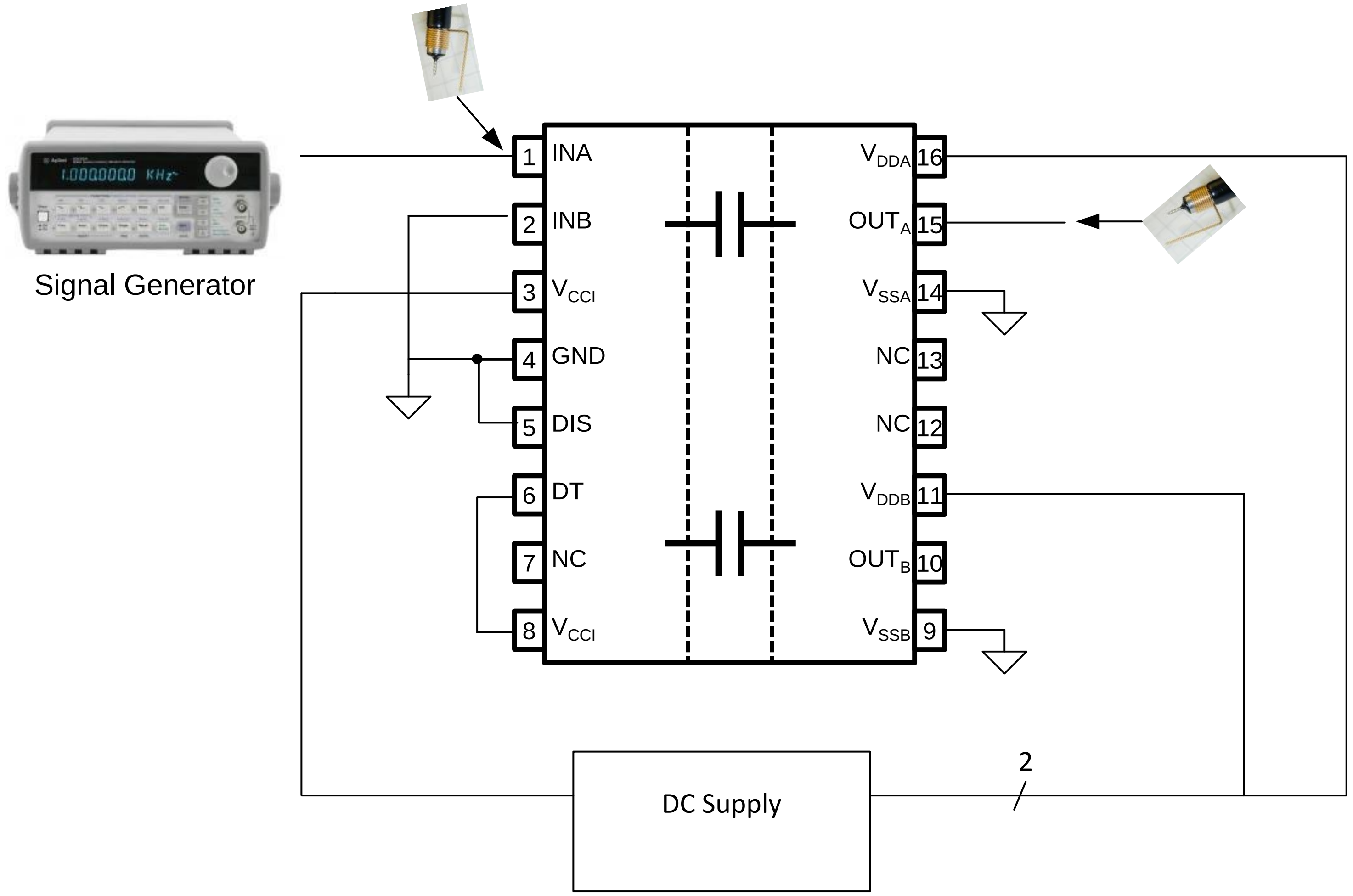
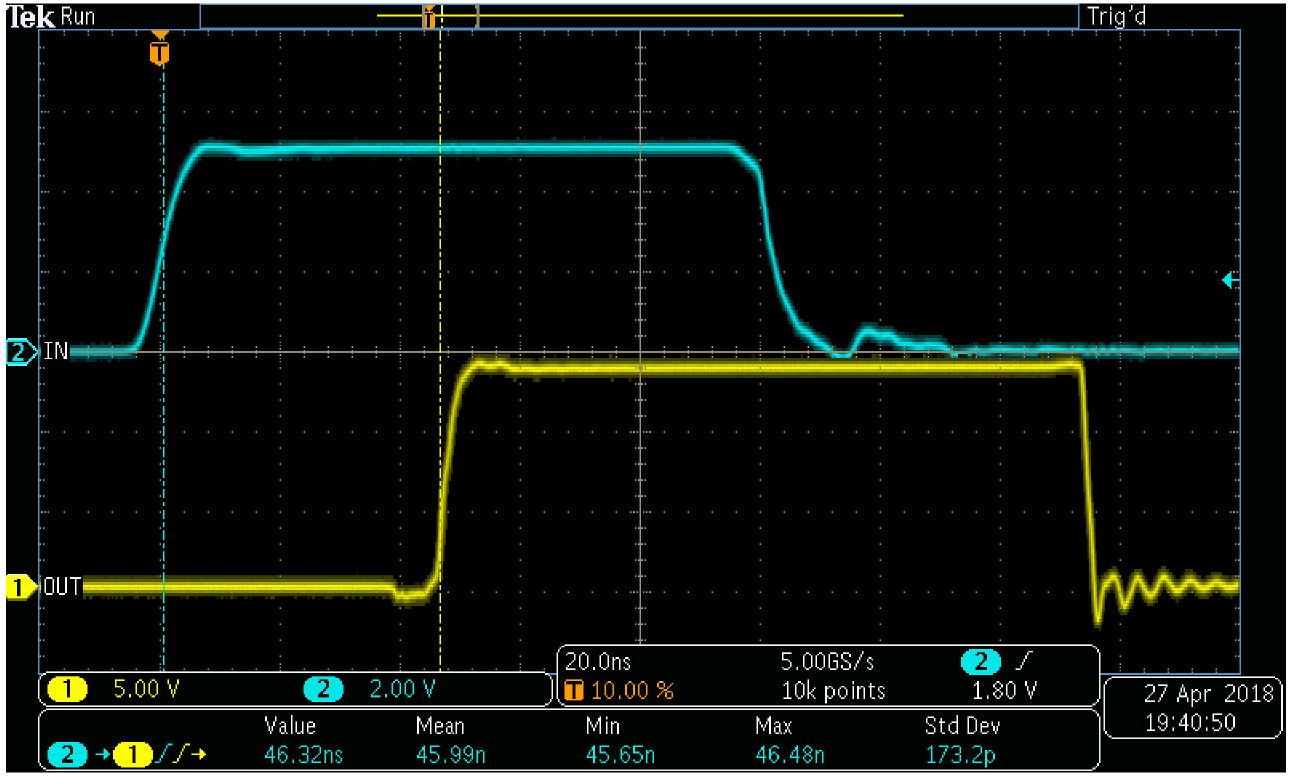


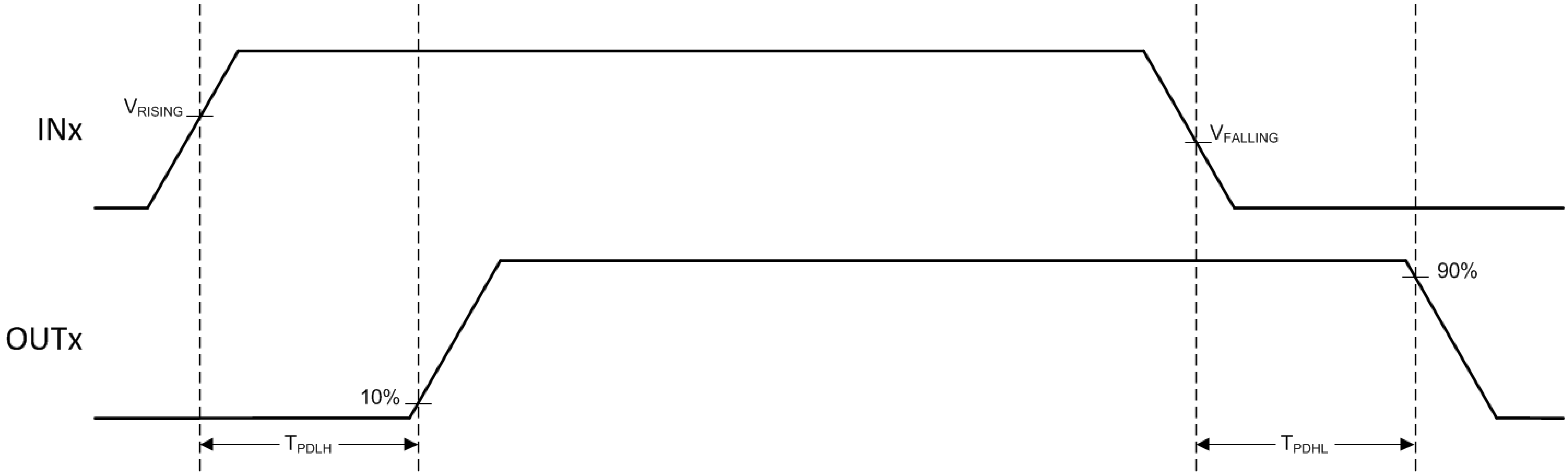
Figure 12. Propagation Delay vs. Temperature

Propagation Delay



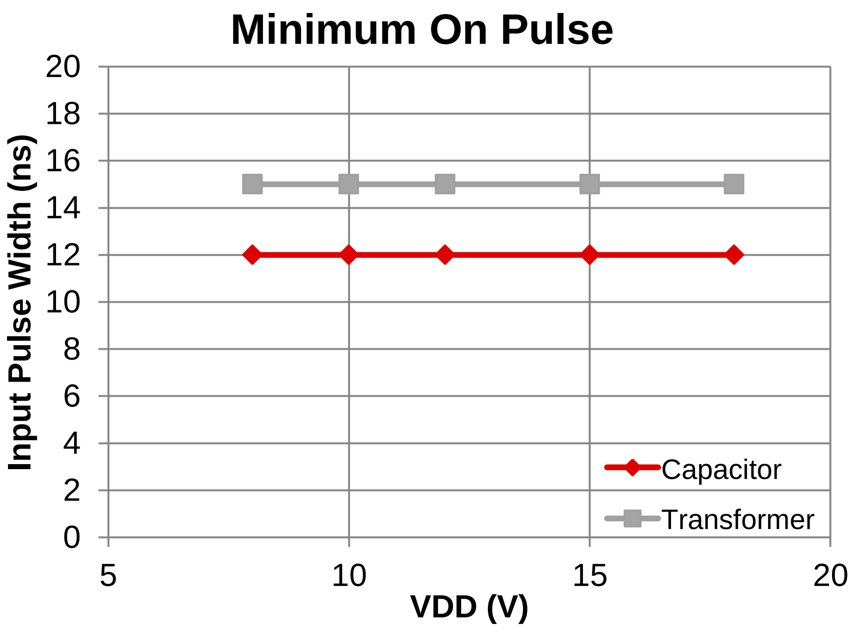


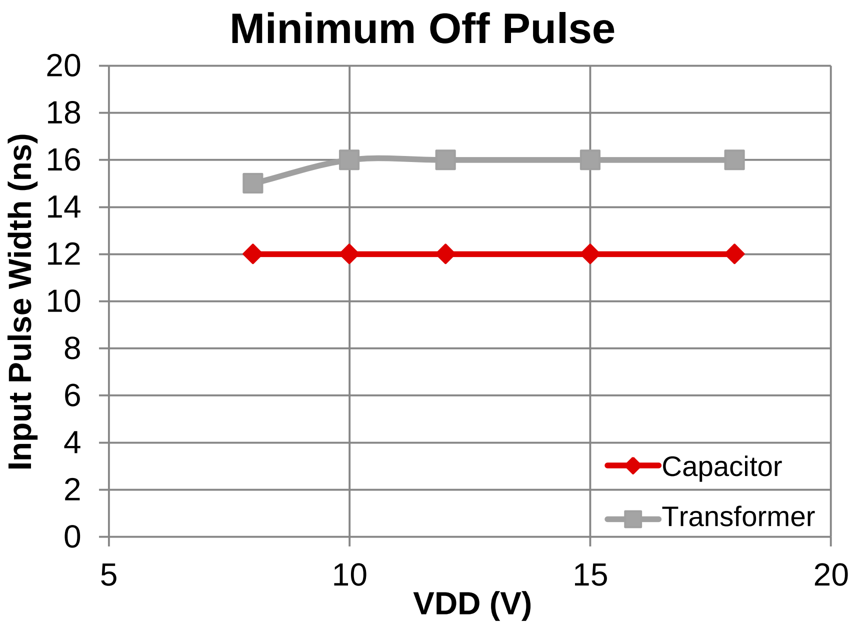
Pulse Duration Distortion

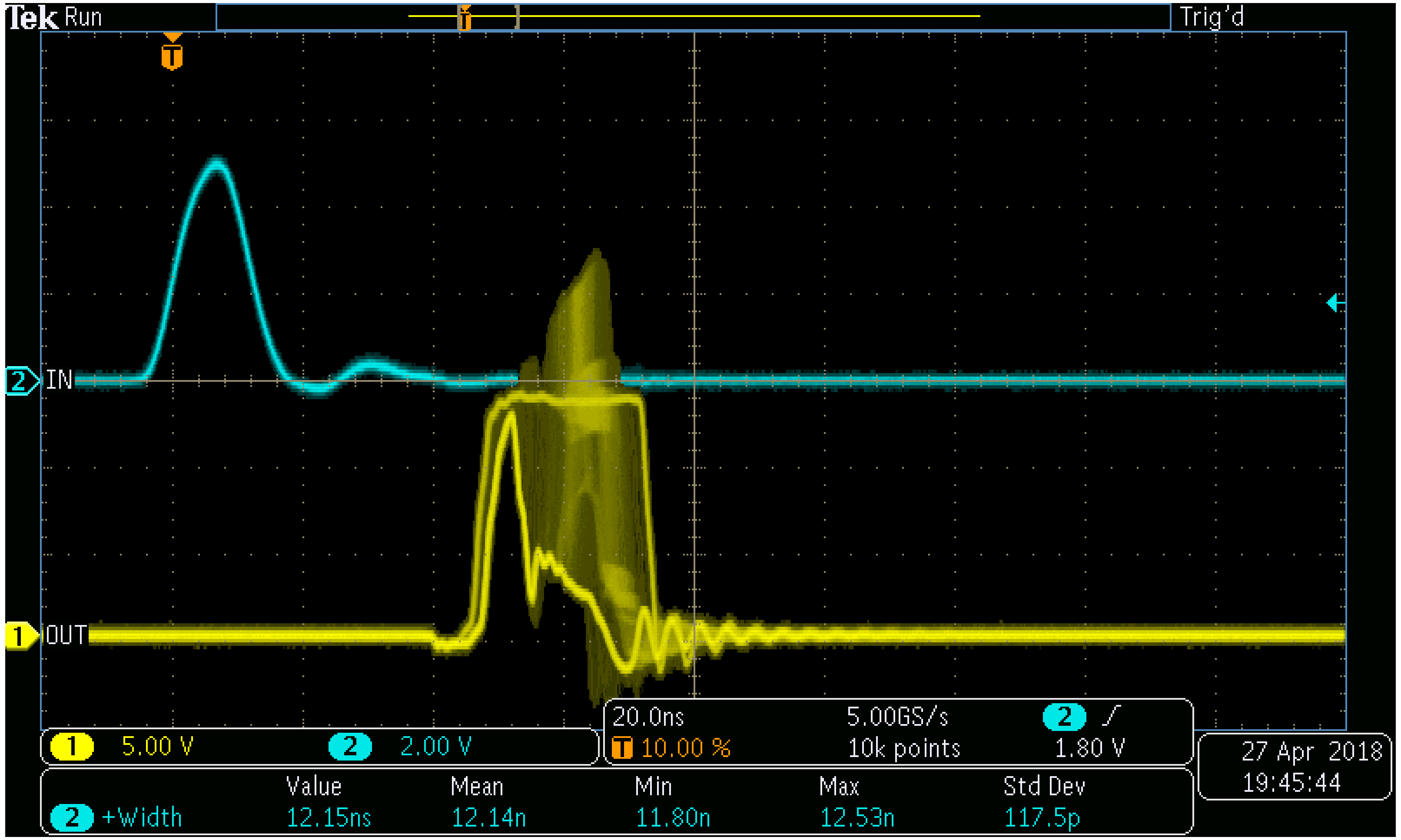


$$T_{PDD} = |T_{PDHL} - T_{PDLH}|$$

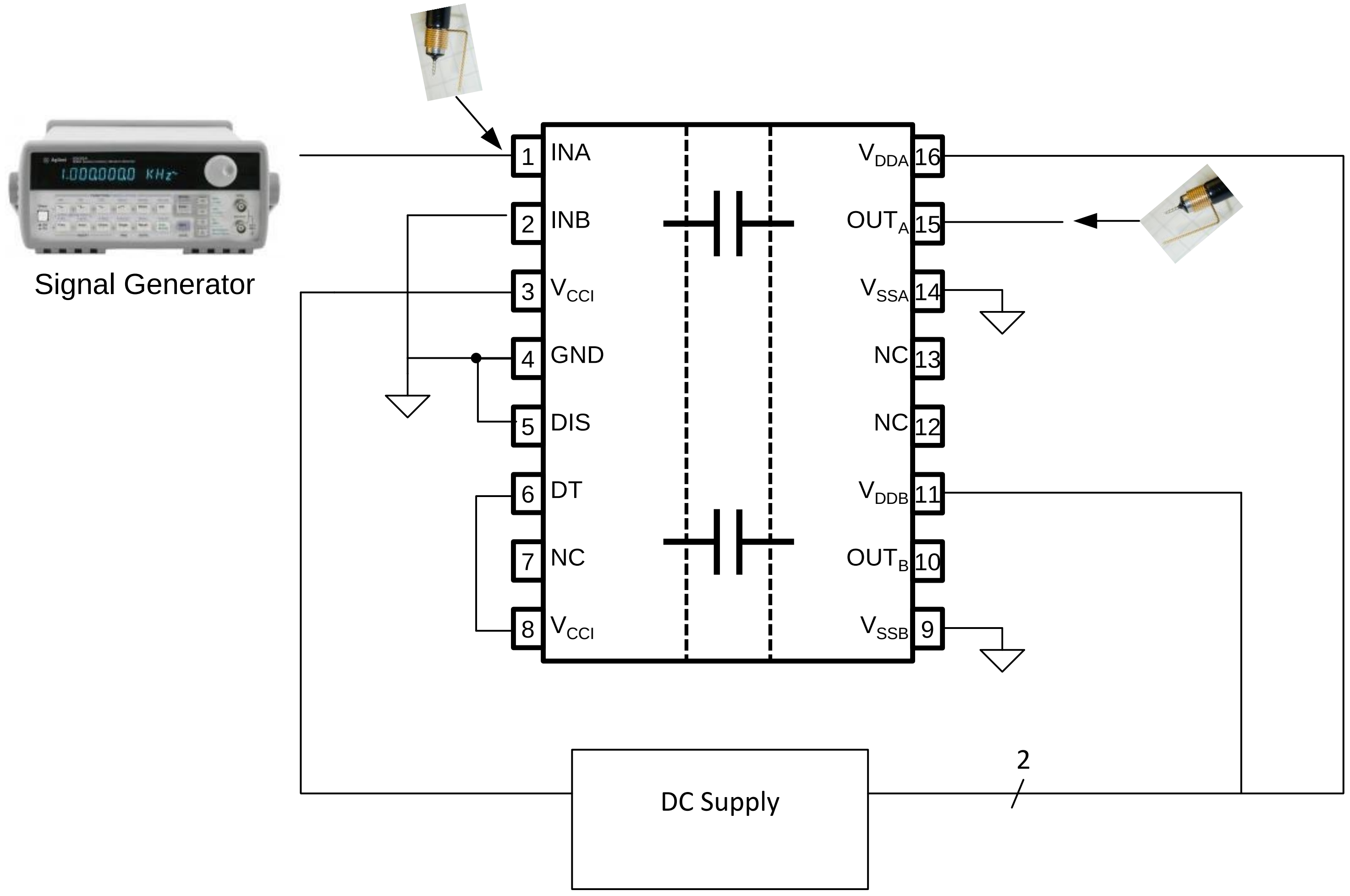
Pulse Duration Distortion

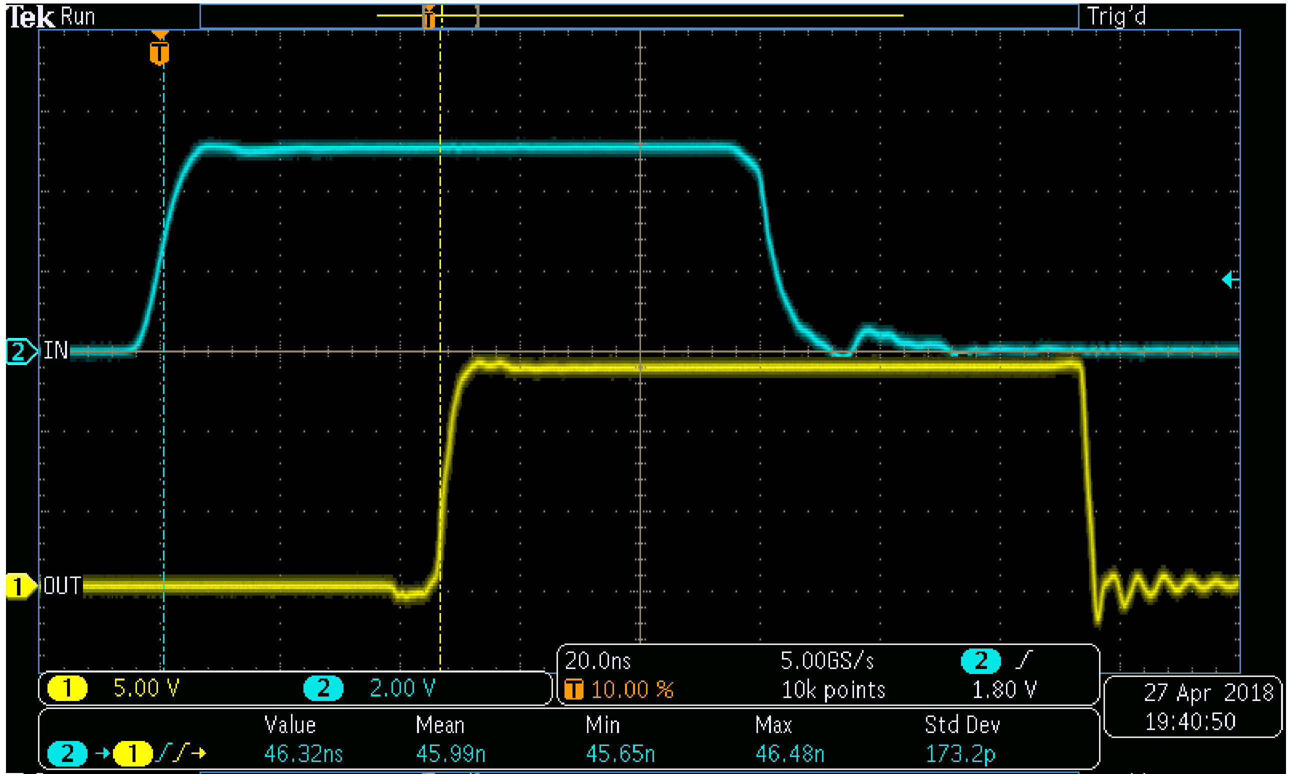


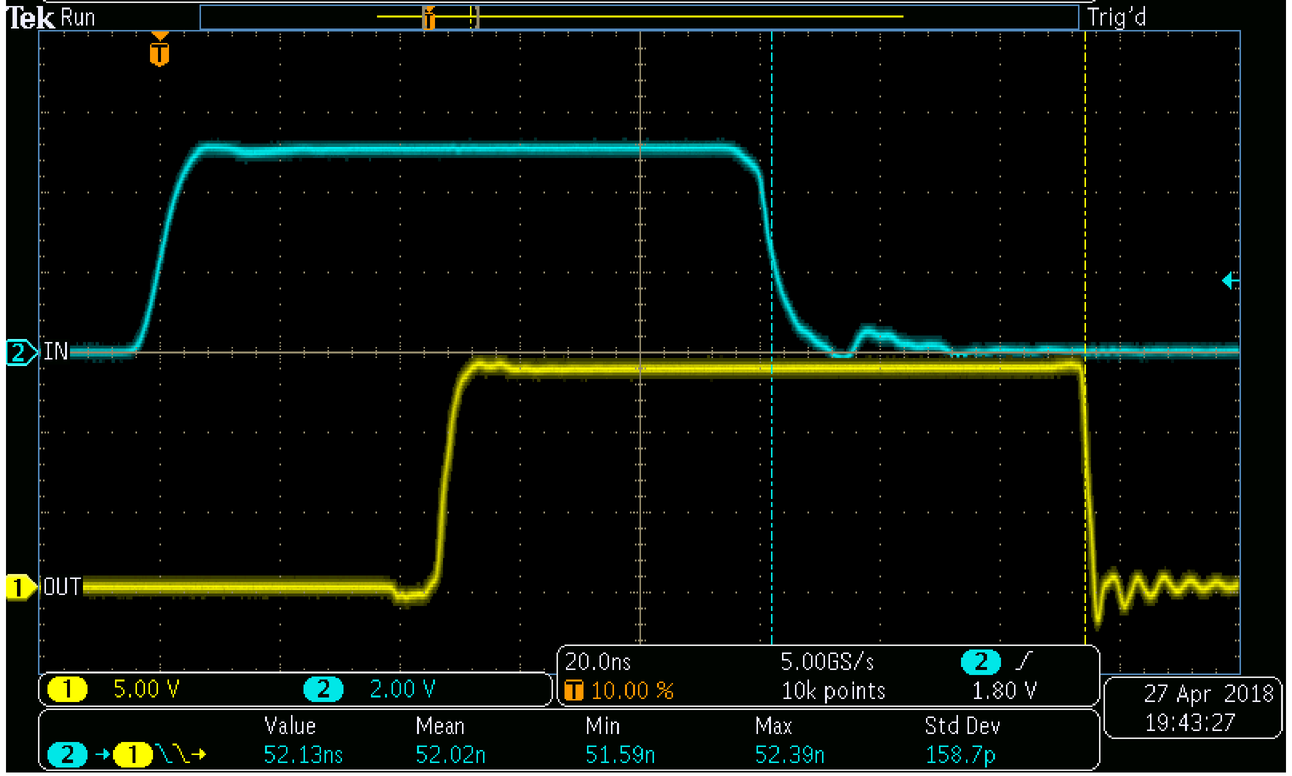




Pulse Duration Distortion

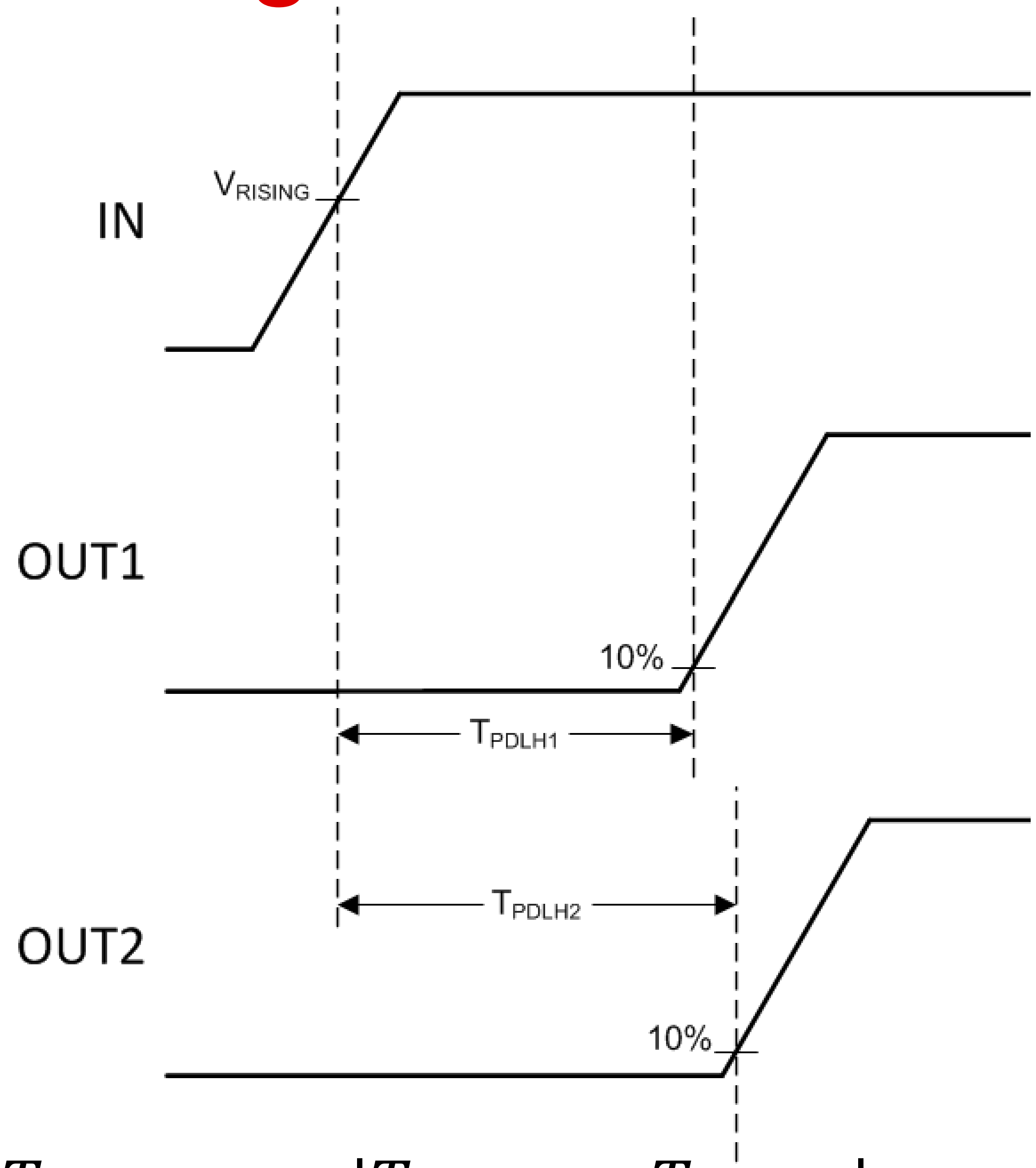




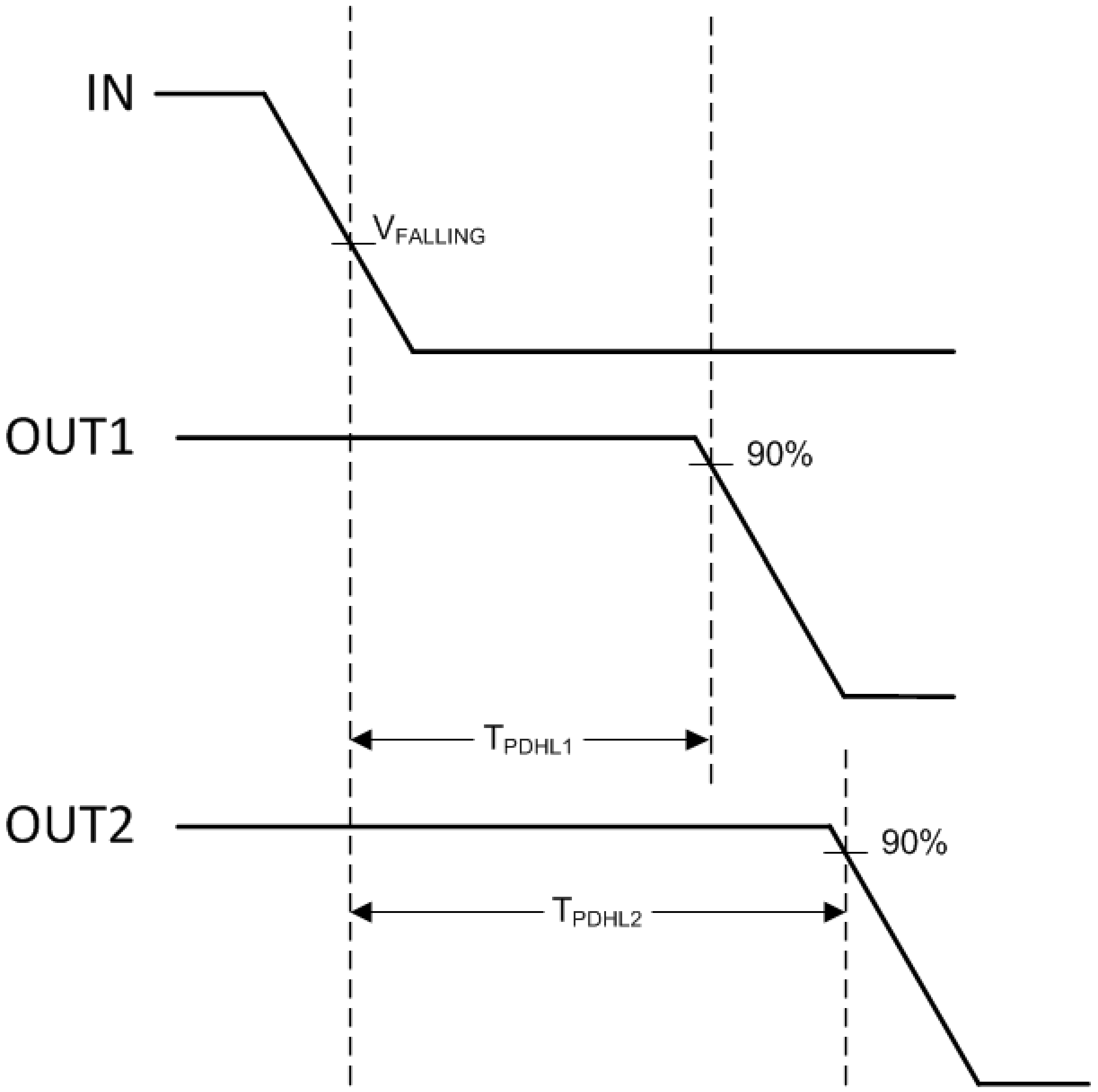


$$T_{PDD} = |52ns - 46ns| = 8ns$$

Timing Skew

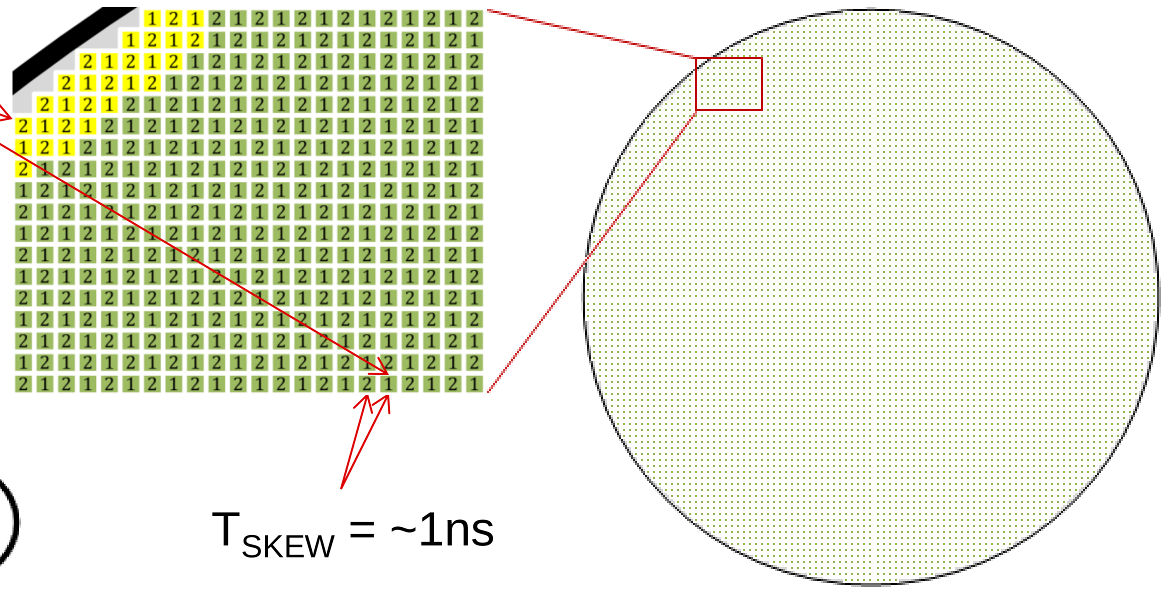


$$T_{SKEW,LH} = |T_{PDLH2} - T_{PDLH1}|$$

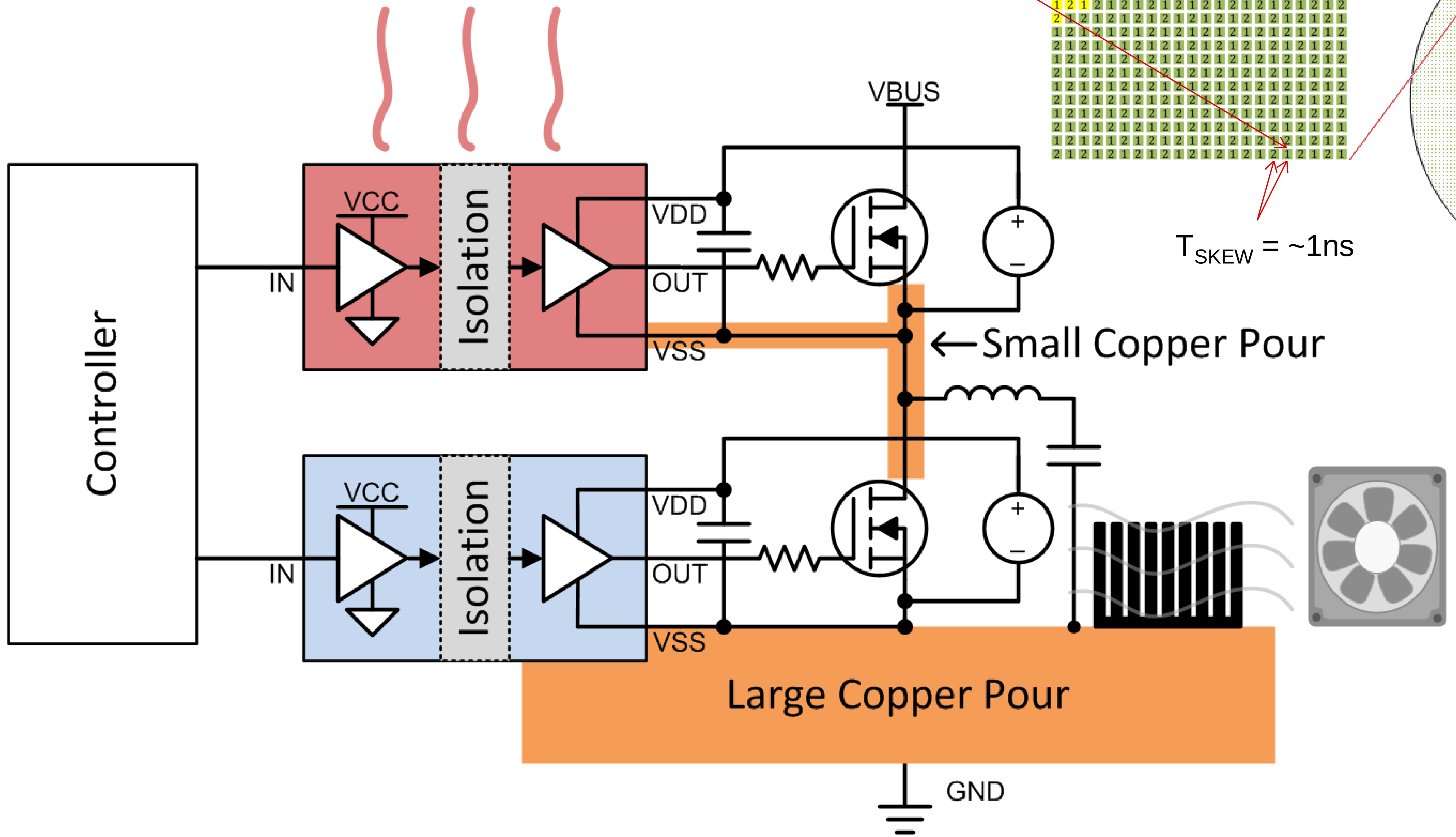


$$T_{SKEW,HL} = |T_{PDHL2} - T_{PDHL1}|$$

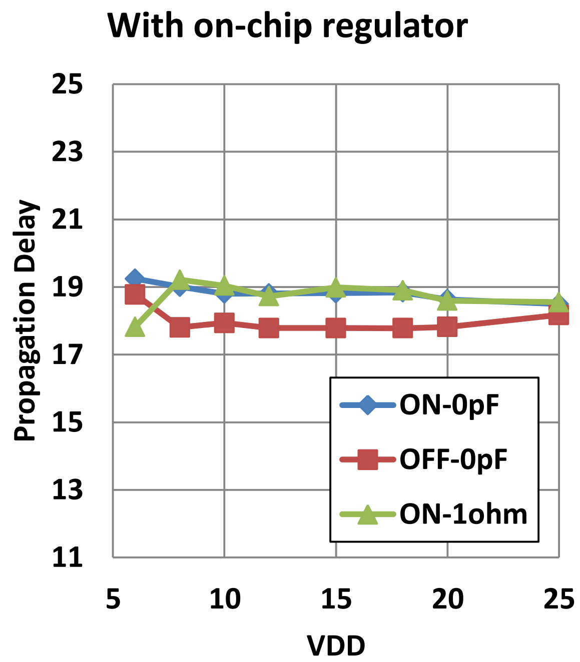
Timing Skew



TSKEW = ~3ns
TSKEW = ~1ns

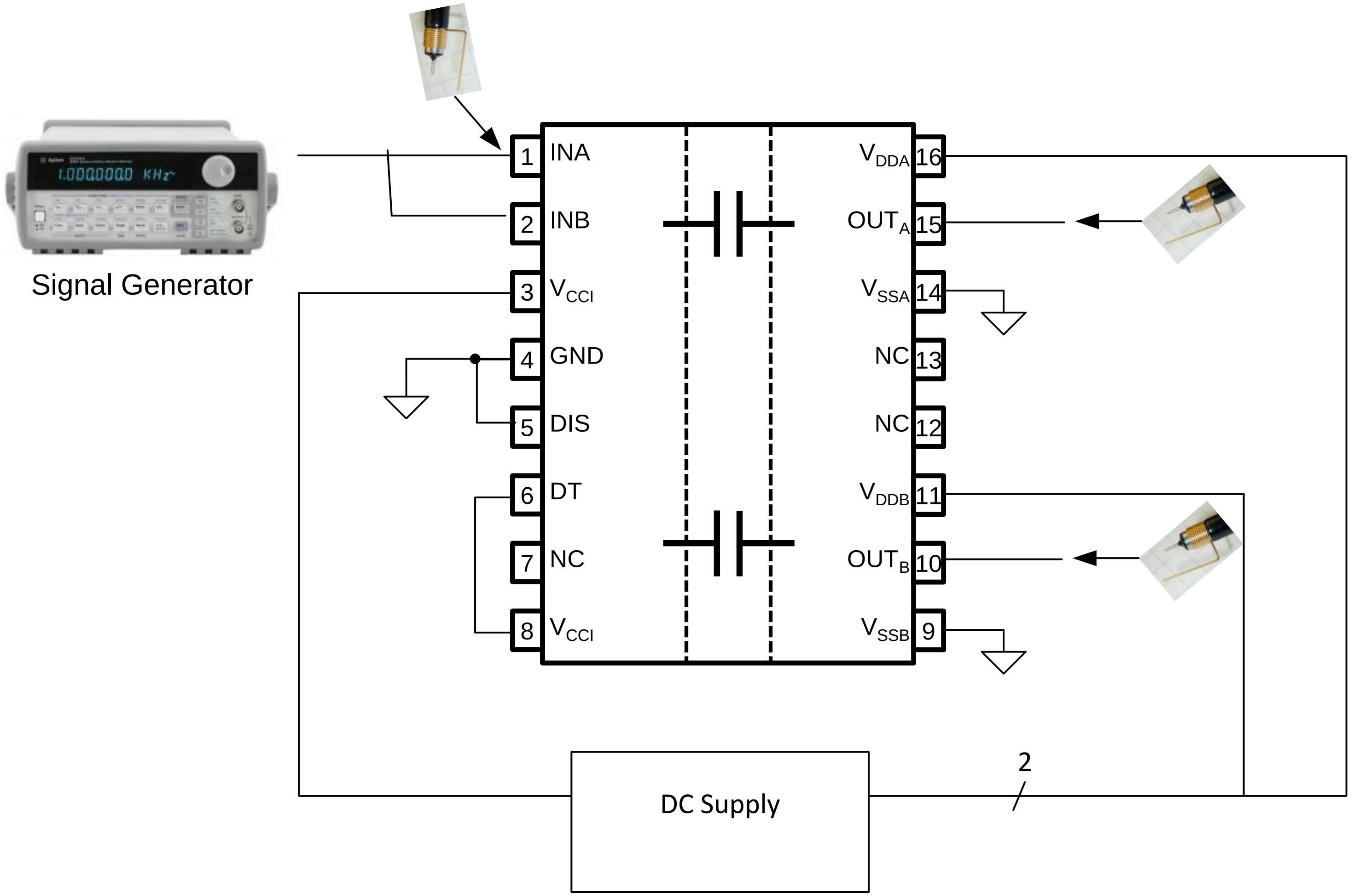


Controller
VCC
IN
Isolation
VDD
OUT
VSS
VBUS
←Small Copper Pour
VCC
IN
Isolation
VDD
OUT
VSS
Large Copper Pour
GND



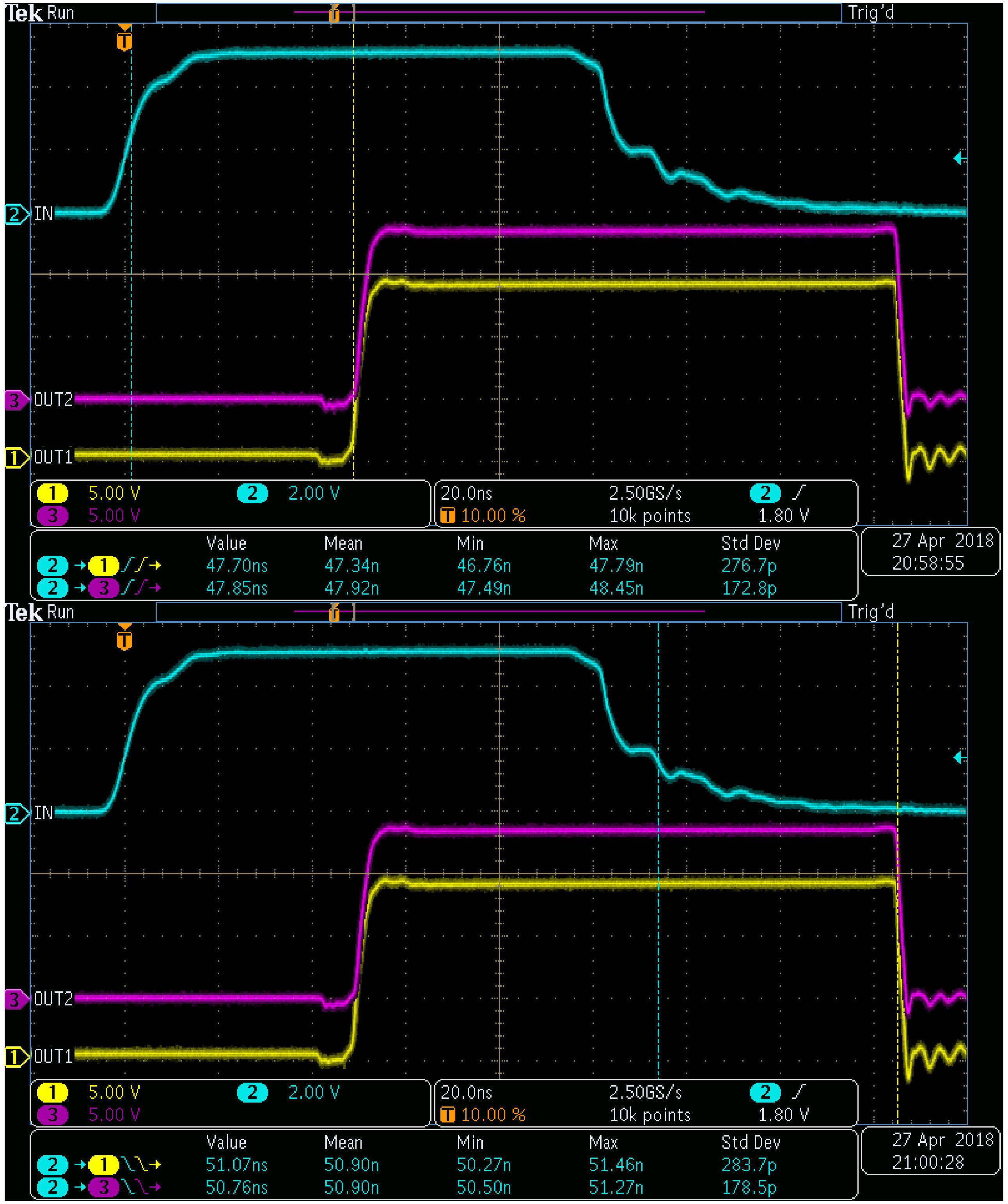
With on-chip regulator
Propagation Delay
VDD
ON-0pF
OFF-0pF
ON-1ohm

Timing Skew



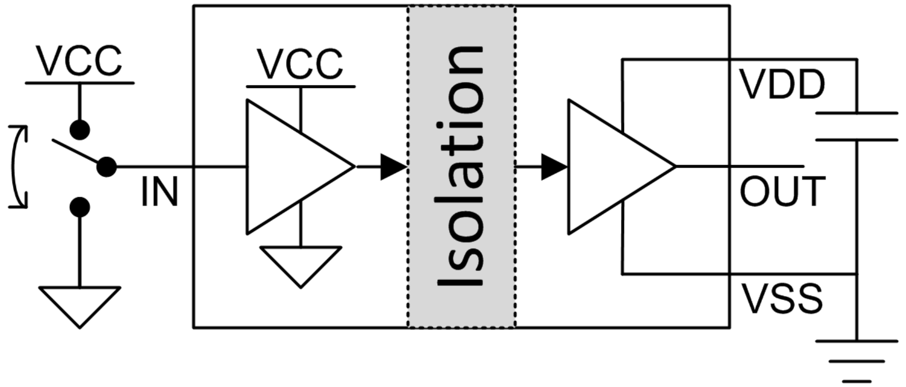
$$T_{SKEW,LH} = |51ns - 51ns| = 0ns$$

$$T_{SKEW,HL} = |48ns - 47ns| = 1ns$$

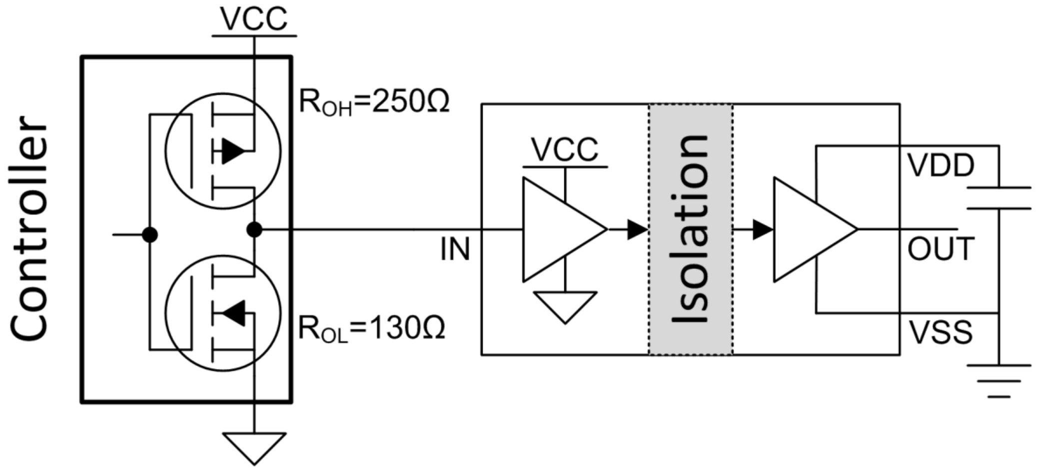


Common-Mode Transient Immunity (CMTI)

OUTA state becomes corrupted at ~190V/ns

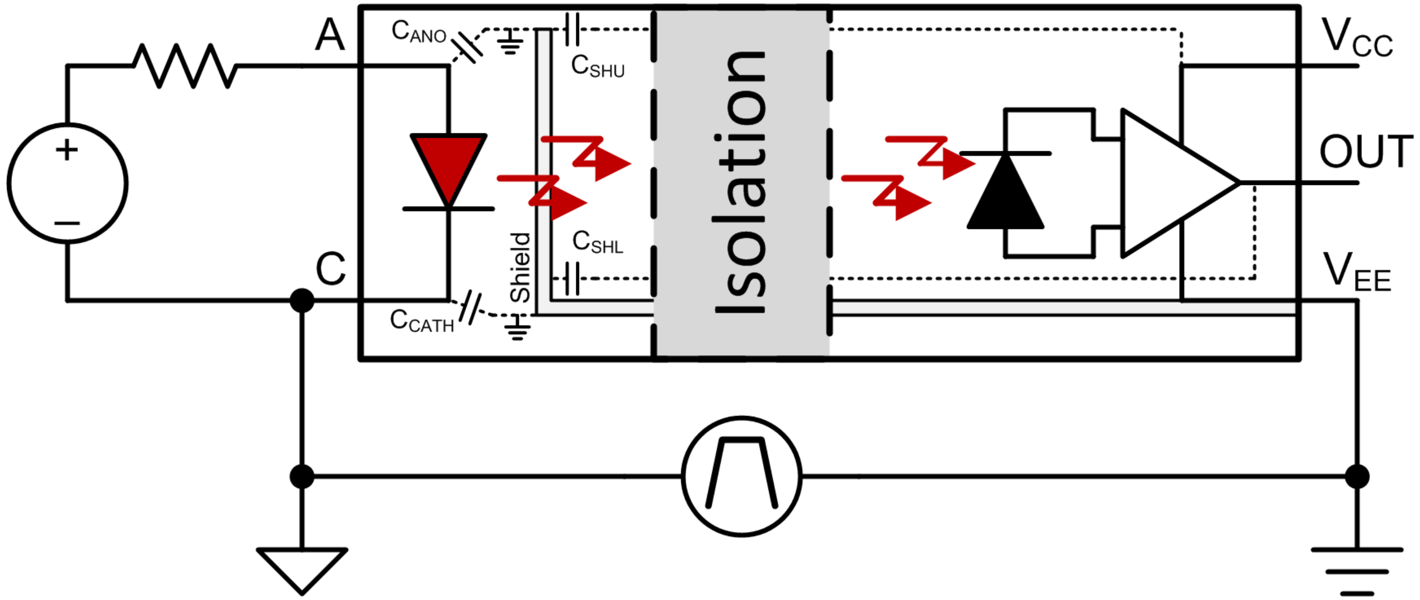


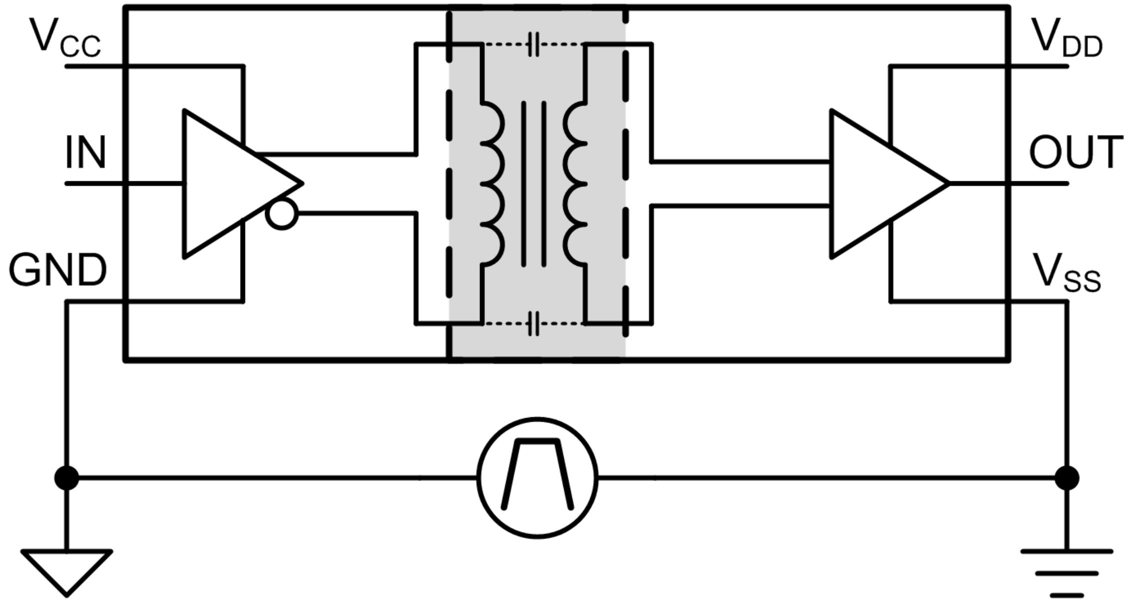
Static test: IN tied to VCC/GND close to the pins

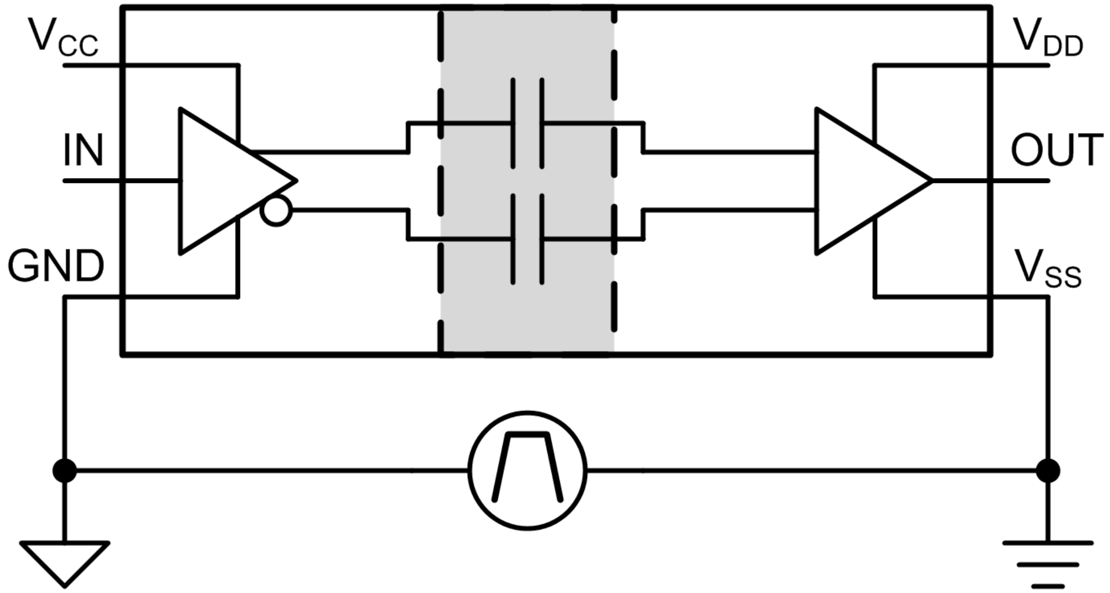


Dynamic test: IN driven with variable resistance and input loop

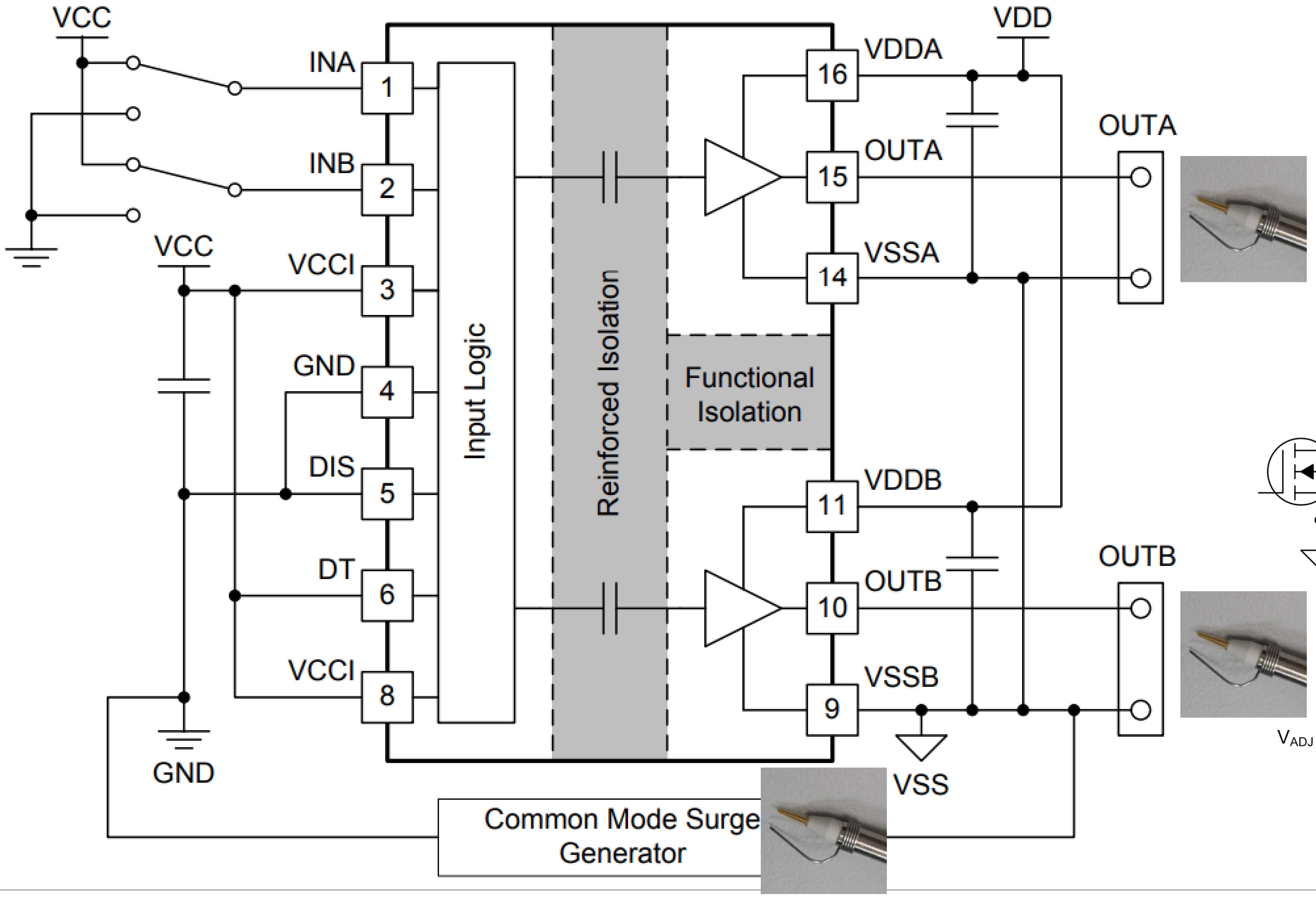
Common-Mode Transient Immunity (CMTI)

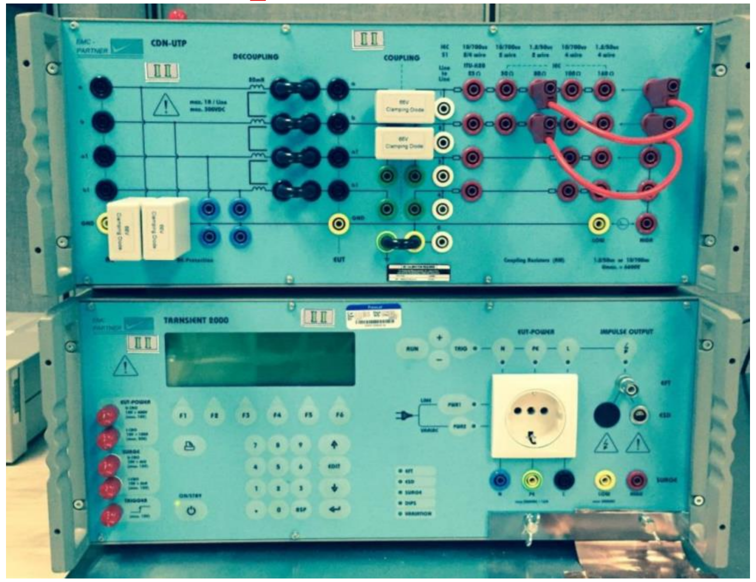


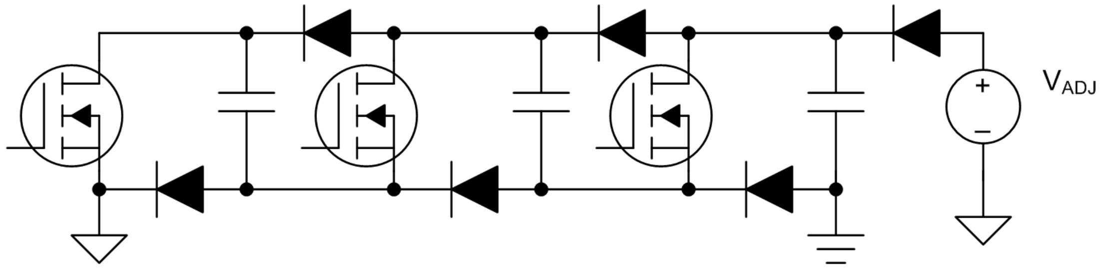


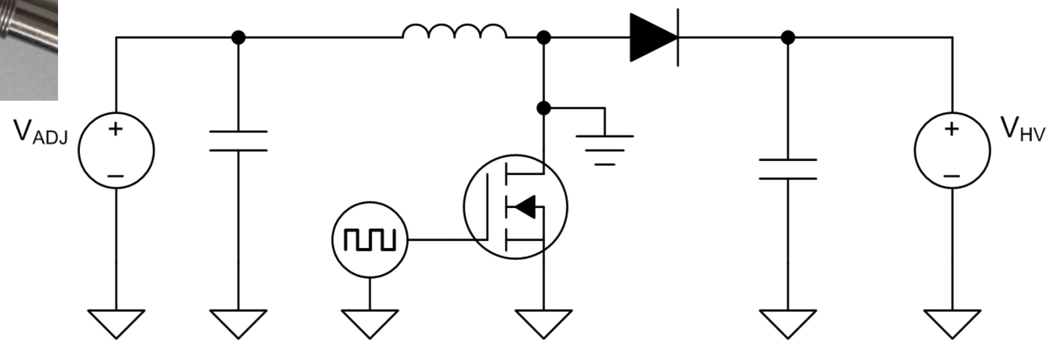


Common-Mode Transient Immunity (CMTI)

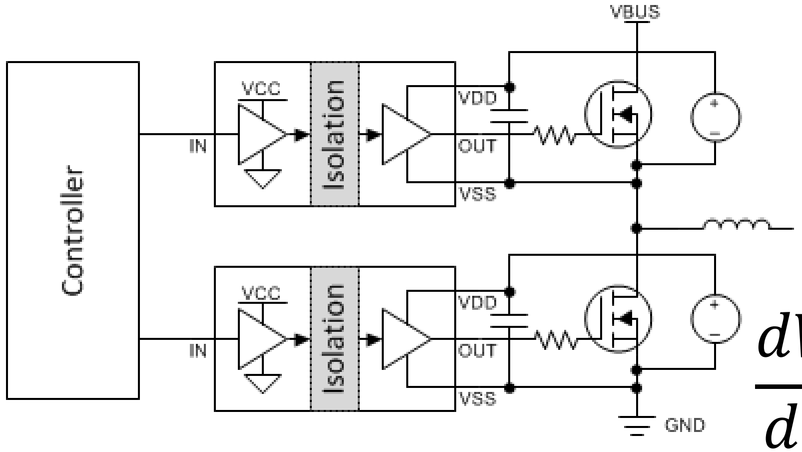








Example: SiC Half Bridge



$$T_{OFF(MAX)} = 35ns$$
$$T_{ON(MIN)} = 25ns$$
$$T_R = 10ns$$
$$T_F = 8ns$$
$$\frac{dV}{dt} = \frac{800V}{8ns} = 100\,V/ns$$

$$DT_{MIN(SKEW)} = T_{SKEW} + \left(T_{OFF(MAX)} - T_{ON(MIN)}\right)$$
$$DT_{MIN(PROP)} = \left(T_{PDHL(MAX)} - T_{PDLH(MIN)}\right) + \left(T_{OFF(MAX)} - T_{ON(MIN)}\right)$$

Capacitive Driver (ISO5852S)		
Propagation Delay	-	110ns max
Pulse Duration Distortion	-	20ns max
Part-to-Part Skew	-	30ns max
CMTI	100V/ns	

$Skew:\ 30ns + (35ns - 25ns) = 40ns$

$t_{PD}: (110ns - 0ns) + (35ns - 25ns) = 110ns$

Transformer Driver		
Propagation Delay	135ns min	225ns max
Pulse Duration Distortion	-25ns min	35ns max
Part-to-Part Skew	-	(60ns max)
CMTI	-	50V/ns

$Skew: 60ns + (35ns - 25ns) = 70ns$

$t_{PD}: (225ns - 135ns) + (35ns - 25ns) = 100ns$

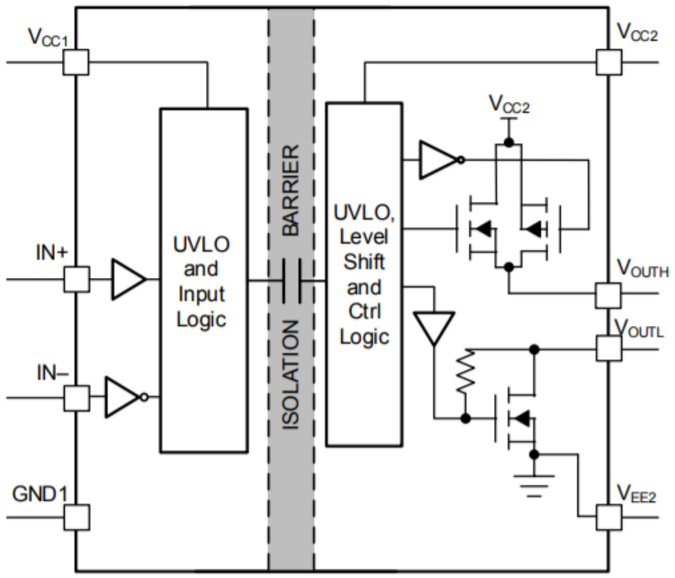
Optoisolator		
Propagation Delay	100ns min	500ns max
Pulse Duration Distortion	-300ns min	300ns max
Part-to-Part Skew	-350ns min	350ns max
CMTI	15V/ns	-

$Skew: 350ns + (35ns - 25ns) = 360ns$

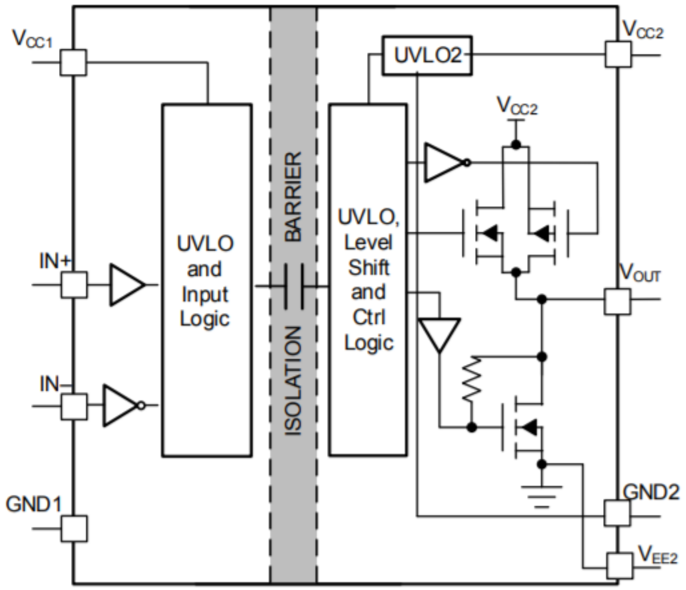
$t_{PD}: (500ns - 100ns) + (35ns - 25ns) = 410ns$

Looking Forward

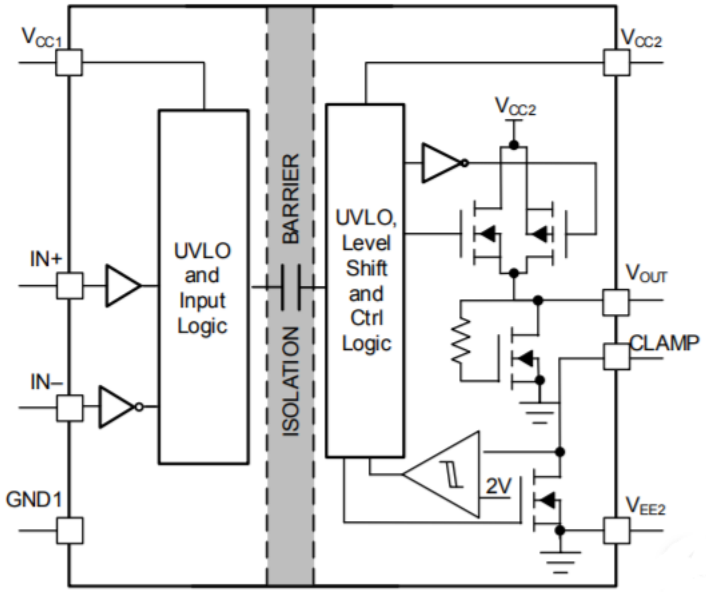
ORDERABLE PART NUMBER	MINIMUM SOURCE AND SINK CURRENT	DESCRIPTION
UCC5310MC	2.4 A and 1.1 A	Miller clamp
UCC5320SC	2.4 A and 2.2 A	Split output
UCC5320EC	2.4 A and 2.2 A	UVLO with respect to IGBT emitter
UCC5350MC	5 A and 5 A	Miller clamp
UCC5350SB	5 A and 5 A	Split Output with 8 V UVLO
UCC5390SC	10 A and 10 A	Split output
UCC5390EC	10 A and 10 A	UVLO with respect to IGBT emitter



S Version



E Version



M Version

Thanks for your time!
Please try the quiz.

Critical Isolated Gate Driver Specifications

Multiple Choice Quiz

TI Precision Labs – Isolation

Quiz: Critical Isolated Gate Driver Specifications

1. **Propagation delay is determined by:**
   a. The speed of electrons through copper
   b. The specific circuitry within the gate driver
   c. The speed of light
   d. The cost of the process used
2. **Pulse duration distortion is conventionally:**
   a. Measured as an absolute value
   b. Measured by both positive and negative distortion
   c. Measured according to the manufacturer’s conventions
   d. Not measured at all
3. **Timing skew is important for systems with ______________**
   a. Very low switching frequencies
   b. Only a single switch (such as single phase boost PFC)
   c. Bridge topologies with high efficiency and minimal dead time requirements
   d. Systems that use IGBTs

Quiz: Critical Isolated Gate Driver Specifications

4. **Common-mode transient immunity is primarily determined by the _____________ between the sides of the isolation barrier.**
   a. Parasitic capacitance
   b. Parasitic inductance
   c. Parasitic resistance
   d. Parasitic BJT
5. **In an application environment, the most common cause for drift in isolated gate driver specifications is:**
   a. Changes in supply voltage
   b. Changes in output load
   c. Changes in semiconductor characteristics over the lifetime of the IC
   d. Changes in temperature

Critical Isolated Gate Driver Specifications

Multiple Choice Quiz – Solutions

TI Precision Labs – Isolation

Quiz: Critical Isolated Gate Driver Specifications

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